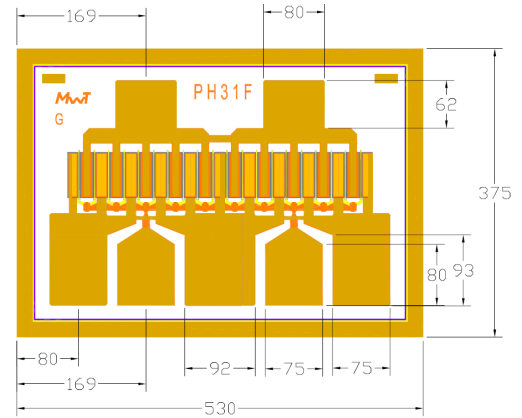


Features:

- 30 dBm of Power at 12 GHz
- 13 dB Small Signal Gain at 12 GHz
- 44% PAE at 12 GHz
- 0.25 x 1200 Micron Refractory Metal/Gold Gate
- Excellent for Medium Power, Gain, and High Power Added Efficiency
- Ideal for Commercial, Military, Hi-Rel Space Applications



Chip Dimensions: 530 x 375 microns
Chip Thickness: 100 microns

Description:

The MwT-PH31F is a AlGaAs/InGaAs pHEMT (Pseudomorphic-High-Electron-Mobility-Transistor) device whose nominal 0.25 micron gate length and 1200 micron gate width make it ideally suited for applications requiring high-gain and medium power up to 18 GHz frequency range. The device is equally effective for either wideband or narrow-band applications. The chip is produced using reliable metal systems and passivated to insure excellent reliability.

Electrical Specifications: at $T_a = 25^\circ\text{C}$

PARAMETERS & CONDITIONS	SYMBOL	FREQ	UNITS	MIN	TYP
Output Power at 1dB Compression $V_{ds}=8.0\text{V}$ $I_{ds}=0.7 \times I_{DSS}$	P1dB	12 GHz	dBm		28.5
Saturated Power $V_{ds}=8.0\text{V}$ $I_{ds}=0.7 \times I_{DSS}$	Psat	12 GHz	dBm		30.0
Output Third Order Intercept Point $V_{ds}=8.0\text{V}$ $I_{ds}=0.7 \times I_{DSS}$	OIP3	12 GHz	dBm		37.0
Small Signal Gain $V_{ds}=8.0\text{V}$ $I_{ds}=0.7 \times I_{DSS}$	SSG	12 GHz	dB		13.0
Power Added Efficiency at P1dB $V_{ds}=8.0\text{V}$ $I_{ds}=0.7 \times I_{DSS}$	PAE	12 GHz	%		44

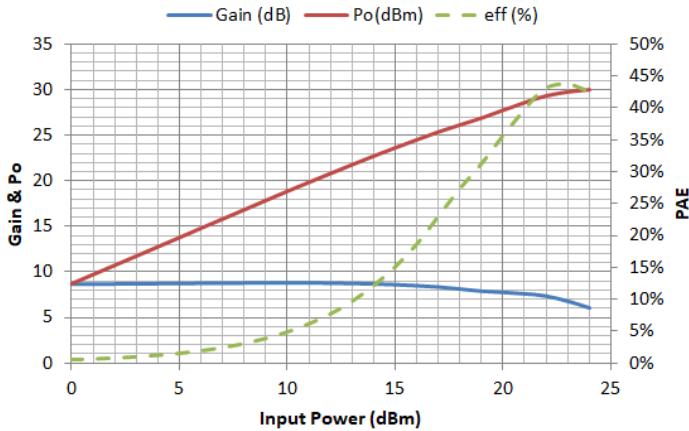
Note: I_{ds} should be between 40% and 80% of I_{DSS} . Currently, our data shows I_{ds} at 70% of I_{DSS} . Low I_{ds} will improve efficiency, but high I_{ds} will make Psat and IP3 better.

DC Specifications: at $T_a = 25^\circ\text{C}$

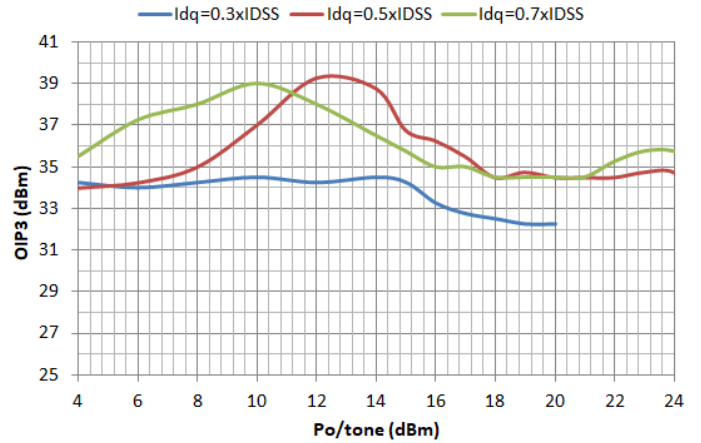
PARAMETERS & CONDITIONS	SYMBOL	UNITS	MIN	TYP	MAX
Saturated Drain Current $V_{ds}= 2.0\text{V}$ $V_{gs}= 0.0\text{V}$	I_{DSS}	mA	240		280
Transconductance $V_{ds}= 2.0\text{V}$ $V_{gs}= 0.0\text{V}$	Gm	mS		260	
Pinch-off Voltage $V_{ds}= 2.0\text{V}$ $I_{ds}= 1.0\text{mA}$	V_p	V		-0.8	-1.0
Gate-to-Source Breakdown Voltage $I_{gs}= -0.3\text{mA}$	BVGSO	V		-17.0	
Gate-to-Drain Breakdown Voltage $I_{gd}= -0.3\text{mA}$	BVGDO	V		-18.0	
Chip Thermal Resistance	Chip & 71 pkg	Rth	C/W	40	

* Overall Rth depends on case mounting

MwT-PH31F, Po, Gain & PAE at 12GHz vs Pin
Vds=8V; Idq=0.7xIDSS



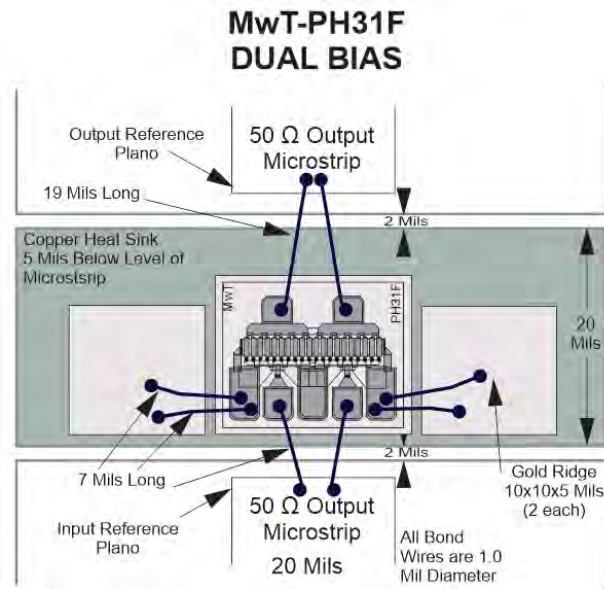
MwT-PH31F, OIP3 with different Idq vs Po/Tone at 12GHz
Vds=8V; Idq=0.7xIDSS



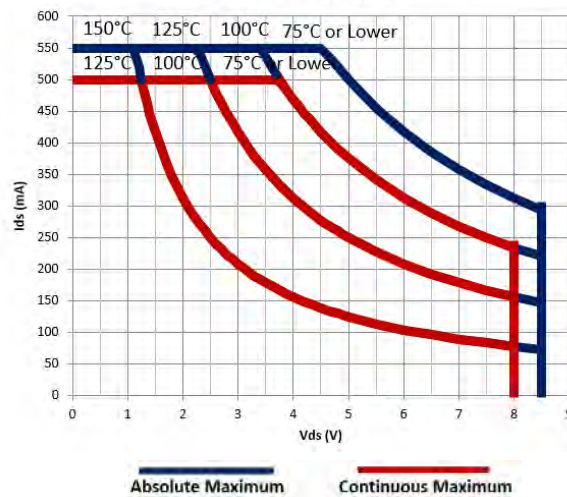
MwT-PH31F, Load Pull Power Data Vds=8V, Idq=0.7xIdss

Freq	ZS		ZL		Psat
	Mag	phase	mag	phase	
2	0.65	117.00	0.32	164.30	30.52
4	0.78	144.00	0.45	153.10	30.17
6	0.88	156.00	0.44	161.30	30.12
8	0.81	158.00	0.49	153.90	30.10
10	0.91	169.00	0.51	158.30	30.13
12	0.92	174.00	0.55	154.90	30.15

The load pull data is based on nonlinear model provided by the foundry that processes the device.



SAFE OPERATING LIMITS vs BACKSIDE TEMPERATURE
MwT-PH31F Chip and 71 Pkg



Absolute Maximum Rating

Symbol	Parameter	Units	Cont Max1	Absolute Max2
VDS	Drain to Source Volt.	V	8.0	8.5
Tch	Channel Temperature	°C	+150	+175
Tst	Storage Temperature	°C	-65 to +150	+175
Pin	RF Input Power	mW	400	500

Notes:

1. Exceeding any one of these limits in continuous operation may reduce the mean-time-to-failure below the design goal.
2. Exceeding any one of these limits may cause permanent damage.