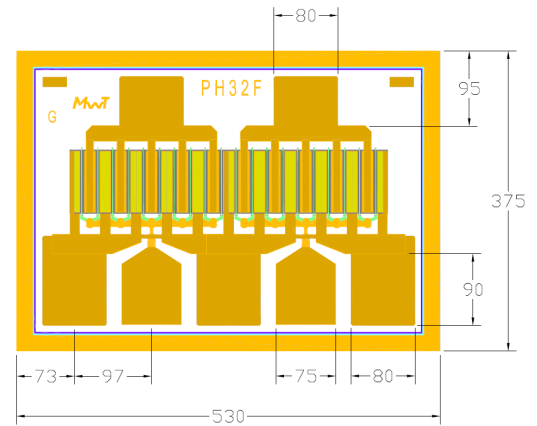


Features:

- 30.5 dBm of Power at 12 GHz
- 13 dB Small Signal Gain at 12 GHz
- 43% PAE at 12 GHz
- 0.25 x 1600 Micron Refractory Metal/Gold Gate
- Excellent for High Power, Gain, and High Power Added Efficiency
- Ideal for Commercial, Military, Hi-Rel Space Applications



Chip Dimensions: 530 x 375 microns
Chip Thickness: 100 microns

Description:

The MwT-PH32F is a AlGaAs/InGaAs pHEMT (Pseudomorphic-High-Electron-Mobility-Transistor) device whose nominal 0.25 micron gate length and 1600 micron gate width make it ideally suited for applications requiring high power and high power added efficiency up to 12.0 GHz frequency range. The device is equally effective for either wideband or narrow-band applications. The chip is produced using reliable metal systems and passivated to insure excellent reliability.

Electrical Specifications: at $T_a = 25\text{ }^\circ\text{C}$

PARAMETERS & CONDITIONS	SYMBOL	FREQ	UNITS	MIN	TYP
Output Power at 1dB Compression $V_{ds}=8.0V$ $I_{ds}=0.7 \times I_{DSS}$	P1dB	12 GHz	dBm		29.5
Saturated Power $V_{ds}=8.0V$ $I_{ds}=0.7 \times I_{DSS}$	Psat	12 GHz	dBm		30.5
Output Third Order Intercept Point $V_{ds}=8.0V$ $I_{ds}=0.7 \times I_{DSS}$	OIP3	12 GHz	dBm		37.0
Small Signal Gain $V_{ds}=8.0V$ $I_{ds}=0.7 \times I_{DSS}$	SSG	12 GHz	dB		13.0
Power Added Efficiency at P1dB $V_{ds}=8.0V$ $I_{ds}=0.7 \times I_{DSS}$	PAE	12 GHz	%		43

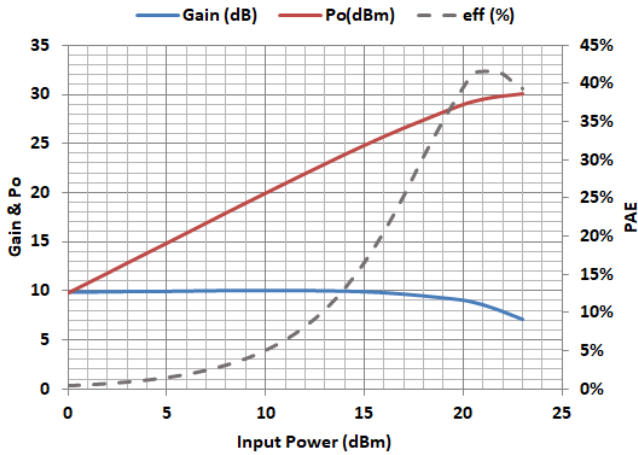
Note: I_{ds} should be between 40% and 80% of I_{DSS} . Currently, our data shows I_{ds} at 70% of I_{DSS} . Low I_{ds} will improve efficiency, but high I_{ds} will make Psat and IP3 better.

DC Specifications: at $T_a = 25\text{ }^\circ\text{C}$

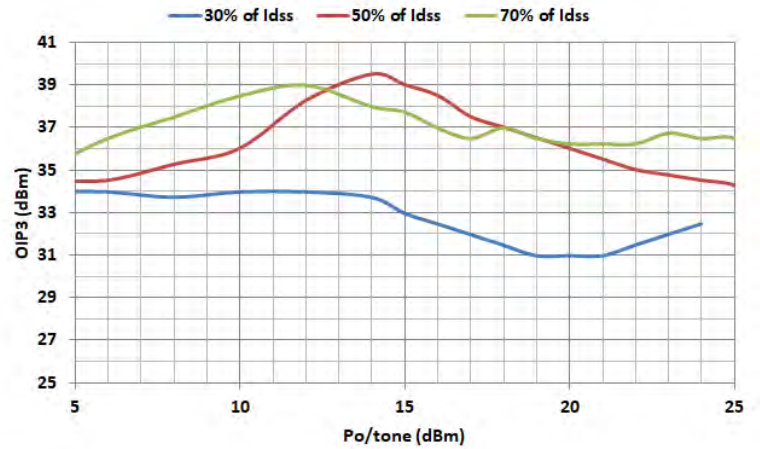
PARAMETERS & CONDITIONS	SYMBOL	UNITS	MIN	TYP	MAX
Saturated Drain Current $V_{ds}= 2.0 V$ $V_{gs}= 0.0 V$	I_{DSS}	mA	310		360
Transconductance $V_{ds}= 2.0 V$ $V_{gs}= 0.0 V$	G_m	mS		500	
Pinch-off Voltage $V_{ds}= 2.0 V$ $I_{ds}= 1.0 mA$	V_p	V		-0.8	-1.0
Gate-to-Source Breakdown Voltage $I_{gs}= -0.3 mA$	BVGSO	V		-16.0	
Gate-to-Drain Breakdown Voltage $I_{gd}= -0.3 mA$	BVGDO	V		-18.0	
Chip Thermal Resistance	Chip & 71 pkg	R_{th}	C/W	35	

* Overall R_{th} depends on case mounting

MwT-PH32F, Po, Gain & PAE vs Pin at 12GHz
Vds=8V; Idq=0.7xIdSS



MwT-PH32F, OIP3 at different Idq vs Po/tone at 12GHz
Vds=8V; Idq=0.7xIdSS

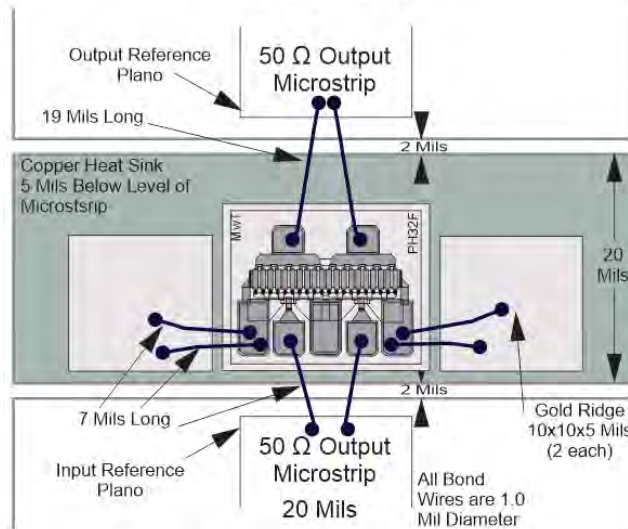


MwT-PH32F, Load Pull Power Data, Vds=8V, Idq=0.7xIdss

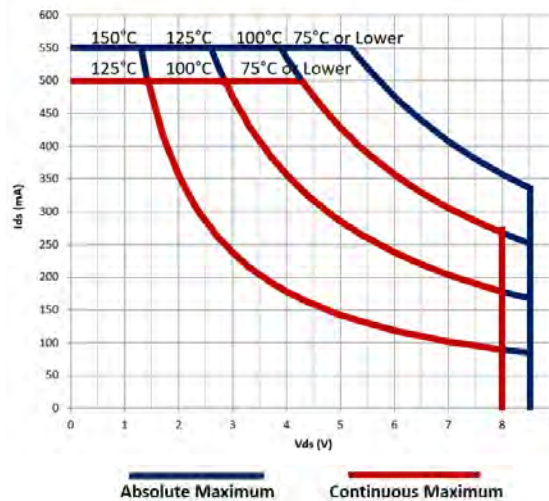
Freq	Zs		ZL		Psat
	Mag	phase	mag	phase	
2	0.75	130.00	0.43	169.60	31.68
4	0.83	154.00	0.52	162.40	31.37
6	0.92	162.00	0.53	164.60	31.33
8	0.89	168.00	0.58	160.80	31.31
10	0.94	175.00	0.57	164.60	31.35
12	0.94	175.00	0.64	161.40	31.27

The load pull data is based on nonlinear model provided by the foundry that processes the device.

MwT-PH32F DUAL BIAS



SAFE OPERATING LIMITS vs BACKSIDE TEMPERATURE
MwT-PH32F Chip and 71 Pkg



Absolute Maximum Rating

Symbol	Parameter	Units	Cont Max1	Absolute Max2
VDS	Drain to Source Volt.	V	8.0	8.5
Tch	Channel Temperature	°C	+150	+175
Tst	Storage Temperature	°C	-65 to +150	+175
Pin	RF Input Power	mW	500	600

Notes:

1. Exceeding any one of these limits in continuous operation may reduce the mean-time-to-failure below the design goal.
2. Exceeding any one of these limits may cause permanent damage.