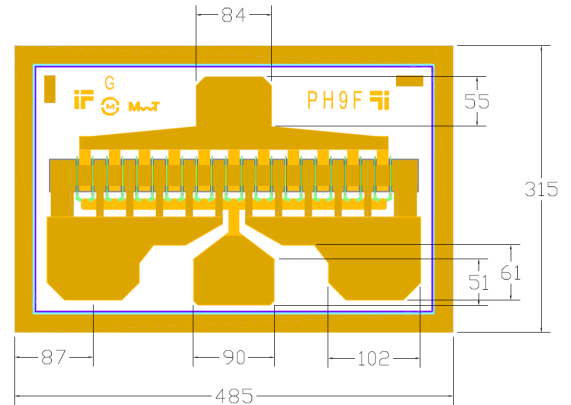


Features:

- 28 dBm of typical Output Power at 12 GHz
- 13 dB typical Small Signal Gain at 12 GHz
- 45% typical PAE at 12 GHz
- 0.25 x 750 Micron Refractory Metal/Gold Gate
- Excellent for Power, Gain, and High Power Added Efficiency Applications
- Ideal for Commercial, Military, Hi-Rel Space Applications



Chip Dimensions: 485 x 315 microns
Chip Thickness: 100 microns

Description:

The MwT-PH9F is a AlGaAs/InGaAs pHEMT (Pseudomorphic-High-Electron-Mobility-Transistor) device whose nominal 0.25 micron gate length and 750 micron gate width make it ideally suited for applications requiring high-gain and power up to 18 GHz frequency range with power outputs ranging from 400 to 500 milli-watts. The device is equally effective for either wideband (e.g. 6 to 18 GHz) or narrow-band applications. The chip is produced using reliable metal systems and passivated to insure excellent reliability.

Electrical Specifications: • at $T_a = 25^\circ C$

PARAMETERS & CONDITIONS	SYMBOL	FREQ	UNITS	MIN	TYP
Output Power at 1dB Compression $V_{ds}=8.0V$ $I_{ds}=0.7I_{dss}$	P1dB	12 GHz	dBm		25.0
Saturated Power $V_{ds}=8.0V$ $I_{ds}=0.7I_{dss}$	Psat	12 GHz	dBm		28.0
Output Third Order Intercept Point $V_{ds}=8.0V$ $I_{ds}=0.7I_{dss}$	OIP3	12 GHz	dBm		34.0
Small Signal Gain $V_{ds}=8.0V$ $I_{ds}=0.7I_{dss}$	SSG	12 GHz	dB		13.0
Power Added Efficiency $V_{ds}=8.0V$ $I_{ds}=0.7I_{dss}$	PAE	12 GHz	%		45

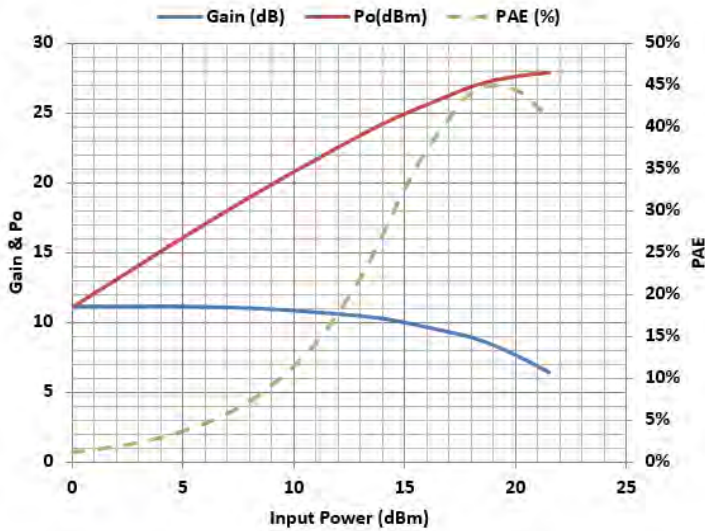
Note: I_{ds} should be between 40% and 80% of I_{dss} . Currently, our data shows I_{ds} at 70% of I_{dss} . Low I_{ds} will improve efficiency, but high I_{ds} will make Psat and IP3 better.

DC Specifications: • at $T_a = 25^\circ C$

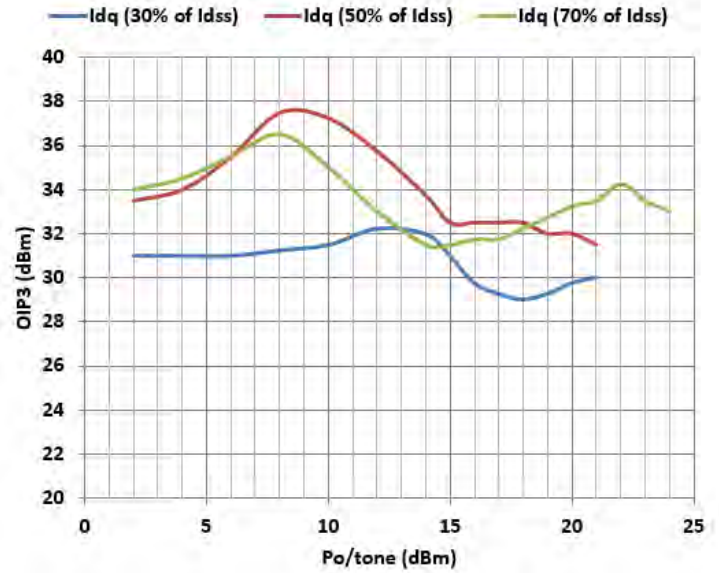
PARAMETERS & CONDITIONS	SYMBOL	UNITS	MIN	TYP	MAX
Saturated Drain Current $V_{ds}= 4.0 V$ $V_{gs}= 0.0 V$	I_{DSS}	mA	180		220
Transconductance $V_{ds}= 2.5 V$ $V_{gs}= 0.0 V$	G_m	mS		270	
Pinch-off Voltage $V_{ds}= 3.0 V$ $I_{ds}= 5.0 mA$	V_p	V		-0.8	
Gate-to-Source Breakdown Voltage $I_{gs}= -1.0 mA$	BVGSO	V		-17.0	
Gate-to-Drain Breakdown Voltage $I_{gd}= -1.0 mA$	BVGDO	V		-18.0	
Chip Thermal Resistance	MwT-PH7F Chip & 70 pkg 71 pkg & 73 pkg	R_{th}	C/W	60 175*	

* Overall R_{th} depends on case mounting

MwT-PH9F, Gain, Po & PAE vs Pin at 12GHz
Vds=8V; Idq=0.7xIDSS



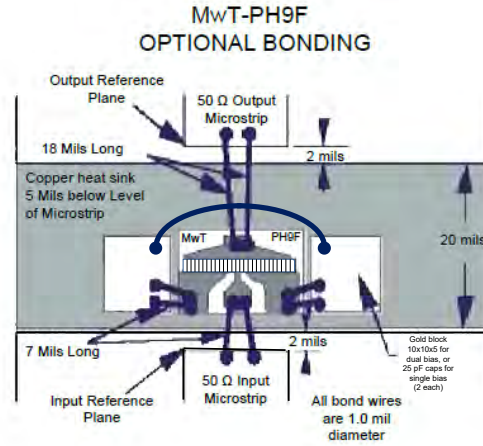
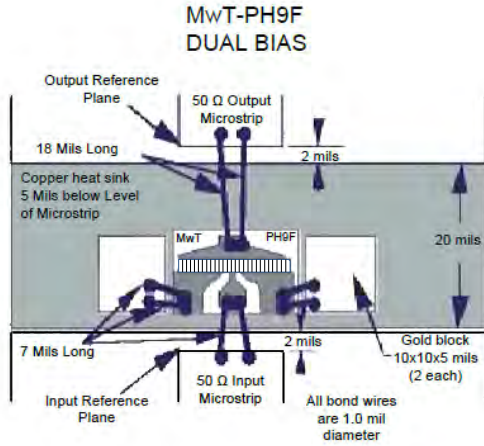
MwT-PH9F, OIP3 at different Idq vs Po/tone at 12GHz



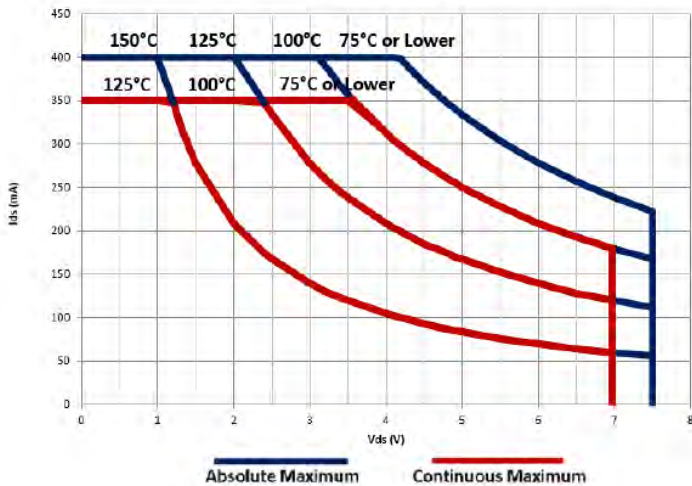
MwT-PH9F, Load Pull data for Power, Vds=8V, Idq=0.7xIdss

Freq (GHz)	Zs		ZL		P _{sat} (dBm)
	Mag	phase	mag	phase	
2	0.60	95.0	0.13	162.3	28.3
4	0.75	135.0	0.23	129.0	27.9
6	0.85	155.0	0.31	121.2	27.4
8	0.90	172.1	0.36	134.2	27.5
10	0.87	175.0	0.42	140.0	27.1
12	0.80	180.0	0.48	143.0	27.1

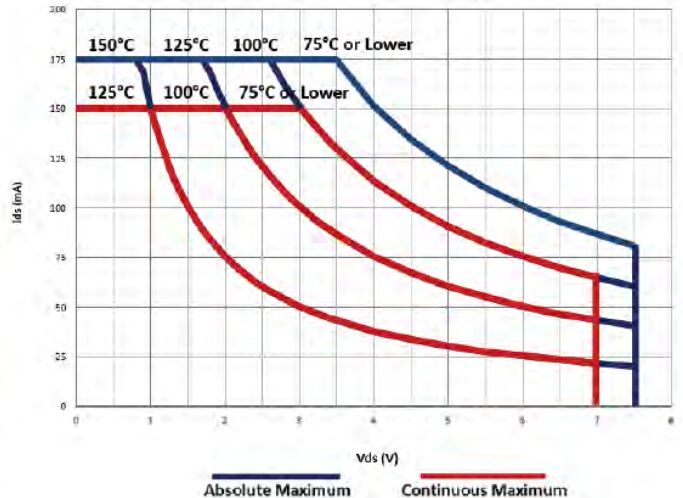
The load pull data is based on nonlinear model provided by the foundry that processes the device.



SAFE OPERATING LIMITS vs BACKSIDE TEMPERATURE
MwT-PH9F Chip and Pkg



SAFE OPERATING LIMITS vs BACKSIDE TEMPERATURE
MwT-PH9F with 70Pkg and 73Pkg



MAXIMUM RATINGS AT Ta = 25 °C

Symbol	Parameter	Units	Cont Max1	Absolute Max2
VDS	Drain to Source Volt.	V	7.5	8.0
Tch	Channel Temperature	°C	+150	+175
Tst	Storage Temperature	°C	-65 to +160	+180
Pin	RF Input Power	mW	240	360
Pt	Total Power Dissipation	mW	2700	3300

Notes:

- Exceeding any one of these limits in continuous operation may reduce the mean-time-to-failure below the design goal.
- Exceeding any one of these limits may cause permanent damage.