2. Signal List

Pin No.		Name	Type	Description
P, DW	TN			
1	1	$\overline{XTAL}$	output	Output of the on-chip Xtal oscillator inverter.
2	2	XTAL/CLOCK	input	Input to the on-chip Xtal oscillator inverter.
3	5	M0	input	A logic level input for setting the mode of the device. See section 4.2
4	6	M1	input	A logic level input for setting the mode of the device. See section 4.2
5	7	RXIN	input	Input to the Rx input amplifier.
6	8	RXAMPOUT	output	Output of the Rx input amplifier.
7	11	TXOUT	output	Output of the FSK generator.
8	12	V_{SS}	power	Negative supply (ground).
9	13	V_{BIAS}	output	Internally generated bias voltage, held at V_{DD} /2 when the device is not in 'Zero-Power' mode. Should be decoupled to V_{SS} by a capacitor mounted close to the device pins.
10	14	RXEQ	input	A logic level input for enabling/disabling the equalizer in the receive filter. See section 4.4
11	17	TXD	input	A logic level input for either the raw input to the FSK Modulator or data to be re-timed depending on the state of the M0, M1 and CLK inputs. See section 4.9
12	18	CLK	input	A logic level input which may be used to clock data bits in/out of the FSK Data Retiming block.
13	19	RXD	output	A logic level output carrying either the raw output of the FSK Demodulator or re-timed characters depending on the state of the M0, M1 and CLK inputs. See section 4.8
14	20	DET	output	A logic level output of the on-chip energy detect circuit.
15	23	$\overline{RDY}$	output	"Ready for data transfer" output of the on-chip data retiming circuit. This open-drain active low output may be used as an Interrupt Request/Wake-up input to the associated C. An external pull-up resistor should be connected between this output and V_{DD}.
16	24	V_{DD}	power	The positive supply rail. Levels and thresholds within the device are proportional to this voltage. Should be decoupled to V_{SS} by a capacitor mounted close to the device pins.
	3, 4, 9, 10 ,15, 16, 21, 22	N/C		No internal connections

This device is capable of detecting and decoding small amplitude signals. Achieving the V_{DD} and V_{BIAS} decoupling and protection of the receive path from extraneous in-band signals is very important. It is recommended that decoupling capacitors be placed so the connection between them and the device pins is as short as possible. A ground plane protecting the receive path will help attenuate interfering signals.