19-0154; Rev 2; 11/05

MAXIM

Nonvolatile RAM Controller

General Description

The MXD1210 nonvolatile RAM controller is a very low-power CMOS circuit that converts standard (volatile) CMOS RAM into nonvolatile memory. It also continually monitors the power supply to provide RAM write protection when power to the RAM is in a marginal (out-of-tolerance) condition. When the power supply begins to fail, the RAM is write-protected, and the device switches to battery-backup mode.

Applications

Microprocessor Systems

Computers

Embedded Systems

Features

- **Battery Backup**
- **Memory Write Protection**
- **230µA Operating Mode Quiescent Current**
- **2nA Backup Mode Quiescent Current**
- **Battery Freshness Seal**
- **Optional Redundant Battery**
- **Low Forward-Voltage Drop on V_{CC} Supply Switch**
- **5% or 10% Power-Fail Detection Options**
- **Tests Battery Condition During Power-Up**
- **8-Pin SO Available**

Ordering Information

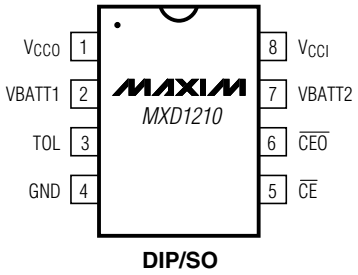
PART	TEMP RANGE	PIN-PACKAGE
MXD1210C/D	0°C to +70°C	Dice*
MXD1210CPA	0°C to +70°C	8 PDIP
MXD1210CSA	0°C to +70°C	8 SO
MXD1210CWE	0°C to +70°C	16 Wide SO
MXD1210EPA	-40°C to +85°C	8 PDIP
MXD1210ESA	-40°C to +85°C	8 SO
MXD1210EWE	-40°C to +85°C	16 Wide SO
MXD1210MJA	-55°C to +125°C	8 CERDIP

**Contact factory for dice specifications.*

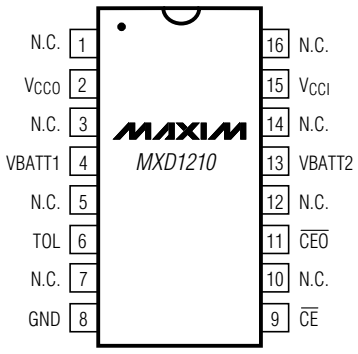
Devices in PDIP and SO packages are available in both leaded and lead-free packaging. Specify lead free by adding the + symbol at the end of the part number when ordering. Lead free not available for CERDIP package.

Pin Configurations

TOP VIEW

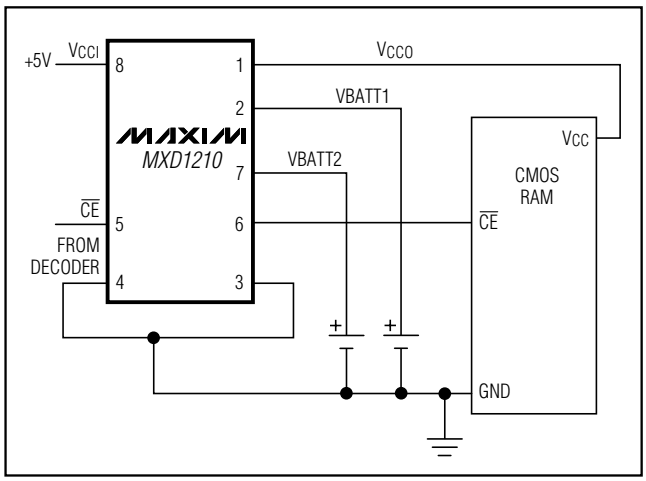


DIP/SO



WIDE SO

Typical Operating Circuit



Nonvolatile RAM Controller

ABSOLUTE MAXIMUM RATINGS

V_{CCI} to GND .....-0.3V to +7.0V
VBATT1 to GND.....-0.3V to +7.0V
VBATT2 to GND.....-0.3V to +7.0V
V_{CCO} to GND .....-0.3V to (V_S + 0.3V)
(V_S = greater of V_{CCI}, VBATT1, VBATT2)
Digital Input and Output
Voltages to GND.....-0.3V to (V_{CCI} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
8-Pin PDIP (derate 9.09mW/°C above +70°C).....727mW
8-Pin SO (derate 5.88mW/°C above +70°C).....471mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C).....640mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) 762mW
Operating Temperature Range
C Suffix.....0°C to +70°C
E Suffix.....-40°C to +85°C
M Suffix .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CCI}	TOL = GND	4.75		5.50	V
		TOL = V_{CCO}	4.50		5.50	
Input High Voltage	V_{IH}		2.2			V
Input Low Voltage	V_{IL}				0.8	V
Battery Voltage	VBATT1 VBATT2	1 or 2 batteries (Note 1)	2.0		4.0	V

ELECTRICAL CHARACTERISTICS—Normal Supply Mode, TOL = V_{CCO}

(V_{CCI} = +4.75V to +5.5V, TOL = GND; or V_{CCI} = +4.5V to +5.5V, TOL = V_{CCO}; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	I_{CCI}	V_{CCO}, $\overline{CEO}$ open, VBATT1 = VBATT2 = 3V			0.23	0.5	mA
Output Supply Voltage	V_{CCO}	I_{CCO1} = 80mA (Note 2)	MXD1210C	V_{CCI} - 0.20			V
			MXD1210E	V_{CCI} - 0.21			
			MXD1210M	V_{CCI} - 0.25			
Output Supply Current	I_{CCO}	V_{CCI} - V_{CCO} ≤ 0.2V (Note 2)	MXD1210C			80	mA
			MXD1210E		0.23	75	
			MXD1210M		0.23	65	
Input Leakage Current	I_{IL}					±1.0	µA
Output Leakage Current	I_{OL}					±1.0	µA
High-Level Output Voltage	V_{OH}	I_{OH} = -1mA		2.4			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 4mA				0.4	V
V_{CCI} Trip Point	V_{CCTP}	TOL = GND		4.50		4.74	V
		TOL = V_{CCO}		4.25		4.49	

ELECTRICAL CHARACTERISTICS—Battery-Backup Mode

(V_{CCI} < V_{BATT}, positive edge rate at VBATT1, VBATT2 > 0.1V/µs, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Current (Note 1)	I_{BATT}	V_{CCO}, $\overline{CEO}$ open, V_{CCI} = 0V	MXD1210C/E		2	100	nA
			MXD1210M			5	µA
Output Supply Current	I_{CCO2}	V_{BATT} - V_{CCO} ≤ 0.2V (Notes 3, 4)				300	µA
$\overline{CEO}$ Output Voltage	V_O	Output open		V_{BATT} - 0.2			V

CAPACITANCE

(T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_{IN}				5	pF
Output Capacitance	C_{OUT}				7	pF

V_{CC} POWER TIMING CHARACTERISTICS

(V_{CCI} = +4.75V to +5.5V, TOL = GND; or V_{CCI} = +4.5V to +5.5V, TOL = V_{CCO}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{CE}$ Propagation Delay	t_{PD}	R_L = 1kΩ, C_L = 50pF	MXD1210C	5	10	20	ns
			MXD1210E	5	10	22	
			MXD1210M	5	10	25	
$\overline{CE}$ High to Power-Fail	t_{PF}	(Note 5)			0		ns

TIMING CHARACTERISTICS

(V_{CCI} < +4.75V to +5.5V, TOL = GND; or V_{CCI} < +4.5V, TOL = V_{CCO}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Recovery at Power-Up	t_{REC}		2	5	20	ms
V_{CC} Slew-Rate Power-Down	t_F	To out-of-tolerance condition	300			µs
	t_{FB}	Tolerance to battery power	10			
V_{CC} Slew-Rate Power-Up	t_R		0			µs
$\overline{CE}$ Pulse Width	t_{CE}	(Note 6)			1.5	µs

Note 1: Only one battery input is required. Unused battery inputs must be grounded.
Note 2: I_{CCO1} is the maximum average load current the MXD1210 can supply to the memories.
Note 3: I_{CCO2} is the maximum average load current the MXD1210 can supply to the memories in battery-backup mode.
Note 4: $\overline{CEO}$ can sustain leakage current only in battery-backup mode.
Note 5: Guaranteed by design.
Note 6: t_{CE} max must be met to ensure data integrity on power loss.

Nonvolatile RAM Controller

Pin Description

PIN		NAME	FUNCTION
8-PIN PDIP/SO	16-PIN WIDE SO		
1	2	V_{CCO}	Backed-Up Supply to RAM
2	4	VBATT1	Battery 1 Positive Connection
3	6	TOL	Tolerance Select Pin
4	8	GND	Ground
5	9	$\overline{CE}$	Chip-Enable Input
6	11	$\overline{CEO}$	Chip-Enable Output
7	13	VBATT2	Battery 2 Positive Connection
8	15	V_{CCI}	5V Power Supply to Chip
—	1, 3, 5, 7, 10, 12, 14, 16	N.C.	No Connection. Not internally connected.

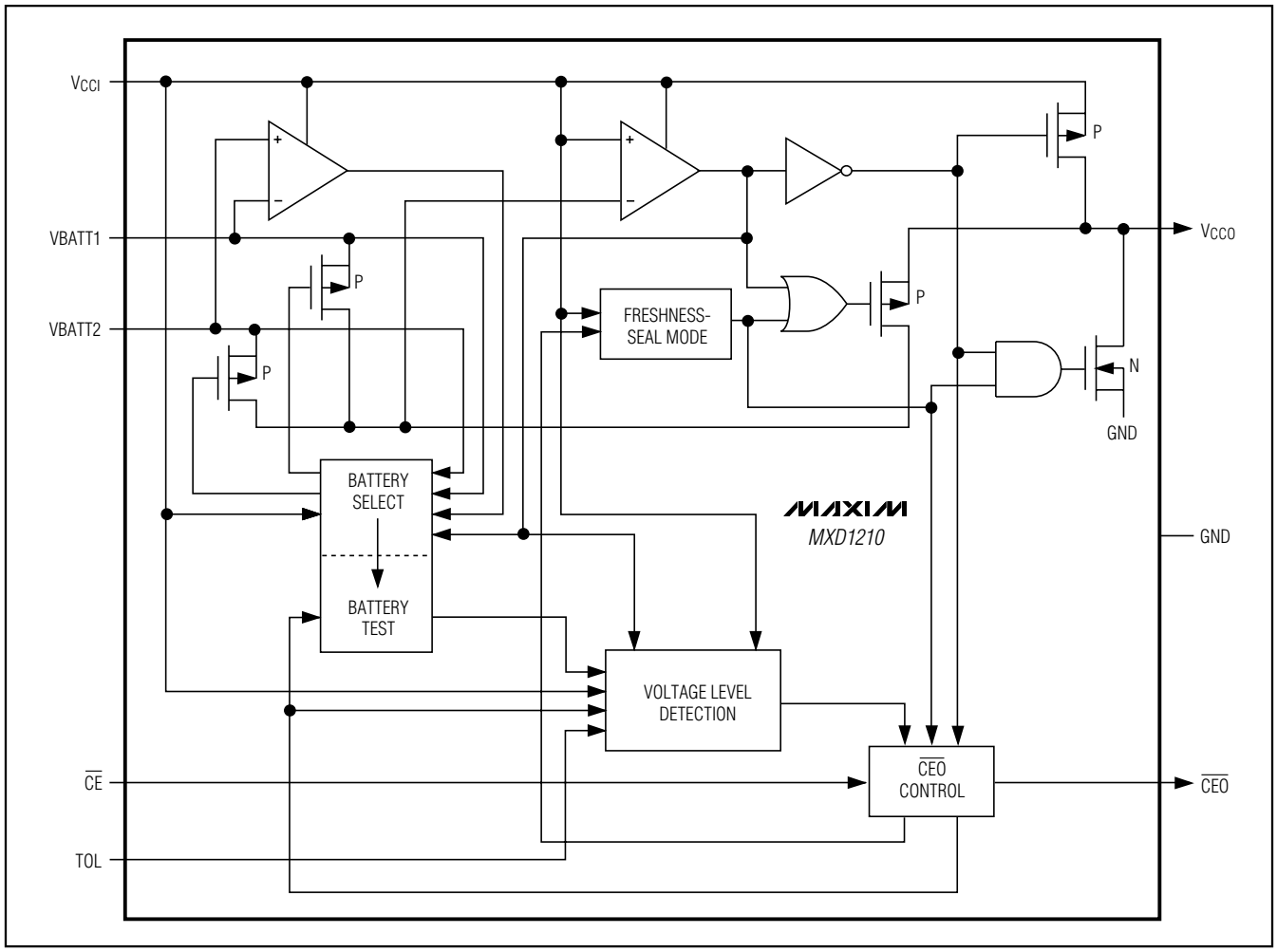


Figure 1. Block Diagram

Detailed Description

Main Functions

The MXD1210 executes five main functions to perform reliable RAM operation and battery backup (see the *Typical Operating Circuit* and Figure 1):

1) RAM Power-Supply Switch: The switch directs power to the RAM from the incoming supply or from the selected battery, whichever is at the greater voltage. The switch control uses the same criterion to direct power to MXD1210 internal circuitry.

2) Power-Failure Detection: The write-protection function is enabled when a power failure is detected. The power-failure detection range depends on the state of the TOL pin as follows:

CONDITION	V_{CCTP} RANGE (V)
TOL = GND	4.75 to 4.50
TOL = V_{CCO}	4.50 to 4.25

Power-failure detection is independent of the battery-backup function and precedes it sequentially as the power-supply voltage drops during a typical power failure.

3) Write Protection: This holds the chip-enable output ($\overline{CEO}$) to within 0.2V of V_{CCI} or of the selected battery, whichever is greater. If the chip-enable input ($\overline{CE}$) is low (active) when power failure is detected, then $\overline{CEO}$ is held low until $\overline{CE}$ is brought high, at which time $\overline{CEO}$ is gated high for the duration of the power failure. The preceding sequence completes the current RD/WR cycle, preventing data corruption if the RAM access is a WR cycle.

4) Battery Redundancy: A second battery is optional. When two batteries are connected, the stronger battery is selected to provide RAM backup and to power the MXD1210. The battery-selection circuitry remains active while in the battery-backup mode, selecting the stronger battery and isolating the weaker one. The battery-selection activity is transparent to the user and the system. If only one battery is connected, the second battery input should be grounded.

5) Battery-Status Warning: This notifies the system when the stronger of the two batteries measures ≤ 2.0V. Each time the MXD1210 is repowered (V_{CCI} > V_{CCTP}) after detecting a power failure, the battery voltage is measured. If the battery in use is low, following the MXD1210 recovery period, the device issues a warning to the system by inhibiting the second memory cycle. The sequence is as follows:

First access: read memory location n, loc(n) = x

Second access: write memory location n,

loc(n) = complement (x)

Third access: read memory location n, loc(n) = ?

If the third access (read) is complement (x), then the battery is good; otherwise the battery is not good. Return to loc(n) = x following the test sequence.

Freshness-Seal Mode

The freshness-seal mode relates to battery longevity during storage rather than directly to battery backup. This mode is activated when the first battery is connected, and is defeated when the voltage at V_{CCI} first exceeds V_{CCTP}. In the freshness-seal mode, both batteries are isolated from the system; that is, no current is drained from either battery, and the RAM is not powered by either battery. This means that batteries can be installed and the system can be held in inventory without battery discharge. The positive edge rate at VBATT1 and VBATT2 should exceed 0.1V/µs. The batteries will maintain their full shelf life while installed in the system.

Battery Backup

The *Typical Operating Circuit* shows the MXD1210 connected to write-protect the RAM when V_{CC} is less than 4.75V, and to provide battery backup to the supply.

Nonvolatile RAM Controller

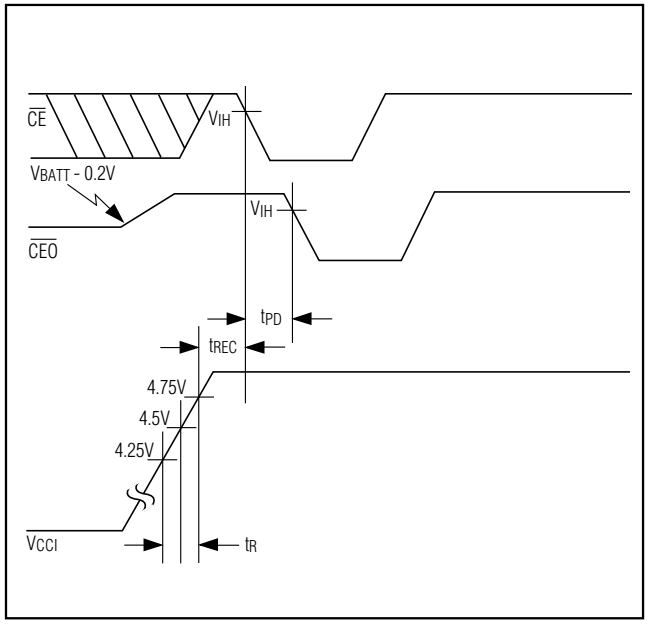


Figure 2. Power-Up Timing Diagram

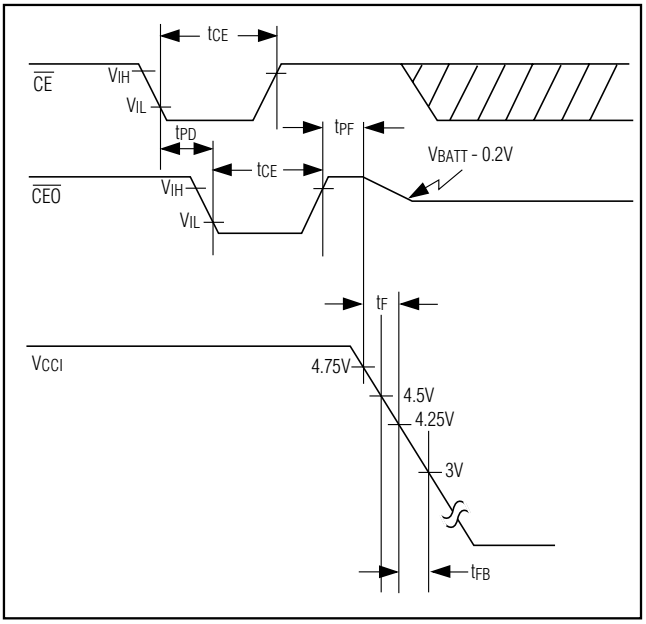
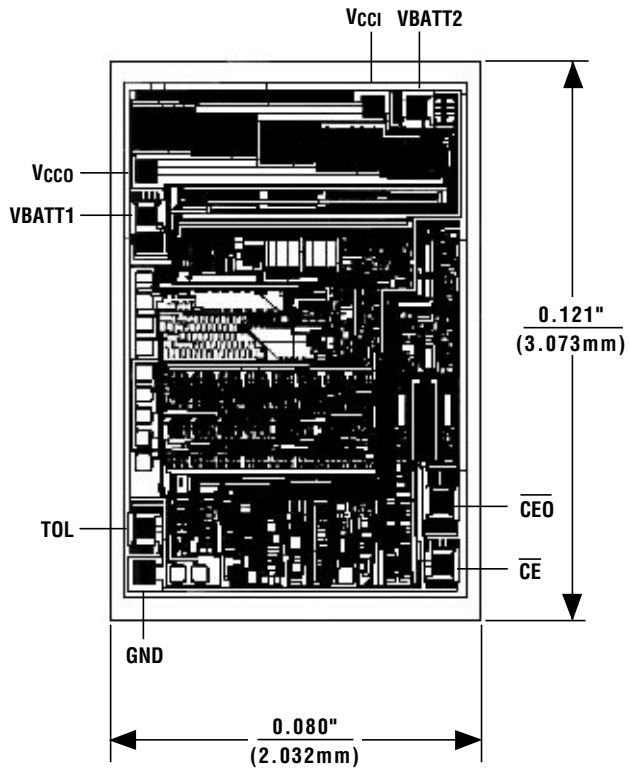


Figure 3. Power-Down Timing Diagram

Chip Topography



TRANSISTOR COUNT: 1436;
LEAVE SUBSTRATE UNCONNECTED.

Nonvolatile RAM Controller

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

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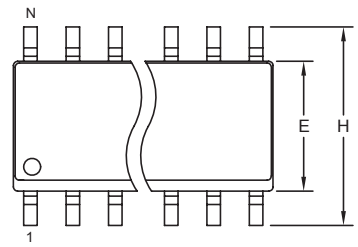
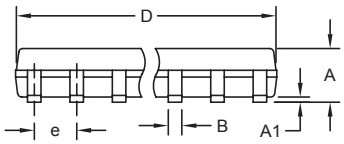
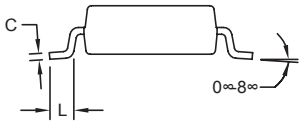


TOP VIEW



FRONT VIEW



SIDE VIEW

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

VARIATIONS:

DIM	INCHES		MILLIMETERS		N	MS012
	MIN	MAX	MIN	MAX		
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, .150" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	B	1/1