MxL76125

22V, 15A, Synchronous Buck Regulator with 2-Bit VID

December 20, 2022

Description

The MxL76125 device is a synchronous step-down regulator combining the controller, driver, bootstrap diode, and MOSFETs in a single package for point-of-load supplies. The MxL76125 device is rated for 15A load. A wide input voltage range from 5V to 22V allows for single supply operation from industry standard 5V, 12V, and 20V rails.

With a proprietary emulated current mode constant on-time (COT) control scheme, the MxL76125 device provides extremely fast line and load transient response using ceramic output capacitors. The controller does not require any external loop compensation, which simplifies the circuit implementation and reduces the overall component count. It also provides 0.1% load and 0.1% line regulation, and maintains constant switching frequency. A selectable power saving mode enables operation in discontinuous conduction mode (DCM) at light loads, thereby significantly increasing the converter efficiency.

The MxL76125 has a 2-bit VID, meeting the core rail requirements of MaxLinear's MxL317xx Wi-Fi 7 SoCs. The VID allows the Wi-Fi 7 SoC to optimize performance while minimizing power consumption in both active and idle states by dynamically changing the output voltage of the MxL76125.

A host of protection features, including overcurrent, over temperature, overvoltage, short-circuit, and UVLO, helps achieve safe operation under abnormal operating conditions.

The MxL76125 device is available in a RoHS compliant, green/halogen-free space-saving 4mm x 5mm QFN package.

FEATURES

- 15A step-down regulator
  - Low V_{IN} operation from 4.5V to 5.5V
  - Wide single input voltage from 5V to 22V
  - V_{IN} operation from 1V to 22V with external 5V bias
  - ≥0.6V adjustable output voltage
  - 2-bit VID for MaxLinear Wi-Fi 7 SoCs
  - Adjustable VID resolution through R_{REF}
- Proprietary constant on-time control
  - No loop compensation required
  - Stable operation with ceramic output capacitors
  - Programmable on-time ≥ 40ns
  - Constant 200kHz-1.25MHz frequency
  - Selectable forced CCM or CCM/DCM operation
- Output over-voltage, over-current and over-temperature protections
- Power-good flag with low impedance when power is removed
- Precision enable
- Programmable soft-start time
- 4mm x 5mm QFN package

APPLICATIONS

- MaxLinear Wi-Fi SoC core rail
- Puma® and AnyWAN® based CPE
- Servers
- Distributed power architecture
- FPGA, DSP and processor supplies
- Base stations, switches/routers

For more details about the ordering information, see "Ordering Information" on page 20.

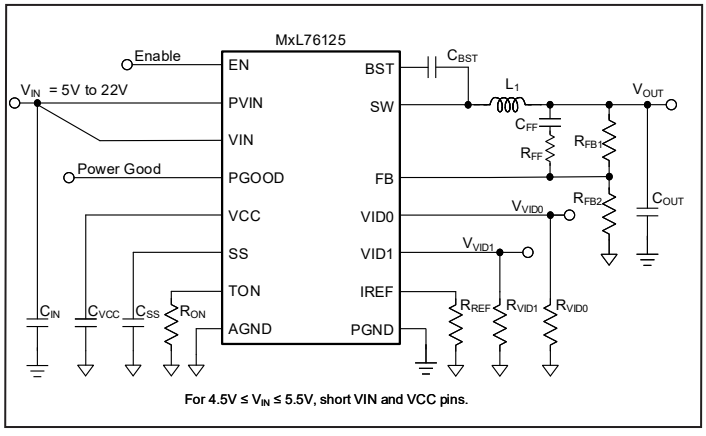


Figure 1. MxL76125 Typical Application Diagram

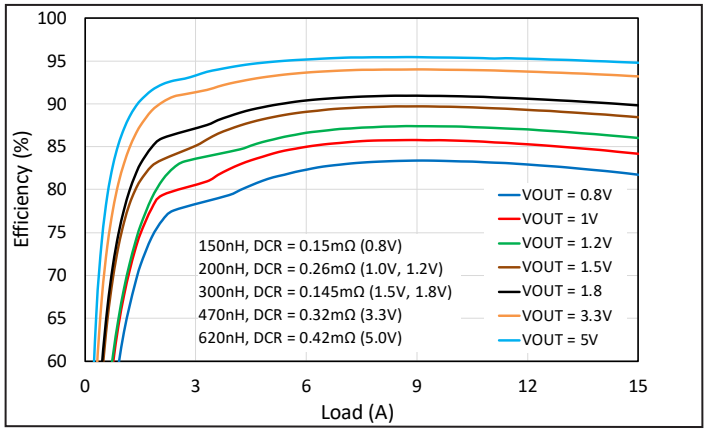


Figure 2. Efficiency at V_{IN}=12V and F_{SW} = 1MHz

Absolute Maximum Ratings

These are stress ratings only and functional operation of the device at these ratings is not implied. Stresses beyond these ratings may cause permanent damage to the device. Exposure to any absolute maximum rating condition for extended periods may affect device reliability and lifetime.

PV_{IN}, V_{IN} ..... From -0.3V to 25V

V_{CC} ..... From -0.3V to 6.0V

BST ..... From -0.3V to 31V(1)

BST-SW ..... From -0.3V to 6V

SW ..... From -1V to 25V(1)(2)

All other pins ..... From -0.3V to V_{CC} + 0.3V

Storage temperature ..... From -65°C to 150°C

Power dissipation ..... Internally limited

Lead temperature (soldering, 10 second) ..... 300°C

ESD rating (Human body model–HBM) ..... ±2kV

ESD rating (Charged device model–CDM) ..... ±500V

Operating Conditions

These are the conditions under which the device is intended to function.

PV_{IN} ..... From 1V to 22V

V_{IN} ..... From 4.5V to 22V

V_{CC} ..... From 4.5V to 5.5V

SW, ... From -1V to 22V(2)

PGOOD, TON, SS, EN ..... From -0.3V to 5.5V

Switching frequency ..... From 200kHz to 1.25MHz(3)

Junction temperature range (T_J) ..... From -40°C to 125°C

Power dissipation max at T_A = 70°C 2.46W

Package thermal resistance, junction to ambient, θ_{JA} ..... 21°C/W(4)

Junction-to-bottom thermal characteristic parameter, ψ_{JB} ..... 7°C/W(4)

NOTES:

1. No external voltage applied.
2. SW pin can go ±5V away with respect to the steady state value during switch transition, for 50ns.
3. Typical.
4. Thermal simulation data.

Electrical Characteristics

Specifications are for operating junction temperature of T_J = 25°C only; limits applying over the full operating junction temperature range are denoted by a •. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise indicated, PVIN is not connected, V_{IN} = 12V, SW = AGND = PGND = 0V, C_{VCC} = 4.7uF.

Symbol	Parameter	Conditions	•	Min	Typ	Max	Units
Power Supply Characteristics							
V_{IN}	Input voltage range	V_{CC} regulating	•	5	12	22	V
		V_{CC} tied to V_{IN}		4.5	5.0	5.5	
I_{VIN}	V_{IN} supply current	Not switching, V_{IN} = 12V, V_{FB} = 0.7V	•	-	0.8	1	mA
I_{VCC}	V_{CC} quiescent current	Not switching, V_{CC} = V_{IN} = 5V, V_{FB} = 0.7V	•	-	0.8	1	mA
I_{VIN}	V_{IN} supply current	F_{SW} = 1MHz, V_{IN} = PV_{IN} = 12V	•	18.9	20	21	mA
I_{OFF}	Shutdown current	Enable = 0V, PV_{IN} = V_{IN} = 12V		-	-	1	µA
Enable, FCCM and CCM/DCM Modes of Operation							
$V_{IH\_EN\_FCCM}$	EN pin rising threshold for FCCM operation	-	•	1.8	1.9	2.0	V
$V_{EN\_HYS\_FCCM}$	EN pin hysteresis for FCCM operation	-		-	50	-	mV
$V_{IH\_EN\_DCM}$	EN pin rising threshold for CCM/DCM operation	-	•	2.9	3	3.1	V
$V_{EN\_HYS\_DCM}$	EN pin hysteresis for CCM/DCM operation	-		-	100	-	mV

Electrical Characteristics (Continued)

Specifications are for operating junction temperature of T_J = 25°C only; limits applying over the full operating junction temperature range are denoted by a •. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise indicated, PVIN is not connected, V_{IN} = 12V, SW = AGND = PGND = 0V, C_{VCC} = 4.7uF.

Symbol	Parameter	Conditions	•	Min	Typ	Max	Units
VID Levels							
V_{IREF}	IREF pin voltage	-	•	544	556	569	mV
I_{FB}	FB pin sourcing current	VID1 = 0b0, VID0 = 0b0, R_{REF} = 56.2kΩ ±1%	•	-10	0	10	nA
		VID1 = 0b0, VID0 = 0b1, R_{REF} = 56.2kΩ ±1%	•	-10.1	-9.91	-9.72	µA
		VID1 = 0b1, VID0 = 0b0, R_{REF} = 56.2kΩ ±1%	•	9.72	9.91	10.1	µA
		VID1 = 0b1, VID0 = 0b1, R_{REF} = 56.2kΩ ±1%	•	19.44	19.82	20.2	µA
-	VID logic low threshold	-	•	-	-	0.4	V
-	VID logic high threshold	-	•	2.4	-	-	V
Undervoltage Lock-Out UVLO							
-	V_{CC} UVLO start threshold, rising edge	-	•	4.00	4.25	4.40	V
-	V_{CC} UVLO hysteresis	-	•	100	170	-	mV
Feedback Reference Voltage							
V_{FB}	Feedback reference voltage	V_{IN} = 5V-22V, V_{CC} regulating		0.597	0.600	0.603	V
		V_{IN} = 4.5V-5.5V, V_{CC} tied to V_{IN}		0.596	0.600	0.604	V
		V_{IN} = 5V-22V, V_{CC} regulating V_{IN} = 4.5V-5.5V, V_{CC} tied to V_{IN}	•	0.594	0.600	0.606	V
-	DC load regulation	CCM operation, closed loop, applies to any C_{OUT}		-	±0.1	-	%
-	DC line regulation			-	±0.1	-	%
Programmable Constant On-Time							
-	On-time 1	R_{ON} = 1.82kΩ, PV_{IN} = 12V		-	78	-	ns
-	f corresponding to on-time 1	V_{OUT} = 0.8V, Load = 11.5A, Efficiency = 81%		-	1	-	MHz
-	On-time 2	R_{ON} = 8.66kΩ, PV_{IN} = 12V		-	275	-	ns
-	f corresponding to on-time 2	V_{OUT} = 3.3V, Load = 8.4A, Efficiency = 94%		-	1	-	MHz
Minimum Off-Time							
-	Minimum off-time	-	•	-	250	350	ns
Soft-Start							
I_{SS_CHARGE}	Charge current	-	•	-14	-10	-6	µA
$I_{SS\_DISCHARGE}$	Discharge current	Fault present	•	1	3	-	mA
V_{CC} Linear Regulator							
V_{CC}	Output voltage	V_{IN} = 6V-22V, I_{LOAD} = 0-30mA	•	4.8	5.0	5.2	V
	Dropout voltage	I_{LOAD} = 0-30mA	•	100	300	490	mV

Electrical Characteristics (Continued)

Specifications are for operating junction temperature of T_J = 25°C only; limits applying over the full operating junction temperature range are denoted by a •. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise indicated, PVIN is not connected, V_{IN} = 12V, SW = AGND = PGND = 0V, C_{VCC} = 4.7uF.

Symbol	Parameter	Conditions	•	Min	Typ	Max	Units
Power Good Output							
-	Power good threshold	-		-10	-7.5	-5	%
-	Power good hysteresis	-		-	1	4	%
-	Power good de-assertion voltage	Maximum ISINK = 1mA		-	-	0.2	V
-	Power good, unpowered (V_{IN} = 0)	ISINK = 1mA		-	-	0.5	V
-	Power good assertion delay, FB rising	-		-	2	-	ms
-	Power good de-assertion delay, FB falling	-		-	65	-	µs
OVP Detect							
-	OVP trip high threshold	V_{FB} rising. Specified as % of V_{REF}	•	115	120	125	%
-	OVP trip low threshold	V_{FB} falling. Specified as % of V_{REF}	•	-	115	-	%
-	OVP comparator delay	V_{FB} rising	•	0.5	1	3.5	µs
-	Delay to turn off power stage from an overvoltage event	V_{FB} rising	•	-	-	3.5	µs
Protection: OCP, OTP, Short-Circuit							
-	Hiccup timeout	-	•	102	105	107	ms
-	OCP threshold (Valley current)	-		-	20	-	A
-	Current limit blanking	-		-	100	-	ns
-	Thermal shutdown threshold	Rising temperature		-	138	-	°C
-	Thermal hysteresis	-		-	15	-	°C
-	Feedback pin short-circuit threshold	• % of V_{REF} • Short-circuit is active • Soft-start completed	•	50	60	70	%
MxL76125 Output Power Stage							
-	High-side MOSFET $R_{DS(ON)}$	I_{DS} = 2A		-	9	-	mΩ
-	Low-side MOSFET $R_{DS(ON)}$	I_{DS} = 2A		-	3.6	-	mΩ
-	Rated output current		•	15	-	-	A
Thermal Resistance							
-	Junction to package top	-	•	-	37.4	-	°C/W
-	Junction to package bottom	-	•	-	5.6	-	°C/W

Pin Configuration

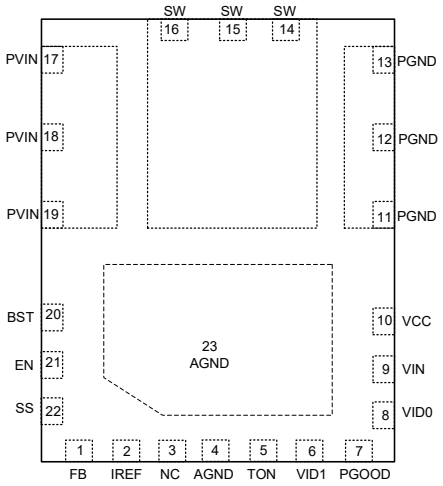


Figure 3. MxL76125 Pin Configuration (Top View)

Pin Functions

Pin Number	Pin Name	Type	Description
1	FB	Analog	Input to the feedback comparator. The reference is fixed at 600mV.
2	IREF	Analog	VID reference current setting pin. Connect a 56.2kΩ resistor to AGND.
3	NC	None	Not connected.
4	AGND	Analog	Signal ground for control circuitry. Internally connected to AGND pad.
5	TON	Analog	Constant on-time programming pin. Connect a resistor to AGND.
6	VID1	Input	MSB of the 2-bit VID reference. Connect a pulldown resistor, R_{VID1} to AGND. It should not be floating.
7	PGOOD	Output, open drain	Power-good output. Open drain to AGND. Low Z when IC unpowered.
8	VID0	Input	LSB of the 2-bit VID reference. Connect a pulldown resistor, R_{VID0} to AGND. It should not be floating.
9	VIN	Analog	Supply input for the regulator's LDO. Connect to PVIN at CIN.
10	VCC	Analog	The output of regulators LDO. It requires a 4.7µF VCC bypass capacitor. For V_{IN} = 5V, VCC should be tied to VIN.
11, 12, 13	PGND	Power	Ground of the power stage. Internally connected to source of the low-side MOSFET.
14, 15, 16	SW	Power	Switch node. Internally it connects source of the high-side MOSFET to drain of the low-side MOSFET.
17, 18, 19	PVIN	Power	Input voltage for power stage. Internally connected to drain of the high-side MOSFET.
20	BST	Analog	High-side driver power supply pin. Connect a 1uF boot-strap capacitor between BST and SW pins.
21	EN	Input	Precision enable input. The voltage level decides FCCM and CCM/DCM modes of operation. For details, see "Electrical Characteristics" on page 2.
22	SS	Analog	Soft start pin. Connect an external capacitor between SS and AGND to program the softstart rate based on a 10µA internal source current.
23	AGND PAD	Analog	Signal ground for control circuitry.

Typical Performance Characteristics

Unless otherwise specified: V_{IN} = 12V, V_{OUT} = 0.8V, F_{SW} = 1MHz, VCC = 5.0V internally generated, C_{OUT} = 265µF, L = 150nH (DCR = 0.15mΩ), C_{FF} = 470pF, R_{FF} = 0Ω, R_{FB1} = 4.99kΩ, R_{FB2} = 15kΩ, FCCM mode of operation, $T_{AMBIENT}$ = 25°C, and no airflow. Efficiency data includes inductor losses.

Efficiency

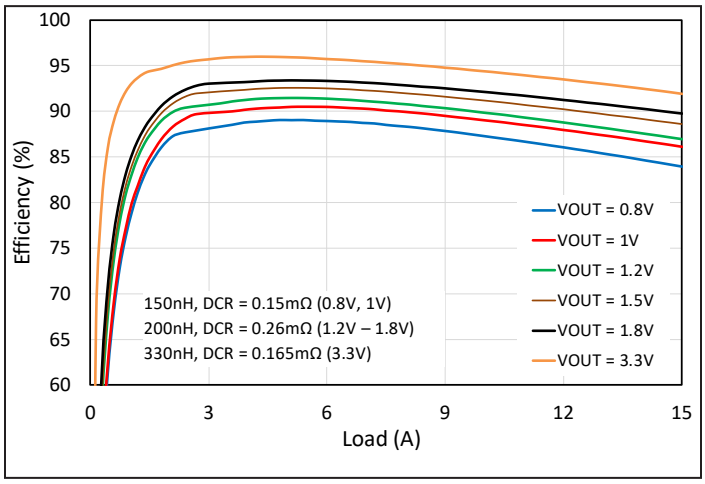


Figure 4. Efficiency at 5V Input in FCCM (VIN and VCC are shorted)

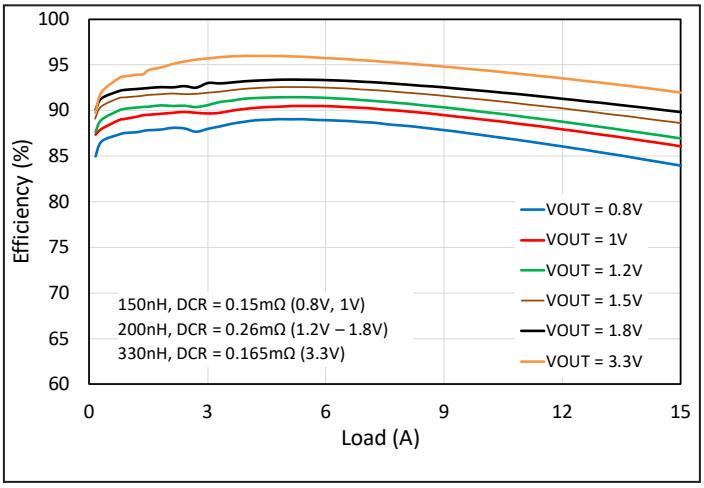


Figure 5. Efficiency at 5V Input in DCM (VIN and VCC are shorted)

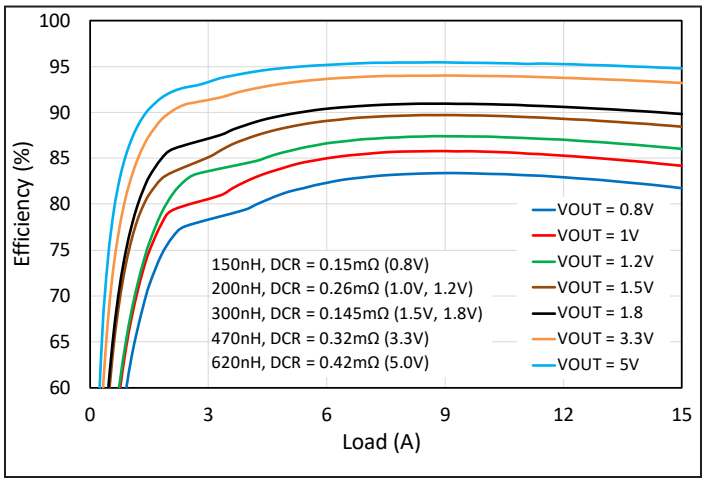


Figure 6. Efficiency at 12V Input in FCCM

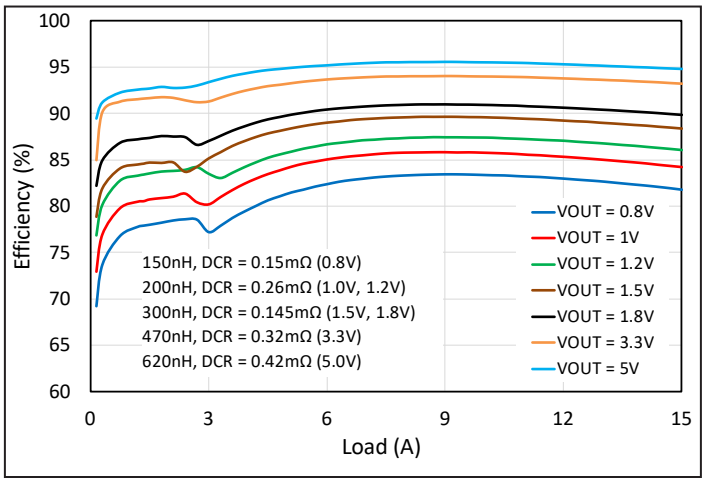


Figure 7. Efficiency at 12V Input in DCM

Startup Sequence

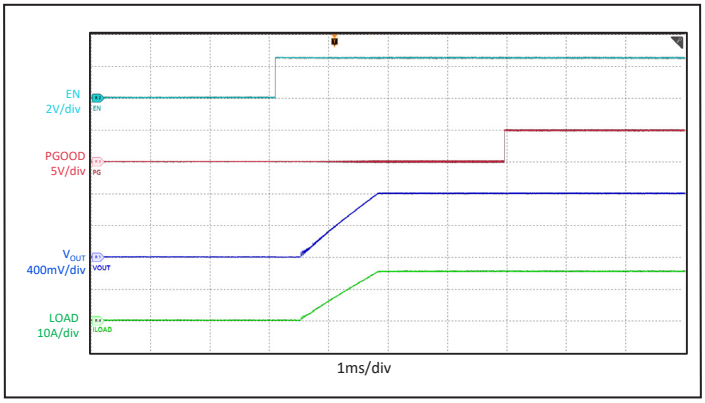


Figure 8. Power-up: I_{OUT} = 15A at 0.8V

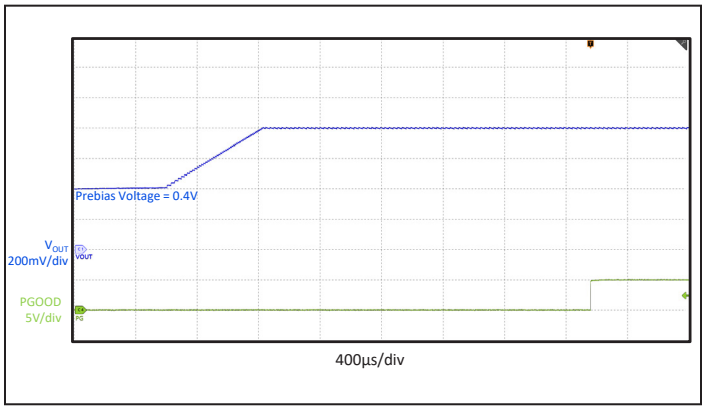


Figure 9. Startup with Prebias Voltage of 400mV: I_{OUT} = 20mA

Shutdown Sequence

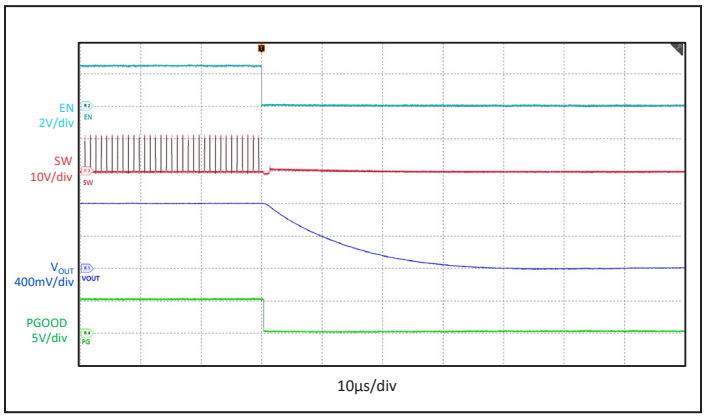


Figure 10. Power Down: I_{OUT} = 15A at 0.8V

Steady State V_{OUT} Ripple

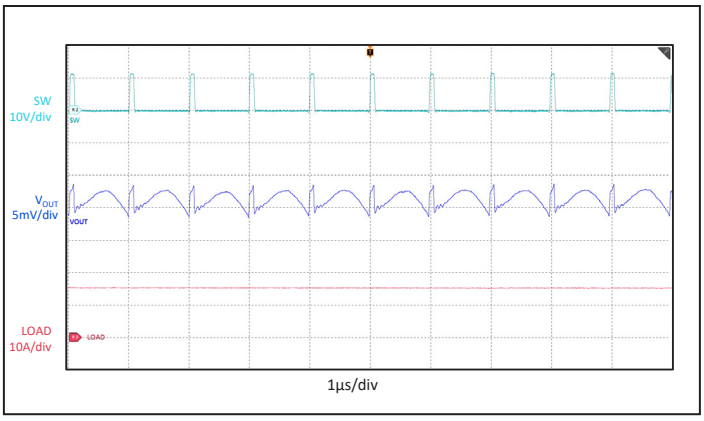


Figure 11. Steady State V_{OUT} Ripple: I_{OUT} = 15A, V_{OUT} = 0.8V

DVS

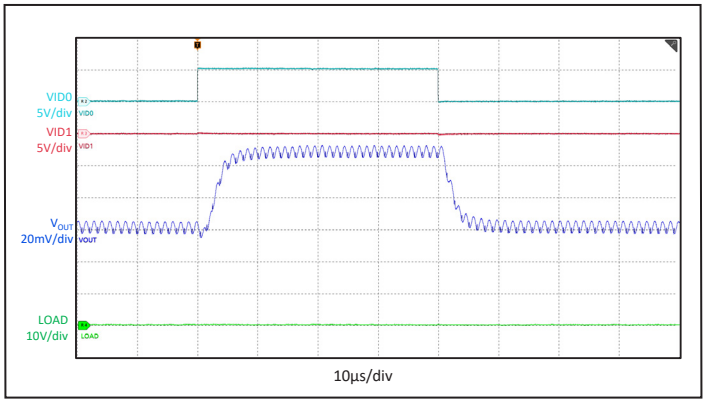


Figure 12. DVS: V_{OUT} = 0.8V to 0.85V and Back; I_{OUT} = 0A; Settling Time = ~4µs

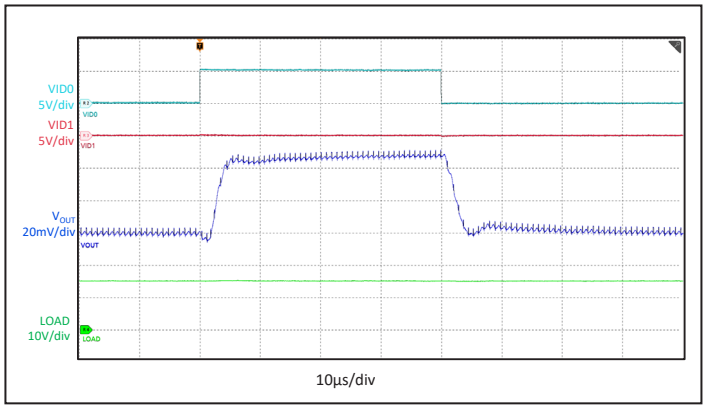


Figure 13. DVS: V_{OUT} = 0.8V to 0.85V and Back; I_{OUT} = 15A; Settling Time = ~4µs

Load Transients

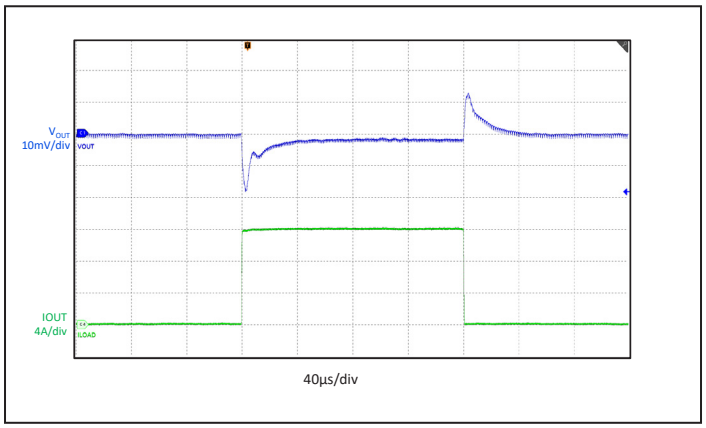


Figure 14. Load Transient from 1.5A to 13.5A and Back in FCCM (C_{OUT} = 350µF)

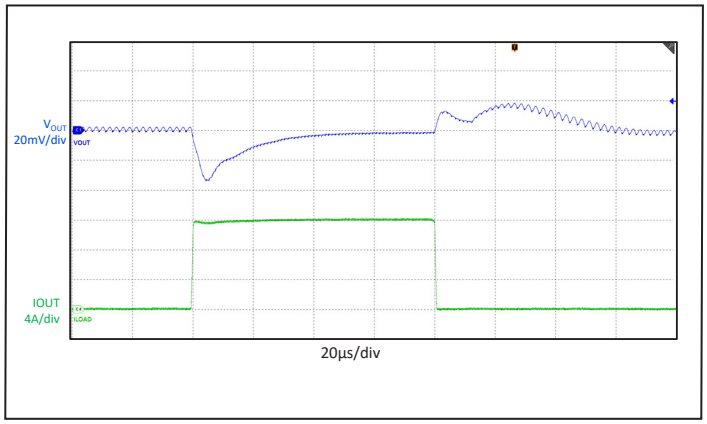


Figure 15. Load Transient from 1.5A to 13.5A and Back in DCM (C_{OUT} = 350µF)

FCCM-DCM Transition

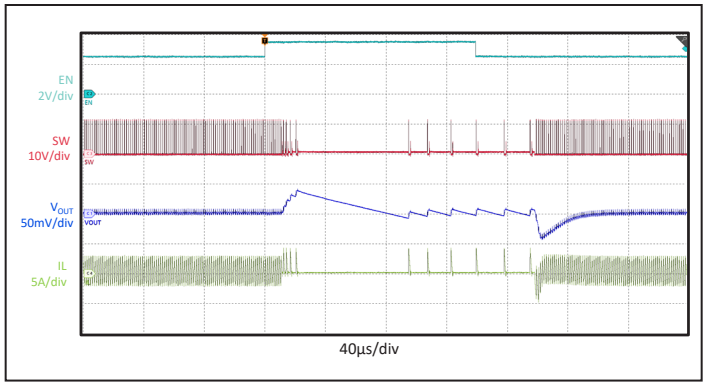


Figure 16. FCCM Mode to DCM Mode and Back: I_{OUT} = 100mA

Short Circuit Recovery

FB pin momentary shorted with AGND

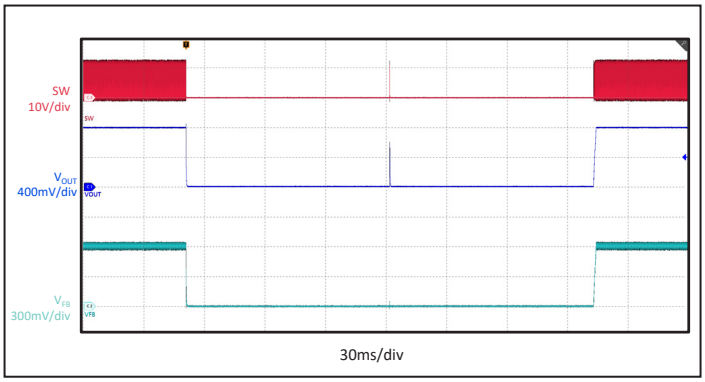


Figure 17. Short Circuit Hiccup and Recovery

Over Current Protection

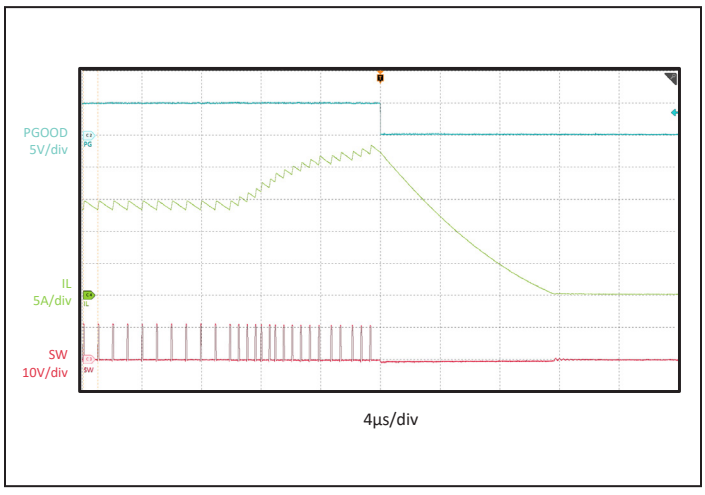


Figure 18. Shutdown during Over Current

Line Regulation

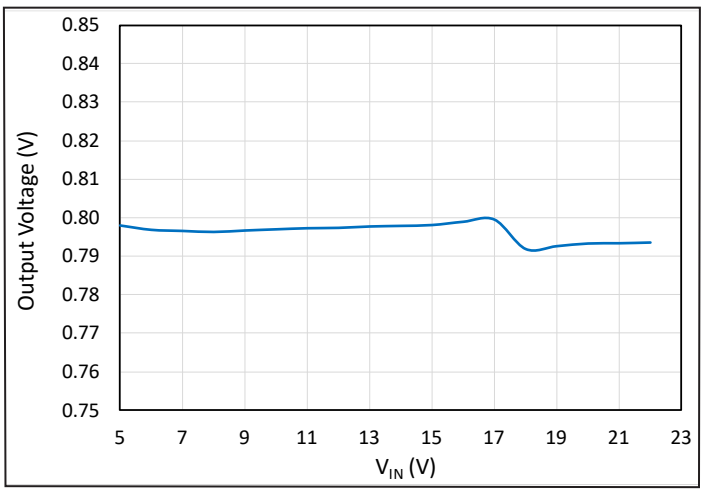


Figure 19. Line Regulation

Load Regulation

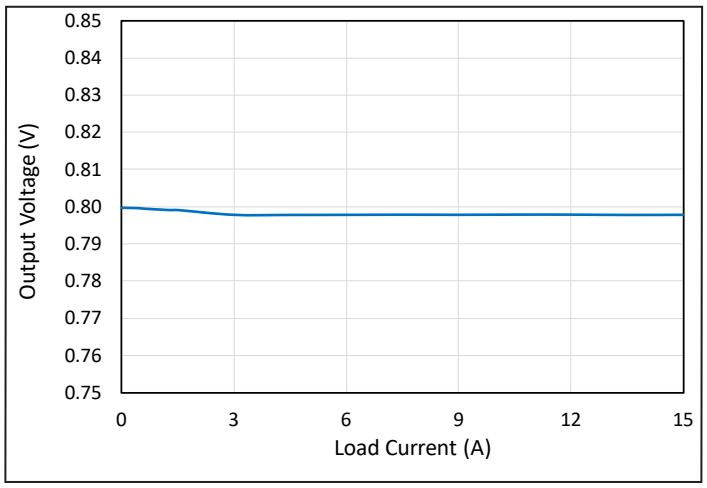


Figure 20. Load Regulation

T_{ON} vs R_{ON} Correlation

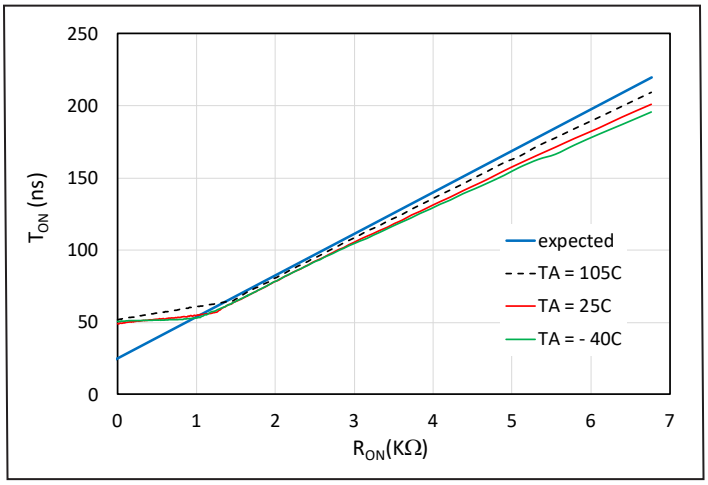


Figure 21. T_{ON} vs R_{ON} Correlation: I_{OUT} = 15A

Frequency vs I_{OUT}

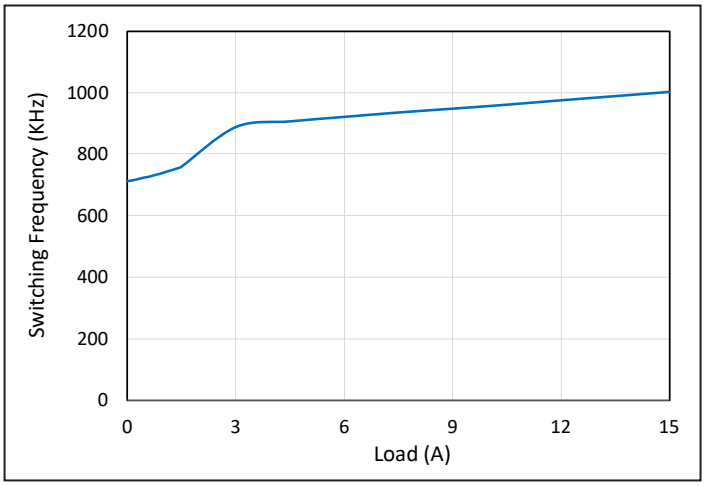


Figure 22. Switching Frequency vs IOUT

V_{FB} Variation with Temperature

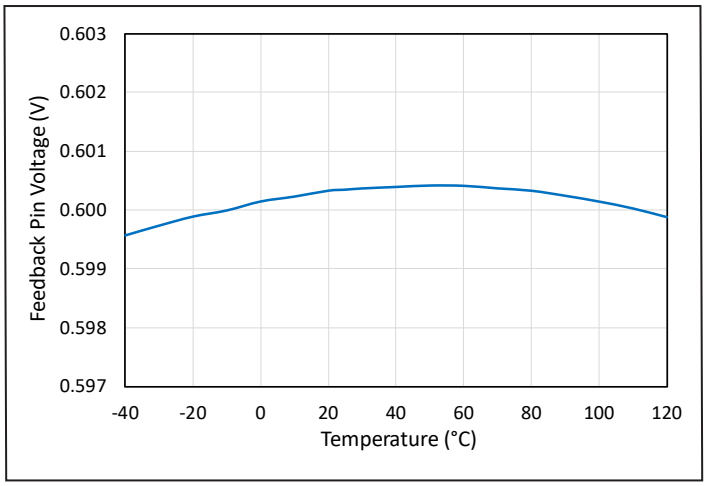


Figure 23. V_{FB} Variation across Temperature: I_{OUT} = 0A

Thermal Derating Curves

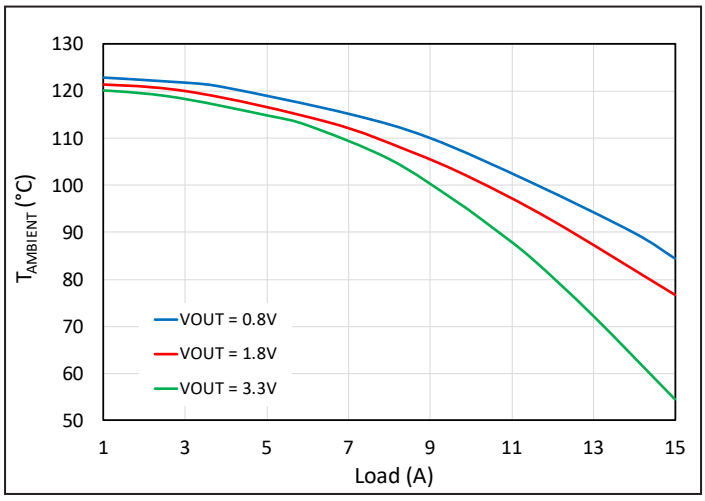


Figure 24. Maximum Ambient Temperature vs. Load Current, V_{IN} = 5V

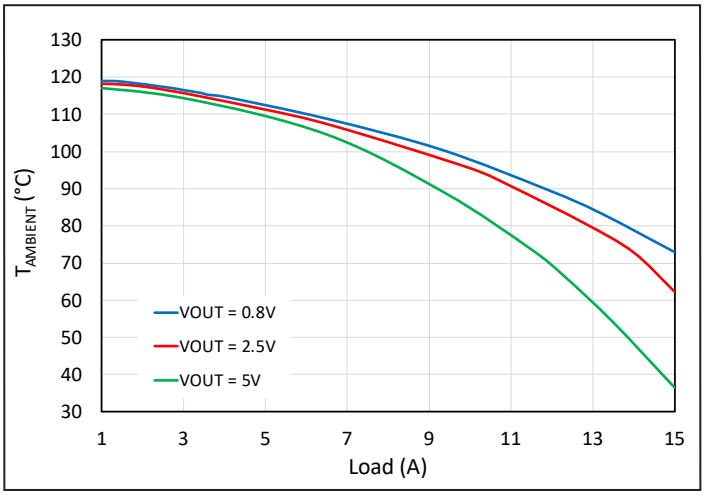


Figure 25. Maximum Ambient Temperature vs. Load Current, V_{IN} = 12V

Functional Block Diagram

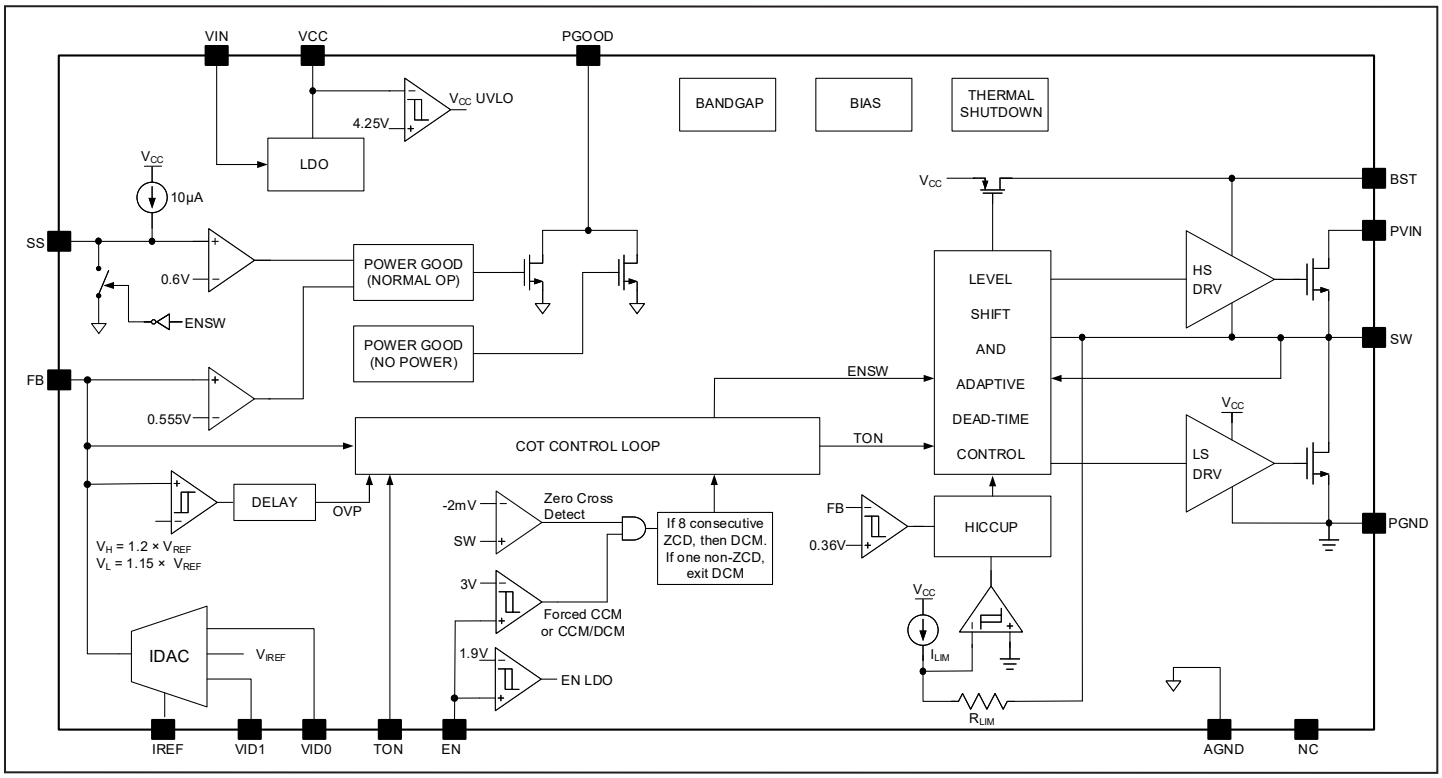


Figure 26. MxL76125 Functional Block Diagram

Applications Information

Detailed Operation

The MxL76125 device is a 15A synchronous step-down switching voltage regulator with a 2-bit VID. MOSFETs, controller, driver, and bootstrap diode are combined in a single package for point-of-load supplies. The output voltage and VID step size are adjustable by external components. The 2-bit VID functionality is targeted to meet core rail requirements of MaxLinear's MxL317xx Wi-Fi 7 SoCs. The VID enables the Wi-Fi SoC to dynamically change the output voltage to switch between active and power saving idle states.

The MxL76125 uses a proprietary emulated current-mode constant on-time (COT) control scheme. The on-time (T_{ON}) is programmable by an external resistor (R_{ON}) and is inversely proportional to V_{IN}. The latter feature offers nearly constant switching frequency over a large V_{IN} range. The emulated current-mode control allows you to use ceramic capacitors (low ESR) in the output filter.

The MxL76125 can operate in both, forced continuous conduction mode (FCCM) for low switching ripple and power saving discontinuous conduction mode (DCM) at light loads. The mode is set by EN voltage levels, as described in the "Enable Input" section.

Enable Input

The enable input (EN) is a high impedance input pin and accepts a tri-level signal. The voltage levels and corresponding functionalities are as follows:

- EN < 1.7V: The MxL76125 is off.
- 2.0V≤ EN < 2.8V: The MxL76125 runs in FCCM mode at all loads.
- EN ≥ 3.1V: The MxL76125 runs in DCM at light loads.

FCCM Mode

This mode is active when the EN pin voltage is between 2.0V and 2.8V. The pin voltage can be controlled by an external signal. Alternatively, it can be derived from V_{IN}. For a well-regulated supply (V_{IN}), a resistor divider can be used. In order to account for any small variations in V_{IN}, MaxLinear recommends you to set the EN voltage to 2.5V. For wide range of V_{IN}, circuits as shown in Figure 27(a) and 27(b) can be used.

DCM/CCM Mode

To enable DCM operation at light loads, ensure that the EN pin voltage is from 3.1V to 5.5V. Like the FCCM mode, the voltage can be controlled by an external signal or can be derived from V_{IN} by using a resistor and a Zener diode, as shown in Figure 27(c). This is valid for the entire range of V_{IN}. However, for a well-regulated V_{IN}, you can use a resistor divider. To account for any small variations in V_{IN}, MaxLinear recommends you to set the EN voltage to 4V.

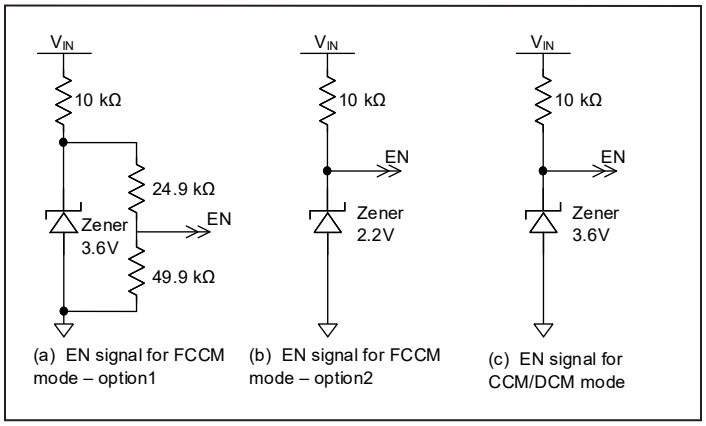


Figure 27. Options to Select FCCM or CCM/DCM Mode using V_{IN}

Programming the Soft Start Time

Figure 28 on page 12 shows a block diagram of the soft-start functionality. During soft start, the feedback reference voltage, V_{REF}, is tied to the SS pin. This pin forces 10µA current into C_{SS}, between the pin and AGND. V_{REF} is the same as V_{CSS} and increases linearly as follows:

$$\frac{dV_{REF}}{dt} = \frac{dV_{CSS}}{dt} = \frac{10\mu A}{C_{SS}}; \quad V_{CSS} = V_{REF} \leq 590mV \quad (1)$$

When the V_{CSS} voltage reaches 590mV, V_{REF} connection shifts from the SS pin to 0.6V, and soft start completes. For a given soft start time (t_{SS}), the required value of C_{SS} is as follows:

$$C_{SS} = t_{SS} \times \frac{10\mu A}{590mV} \quad (2)$$

Applications Information (Continued)

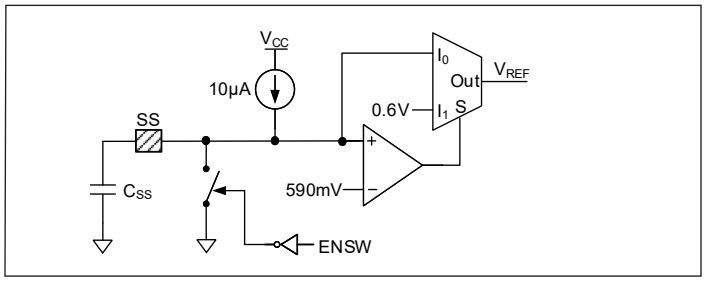


Figure 28. Start Soft Block Diagram

Soft start occurs in the following conditions:

- EN toggles from low to high.
- EN is high and VCC rises above the UVLO threshold.
- A fault occurs and the hiccup timer expires.

Pre-Bias Startup

The MxL76125 device can power up with a pre-charged output. During soft start, initially, both FETs are tri-stated. Once V_{REF} exceeds V_{FB}, the control loop takes over and switching starts to regulate the output. The MxL76125 starts in DCM to ensure that the output is not discharged. Figure 9 on page 7 shows a typical pre-bias startup waveforms.

Programming the Output Voltage

The feedback reference, V_{REF} is internally fixed to 0.6V. To obtain the desired output voltage, (V_{OUT}), use a feedback divider (R_{FB1}-R_{FB2}), as shown in Figure 1 on page 1.

$$\frac{V_{REF}}{V_{OUT}} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \Rightarrow R_{FB2} = R_{FB1} \times \frac{0.6}{V_{OUT} - 0.6} \quad (3)$$

MaxLinear recommends that the value of R_{FB1} is 4.99kΩ. However, you can change it as per VID resolution requirement, as described in the "VID Functionality" section.

VID Functionality

Nominal output voltage is set by an appropriate choice of feedback resistors, as described in the "Programming the Output Voltage" section. The output voltage can be varied from nominal in fixed step (50mV typical), by using VID0 and VID1 pins, as listed in Table 1. For more information about logic high/low voltage levels of these pins, see "Electrical Characteristics" on page 2. These pins have high input impedance and are required to be pulled to appropriate levels externally. If unused, these pins should be connected to ground or pulled down with external resistors, R_{VIDx}.

Figure 29 shows the VID functional diagram. VID implementation includes an IDAC. The reference current I_{IREF} is set by an accurate internal reference (V_{IREF}) and an external resistor R_{REF}. These are related as follows:

$$I_{REF} = \frac{V_{IREF}}{R_{REF}} \quad (4)$$

The recommended value of R_{REF} is 56.2kΩ. I_{REF} and VID govern current sourced by FB pin (I_{FB}), as listed in the following table.

Table 1. VID vs V_{OUT} for VID step being 50mV (R_{FB1} = 4.99kΩ, R_{REF} = 56.2kΩ)

VID1	VID0	VOUT	FB Current, I_{FB}
0	1	Nominal + 50mV	$-I_{IREF}$
0	0	Nominal	0
1	0	Nominal - 50mV	I_{IREF}
1	1	Nominal - 100mV	2 x I_{IREF}

Note: + I_{FB} implies current flowing out of the FB pin and -I_{FB} implies current entering into the FB pin.

In steady state the feedback node voltage (V_{FB}) is controlled to a fixed reference (V_{REF}). As a result, when I_{FB} flows out of the FB pin, current through R_{FB1} is reduced by the same amount. Therefore, the voltage across R_{FB1} is reduced by $I_{FB} \times R_{FB1}$. The output voltage also decreases by the same magnitude. Hence, the VID step size, ΔV_{VID} is expressed in terms of R_{FB1} and I_{REF} as follows:

$$\Delta V_{VID} = R_{FB1} \times I_{IREF} = R_{RB1} \times \frac{V_{IREF}}{R_{REF}} \quad (5)$$

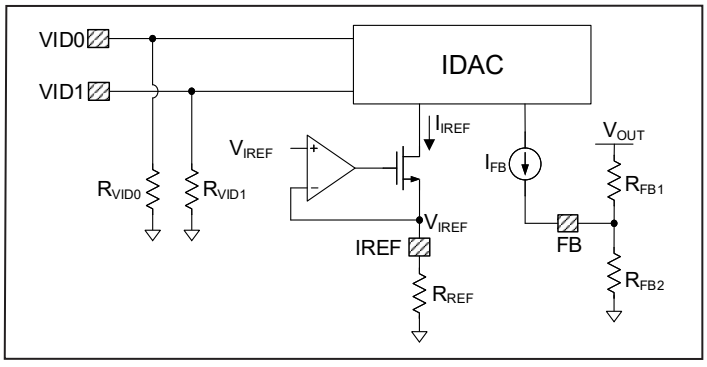


Figure 29. MxL76125 VID Functional Diagram

Applications Information (Continued)

Similarly, if I_{FB} flows into the FB pin (as listed in the fist line of Table 1 on page 12) the current through R_{FB1} is increased by the same amount as I_{FB}. Therefore, the voltage across R_{FB1} is increased by $I_{FB} \times R_{FB1}$. The output voltage also increases by the same magnitude.

Wi-Fi 7 SoC Design Example

- Target nominal output voltage = 800mV.
- VID step size = 50mV.
- Feedback reference voltage = 600mV (V_{REF}).

From Figure 1 on page 1:

$$\frac{R_{FB2}}{R_{FB1}+R_{FB2}} = \frac{600mV}{800mV} \Rightarrow \frac{R_{FB2}}{R_{FB1}} = 3 \qquad (6)$$

From (5) and (6), for R_{REF} = 56.2kΩ, the recommended feedback resistors are: R_{FB1} = 4.99kΩ and R_{FB2} = 15kΩ.

Power Good (PGOOD) Function

Figure 30 shows a simplified functional block diagram for the PGOOD pin. This pin is an open drain output and has active high logic. Therefore, this pin needs to be pulled up. The pull-up voltage can be tied to the VCC or some external supply. During regular operation the PGOOD is high, if the $V_{FB} \geq 92.5\%$ of the V_{REF} (555mV). The PGOOD assertion delay is typically 2ms. The typical waveform of the PGOOD during different intervals of operation is shown in Figure 31.

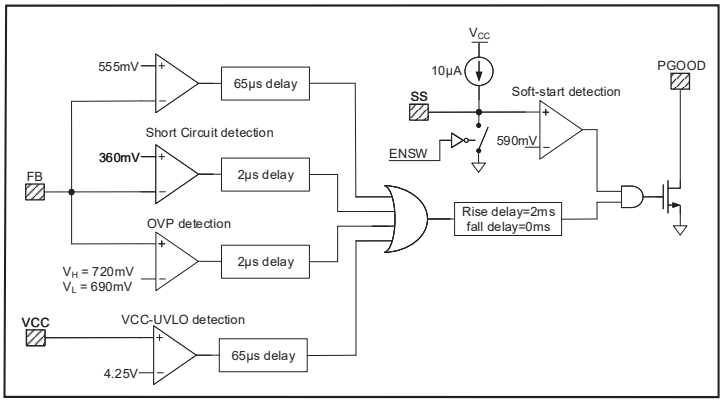


Figure 30. PGOOD Function Block Diagram

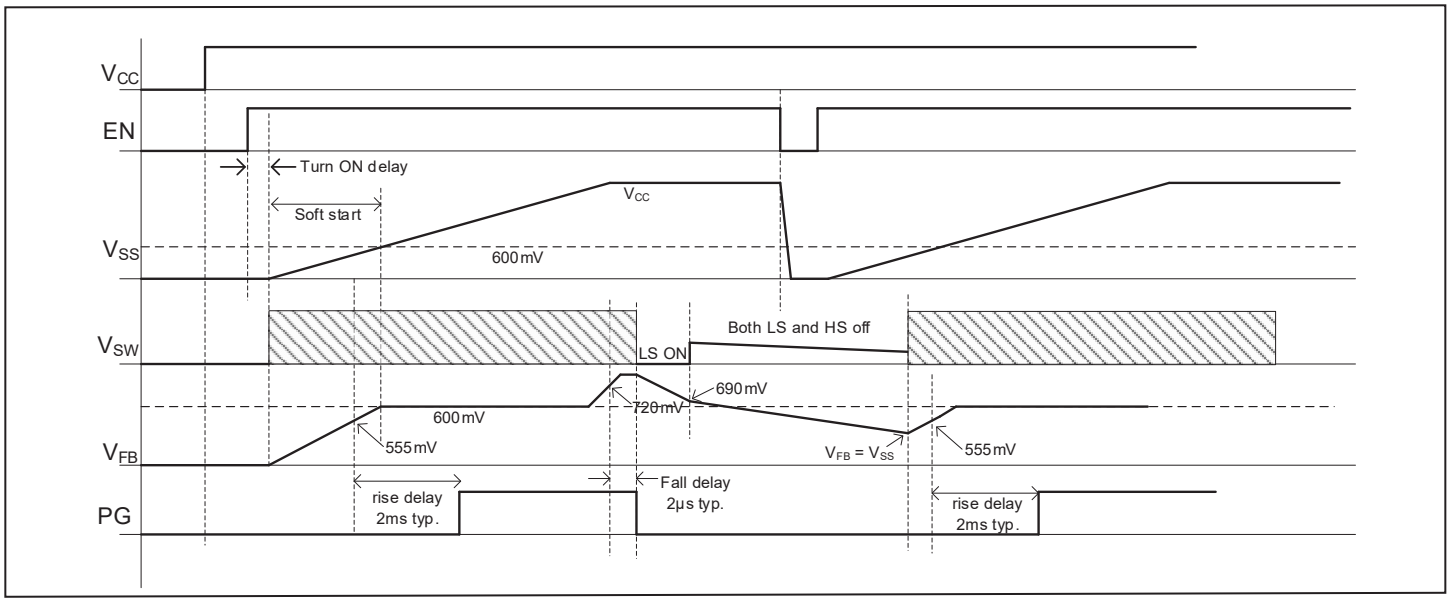


Figure 31. OVP Response and PGOOD Waveform during different V_{OUT} Conditions
(a) VCC = 0, (b) Soft Start, and (c) OV Fault

The PGOOD is de-asserted in any of the following events:

- During soft start.
- During output short circuit. V_{FB} < 360mV (60% of V_{REF}). PGOOD de-assertion delay = 2µs.
- Output under voltage condition (369mV < V_{FB} < 555mV). PGOOD de-assertion delay = 65µs.
- If OVP is detected (V_{FB} ≥ 720mV). PGOOD de-assertion delay = 2µs.
- VCC < UVLO threshold (4.25V typical). PGOOD de-assertion delay = 65µs.
- If V_{IN} = V_{CC} = 0 (The MxL76125 is unpowered).
- If T_J ≥ 138°C (over temperature fault).
- Over current protection is triggered.
- If the EN is low, the delay from the EN going low to PGOOD low is up to 350 ns.

The PGOOD pin is low impedance when the MxL76125 is unpowered. It ensures that the device does not give any invalid PGOOD signal if the input supply is removed.

Operation

A typical application schematic is shown in Figure 1 on page 1. The external components that require appropriate selection for a given application are the input capacitance (C_{IN}), the output filter components (C_{OUT} - L_{OUT}), and the switching frequency (or T_{ON}) selection resistor (R_{ON}). All other component values in the typical application schematic are recommendations for safe operation of the device.

Programming the On-Time (T_{ON})

For a given switching frequency (F_{SW}) required value of T_{ON} is as follows:

$$T_{ON} = \frac{V_{OUT}}{V_{IN} \times 1.06 \times F_{SW} \times \eta} \quad (7)$$

Where η is the converter efficiency.

The MxL76125 allows you to set T_{ON} by using resistor R_{ON}. The corresponding relation is expressed as follows:

$$R_{ON} = V_{IN} \times \frac{T_{ON} - 2.5 \times 10^{-8}}{3.45 \times 10^{-10}} \quad (8)$$

Table 2 lists the values of R_{ON} for different V_{OUT} at V_{IN} = 12V, F_{SW} = 1MHz, and I_{OUT} = 15A. It uses efficiency numbers from Figure 2 on page 1.

Table 2: R_{ON} Recommendation for V_{IN} = 12V

V_{OUT}	η%	F_{sw} (MHz)	R_{ON} kΩ
0.8V	78.8	1	1.82
3.3V	91.2	1	9.31

Note that during soft start, the MxL76125 operates with minimum T_{ON}, which is typically 55ns.

Selection of the Output Filter Inductor (L_{OUT})

A larger inductor offers smaller switching ripple in inductor current and in V_{OUT}, but at cost of larger physical size. To balance size and ripple current magnitude, the recommended peak to peak ripple (ΔI_L) is 25%-40% of full load. The inductance is calculated as follows:

$$L_{OUT} = \frac{(V_{IN} - V_{OUT})}{F_{SW} \times \Delta I_L} \times \frac{V_{OUT}}{V_{IN}} \quad (9)$$

Example:

For V_{IN} = 12V, V_{OUT} = 0.8V, I_{OUT} = 15A, F_{SW} = 1MHz and ΔI_L = 5A, from (9) L_{OUT} = 150nH

Selection of the Output Capacitor (C_{OUT})

The output filter capacitor is designed considering unloading transient overshoot, loading transient undershoot, and steady state ripple specifications, individually. The final capacitance is maximum of the three values meeting these specifications.

Filter capacitor design for meeting switching ripple specifications

In this analysis, parasitic inductance and resistance of the output filter capacitor are neglected.

In steady state the inductor ripple current is filtered by C_{OUT}. The charge which produces switching ripple in C_{OUT} is the area under the shaded triangle as shown in Figure 32. Mathematically:

$$Q_{COUT} = C_{OUT}\Delta V_{SW} = \frac{1}{2} \times \frac{\Delta I_L}{4F_{SW}} \qquad (10)$$

where, the ΔV_{SW} is the peak to peak switching ripple in the V_{OUT}. Hence, the minimum capacitance to meet steady state V_{OUT} ripple is as follows:

$$C_{OUT_{RIPPLE}} \geq \frac{\Delta I_L}{8 \times F_{SW} \times \Delta V_{SW}} \qquad (11)$$

Note that the regulator runs as expected when the steady state switching ripple on the FB node is below 50mV. From this an upper bound on ΔV_{SW} for $C_{FF} \neq 0$ is as follows.

$$\Delta V_{SW} \leq 50mV \qquad (12)$$

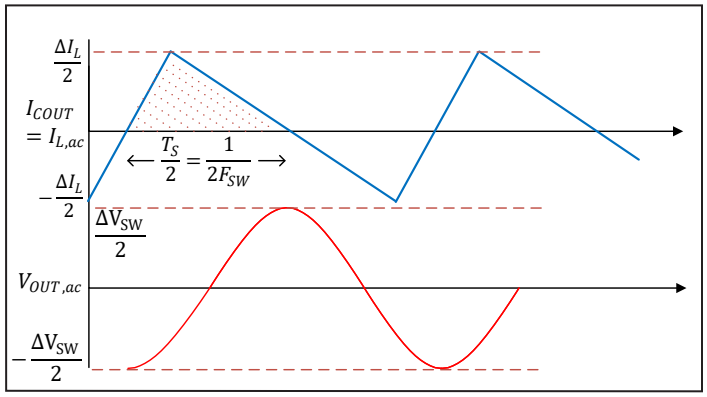


Figure 32. V_{OUT} Switching Ripple

Filter capacitor design for meeting transient overshoot specifications

The transient overshoot happens when the load current is rapidly reduced (load throw off event). In this situation, the load slew rate (SR) magnitude is larger than the inductor current falling rate, as shown in Figure 33. In a COT controlled converter, the maximum overshoot in the output voltage can happen, when the load throw-off occurs immediately after start of a TON pulse. Accordingly, the required capacitance is as follows:

$$C_{OUT\_OV} = \frac{1}{2\,\Delta V_{OV}} \times \left(\Delta I_{load} + \frac{\Delta I_L}{2}\right)^2 \times \left(\frac{L}{V_{OUT}}\right) + \frac{(T_{ON} \times \Delta I_{load})}{\Delta V_{OV}} - \frac{(\Delta I_{load})^2}{SR\,\Delta V_{OV}} \qquad (13)$$

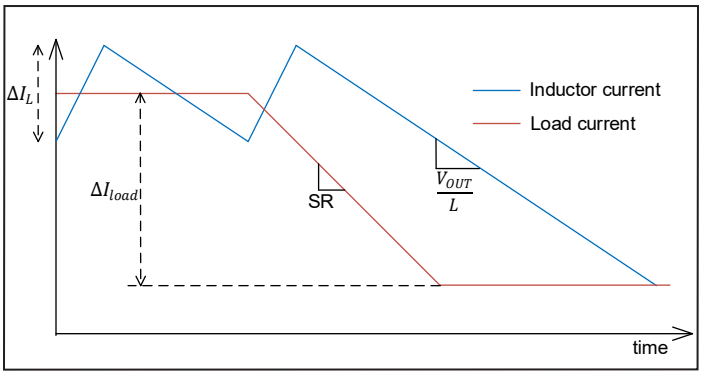


Figure 33 Inductor Current during Unloading

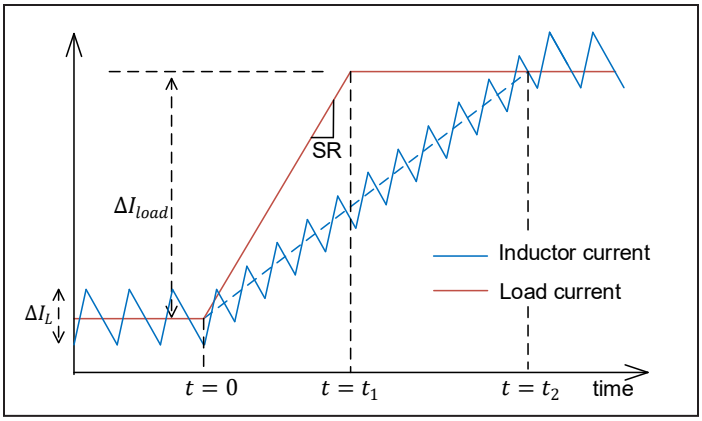


Figure 34. Inductor Current during Loading

Filter capacitor design for meeting transient undershoot specifications

The transient undershoot occurs when the load current rapidly increases. In this case, the load current slew rate is larger than the inductor current ramp up rate. In a COT controlled converter, when V_{OUT} drops, the off duration shrinks to its minimum value (T_{OFFMIN}) and T_{ON} remains unchanged. Worst-case for transient undershoot is when the inductor current is at its valley and loading event starts. In this case, the required output filter capacitance is as follows:

$$C_{OUT\_UV} = \frac{0.5 \times (t_2 - t_1) \times \Delta I_{load} + 0.25 \times \Delta I_L \times t_2}{\Delta V_{UV}} \qquad (14)$$

where, the load current transition time is:

$$t_1 = \frac{\Delta I_{load}}{SR} \qquad (15)$$

and the inductor current transition time is:

$$t_2 = \left(\frac{\Delta I_L}{2} + \Delta I_{load}\right) \times \frac{L}{V_{IN} \times \left(\frac{T_{ON}}{T_{ON} + T_{OFFMIN}}\right) - V_{OUT}} \qquad (16)$$

Selection of Input Capacitor (C_{IN})

The input current to the converter is discontinuous in nature. Input capacitors (C_{IN}) are required to supply choppy AC currents while maintaining the DC supply voltage. For a given input voltage ripple (ΔV_{IN}), the required input capacitance, as a function of duty cycle ratio (D) is as follows:

$$C_{IN} \geq \frac{D \times (1 - D) \times I_{load}}{\Delta V_{IN} \times F_{SW}} \quad (17)$$

Net r.m.s. current in C_{IN} is:

$$I_{CIN,RMS} = I_{load} \times \sqrt{D \times (1 - D)} \times \sqrt{1 + \frac{1 - D}{12}\left(\frac{V_{OUT}}{L \times F_{SW} \times I_{OUT}}\right)^2} \quad (18)$$

Considering the space constraint and depending on the application, these capacitors are typically a combination of electrolytic capacitors, ceramic capacitors (MLCC), and/or SP capacitors. Typical combinations of the PVIN capacitors are as follows:

PV_{IN} = 12V, V_{OUT} = 0.8V Example: POSCap 1 x 270uF, MLCC's 2 x 22uF or 4 x 10uF, 2 x 2.2uF.

The MLCC's must have low ESR and ESL. To reduce switching spikes across the FETs, inductance in loop formed by these ceramic capacitors and FETs should be minimized.

Feed-Forward Capacitor (C_{FF}) and Feed-Forward Resistor (R_{FF})

These two are connected in series and placed across R_{FB1} as shown in Figure 1 on page 1. With this, the V_{OUT} to V_{FB} open loop transfer function is as follows:

$$\frac{V_{FB}(s)}{V_{OUT}(s)} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \times \frac{1 + (R_{FB1} + R_{FF})\, C_{FF} s}{1 + \left(\frac{R_{FB1} R_{FB2}}{R_{FB1} + R_{FB2}} + R_{FF}\right) C_{FF} s} \quad (19)$$

It shows that,

- C_{FF} introduces a low frequency zero (ω_Z) and high frequency pole (ω_P), which gives phase boost in a range of frequency from $\omega_Z/10$ to $10\omega_P$.
- With increase in R_{FF}, the frequency of both the pole and zero reduces.
- With R_{FF} = 0, ratio of ω_Z and ω_P (<1) is the same as the feedback attenuation ratio. With increase in R_{FF}, this ratio moves towards unity. Therefore, for low V_{OUT}, phase boosting is not helpful.

As a rule of thumb, C_{FF} should be selected such that ω_Z is 5 times of buck output filter resonance frequency, and $R_{FF} << R_{FB1}$. Hence,

$$C_{FF} \approx \frac{\sqrt{L_{OUT} C_{OUT}}}{5 \times R_{FB1}} \quad (20)$$

You must use manufacturer's DC derating curves to determine the effective capacitance corresponding to V_{OUT}. A load step test and/or a loop frequency response test should be performed. From this C_{FF} can be adjusted to get damped transient load response.

The frequency of the pole in (19) should be below the switching frequency, F_{SW} to add gain margin. Hence,

$$R_{FF} = \frac{1}{2\pi F_{SW} C_{FF}} \quad (21)$$

In the MxL76125, the C_{FF} also decides the V_{OUT} transition rate during DVS. The corresponding time constant, τ_{DVS}, is as follows:

$$\tau_{DVS} = R_{FB1} \times C_{FF} \quad (22)$$

Wi-Fi 7 SoC Design Example

For the parameters given in the Wi-Fi 7 SoC design example on page 13 and τ_{DVS} = 2µs, from (22):

R_{FF} = 0 and C_{FF} = 400pF

Device Protection

Overvoltage Protection (OVP)

The OVP detection is based on the FB pin voltage. The OVP threshold is set to 720mV, which is 1.2 times V_{REF}. When the FB voltage exceeds the OVP threshold, an internal overvoltage signal is asserted with a typical delay of 2µs. This signal latches off the high-side FET, turns on the low-side FET and de-asserts PGOOD. The low-side FET remains on to discharge the output capacitor until the FB voltage drops to 690mV (1.15 x V_{REF}). Then low-side FET also turns off to prevent complete discharge of V_{OUT}. Both FETs remain latched off until the V_{IN} or EN is recycled. Note that the OVP protection is designed to protect the SoC. If a strong external source is connected to the output, the low side MOSFET can be damaged.

Overcurrent Protection (OCP)

The OCP threshold is referred to inductor valley current. If the valley current exceeds the programmed threshold, the I_{OCP} for four consecutive switching cycles, the regulator enters hiccup mode. In this mode, switching is turned off for hiccup timeout period. Following the hiccup timeout, a soft start is attempted. If the OCP persists, hiccup timeout repeats. The regulator remains in hiccup mode until the load current is reduced to ensure that the valley current is below the programmed value. The OCP threshold is internally set to 20A (typical).

Short-Circuit Protection (SCP)

If the output voltage drops below 60% of its programmed value (that is, FB drops below 0.36V), the regulator enters hiccup mode. The hiccup mode persists until short-circuit is removed. Note that the SCP is activated only after PGOOD goes high. Therefore, during short circuit the SCP turns off the device the first time, but in subsequent hiccups the OCP turns off the device.

Over Temperature Protection (OTP)

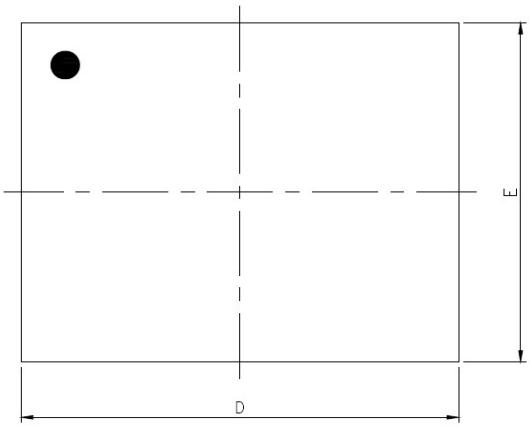
The OTP is triggered when the junction temperature reaches 138°C (typical). The protection feature turns OFF both power FETs until the junction cools down to 123°C. After this, soft start is initiated and regular operation resumes.

Thermal Design

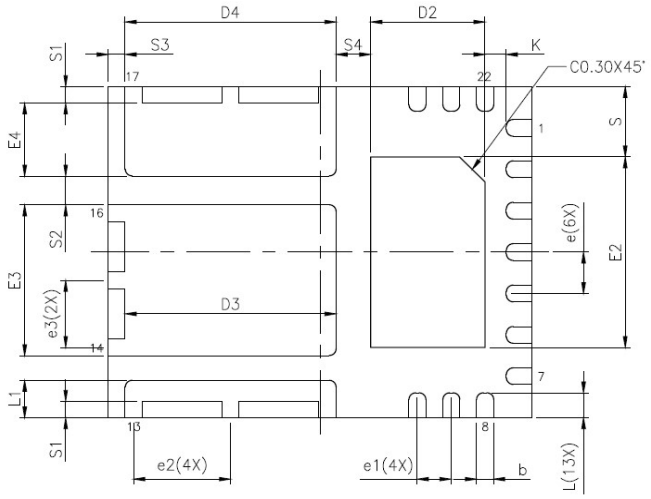
The proper thermal design is critical in controlling device temperatures and in achieving robust designs. There are several factors that affect the thermal performance, such as the temperature rise of the device in the package. This is a function of the thermal resistances of the MxL76125 inside the package and the power being dissipated.

For more information about thermal resistances, see "Electrical Characteristics" on page 2. Note that the values are obtained from simulation. Since your actual board design could be different, the thermal resistances in your actual and final board design may differ to the values listed in that section. The package thermal derating curves are shown in Figure 24 and Figure 25 on page 9.

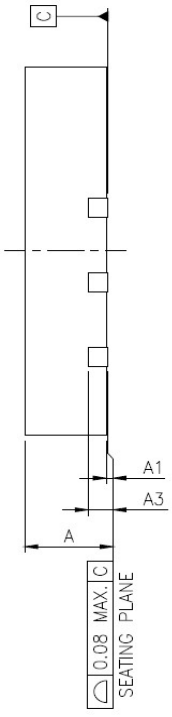
Package Description



Top View



Bottom View



Side View

JEDEC OUTLINE	N/A		
PKG CODE	VQFN		
SYMBOLS	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF		
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	3.90	4.00	4.10
e	0.50 BSC		
e1	0.40 BSC		
e2	1.145 BSC		
e3	0.81 BSC		
D2	1.30	1.35	1.40
D3	2.44	2.49	2.54
D4	2.44	2.49	2.54
E2	2.25	2.30	2.35
E3	1.77	1.82	1.87
E4	0.83	0.88	0.93
L	0.25	0.30	0.35
L1	0.40	0.45	0.50
K	0.20	-	-
S	0.85 REF		
S1	0.20 REF		
S2	0.35 REF		
S3	0.20 REF		
S4	0.41 REF		

LEAD FINISH		JEDEC CODE
Pure Tin	PPF	
V	X	N/A

NOTE:
1. All dimensions are in millimeters
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.
3. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.

Document #	Revision
POD-00000167	A

Figure 35. MxL76125 Package Description

Land Pattern and Stencil Design

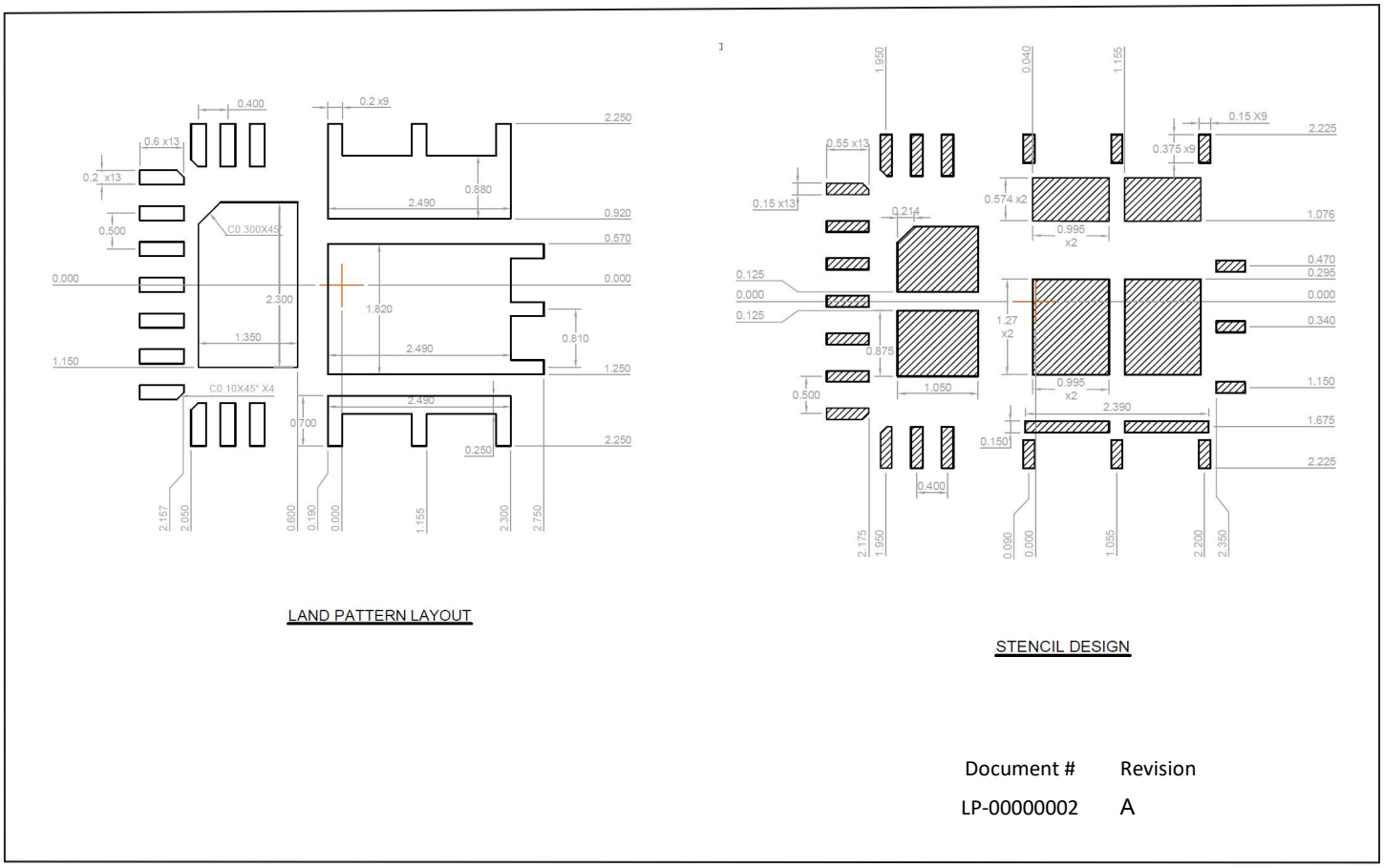


Figure 36. MxL76125 Land Pattern and Stencil Design