MxL7704-B

Data Sheet

Five Output Universal PMIC

General Description

The MxL7704-B is a five output Universal PMIC optimized for powering low power FPGAs, DSPs, and microprocessors from 5V inputs. Four synchronous step down buck regulators range from 1.5A system power to 4A core power.

A 100mA LDO provides a clean 3.3V power for auxiliary devices. All of the outputs support ±10% margining. The two highest power outputs also support dynamic voltage control which saves power in processors that can use this function. You can monitor an input voltage flag and PGOOD flags for each output through a 400kHz I^2C interface. The I^2C port can enable you to modify the power up and down sequencing options, assign PGOOD outputs to the PGOOD pins, enable outputs, and select switching frequency.

The high switching frequency and current mode architecture with internal compensation enable a very fast transient response to line and load changes without sacrificing stability and keeping board space to a minimum.

The MxL7704-B built-in one-time programmable (OTP) memory stores key startup configurations. It reduces the external components typically used to set output voltage and sequence of regulators. Regulator parameters are adjustable through high-speed I^2C after the start up which offers flexibility for different system states.

The fault protection features include input undervoltage lockout, overcurrent protection, and thermal protection. The MxL7704-B is offered in a 5mm x 5mm QFN package.

Features

- Input voltage range from 4.0V to 5.5V
- Four synchronous buck regulators
  - Internally compensated current mode
  - From 1MHz to 2.1MHz switching frequency
  - Buck 1: 3.0V-3.6V, 20mV step, 1.5A
  - Buck 2: 1.3V-1.92V, 20mV step, 1.5A
  - Buck 3: 0.8V-1.6V, 6.25mV step, 2.5A
  - Buck 4: 0.6V-1.4V, 6.25mV step, 4A
- 100mA LDO 3.3V
- ±2% maximum total DC output error over line, load, and temperature
- 3.3V/5V 400kHz I^2C interface
  - Dynamic voltage scaling
  - Status monitoring by channel
  - Sequencing control
  - Input voltage status register
- Highly flexible conditional sequencing engine with external input
- Two configurable PGOOD outputs
- Adjustable switching frequency
- 5mm x 5mm 32-pin QFN package

Applications

- Low power processor, ASIC, and FPGA power
- Industrial control
- Test equipment
- POS terminals

For more information about the ordering information, see "Ordering Information" on page 32.

Revision History

Document No.	Release Date	Change Description

200-7704BDSR02	September 20, 2023	**Updated:**
		■ "MxL7704-BQB" occurrences replaced with "MxL7704-B" throughout the document (except in "Ordering Information" table).
		■ In "Default Values" table:
		  ■ Default value of "0x17" address.
		  ■ Default value and value description of "0x19" address.
		■ In "SEQ EN Assign and PG1 Routing (0x17)—Read/Write" table under "Register Descriptions" section, description of bit 5.
		■ In "Fault Actions, Down Sequencing, Frequency (0x19)—Read/Write" table under "Register Descriptions" section, description of bit 5.
		Added:
		■ "Output Voltages Outside Ranges Guaranteed in Electrical Table" section.
		Removed:
		■ In "Ordering Information" table, "MxL7704-B-EVB" obsolete part number.

200-7704BDSR01	January 26, 2022	Initial release.

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MxL7704-B Specifications

Absolute Maximum Ratings

Important: The stresses above what is listed under Table 1 may cause permanent damage to the device. This is a stress rating only—functional operation of the device above what is listed under Table 1 or any other conditions beyond what MaxLinear recommends is not implied. Exposure to conditions above what is listed under Table 3 for extended periods of time may affect device reliability. Solder reflow profile is specified in the *IPC/JEDEC J-STD-020C* standard.

Table 1: Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
V_{IN}, V_{IN1}, V_{IN2}, V_{IN3}, V_{IN4}, 5VSYS	-0.3	6	V
SDA, SCL, VDDIO	-0.3	6	V
AN0, AN1	-0.3	6	V
PG1, PG2, GLOBAL EN, SEQ EN	-0.3	6	V
LDO	-0.3	6	V
V_{OUT1}, V_{OUT2}, V_{OUT3}, V_{OUT4}	-0.3	V_{INx} - 0.3V(1)	V
Storage Temperature Range	-55	150	°C
Peak Package Body Temperature	-	260	°C

1. x = Buck number

ESD Ratings

Table 2: ESD Ratings

Parameter	Minimum	Maximum	Units
Human body model (HBM)	-	2.5	kV
Charged device model (CDM)	-	750	V

Operating Conditions

Table 3: Operating Conditions

Parameter	Minimum	Maximum	Units
V_{IN}, V_{IN1}, V_{IN2}, V_{IN3}, V_{IN4}, 5VSYS	4.0	5.5	V
SDA, SCL, VDDIO	3.3	5.5	V
AN0, AN1	0	3	V
PG1, PG2, GLOBAL EN, SEQ EN	0	5.5	V
LDO	0	V_{IN} - 0.3V(1)	V
LX1, LX2, LX3, LX4	–1	5.5(2)	V
Switching frequency	1000	2100	kHz
Junction temperature range (T_J)	–40	125	°C
Package power dissipation max at 25°C	-	3.65	W
Package thermal resistance Θ_{JA}	-	27	°C/W

1. LDO set to 3.3V.
2. LX pin's DC range is –1V for less than 50ns.

Electrical Characteristics

The specifications listed in this section only apply for operating junction temperature of T_J = 25°C only. The limits that apply to the full operating junction temperature range are denoted by a "•". The typical values represent the most common parametric norm at T_J = 25°C and are provided for reference purposes only unless otherwise indicated,
V_{IN} = 5VSYS = 5.0V

Table 4: Electrical Characteristics

Symbol	Parameter	Conditions	•	Minimum	Typical	Maximum	Units
DC Specifications							
V_{IN}	Input DC voltage	-	•	4.0	5.0	5.5	V
UVLO	Under voltage lockout	Rising		-		3.9	V
	Under voltage lockout hysteresis	Falling		-	210	-	mV
$I_{Q\_SHUTDOWN}$	Shutdown quiescent current	GLOBAL EN = logic LOW. All outputs <20% of set point or initial power applied.		-	10	-	µA
$I_{Q\_OPERATING\_5VSYS}$	5VSYS operating quiescent current	GLOBAL EN = logic HIGH. All outputs in regulation no load. f_{OSC} = 1.5MHz		-	8	-	mA
T_{SD}	Thermal shutdown threshold	Temperature rising		-	145	-	°C
T_{SDH}	Thermal shutdown hysteresis	Temperature falling		-	20	-	°C
Buck Regulators 1 - 4							
V_{IN}	Operational voltage range	-	•	4.0	-	5.5	V
V_{OUT} accuracy	Output voltage accuracy	Load current = 10mA to full load V_{IN} = 5VSYS = 4.0V-5.5V	•	-2	-	+2	%
V_{OUT} initial accuracy	Output voltage accuracy	Load current = 10mA V_{IN} = 5VSYS = 4.5V-5.5V		-0.5	-	+0.5	%
Buck 1 V_{OUT} range	Output voltage set point range	20mV resolution, 8 bit		3.0	-	3.6	V
Buck 2 V_{OUT} range	Output voltage set point range	20mV resolution, 8 bit		1.30	-	1.92	V
Buck 3 V_{OUT} range	Output voltage set point range	6.25mV resolution, 8 bit		0.800(1)	-	1.59375	V
Buck 4 V_{OUT} range	Output voltage set point range	6.25mV resolution, 8 bit		0.600(1)	-	1.39375	V
V_{OUT_DYN}	Dynamic output slew rate	Closed loop controlled		-	10	-	V/ms
V_{OUT_SS} V_{OUT_SO}	soft-start slew rate and soft off slew rate	Closed loop controlled		-	1	-	V/ms
$V_{OUT\_DISCHARGE}$	Pre-bias discharge threshold	Output falling		-	200	-	mV
R_{AD}	Output active discharge resistance	Converter disabled and option selected		-	78	-	Ω

Table 4: Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	•	Minimum	Typical	Maximum	Units
I_{OUT}	Full load rated current	Buck 1	•	1.5	-	-	A
		Buck 2	•	1.5	-	-	A
		Buck 3	•	2.5	-	-	A
		Buck 4	•	4.0	-	-	A
I_{CLIM}	Peak current limit These current limits help define maximum inductor ripple and to protect the internal power switches from an EOS event.	Buck 1	•	2.5	3.4	4.5	A
		Buck 2	•	2.5	3.4	4.5	A
		Buck 3	•	3.5	4.5	5.5	A
		Buck 4	•	5.5	6.5	9.0	A
V_{UVP}	Under voltage protection (UVP) threshold	soft-start completed, DVS inactive		-	70	-	%
	UVP deglitch				10		µs
f_{OSC_RANGE}	Switching frequency programmable range	See Figure 8 on page 9		1000	-	2000	kHz
	Oscillator accuracy	At 1.5MHz b1001	•	-10	-	10	%
t_{ON-MIN}	Minimum controllable on-time	Full load		-	92	120	ns
R_{DSON} (P)	Pin to pin resistance PFET High-side MOSFET	Buck 1		-	146	-	mΩ
		Buck 2		-	146	-	mΩ
		Buck 3		-	67	-	mΩ
		Buck 4		-	60	-	mΩ
R_{DSON} (N)	Pin to pin resistance NFET Low-side MOSFET	Buck 1		-	103	-	mΩ
		Buck 2		-	103	-	mΩ
		Buck 3		-	32	-	mΩ
		Buck 4		-	27	-	mΩ
Low Dropout Regulator, LDO							
V_{IN}	Operational voltage range	-	•	4.0	-	5.5	V
V_{OUT} accuracy	Output voltage accuracy	Load current = 1mA-100mA V_{IN} = 4.0V-5.5V	•	-2	-	2	%
V_{OUT} default	Default set point			-	3.3	-	V
V_{OUT_DYN}	Dynamic output slew rate	Closed loop controlled, load = 25mA		-	10	-	V/ms
V_{OUT_SS}	soft-start slew rate	Closed loop controlled		-	1	-	V/ms
I_{SC}	Short circuit current limit	3v3LDO = 0V	•	120	230	260	mA
V_{DO}	Dropvout voltage (defined as a drop of 2% from initial value)	Load current = 10mA	•	-	11	30	mV
		Load current = 100mA	•	-	210	300	mV

Table 4: Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	•	Minimum	Typical	Maximum	Units
PSRR	Power supply rejection ratio	f = 1kHz, I_{OUT} = 10mA, V_{IN} = 4.3V, V_{OUT} = 3.3V		-	56	-	dB
		f = 10kHz, I_{OUT} = 10mA, V_{IN} = 4.3V, V_{OUT} = 3.3V		-	40	-	dB
C_{OUT}	Output capacitor (ceramic)	Capacitance (effective capacitance)		0.68	1.0	-	µF
		ESR		1	-	100	mΩ
Θ_N	Supply output noise	10Hz ≤ f ≤ 100kHz, V_{IN} = 4.3V, V_{OUT} = 3.3V		-	470	-	µVrms
R_{AD}	Output active discharge resistance	Converter disabled and option selected		-	78	-	Ω
Power Good Outputs							
	Power good threshold	V_{OUT} rising as a % of Vout	•	85	90	95	%
	Power good hysteresis Buck 1 and LDO	V_{OUT} falling		-	122	-	mV
	Power good hysteresis Buck 3 and Buck 4	V_{OUT} falling		-	38	-	mV
	Power good hysteresis Buck 2	V_{OUT} falling		-	67	-	mV
	Power good assertion delay, FB rising	-		-	2	-	ms
	Power good de-assertion delay, FB falling	-		-	65	-	µs
V_{OL}	Output level low	I_{SINK} = 1mA	•	-	-	0.4	V
GLOBAL EN and SEQ EN Input							
V_{IL}	Input low level	-		-	-	0.8	V
V_{IH}	Input high level	-		2.0	-	-	V
	GLOBAL EN input current	GLOBAL EN = 5.5V		-	4	30	µA
	SEQ EN input current	SEQ EN = 5.5V		-	4	30	µA
Input Voltage Monitor Flag							
V_{TH_RISING}	Input voltage good threshold	Voltage rising		4.59	4.63	4.7	V
$V_{TH\_FALLING}$	Input voltage good threshold	Voltage falling		4.52	4.57	4.65	V

Table 4: Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	•	Minimum	Typical	Maximum	Units
ADC, Temperature Monitoring							
	Input range	5VSYS ≥ 4.2V	•	0	-	2.55 + offset(1)	V
	Input range	5VSYS ≥ 4.0V	•	0	-	2.35	V
	Nominal Resolution	8 bit		-	10	-	mV/ LSB
	INL	-		-	-	±2	LSB
	DNL, differential nonlinearity	-		-	-	±1	LSB
	Full scale error	-		-	-	±2	LSB
	Zero error (offset)	-		-	+1	-	LSB
	Full scale error temperature coefficient	-		-	±0.03	±0.05	%/°C
	ADC conversion frequency	-		-	5.56	-	kHz
	Input capacitance	-		-	4	-	pF
	AN0/1 DC input impedance	-		-	10	-	MΩ
T_{RANGE}	Temperature monitoring range	-		-40	-	Thermal Shutdown	°C
T_{RES}	Temperature monitoring range	-		-	1.06	-	°C
$T_{ACCURACY}$	Temperature monitoring accuracy	25°C (h'5F)		-2	-	2	°C
		105°C (h'B4)		-7	-	7	°C
I^2C Interface - Default Address 7'b0011101 (0x1D), see Figure 8 on page 9							
V_{IL}	Input low level	-		-	-	0.8	V
V_{IH}	Input high level	-		2.0	-	-	V
V_L	VDDIO supply voltage	-		3.0	-	5.5	V
V_{OL_I2C}	SDA logic output low voltage	3mA sink current	•	-	-	0.8	V
f_{SCL}	SCL clock frequency	-	•	-	-	400	kHz
t_{SCL_H}	SCL clock high period	-	•	0.6	-	-	µs
t_{SCL_L}	SCL clock low period	-	•	1.3	-	-	µs
t_{SP}	I^2C spike rejection filter pulse width 1	-	•	0	-	50	ns
t_{SU_DAT}	I^2C data setup time	-	•	100	-	-	ns
t_{HD_DAT}	I^2C data hold time	-	•	0		900	ns
t_{R_I2C}	SDA, SCL rise time	C_B = total capacitance of bus line in pF	•	-	20 + 0.1*C_B	300	ns
t_{F_I2C}	SDA, SCL fall time	C_B = total capacitance of bus line in pF	•	-	20 + 0.1*C_B	300	ns
t_{BUF}	I^2C bus free time between stop and start	-	•	1.3	-	-	µs

Table 4: Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	•	Minimum	Typical	Maximum	Units
t_{SU_STA}	I^2C repeated start condition setup time	-	•	0.6	-	-	µs
t_{HD_STA}	I^2C repeated start condition hold time	-	•	0.6	-	-	µs
t_{SU_STO}	I^2C stop condition setup time	-	•	0.6	-	-	µs
C_B	I^2C bus capacitive load	-	•	-	-	400	pF
C_{SDA}	SDA input capacitance	-	•	-	-	10	pF
C_{SCL}	SCL input capacitance	-	•	-	-	10	pF

1. Limited by minimum t_{ON}. For minimum permissible V_{OUT} versus frequency, see Table 6 on page 18.

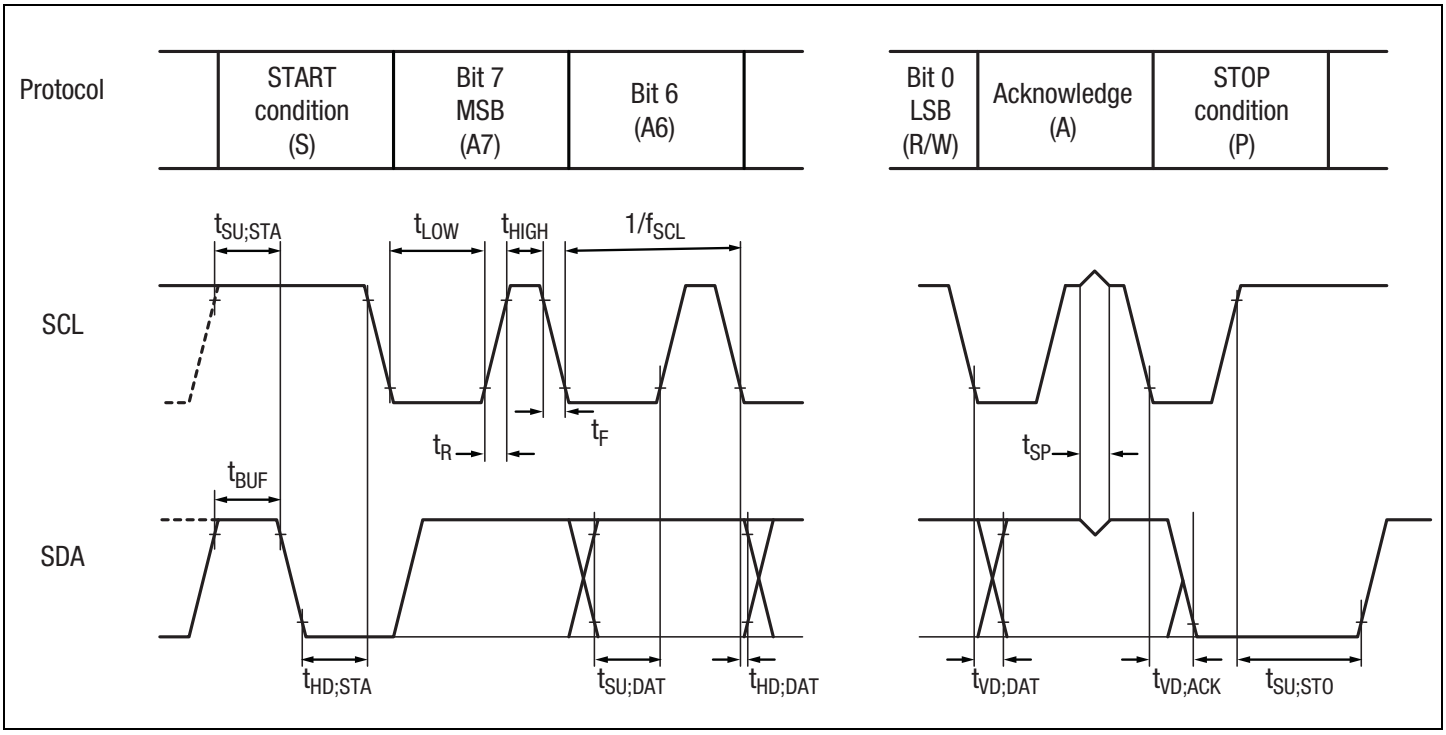


Figure 1: I^2C Bus Timing Diagram

Pin Information

Pin Configuration

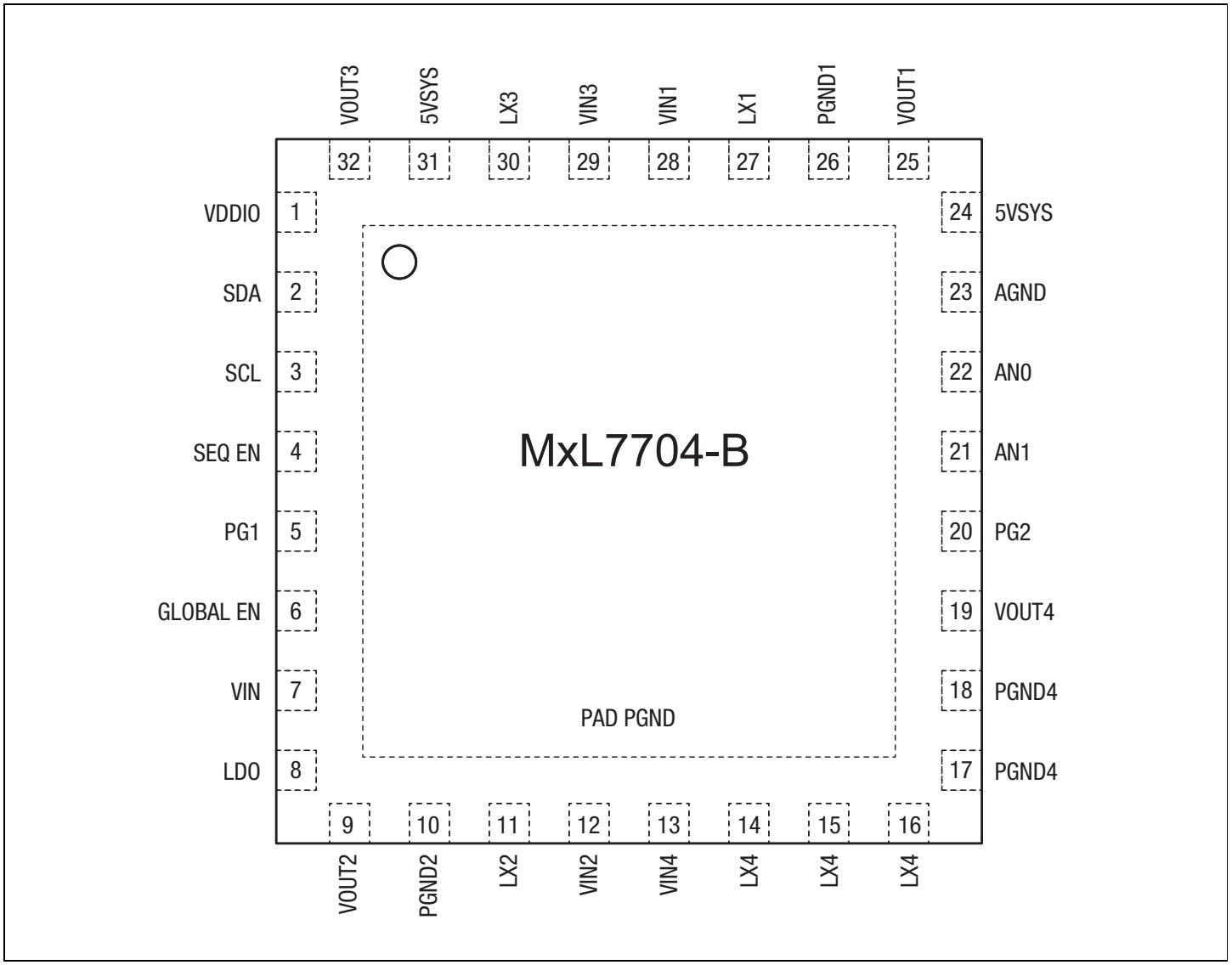


Figure 2: Pin Configuration (Top View)

Pin Description

Table 5: Pin Names and Description

Pin Number	Pin Name	Description
1	VDDIO	Supply for I^2C Interface, from 3.3V to 5V nominal.
2	SDA	I^2C data.
3	SCL	I^2C clock.
4	SEQ EN	Sequence enable. Input which can be added as an external gate to the power up sequencing. It Is ANDed to the power up sequencing. It has no effect on power down sequencing. See register map. If not used, tie to 5VSYS pin.
5	PG1	Power good output 1, open drain. It can consist of any ANDed output of all of the five regulators. See register map.
6	GLOBAL EN	Device enable. When pulled low, shuts down entire chip after power down sequencing complete.
7	VIN	Input supply to the LDO.
8	LDO	Output of the 100mA LDO.
9	VOUT2	Feedback pin for Buck 2. Buck 2 can be programmed from 1.3V to 1.92V in 20mV steps.
10	PGND2	Power ground. Source of the low-side MOSFET for Buck 2.
11	LX2	Switch node of Buck 2. Connect to the output inductor.
12	VIN2	Input supply to Buck 2. Bypass to the PGND.
13	VIN4	Input supply to Buck 4. Bypass to the PGND.
14, 15, 16	LX4	Switch node of Buck 4. Connect to the output inductor.
17, 18	PGND4	Power ground. Source of the low-side MOSFET for Buck 4.
19	VOUT4	Feedback pin for Buck 4. Buck 4 can be programmed from 0.6V to 1.39375V in 6.25mV steps.
20	PG2	Power good output 2, open drain. It can consist of any ANDed output of all of the five regulators. See register map.
21	AN1	Input to ADC. If not used, tie to the AGND.
22	AN0	Input to ADC. If not used, tie to the AGND.
23	AGND	Signal analog ground. Connect to the system ground.
24	5VSYS	Filtered from VIN through an RC to provide internal circuits with clean 5V. Place a 100nF capacitor between this pin and the AGND as close as possible to the device.
25	VOUT1	Feedback pin for Buck 1. Buck 1 can be programmed from 3.0V to 3.6V in 20mV steps.
26	PGND1	Power ground. Source of the low-side MOSFET for Buck 1.
27	LX1	Switch node of Buck 1. Connect to the output inductor.
28	VIN1	Input supply to Buck 1. Bypass to the PGND.
29	VIN3	Input supply to Buck 3. Bypass to the PGND.
30	LX3	Switch node of Buck 3. Connect to the output inductor.
31	5VSYS	Connect to 5V input. Unlike Pin 24, bypassing is unimportant.
32	VOUT3	Feedback pin for Buck 3. Buck 3 can be programmed from 0.8V to 1.59375V in 6.25mV steps.
PAD	PGND	Package central pad. Connect to the PGND.

Typical Performance Characteristics

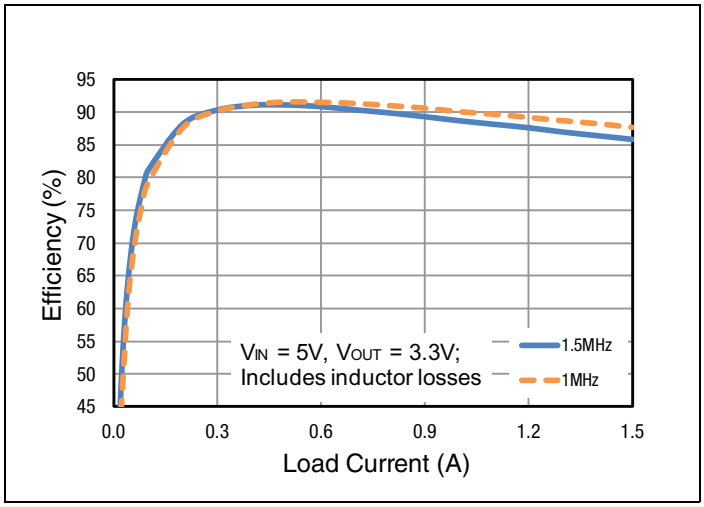


Figure 3: Buck 1 Efficiency

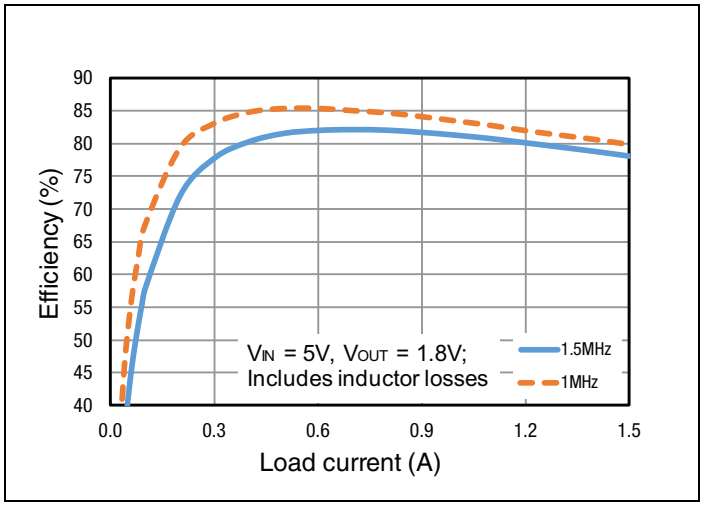


Figure 4: Buck 2 Efficiency

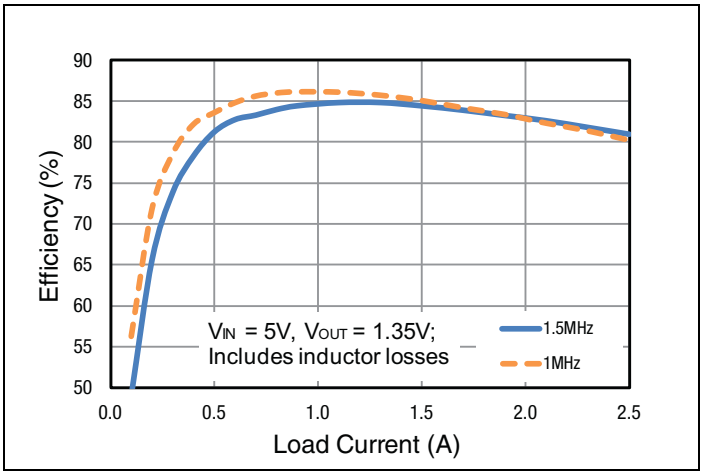


Figure 5: Buck 3 Efficiency

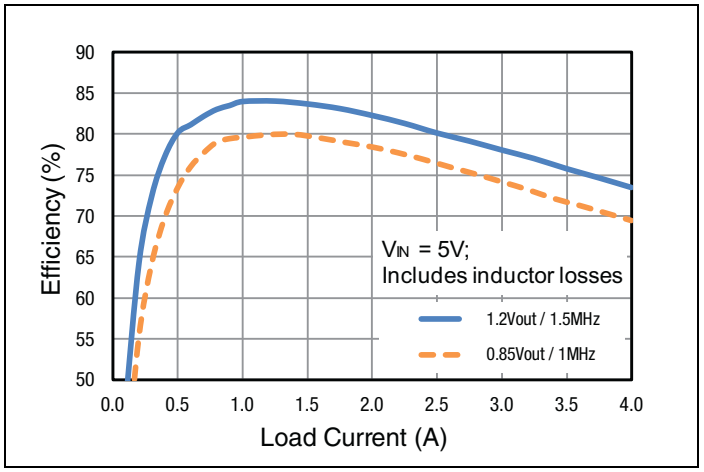


Figure 6: Buck 4 Efficiency

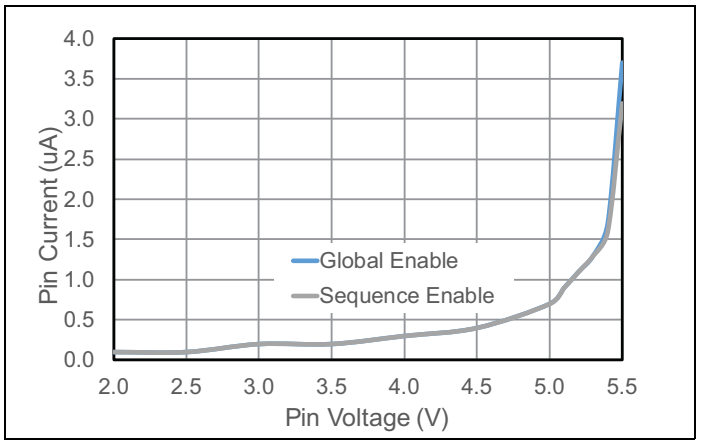


Figure 7: GLOBAL EN and SEQ EN Input Current vs Voltage

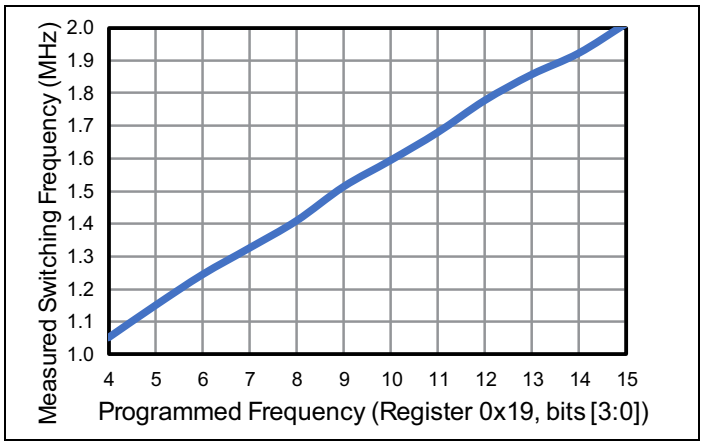


Figure 8: Measured vs Programmed Frequency

Typical Performance Characteristics (Continued)

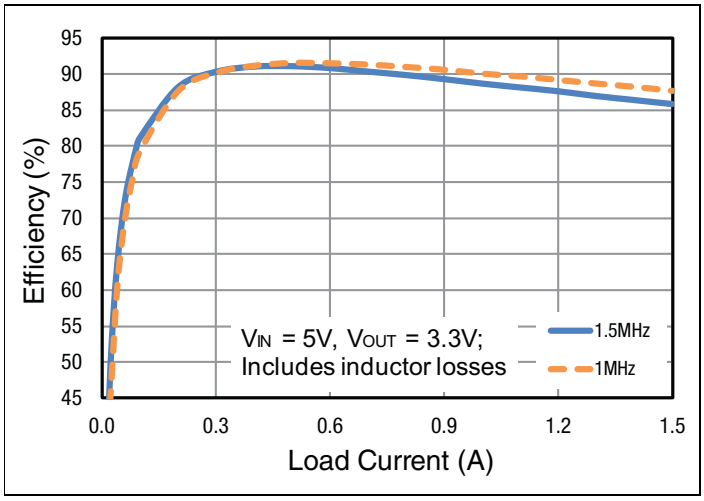


Figure 9: Buck 1 Power Loss

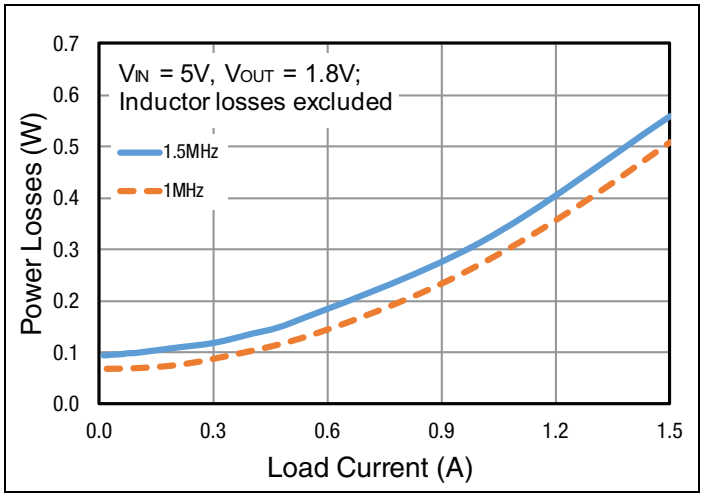


Figure 10: Buck 2 Power Loss

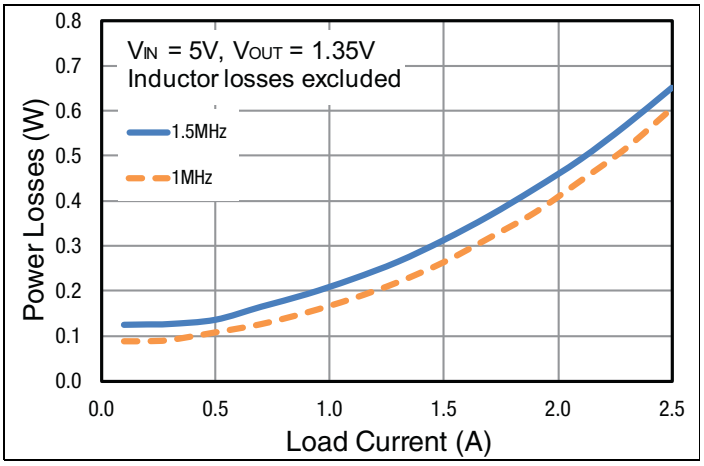


Figure 11: Buck 3 Power Loss

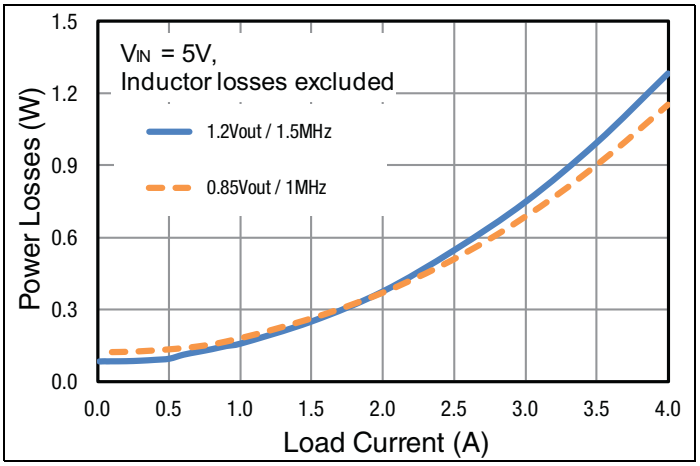


Figure 12: Buck 4 Power Loss

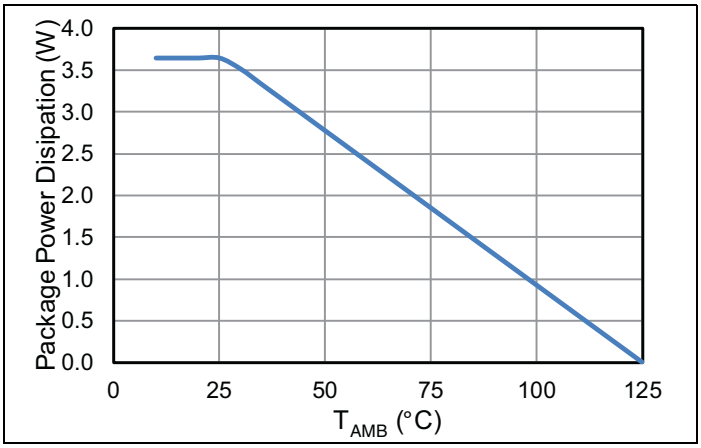


Figure 13: Package Derating

Functional Block Diagram

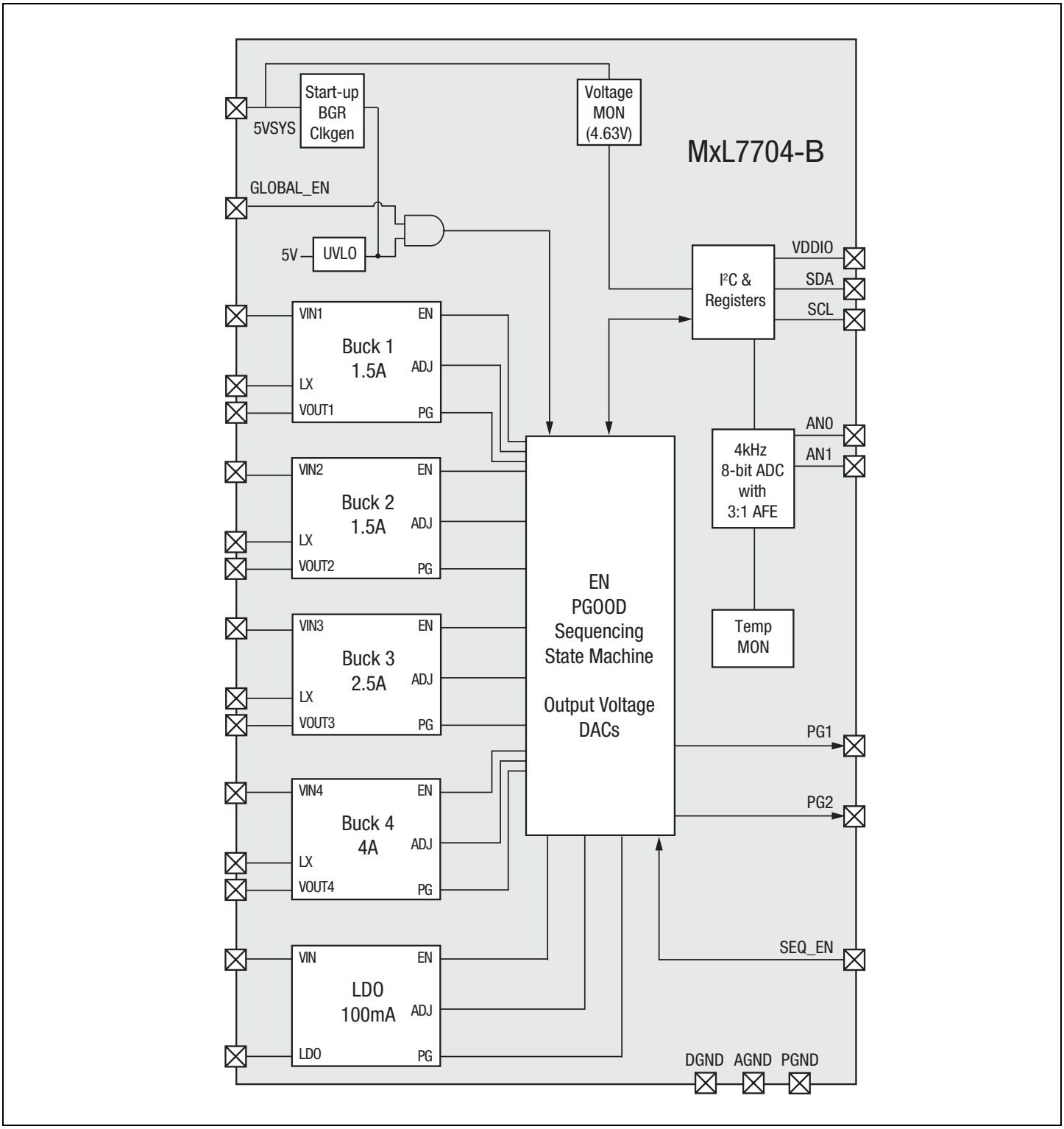


Figure 14: Functional Block Diagram

Applications Information

Operation

The MxL7704-B device is a 5-output universal PMIC optimized for powering low power FPGAs, DSPs, and microprocessors from a 5V input. Four independent buck the regulators provide load currents of 1.5A for the system power, 1.5A for I/O, 2.5A for memory, and 4A for core power. A 100mA LDO provides a clean 3.3V power for auxiliary devices. All outputs support margining where the initial set point can be changed by an 8-bit code. All outputs also support dynamic voltage scaling (DVS) where the output voltage can be dynamically ramped up or down at a preset rate to save power in processors that can use this function.

The I^2C interface allows you to monitor an input voltage flag and PGOOD flags for each output. The I^2C port can be also used to modify the power up and power down sequencing options, assign power good outputs to PG1 and PG2 pins, enable the PMIC outputs, and select the switching frequency.

All buck regulators employ peak current mode control architecture with internal compensation and high switching frequency. This provides fast transient response to load and line changes without sacrificing stability and keeping small component sizes on board.

Fault protection features include input undervoltage lockout (UVLO), output overcurrent protection (OCP), undervoltage protection (UVP), and over temperature (OTP) or thermal protection.

Two power good outputs are available (PG1, PG2).

Each channel has a soft-start, soft stop function and a DVS.

Output Voltage Scaling

All outputs support margining where the initial set point can be changed by an 8-bit code. Back to back voltage commands are not supported. You must wait for PGOOD blanking (2.2ms maximum) to complete before a subsequent DVS command can be sent. For reference, see Figure 16 on page 16.

The channel 1 range is from 3.0V to 3.6V with 20mV resolution.

Note: The channel 1 regulation is limited by maximum duty cycle.

The channel 2 dynamic range is from 1.3V to 1.92V with 20mV resolution, the channel 3 from 0.8V to 1.6V with 6.25mV resolution, and the channel 4 from 0.6V to 1.4V with 6.25mV resolution.

The channel 3 and 4 lower regulation range is limited by the minimum on time of 120ns.

The LDO dynamic range is from 1.5V to 3.3V with 20mV resolution. Rather than change the voltage divider resistances in the feedback path, the error amplifier reference is changed. This ensures that the gain of the control loop remains unchanged as the voltage is changed. When a voltage change is requested, the output slews at 10V/ms which minimizes the latency when moving from low power states to high power states.

Although the 8-bit register accepts values outside those within the ranges previously listed, the accuracy of the output is not guaranteed.

Sequencing

Power up and down sequencing is controlled by setting registers 0x15, 0x16, 0x17 and 0x19. Each channel (BUCK or LDO) can be assigned to be in any of four groups (group 0 thru 3) by programing register 0x15 and 0x16 (each of them has a 2-bit group register that assigns them to each of the four groups). When enabled through GLOBAL EN or the input voltage rising above the UVLO point, all outputs are discharged by enabling the 78Ω discharge resistors. This ensures proper sequencing after an input voltage glitch.

The sequencing state machine starts with group 0 and looks for any channels if assigned to it by their respective 2-bit group settings.

If any channels are assigned to group 0, the state machine starts them up at the same time, provided 5VSYS UVLO is cleared and the outputs assigned to GROUP 0 are discharged by the 78Ω resistor to <200mV.

Once all group 0 channels are up (all PGOODs are found with the 2ms blanking time added), the sequencing state machine moves to group 1 and repeats the same process, omitting the wait of the output to be discharged to <200mV. It continues to group and then group 3.

If one group is not up (at least one channel in the group is at fault or disabled thru register setting 0x16), all subsequent groups are not started. If a group does not have any channels, it is ignored and the sequencing state machine moves to the next one.

Power Down Sequencing of Channels

After a normal power up sequence is completed, the power down sequencing can be controlled by pulling GLOBAL EN LOW. Power down sequencing of channels follows the reverse order of the power up sequencing of channels (group 3 thru 0). Depending on the soft off enable setting (bit 6 of 0x19), channels are sequenced down in the method:

- Soft off enabled: Channels dynamically slewed down for Xms (where X = Vout) and discharged through the 78Ω resistor (default).

The LDO cannot slew negative by default. Thus it is immediately considered soft-off complete.

The MxL7704-B uses a digitally controlled soft-start and soft off. Each output, including the LDO, has an 8-bit reference DAC feeding the error amplifier input. Although the registers accept a value across the entire DAC range, the outputs are optimized for the output voltage ranges listed in Table 4 on page 2.

Note that after all channels are sequencing down by pulling GLOBAL EN LOW, the device is in a hard-reset mode.

When the device is shut down via thermal shutdown (TSD), the channels are immediately tri-stated and discharged by the 78Ω active discharge resistance. Bit 6 at register address 0x19 is ignored.

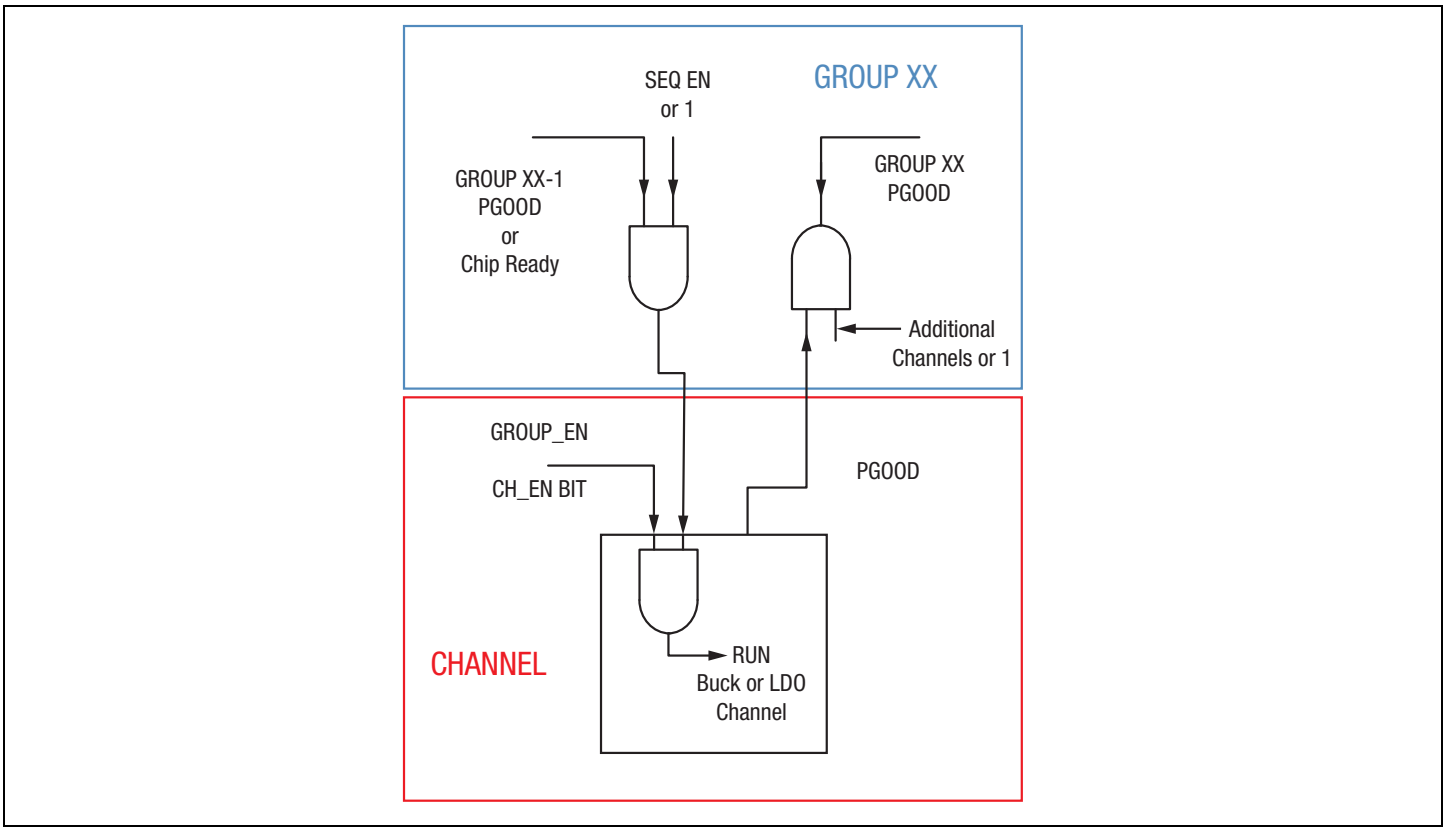


Figure 15: Sequencing

SEQ EN and Channel Enable Bits

The SEQ EN pin input can be assigned to any of the sequence groups and an external signal can gate sequencing. This is accomplished by setting bits [7:6] of register 0x17, which acts as an enabler to that group and all other subsequently higher groups. Therefore each channel has its own channel enable (bits [4:0] of register 0x16), group enable needs to be enabled as well to effectively enable a channel.

- If SEQ EN is LOW at start, it gates the startup of the group that is assigned to it, and hence all other subsequent higher groups.
- Having SEQ EN HIGH at startup, it voids its effect (all group enabled are ON) on the soft-start sequencing.

You can always use SEQ EN (pulling HIGH/LOW) to turn on/off multiple groups/channels at any time by moving/setting SEQ EN group assign (bit [7:6] of register 0x17).

- If SEQ EN is LOW, the group/channel(s) assigned to the SEQ EN shuts down according to the soft off enable setting (bit 6 of 0x19) without any power down sequencing.
- If SEQ EN is HIGH, when GLOBAL EN is driven low, it does not gate the sequential power down of the sequencing groups.

You can always use channel enable bits (bits [4:0] of the register 0x16) to gate sequencing through the I^2C interface. However once power up sequencing is completed, the channel enable bits can only turn on or off particular channels.

Changing Sequencing Registers While Operating

Sequencing registers can be changed during chip operation. Therefore, you can change the power down behavior versus the startup behavior.

Note: MaxLinear recommends that you do not write to these registers when the device is powering up or down.

PGOOD

The state of the PGOOD of each channel gates power up of subsequent higher groups. The state of the PGOOD signals are reported in the status register 0x1A bits [4:0].

At the end of the soft-start, the PGOOD increases after the 2ms PGOOD assertion delay. If a channel goes out of the regulation window for more than 65µs during regulation, the PGOOD decreases. It asserts again after the 2ms assertion delay, assuming the channel is back into the regulation window. If the glitch is faster than 65µs, PGOOD does not record it.

During the DVS, the PGOOD is blanked and held HIGH. Once the DVS is done, the PGOOD is re-evaluated and an effective PGOOD is updated.

In the event of a fault, the PGOOD is pulled low immediately.

The registers 0x17 and 0x18 are used to route the PGOOD signals from all channels to the PG1 and the PG2 outputs respectively. Multiple channels can be assigned and the PG1 or PG2 signals is logic function AND of the selected PGOOD signals. If no channels are assigned to a PG pin, the pin is high impedance.

Input Voltage Monitor Flag

The device is continually monitoring voltage at the 5VSYS pin. The status of this pin is kept in register 0x1A (bit [6:5]).

Bit 5 provides the current status of this pin while bit 6 is *sticky* set once the 5VSYS pin is above 4.63V. If the voltage at the 5VSYS pin is above 4.63V, bit 5 is set or vice versa. The host can poll these two bits to check the status of this pin.

Bit 6 can only be cleared by the host writing *1* to it.

Hot Start

If chip fault action is selected and a fault occurs, the start-up sequencing varies from a cold start where the GLOBAL EN or UVLO enables the device.

Only the outputs in sequencing group 0 is discharged; instead of discharging all outputs in all sequencing groups to <200mV.

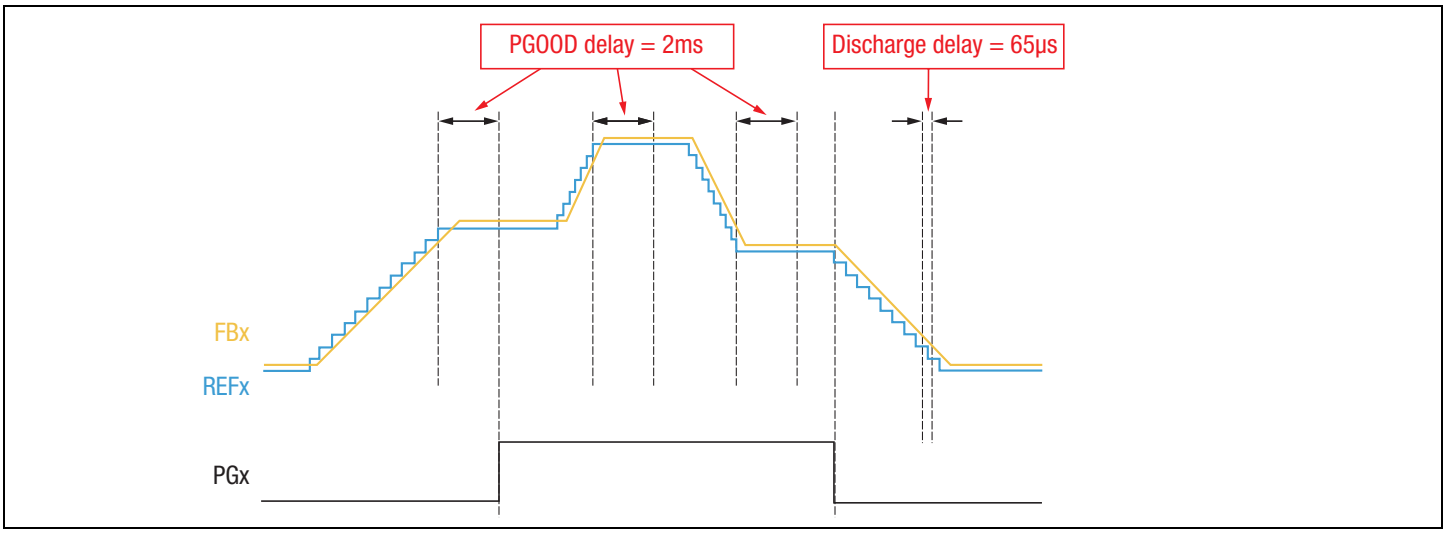


Figure 16: Power Good Timing

Faults

Under Voltage Protection (UVP)

A fault condition is reported by the switching regulators and a restart is initiated when an under voltage is detected on the output. That channel immediately tri-states and applies the 78Ω discharge. If a device fault action is selected, all of the other outputs simultaneously power down based on their power down settings. Once all of the channels are powered down, a 1ms delay gates the restart of the channel or the device. In a restart, just as in initial power up, the first sequencing GROUP channels is discharged to <200mV before power up sequence initiates.

Output Over Voltage Protection (OVP)

When an output is accidentally connected to a source higher than the target voltage of the buck regulator, the buck regulator can clamp that voltage. It is the natural response of the control loop to turn on the low side MOSFET and tries to clamp the output voltage. The buck regulator tries to protect the lower voltage, higher value circuitry to the point of destruction.

Over Current Protection (OCP)

A current limit event occurs when the over current threshold exceeds for eight or more switching cycles. Once detected, the switches are placed into tri-state. As it happens with UVP, that channel tri-states and applies the 78Ω discharge. If a device fault action is selected, all of the other outputs simultaneously power down based on their power down settings. Once all of the channels are powered down, a 1ms delay gates the restart of the channel or the device.

Unlike the initial power up where all of the outputs are discharged before sequencing initiates with sequencing group 0, during any *hot* restart, the outputs for a given group are discharged before to that group that is enabled.

During soft-start, the OCP is disabled for the first 25% of the soft-start time period. If the output voltage is 1V, then the soft-start time is 1ms and thus the current limit is enabled after the first 250µs. The LDO OCP is activated after its soft-start timer expires.

Channel/Chip Fault Actions

The register 0x19 bit 7 allows you to choose whether a fault on a given channel only affects that channel or causes an entire restart of the power system. If *channel* is selected, 0x19 bit 7 = 0, then when a fault occurs on any channel, that channel faults and initiates a restart without affecting any of the other outputs.

If *chip* is selected, 0x19 bit 7 = 1, a fault on any channel causes the other channels to down sequence together based on the register 0x19 bit 6 setting and subsequently initiate power up sequence once channels discharge and the 1ms hiccup timer expires.

This register can be changed during chip operation. If the fault action is changed from the channel to the chip while the outputs are enabled and a fault previously occurs, then the chip detects that fault and initiates a chip fault action. If the outputs are shut down when this change is made to the register no restart occurs.

Thermal Design

Proper thermal design is critical when you control the device temperatures and develop robust designs. One key factor that affects the thermal performance is the temperature rise of the devices in the package. It is a function of the thermal resistances of the package and the power that is internally dissipated .

“Operating Conditions” on page 1 describes the thermal resistance of MxL7704-B (27°C/W). The Θ_{JA} thermal resistance specification is based on the MxL7704-B evaluation board that operates without forced airflow.

The package thermal derating and power loss curves are shown in Figure 9 on page 10 through Figure 13 on page 10.

Layout Guidelines

The PCB layout determines a good thermal and electrical performance.

For thermal considerations, it is essential to use more thermal vias to connect the central thermal pad to the ground layer(s).

To achieve good electrical and noise performance, MaxLinear recommends the following steps:

1. Place the output inductor close to the LX pins and minimize the connection area. MaxLinear recommends that you do this on the top layer.
2. Connect the central thermal pad of the power ground connections to as many layers as possible. It improves the thermal conduction.
3. Ensure that the output filtering capacitor shares the same power ground connection as the input filtering capacitor of the same buck converter. This should be connected to the signal ground plane with vias placed at the output filtering capacitors.
4. Minimize the AC current loops formed by input filtering capacitors, output filtering capacitors, output inductors, and the regulator pins.
5. Connect the AGND pins to the signal ground plane.
6. Place a low pass filter in front of the 5VSYS pin.
7. Place also a 100nF capacitor between the 5VSYS and AGND as close as possible to the device.

I²C Operation

The interface is 3.3V with tolerance to 5.5V.

Since there is no clock stretching allowed, the MxL7704-B responds by not acknowledging (NAK) some I²C commands. It informs the host that it cannot service them.

The MxL7704-B device responds with a NAK if the delay between writing to the same LDO or soft-start register is less than 2.2ms (2ms + 10% internal oscillator accuracy). In addition, if multiple LDO or Buck outputs are changed within 2.2ms of each other, then each output can only be changed once within those 2.2ms. The I²C master must wait at least 2.2ms after the last I²C write to the LDO or VBuckx register before writing to them again.

Example 1: Changing outputs for VBuck3 and VBuck4.

If writing to VBuck3 followed by VBuck4, then the I²C master must wait at least 2.2ms after the write to VBuck4 before writing to VBuck3 or VBuck4 again.

Example 2: Changing all outputs.

If writing to VLDO, VBuck1, VBuck2, VBuck3 and VBuck4, then the I²C master must wait for at least 2.2ms after the last write to these registers before writing to any of these registers again.

Minimum t_{ON} and Minimum Duty Cycle Limitation

The minimum on-time t_{ON} of the MxL7704-B device is at 120ns. If a low duty cycle application requires a shorter t_{ON}, the regulation is lost. The minimum permissible V_{OUT} corresponding to switching frequency *f* with an assumed efficiency of <85% can be calculated as follows:

$$0.85 \times \frac{V_{OUT}}{V_{IN}} = \frac{t_{ON}}{T} = t_{ON} \times f$$

$$V_{OUT} = V_{IN} \times f \times 120ns \times 0.85$$

Where $V_{IN(MAX)}$ = 5.5V.

Table 6: Minimum Permissible V_{OUT}

f (MHz)	$V_{OUT(MIN)}$ (V)
1	0.600
1.1	0.617
1.2	0.673
1.3	0.729
1.4	0.785
1.5	0.842
1.6	0.898
1.7	0.954
1.8	1.010
1.9	1.066
2	1.122
2.1	1.178

Buck 1 Operation at Low V_{IN}

When V_{IN} - V_{OUT} is lower than 0.8V (for example, V_{OUT} = 3.6V, V_{IN} < 4.4V) the controller skips pulses to maintain regulation. Under steady-state operation, the controller typically regulates with V_{IN} as low as 4.0V. If conditions result in a dropout, the upper MOSFET can operate at 100% duty cycle. Operating at or near the dropout can affect the dynamic performance including a load transient response and a positive dynamic voltage scaling.

Minimum Effective C_{OUT}

The MxL7704-B device has internal feedback loop compensation. Each channel requires a minimum COUT to have a sufficient phase margin and stable feedback loop. The effective COUT for a couple of different use cases is listed in Table 7. The 1MHz case is that shown in Figure 19 on page 23. The nominal capacitance for a given set of operating conditions must be calculated from manufacturer's data sheet by using applicable derating curves.

Table 7: Recommended L and C_{OUT}

f (MHz)	Channel	V_{OUT} (V)	L (µH)	Effective COUT (µF)
1.5	1	3.3	2.2	15
	2	1.8	1	20
	3	1.35	0.47	90
	4	1.2	0.47	110
1	1	3.3	2.2	22
	2	1.8	2.2	27
	3	1.35	1	110
	4	0.85	0.47	210

You can calculate the inductor value for different V_{OUT} as follows:

$$L \geq \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\Delta i \times f \times V_{IN}}$$

V_{IN} = Typical input voltage.

V_{OUT} = Desired output voltage.

f = Switching frequency of the converter.

Δi = inductor ripple current.

An expected estimate for the inductor ripple current (Δi) is from 20% to 40% of the maximum output current. For more information, see I_{OUT} in Table 4 on page 2.

If you do not use an output at the maximum output current, MaxLinear recommends that you use an inductor value that do not exceed 50% of the calculated inductor value with the maximum output current.

Note that the inductor must always have a higher rating than the maximum current because the current increases with decreasing inductance.

Dynamic Voltage Scaling

All four buck regulators support DVS. The dynamic output slew rate is 10V/ms (nominal).

Note: MaxLinear recommends that you do not ramp up DVS (that is, increase V_{OUT}) at the maximum rated current. It can cause a premature over-current protection (OCP) event caused by the high inrush current due to the high slew rate of 10V/ms.

As an example, consider Buck 4 of MxL7704-B operating at 1MHz with L = 0.47µH and COUT (effective) = 210µF. The inrush current corresponding to the DVS can be calculated as follows:

$$I_{INRUSH} = 210\mu F \times 10V/ms = 2.1A$$

$$I_{INRUSH} = C_{OUT} \times \frac{\Delta V_{OUT}}{\Delta t}$$

Therefore, peak inrush current is:

$$I_{INRUSHPEAK} = 2.1A + (0.5 \times 1.52A) = 2.86A$$

The minimum current limit is 5.5A for Buck 4. Therefore, the maximum permissible output current while using the DVS is as follows:

$$I_{OUT} = 5.5A - 2.86A = 2.64A$$

The actual analysis should be carried out to ensure that the inrush current of a large C_{OUT} does not result in a premature OCP.

Output Voltages Outside Ranges Guaranteed in Electrical Table

The MxL7704-B has four internally compensated current-mode synchronous buck regulators that are characterized from 1MHz to 2.1MHz switching frequency according to the electrical table:

- Buck 1: 3.0V–3.6V, 20mV step, 1.5A
- Buck 2: 1.3V–1.92V, 20mV step, 1.5A
- Buck 3: 0.8V–1.6V, 6.25mV step, 2.5A
- Buck 4: 0.6V–1.4V, 6.25mV step, 4A

The accuracy of the output voltages is guaranteed over these ranges and the internal compensation is optimized for these operating points. However, the programmable range for the Buck 1 and Buck 2 voltage set point register is 20mV to 3.6V and for Buck 3 and Buck 4 it is 6.25mV to 1.59375V.

Although accuracy is not guaranteed outside the limits of the data sheet, the DACs are tested across the entire settable range. Testing the DACs is necessary because they are used to implement the startup (soft-start) and shutdown sequencing. Figure 16 on page 16 shows *REFx*, which is the DAC output. As such, at each startup, the device is demonstrated to operate properly across the entire DAC range.

The MxL7704-B can operate across this range because it changes the DAC voltage into the error amplifier rather than changing the feedback resistors. The control loop gain is thus held constant across the entire DAC range.

$$H(s)\alpha - \frac{V_{REF}}{V_{OUT}}$$

The control loop gain is proportional to the ratio between V_{REF} and V_{OUT}.

The following figure shows the control loop architecture of the MxL7704-B.

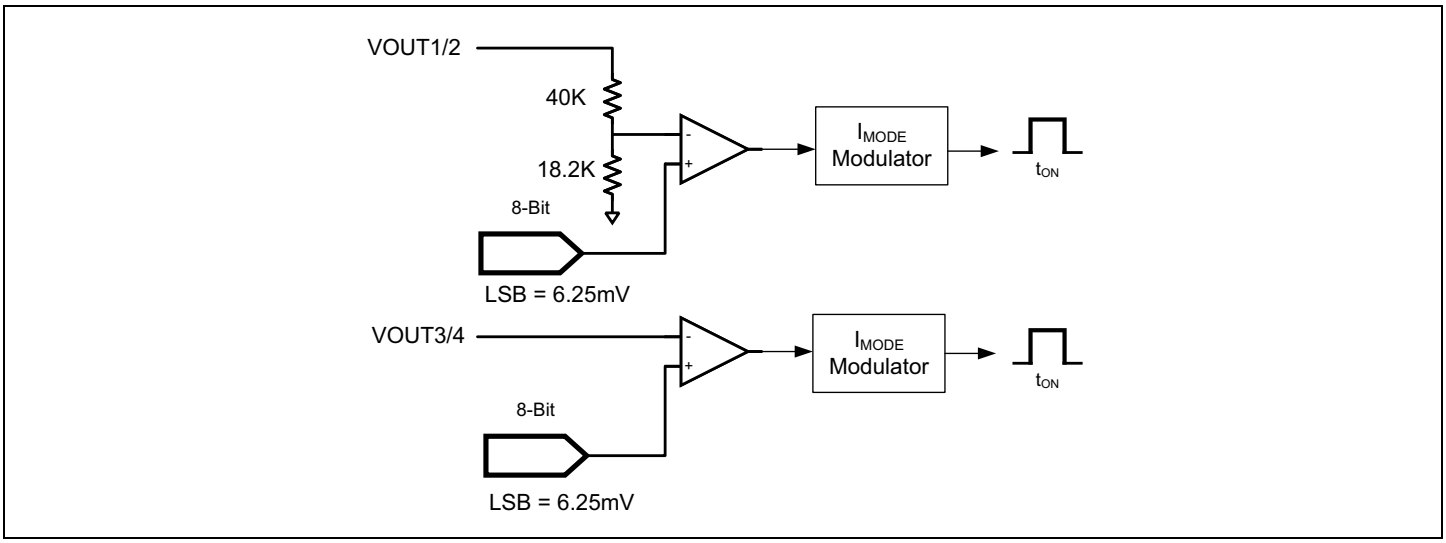


Figure 17: MxL7704-B Control Loop Architecture

If you wish to use the MxL7704-B outside the voltage limits stated on the data sheet, MaxLinear recommends that you perform simple transient tests to check stability before releasing a design to production. These tests are:

- 25% to 75% load change at 1A/µs
- 75% to 25% load change at 1A/µs

The result should show a damped response without ringing like the example shown in Figure 18. This is Buck 3 set to 1.2V output at 1MHz switching frequency using a 1µH inductor and three JMK212BBJ476MG ceramic capacitors with an effective capacitance of 110µF. The load step is from 0A to 2.5A. If the output shows ringing during the transient test, reducing the inductance generally improves the results.

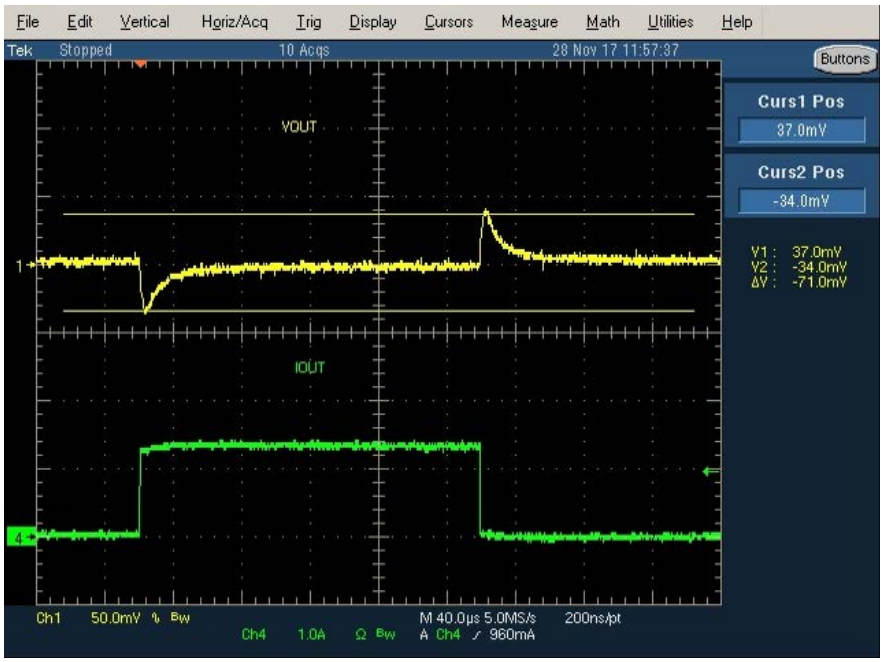


Figure 18: Damped Response without Ringing

Analog to Digital Converter and Temperature Sensor

The MxL7704-B device has a built in 8-bit analog-to-digital converter (ADC) and a temperature sensor. The ADC has three analog inputs: AN0, AN1, and TEMP. The AN0 and AN1 inputs are external analog signals that you can apply for conversion. The TEMP input internally monitors the temperature sensor output. Temperature data can be read from the register address 0x1B and is calculated as follows:

$$DECIMAL = [(T_{SENSOR} - 25°C) \times 1.06LSB/°C] + 95$$

Where:

T_{SENSOR} = Temperature of the internal sensor.

1.06LSB/°C = Nominal resolution of the DAC.

Therefore, at an ambient of 25°C the register should typically return a value of 95 (decimal) or 0x5F (hex) when the four bucks are turned off to reduce internal heating.

The register addresses 0x1C and 0x1D contain the outputs that correspond to the analog inputs AN0 and AN1 respectively. The ADC has a nominal zero error (offset) of typically +3 LSB. Therefore, an input voltage of 30mV is required to produce an output transition of 00 to 01. INL is calibrated at (1.75V + offset) and specified ±2 LSB. For best ADC performance, the 5VSYS pin must be bypassed to the AGND with a 10µF, 1µF and 0.1µF capacitor. You must place the 0.1µF as close to the device as possible. MaxLinear recommends that you use a lowpass filter 0.1µF/100Ω at the AN0 and AN1 inputs.

The default ADC EN bit in MxL7704-B is enabled and automatically calibrated every time when the PMIC is powered.

Typical Application

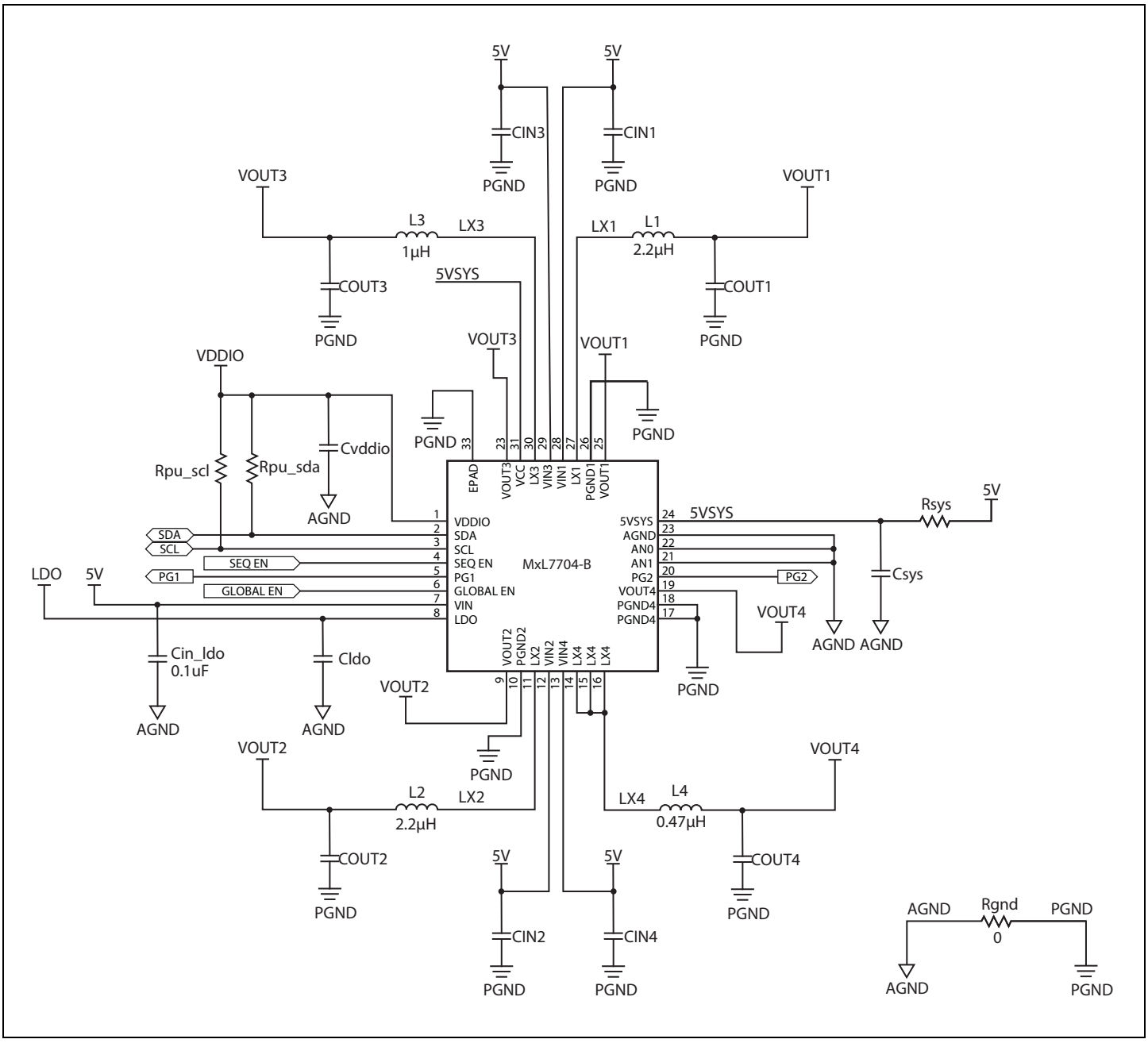


Figure 19: MxL7704-B Typical Application

Register Information

Slave I²C Address

Table 8: Slave I²C Address

Device	7-Bit Address
MxL7704-B	0x2D

Register Map

The runtime registers can be changed through the I²C.

Table 9: Register Map

Address	Register	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x01	ADC enable	R/W	-	-	-	-	-	-	-	ADC EN
0x11	Vout Buck 1	R/W	VBuck1[7:0]							
0x12	Vout Buck 2	R/W	VBuck2[7:0]							
0x13	Vout Buck 3	R/W	VBuck3[7:0]							
0x14	Vout Buck 4	R/W	VBuck4[7:0]							
0x15	Buck sequence group assignment	R/W	Buck 4 [1:0]		Buck 3 [1:0]		Buck 2 [1:0]		Buck 1 [1:0]	
0x16	LDO sequence group assignment and channel enables	R/W	LDO[1:0]		-	EN4	EN3	EN2	EN1	ENL
0x17	SEQ EN assign and PG1 routing	R/W	EN Assign		-	Buck 4	Buck 3	Buck 2	Buck 1	LDO
0x18	PG2 routing	R/W	-	-	-	Buck 4	Buck 3	Buck 2	Buck 1	LDO
0x19	Fault actions, down sequencing, and frequency	R/W	Chip/ Channel	Soft Off EN	78Ω Discharge		FREQ[3:0](1)			
0x1A	PGOOD and UV	R	TWARN 105C	UV Flag	UV Current	PG Buck4	PG Buck3	PG Buck2	PG Buck1	PG LDO
0x1B	Temp	R	Temp[7:0]							
0x1C	ADC0	R	ADC1[7:0]							
0x1D	ADC1	R	ADC2[7:0]							

1. Must not be written dynamically.

Default Values

Table 10: Default Values

Address	Register	Default Value	Value Description
0x01	ADC enable	0x01	Enabled.
0x10	Vout LDO	0xA5	3.3V.
0x11	Vout Buck 1	0x00	Unprogrammed.
0x12	Vout Buck 2	0x00	
0x13	Vout Buck 3	0x00	
0x14	Vout Buck 4	0x00	
0x15	Buck sequence group assignment	0x00	
0x16	LDO sequence group assignment and channel enables	0x00	
0x17	SEQ EN assign and PG1 routing	0x20	
0x18	PG2 routing	0x00	
0x19	Fault actions, down sequencing, frequency	0x00	-
0x1A	PGOOD and UV	Read	-
0x1B	Temp	Read	-
0x1C	AN0	Read	-
0x1D	AN1	Read	-

Note: For more information about how to generate register values, go to MxL7704 Configuration Tool Rev 2.0 and download an Excel based configuration tool.

Register Descriptions

V_{OUT} Buck 1 (0x11)—Read/Write

Bit	Description
7:0	VBuck1[7:0] Buck 1 Output voltage setting. 20mV resolution. The device NAK if the output has not completed the prior voltage change and a second voltage change is requested on this channel. For more details, see "I²C Operation" on page 18. Although this register accepts any value in its range from 0x00 to 0xFF, the output voltage accuracy is not guaranteed outside the range listed in Table 4 on page 2. Note that 0xBF corresponds to 3.6V, the maximum Buck 1 voltage.

V_{OUT} Buck 2 (0x12)—Read/Write

Bit	Description
7:0	VBuck2[7:0] Output voltage setting. 20mV resolution. The device NAK if the output has not completed the prior voltage change and a second voltage change is requested on this channel. For more details, see "I²C Operation" on page 18. Although this register accepts any value in its range from 0x00 to 0xFF, the output voltage accuracy is not guaranteed outside the range listed in Table 4 on page 2. Note that 0x60 corresponds to 1.92V, the maximum Buck 2 voltage. Minimum controllable output voltage is a function of the selected frequency and the minimum on-time. For more information, see Table 6 on page 18.

V_{OUT} Buck 3 (0x13)—Read/Write

Bit	Description
7:0	VBuck3[7:0] Output voltage setting. 6.25mV resolution. The device NAK if the output has not completed the prior voltage change and a second voltage change is requested on this channel. For more details, see "I²C Operation" on page 18. Although this register accepts any value in its range from 0x00 to 0xFF, the output voltage accuracy is not guaranteed outside the range listed in Table 4 on page 2. Note that 0xFF corresponds to 1.59375V, the maximum Buck 3 voltage. Minimum controllable output voltage is a function of the selected frequency and the minimum on-time. For more information, see Table 6 on page 18.

V_{OUT} Buck 4 (0x14)—Read/Write

Bit	Description
7:0	VBuck4[7:0] Output voltage setting. 6.25mV resolution. The device NAK if the output has not completed the prior voltage change and a second voltage change is requested on this channel. For more details, see "I²C Operation" on page 18. Although this register accepts any value in its range from 0x00 to 0xFF, the output voltage accuracy is not guaranteed outside the range listed in Table 4 on page 2. Note that 0xDF corresponds to 1.39375V, the maximum Buck 4 voltage. Minimum controllable output voltage is a function of the selected frequency and the minimum on-time. For more information, see Table 6 on page 18).

Buck Sequence Group Assignment (0x15)—Read/Write

Bit		Description
7:6	Buck 4	Sequencing. 2 bits assigns each buck regulator to a sequencing group. Sequencing powers up each group 00, 01, 10, and 11 in order and in power down sequencing, the order is reversed. Skipping a value has no effect on the power up.
5:4	Buck 3	
3:2	Buck 2	
1:0	Buck 1	

LDO Sequence Group Assignment and Channel Enables (0x16)—Read/Write

Bit		Description
7:6	LDO	Sequencing. 2 bits assigns LDO to a sequencing group. Skipping a value has no effect on the power up.
5	Unused	
4	EN4	Channel enable. If OTP value 0 and assigned a slot in the sequencing, sequencing stops at this device. To complete power up sequencing, the host must change this bit to 1.
3	EN3	
2	EN2	
1	EN1	
0	ENL	

SEQ EN Assign and PG1 Routing (0x17)—Read/Write

Bit	Description
7:6	SEQ EN Assign. Assigns the SEQ EN input to the sequence group. It is logically ANDed to the prior groups PGOOD. For example, if assigned to group 00, then the device enables, but no outputs power on until SEQ EN is logic HIGH. This configuration can help when debugging system sequencing requirements.
5	Unused. Default value from factory is 1.
4	PG1 Routing Buck 4. 1: Selects the PG status of that output and the AND gate with others selected.
3	PG1 Routing Buck 3. 1: Selects the PG status of that output and the AND gate with others selected.
2	PG1 Routing Buck 2. 1: Selects the PG status of that output and the AND gate with others selected.
1	PG1 Routing Buck 1. 1: Selects the PG status of that output and the AND gate with others selected.
0	PG1 Routing LDO. 1: Selects the PG status of that output and the AND gate with others selected.

PG2 Routing (0x18)—Read/Write

Bit	Description
7:5	unused.
4	PG2 Routing Buck 4. 1: Selects the PG status of that output and the AND gate with others selected.
3	PG2 Routing Buck 3. 1: Selects the PG status of that output and the AND gate with others selected.
2	PG2 Routing Buck 2. 1: Selects the PG status of that output and the AND gate with others selected.
1	PG2 Routing Buck 1. 1: Selects the PG status of that output and the AND gate with others selected.
0	PG2 Routing LDO. 1: Selects the PG status of that output and the AND gate with others selected.

Fault Actions, Down Sequencing, Frequency (0x19)—Read/Write

Bit	Description
7	Chip/Channel. 0: Only the individual channel resets during a fault on that channel. 1: Whole device resets if any output faults.
6	Soft Off. 0: Disabled—immediate tri-state when shut down. 1: Slews output to Ref DAC = 0V and then tri-state.
5	78Ω discharge. 1: Connects 78Ω to ground when the channel is shut down. If Bit 6 = 1, 78Ω is connected once Ref DAC = 0V. MaxLinear recommends that you set this bit to 1 to ensure full discharge of the outputs.
4	Reserved.
3:0	FREQ. Switching frequency from 1MHz to 2.1MHz, 90kHz resolution 4-bit.

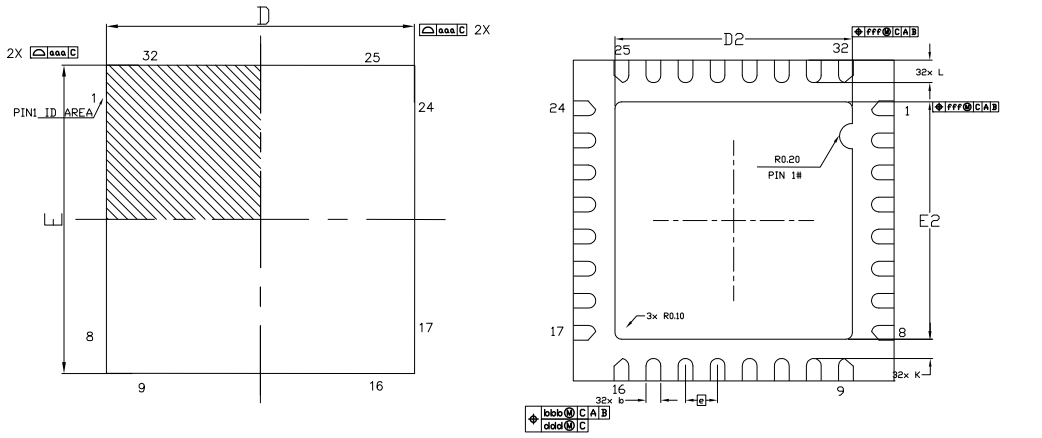
PGOOD and UV (0x1A)—Read/Write

Bit	Description
7	If the: ■ Device temperature > 105°C, this bit sets as the temperature warning flag. ■ Device temperature ≤ threshold, this bit is cleared.
6	UV Flag. Indicates the input voltage is once lower than 4.63V after having once higher than it. If this bit is 0 and bit 5 is 1, the input has never risen above the UV threshold. This is a sticky flag. It can ONLY be cleared by writing 1 to this bit. The register updates any cleared value every 250µs.
5	Provides the current status of 5VSYS pin.
4	PG Buck 4. 0: Output is lower than 94% of target V_{OUT} (nominal).
3	PG Buck 3. 0: Output is lower than 94% of target V_{OUT} (nominal).
2	PG Buck 2. 0: Output is lower than 94% of target V_{OUT} (nominal).
1	PG Buck 1. 0: Output is lower than 94% of target V_{OUT} (nominal).
0	PG LDO. 0: Output is lower than 94% of target V_{OUT} (nominal).

Note: Writing to this register only affects the UV flag (bit 6) of this register in the meaning of clearing the flag.

Mechanical Dimensions

5mm x 5mm 32-Pin QFN



DIM / SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	---	0.20Ref	---
b	0.18	0.23	0.28
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
D2	3.55	3.65	3.75
E2	3.55	3.65	3.75
L	0.30	0.35	0.40
K	0.20	–	–
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	
N		32	

TERMINAL DETAILS

- ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.
- DIMENSIONS AND TOLERANCE PER JEDEC MO-220.

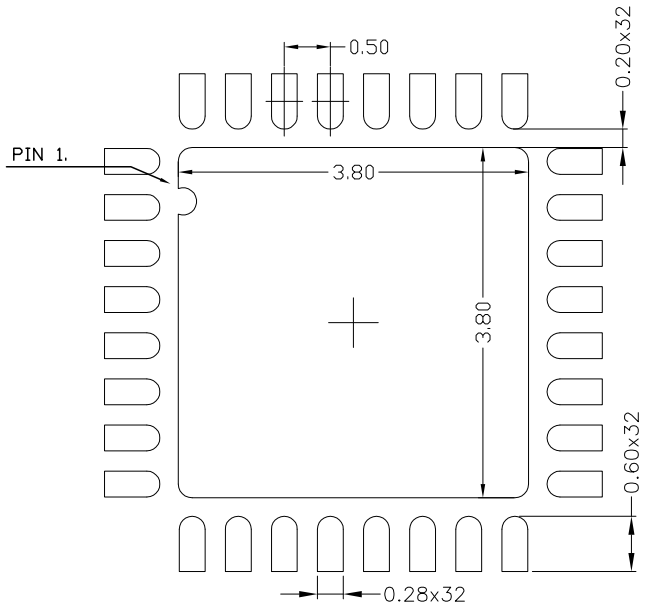
Drawing No.: POD-00000104

Revision: B.1

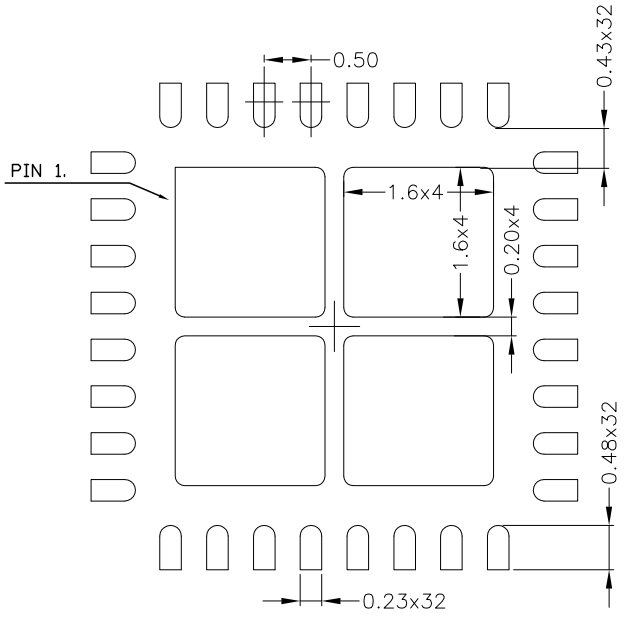
Figure 20: Mechanical Dimensions

Recommended Land Pattern and Stencil

5mm x 5mm 32-Pin QFN



TYPICAL RECOMMENDED LAND PATTERN



TYPICAL RECOMMENDED STENCIL

Drawing No.: POD-00000104

Revision: B.1

Figure 21: Recommended Land Pattern and Stencil