MYiR 米尔电子
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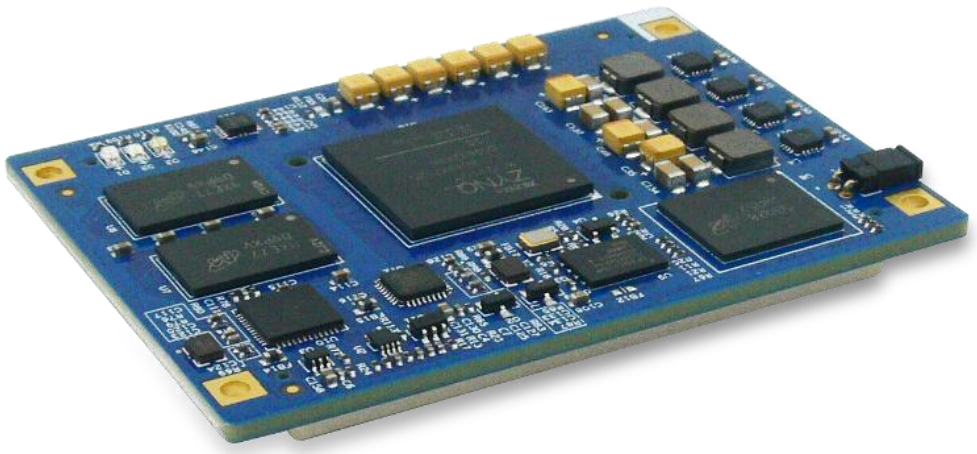
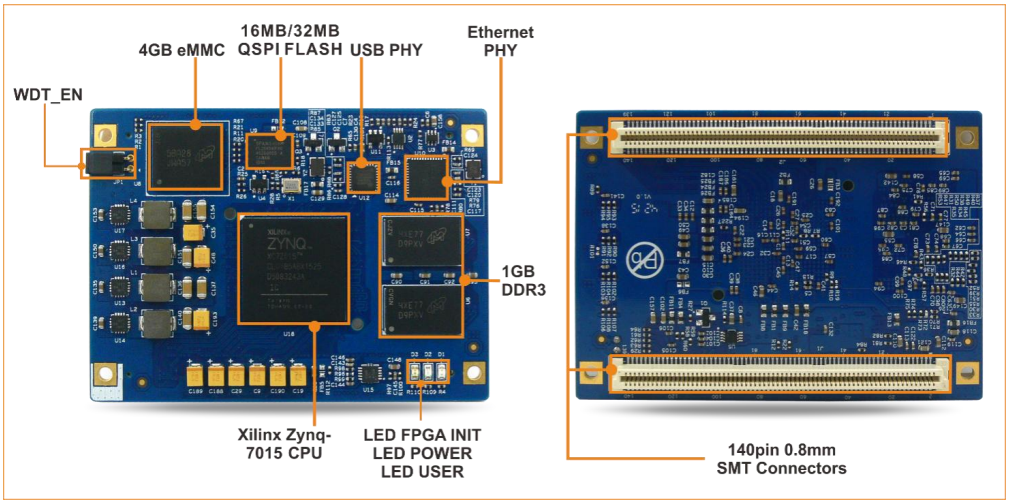
MYC-C7Z015 CPU Module Overview



- ✓ *766MHz Xilinx XC7Z015 Dual-core ARM Cortex-A9 Processor with Xilinx 7-series FPGA logic*
- ✓ *1GB DDR3 SDRAM (2 x 512MB, 32-bit), 4GB eMMC, 32MB QSPI Flash*
- ✓ *On-board Gigabit Ethernet PHY*
- ✓ *Two 0.8mm pitch 140-pin Board-to-Board Expansion Connectors*
- ✓ *Ready-to-Run Linux 5.4.0*

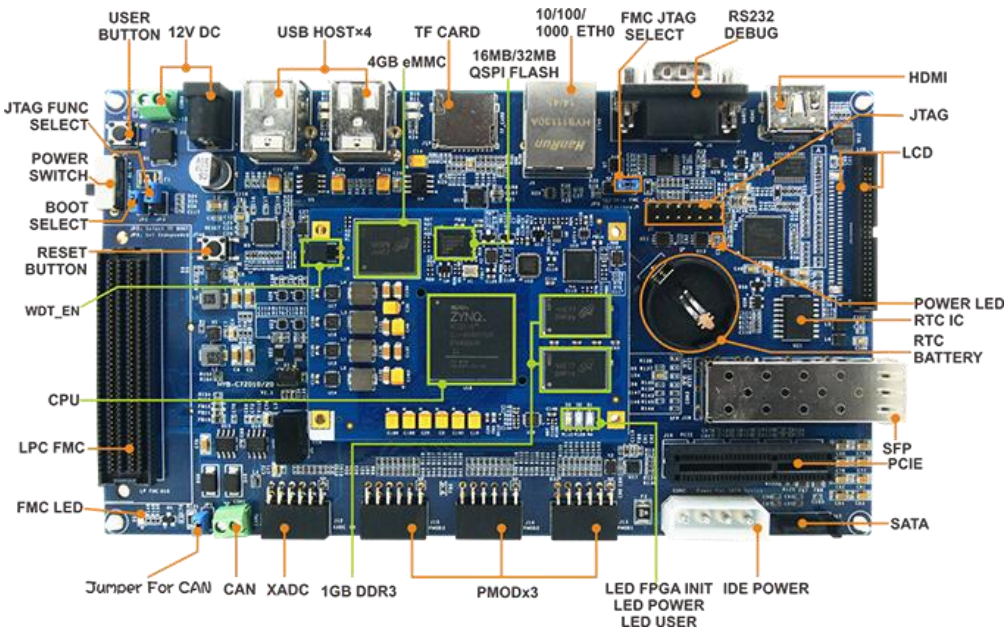
The **MYC-C7Z015 CPU Module** is an SOM (System on Module) board based on Xilinx XC7Z015 (Z-7015) All Programmable System-on-Chip (SoC) which is among the **Xilinx Zynq-7000** family, featuring integrated dual-core **ARM Cortex-A9** processor with Xilinx 7-series FPGA logic, four 6.25Gbps SerDes transceivers and one PCIe Gen2 x 4 integrated block. The MYC-C7Z015 module has **1GB DDR3 SDRAM, 4GB eMMC, 32MB quad SPI Flash, a Gigabit Ethernet PHY, a USB PHY and external watchdog** on board. It provides a large number of I/O signals for ARM peripherals and FPGA I/Os through **two 0.8mm pitch 140-pin board-to-board connectors**, which is ideal for your next embedded design.



MYC-C7Z015 CPU Module

The MYC-C7Z015 CPU Module is compatible with MYIR's MYC-C7Z010/20 CPU Modules and they can share the same base board which is designed by MYIR for evaluation or prototype purpose. The **MYD-C7Z015 development board** takes full features of the Zynq-7015 SoC. It has full features of the MYD-C7Z010/20 development board, additionally, it has one PCIe interface with two lanes and one SFP transceiver module interface.

The MYC-C7Z015 CPU Module is ready to run Linux 5.4.0. It can be used in a variety of commercial, medical, automation, industrial, and military embedded applications.



MYD-C7Z015 Development Board

Hardware Specification

The Zynq™-7000 family of devices combines the software programmability of a Processor with the hardware programmability of an FPGA, resulting in unrivaled levels of system performance, flexibility, scalability while providing system benefits in terms of power reduction, lower cost with fast time to market. Unlike traditional SoC processing solutions, the flexible programmable logic of the Zynq-7000 devices enables optimization and differentiation, allowing designers to add peripherals and accelerators to adapt to a broad base of applications.

The Zynq-7000 AP SoC leverages the 28nm scalable optimized programmable logic used in Xilinx's 7 series FPGAs. Each device is designed to meet unique requirements across many use cases and applications. The Z-7010, Z-7015, and Z-7020 leverage the Artix®-7 FPGA programmable logic and offer lower power and lower cost for high-volume applications. The Z-7030, Z-7035, Z-7045, and Z-7100 are based on the Kintex®-7 FPGA programmable logic for higher-end applications that require higher performance and high I/O throughput.

	Z-7010	Z-7015	Z-7020	Z-7030	Z-7035	Z-7045	Z-7100
Processor Core	Dual ARM® Cortex™-A9 MPCore™ with CoreSight™						
Processor Extensions	NEON™ & Single / Double Precision Floating Point for each processor						
L1 Cache	32 KB Instruction, 32 KB Data per processor						
L2 Cache	512 KB						
On-Chip Memory	256 KB						
Memory Interfaces	DDR3, DDR3L, DDR2, LPDDR2, 2x Quad-SPI, NAND, NOR						
Peripherals	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO						
Logic Cells	28K Logic Cells	74K Logic Cells	85K Logic Cells	125K Logic Cells	275K Logic Cells	350K Logic Cells	444K Logic Cells
BlockRAM (Mb)	2.1	3.3	4.9	9.3	17.6	19.2	26.5
DSP Slices	80	160	220	400	900	900	2,020
Transceiver Count		4 (6.25 Gb/s)		up to 4 (12.5 Gb/s)	up to 16 (12.5 Gb/s)	up to 16 (12.5 Gb/s)	up to 16 (10.3125 Gb/s)

ZYNQ-7000 Devices

Zynq-7000 Devices

Mechanical Parameters

- Dimensions: 75mm x 55mm (12-layer PCB design)
- Power supply: 5V/0.5A
- Working temp.: -40~85 Celsius (industrial grade)

SoC

- Xilinx XC7Z015-2CLG485 (Zynq-7015)
  - 766MHz ARM® dual-core Cortex™-A9 MPCore processor (up to 866MHz)
  - Integrated Artix-7 class FPGA subsystem with 74K logic cells, 46,200 LUTs, 160 DSP slices
  - NEON™ & Single / Double Precision Floating Point for each processor
  - Supports a Variety of Static and Dynamic Memory Interfaces
  - Four high-speed SerDes transceivers up to 6.25Gbps
  - Four PCIe Gen2 hardened, integrated IP blocks

Memory

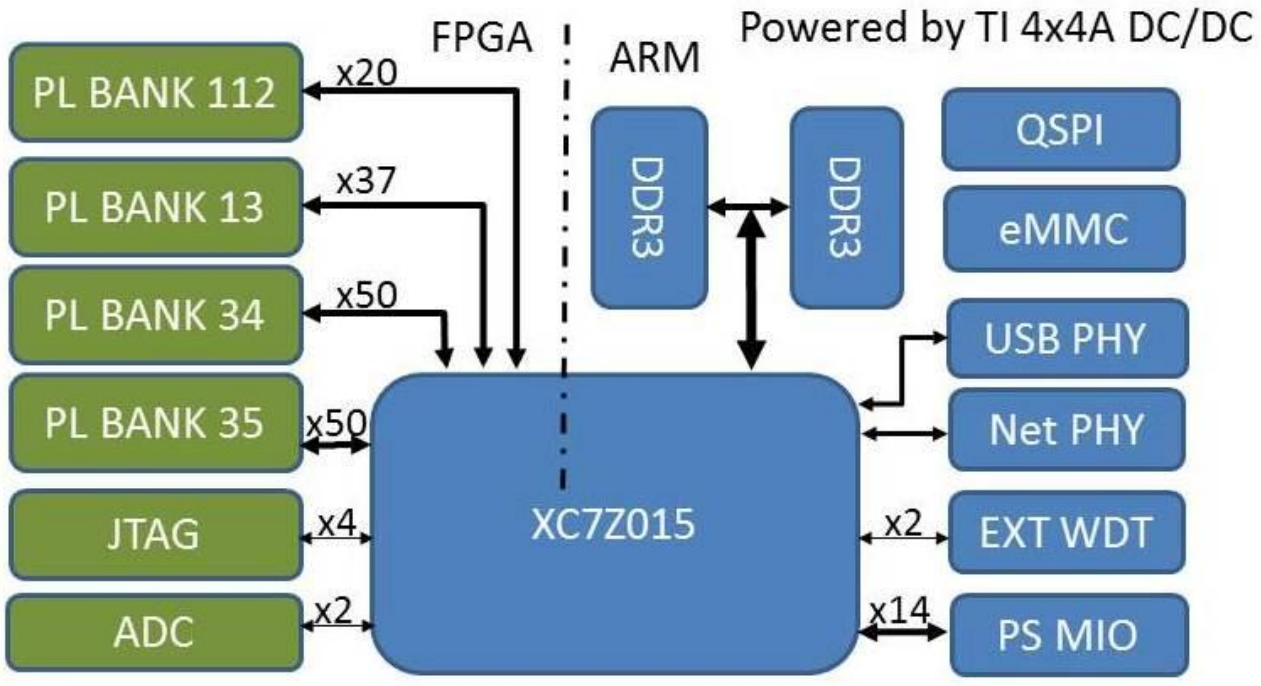
- 1GB DDR3 SDRAM (512MB*2）
- 4GB eMMC
- 32MB QSPI Flash (16MB is optional)

Peripherals and Signals Routed to Pins

- One 10/100/1000M Ethernet PHY with SGMII
- One USB 2.0 ULPI PHY
- External watchdog
- Three LEDs
  - One blue LED for power indicator
  - One red LED for FPGA program done indicator
  - One green user LED

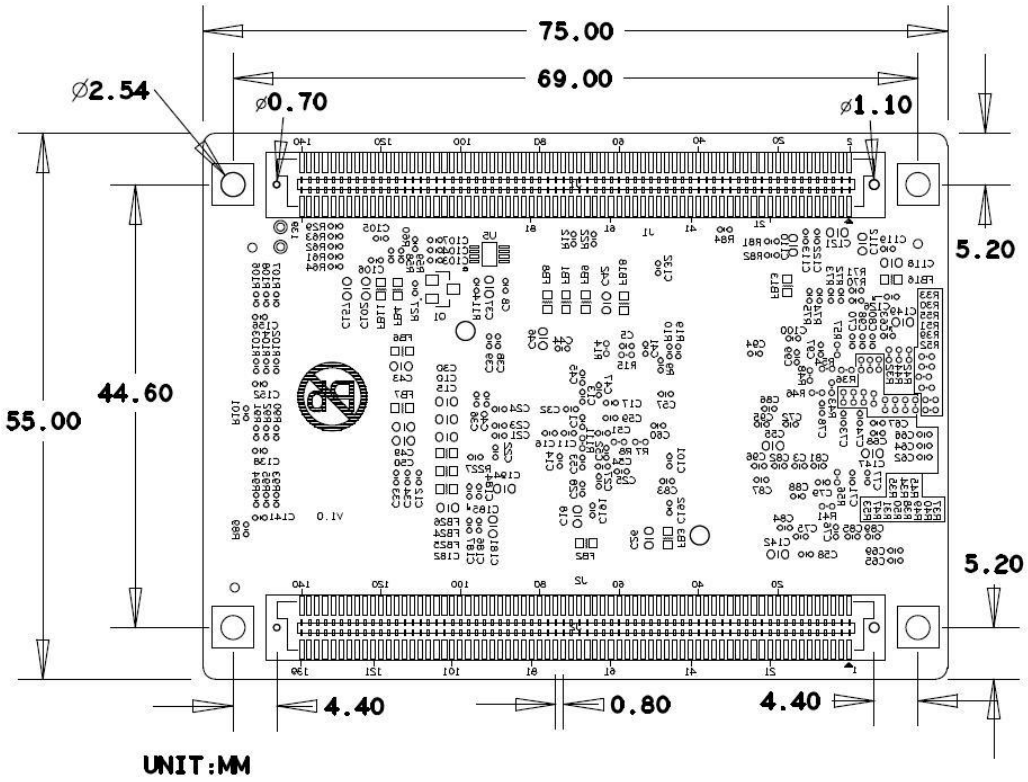
- Two 0.8mm pitch 140-pin board-to-board expansion connectors bring out below signals:
  - One Gigabit Ethernet (PS Ethernet 0)
  - One USB OTG 2.0 (PS USB 0)
  - Up to two Serial ports (reused from PS_MIO, can also be implemented through PL pins)
  - Up to two I2C (reused from PS_MIO, can also be implemented through PL pins)
  - Up to two CAN BUS (reused from PS_MIO, can also be implemented through PL pins)
  - One SPI (reused from PS_MIO, can also be implemented through PL pins)
  - ADC (one independent differential ADC, 16-channel ADC brought out through PL pins)
  - One SDIO (PS SDIO 0)
  - Bank 13 (PL I/O configurable as up to 18 LVDS pairs and 1 single-ended I/O or 37 single-ended I/O)
  - Bank 34 (PL I/O configurable as up to 24 LVDS pairs and 2 single-ended I/O or 50 single-ended I/O)
  - Bank 35 (PL I/O configurable as up to 24 LVDS pairs and 2 single-ended I/O or 50 single-ended I/O)
  - Bank 112 (4 GTP serial transceivers, 2 reference clock input)

Function Block Diagram



MYC-C7Z015 Function Block Diagram

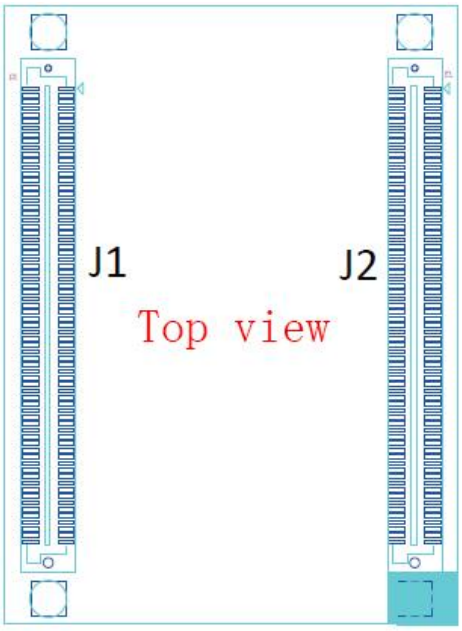
Dimension Chart



Dimensions of MYC-C7Z015

Expansion Connectors

The MYC-C7Z015 CPU Module is using two 0.8mm pitch 140-pin board-to-board female connectors for extension. Please refer to the file "MYC-C7Z015 Pin description Table" to know the signals routed to the connectors. You can download the file from MYIR's website: www.myirtech.com.



Expansion Connectors of MYC-C7Z015

Software Features

The MYC-C7Z015 CPU Module is capable of running Linux 5.4.0. MYIR provides software package in product disk along with the goods delivery. The software package features as below:

Item	Features	Description	Remark
Cross compiler	gcc 9.2.0	arm-xilinx-linux-gnueabi-gcc (GCC) 9.2.0	
Boot program	BOOT.BIN	First boot program including FSBL, bitstream	Source code provided
	u-boot	Secondary boot program	Source code provided
Linux Kernel	Linux 5.4.0	Customized kernel for MYC-C7Z015	Source code provided
Drivers	USB Host	USB Host driver	Source code provided
	PCI-E	PCIE driver	Source code provided
	SFP	SFP transceiver driver	Source code provided
	Ethernet	Gigabit Ethernet driver	Source code provided
	MMC/SD/TF	MMC/SD/TF card driver	Source code provided
	CAN	CAN driver	Source code provided
	LCD Controller	XYLON LCD driver	Source code provided
	HDMI	HDMI (SII902X chip) driver	Source code provided
	Button	Button driver	Source code provided
	UART	Serial port driver	Source code provided
	LED	LED driver	Source code provided
	GPIO	GPIO driver	Source code provided
	QSPI	QSPI Flash S25FL256S driver	Source code provided
	RTC	DS3231 RTC driver	Source code provided
	Resistive Touch	TSC2007 resistive touch screen driver	Source code provided
	Capacitive Touch	FT5X0X capacitive touch screen driver	Source code provided
	ADC	ADC driver	Source code provided
File System	Ramdisk	Ramdisk system image	
	RootFS	Build from buildroot tools, With Qt 5.11.3	
	Ubuntu Desktop 18.04	tar archive file and SD image	

Linux Software Package Features