MYiR 米尔电子
Make Your Idea Real

MYD-C7Z015 Development Board

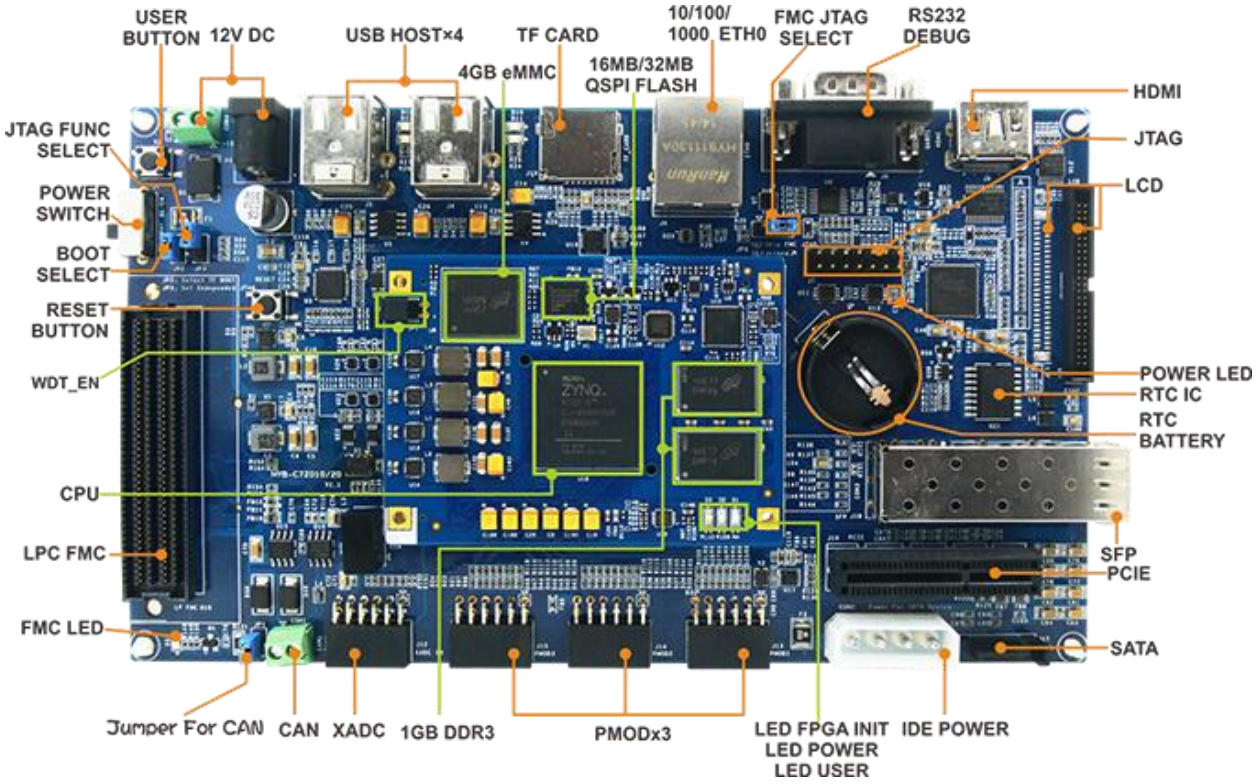
Overview

- ✓ *MYC-C7Z015 CPU Module as Controller Board*
- ✓ *Two 0.8mm pitch 140-pin Connectors for Board-to-Board Connections*
- ✓ *766MHz Xilinx XC7Z015 Dual-core ARM Cortex-A9 Processor with Xilinx 7-series FPGA logic*
- ✓ *1GB DDR3 SDRAM (2 x 512MB, 32-bit), 4GB eMMC, 32MB QSPI Flash*
- ✓ *Serial port, 4 x USB2.0 Host, Gigabit Ethernet, CAN, RTC, HDMI, LCD, TF*
- ✓ *1 x XADC, 3 x PMoD, 1 x FMC, 1 x SFP Transceiver Module, 1 x PCIe*
- ✓ *Optional 4.3- or 7-inch LCD/TSP*
- ✓ *Ready-to-Run Linux 5.4.0*

The **MYD-C7Z015 development board** is a programmable, low-cost and high-performance board designed by MYIR. It integrates Xilinx XC7Z015 (Z-7015) Dual-core **ARM Cortex-A9** Processor with Xilinx 7-series FPGA logic from **Xilinx Zynq-7000** family, with one PCIe interface and one SFP transceiver module interface on the base board to allow users to expand numerous of high-speed devices. Its typically applications range from Industrial Automation, Test & measurement, Medical Equipment, Aerospace to military and more others.

The MYD-C7Z015 development board is using the **MYC-C7Z015 CPU Module** as the core controller board which integrates the core components including the **Zynq-7015 processor, 1GB DDR3 SDRAM, 4GB eMMC, 32MB quad SPI Flash, a Gigabit Ethernet PHY, a USB PHY and external watchdog**. The MYC-C7Z015 CPU Module is mounted on to the MYD-C7Z015 base board through **two 0.8mm pitch 140-pin Board-to-Board connectors**. Compared with the Zynq-7010, the processor Zynq-7015, has more logic cells, Block RAM and DSP slices, which makes the board obtain more powerful programmable function for users.

The MYD-C7Z015 development board takes full features of the Zynq-7015 SoC to create a rich set of peripherals to the base board through headers and connectors including one RS232 serial port, four USB Host ports, one Gigabit Ethernet port, CAN, HDMI, LCD/Touch screen, TF card slot, RTC, one XADC header to allow you take advantage of Xilinx XADC and one low-pin count FMC connector to allow various FMC cards for custom I/O options. Especially, it has one SFP transceiver module to keep higher transmission speed and better stability during your evaluation, as well as one PCIe interface, which contributes the data transmission speed to a high frequency when customers using the board.



MYD-XC7Z015 Development Board

The MYD-C7Z015 development board is preloaded with Linux and delivered with necessary cable accessories. It is a high-performance and low-cost development platform for evaluation and prototype based on Xilinx Zynq-7000 All Programmable SoC family.

Hardware Specification

The Zynq™-7000 family of devices combines the software programmability of a Processor with the hardware programmability of an FPGA, resulting in unrivaled levels of system performance, flexibility, scalability while providing system benefits in terms of power reduction, lower cost with fast time to market. Unlike traditional SoC processing solutions, the flexible programmable logic of the Zynq-7000 devices enables optimization and differentiation, allowing designers to add peripherals and accelerators to adapt to a broad base of applications.

The Zynq-7000 AP SoC leverages the 28nm scalable optimized programmable logic used in Xilinx's 7 series FPGAs. Each device is designed to meet unique requirements across many use cases and applications. The Z-7010, Z-7015, and Z-7020 leverage the Artix®-7 FPGA programmable logic and offer lower power and lower cost for high-volume applications. The Z-7030, Z-7035, Z-7045, and Z-7100 are based on the Kintex®-7 FPGA programmable logic for higher-end applications that require higher performance and high I/O throughput.

	Z-7010	Z-7015	Z-7020	Z-7030	Z-7035	Z-7045	Z-7100
Processor Core	Dual ARM® Cortex™-A9 MPCore™ with CoreSight™						
Processor Extensions	NEON™ & Single / Double Precision Floating Point for each processor						
L1 Cache	32 KB Instruction, 32 KB Data per processor						
L2 Cache	512 KB						
On-Chip Memory	256 KB						
Memory Interfaces	DDR3, DDR3L, DDR2, LPDDR2, 2x Quad-SPI, NAND, NOR						
Peripherals	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO						
Logic Cells	28K Logic Cells	74K Logic Cells	85K Logic Cells	125K Logic Cells	275K Logic Cells	350K Logic Cells	444K Logic Cells
BlockRAM (Mb)	2.1	3.3	4.9	9.3	17.6	19.2	26.5
DSP Slices	80	160	220	400	900	900	2,020
Transceiver Count		4 (6.25 Gb/s)		up to 4 (12.5 Gb/s)	up to 16 (12.5 Gb/s)	up to 16 (12.5 Gb/s)	up to 16 (10.3125 Gb/s)

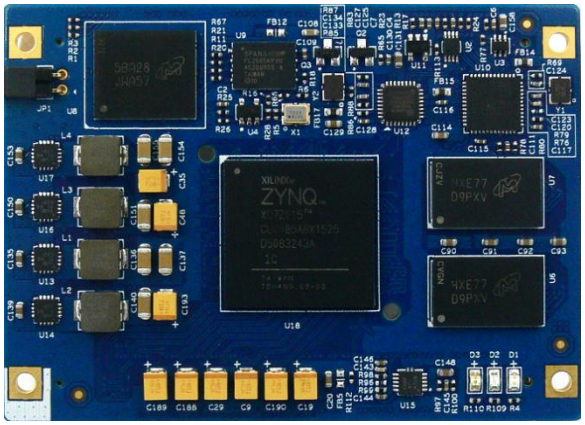
ZYNQ-7000 Devices

Zynq-7000 Devices

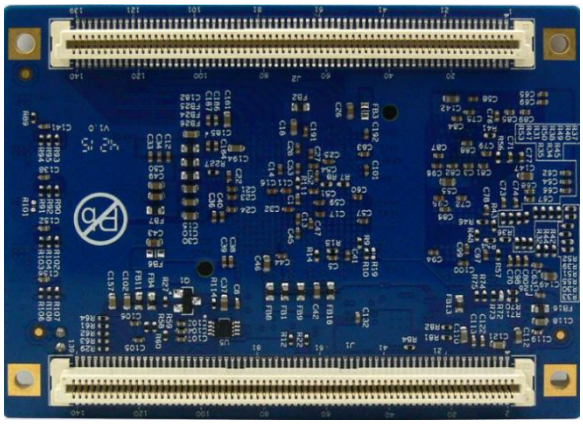
Mechanical Parameters

- Dimensions: 190mm x 110mm (base board), 75mm x 55mm (CPU Module)
- PCB layers: 4-layer design (base board), 12-layer design (CPU Module)
- Power supply: 12V/0.5A (base board), 5V/0.5A (CPU Module)
- Working temp.: -40~85 Celsius (industrial grade)

The MYD-C7Z015 Controller Board (MYC-C7Z015 CPU Module)



MYC-C7Z015 CPU Module Top-view



MYC-C7Z015 CPU Module Bottom-view

SoC

- Xilinx XC7Z015-2CLG485 (Zynq-7015)
  - 766MHz ARM® dual-core Cortex™-A9 MPCore processor (up to 866MHz)
  - Integrated Artix-7 class FPGA subsystem with 74K logic cells, 46,200 LUTs, 160 DSP slices
  - NEON™ & Single / Double Precision Floating Point for each processor
  - Supports a Variety of Static and Dynamic Memory Interfaces
  - Four high-speed SerDes transceivers up to 6.25Gbps
  - Four PCIe Gen2 hardened, integrated IP blocks

Memory

- 1GB DDR3 SDRAM (512MB*2）
- 4GB eMMC
- 32MB QSPI Flash (16MB is optional)

Peripherals and Signals Routed to Pins

- One10/100/1000M Ethernet PHY
- One USB PHY
- External watchdog
- Three LEDs
  - One blue LED for power indicator
  - One red LED for FPGA program done indicator
  - One green user LED
- Two 0.8mm pitch 140-pin board-to-board expansion connectors bring out below signals:
  - One Gigabit Ethernet (PS Ethernet 0)
  - One USB OTG 2.0 (PS USB 0)
  - Up to two Serial ports (reused from PS_MIO, can also be implemented through PL pins)
  - Up to two I2C (reused from PS_MIO, can also be implemented through PL pins)
  - Up to two CAN BUS (reused from PS_MIO, can also be implemented through PL pins)
  - One SPI (reused from PS_MIO, can also be implemented through PL pins)
  - ADC (one independent differential ADC, 16-channel ADC brought out through PL pins)
  - One SDIO (PS SDIO 0)
  - Bank 13 (PL I/O configurable as up to 18 LVDS pairs and 1 single-ended I/O or 37 single-ended I/O)
  - Bank 34 (PL I/O configurable as up to 24 LVDS pairs and 2 single-ended I/O or 50 single-ended I/O)
  - Bank 35 (PL I/O configurable as up to 24 LVDS pairs and 2 single-ended I/O or 50 single-ended I/O)
  - Bank 112 (4 GTP serial transceivers, 2 reference clock input)

The MYD-C7Z015 Base Board (MYB-C7Z015)

MYD-C7Z015 Base Board for MYC-C7Z015 CPU Module

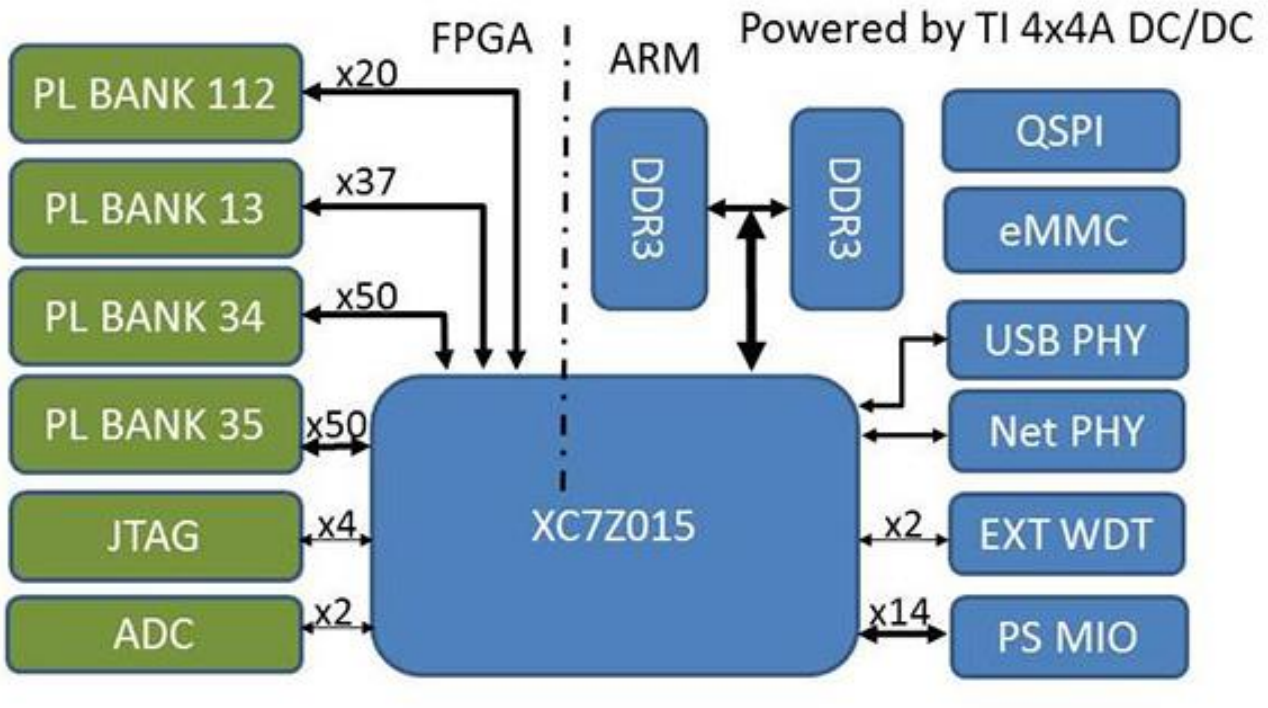
PS Unit

- Four USB 2.0 Host ports (through USB Hub)
- One RS232 (DB9 port)
- One TF card slot (bootable)
- One CAN interface
- One 10/100/1000M Ethernet
- One 2.54mm pitch 14-pin JTAG interface (PS, PL reused)
- Battery backed RTC
- One User Button (One I2C, can be connected to LCD and Resistive Touch Screen)
- Jumpers
  - One for booting selection from TF card or QSPI
  - One for JTAG selection for using PS and PL reused or independent JTAG configured through PL pins
  - One for selection if adding FMC module to JTAG

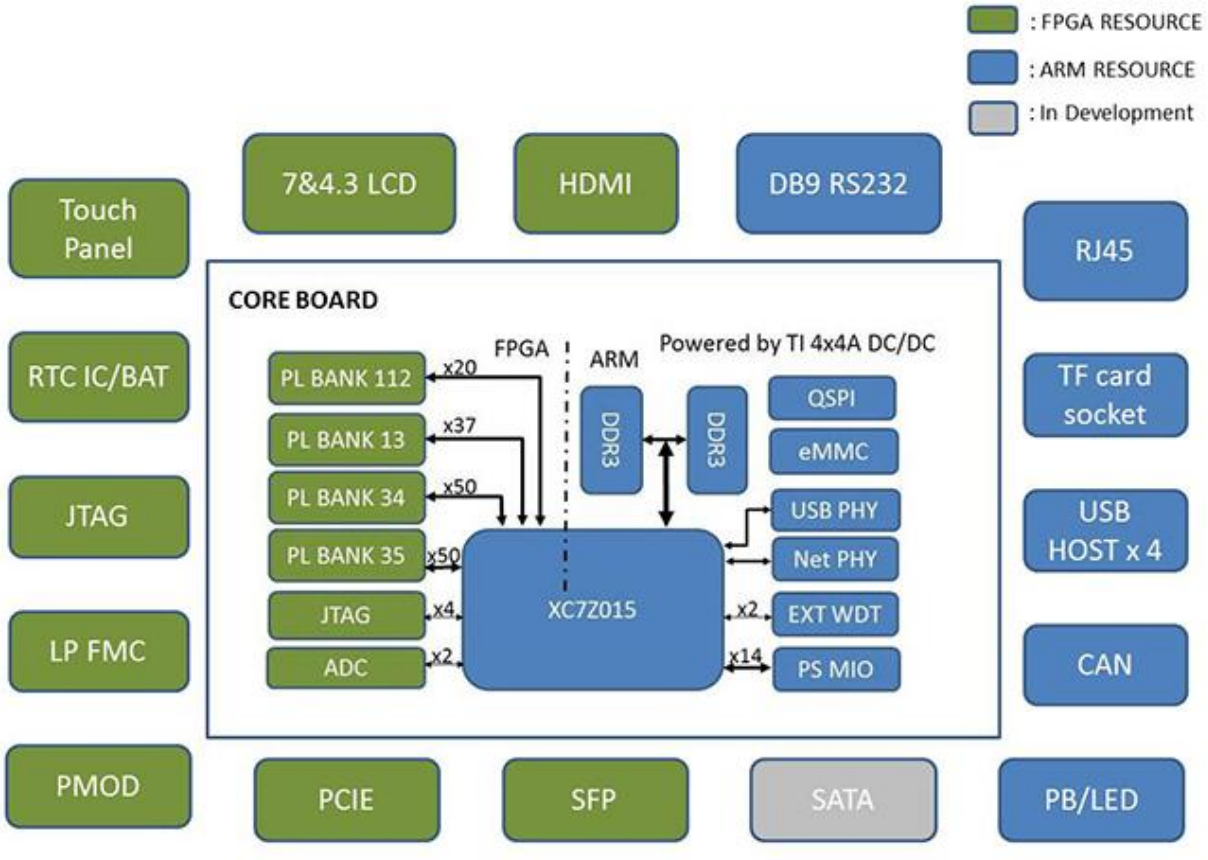
PL Unit

- One XADC interface
- One Xilinx standard LPFMC interface
- One HDMI interface (16-bit YCrCb, support 1080p display, do not support audio)
- LCD/Touch screen interface (16-bit RGB, signals reused with HDMI, supports resistive and capacitive touch screen)
- Two LEDS (one for FMC module detection, one for power indicator)
- Three-channel PMoD
- One SFP transceiver module with RJ45 interface (SFP-GE-T module, up to 1000Mbps)
- One PCIe interface

Function Block Diagram

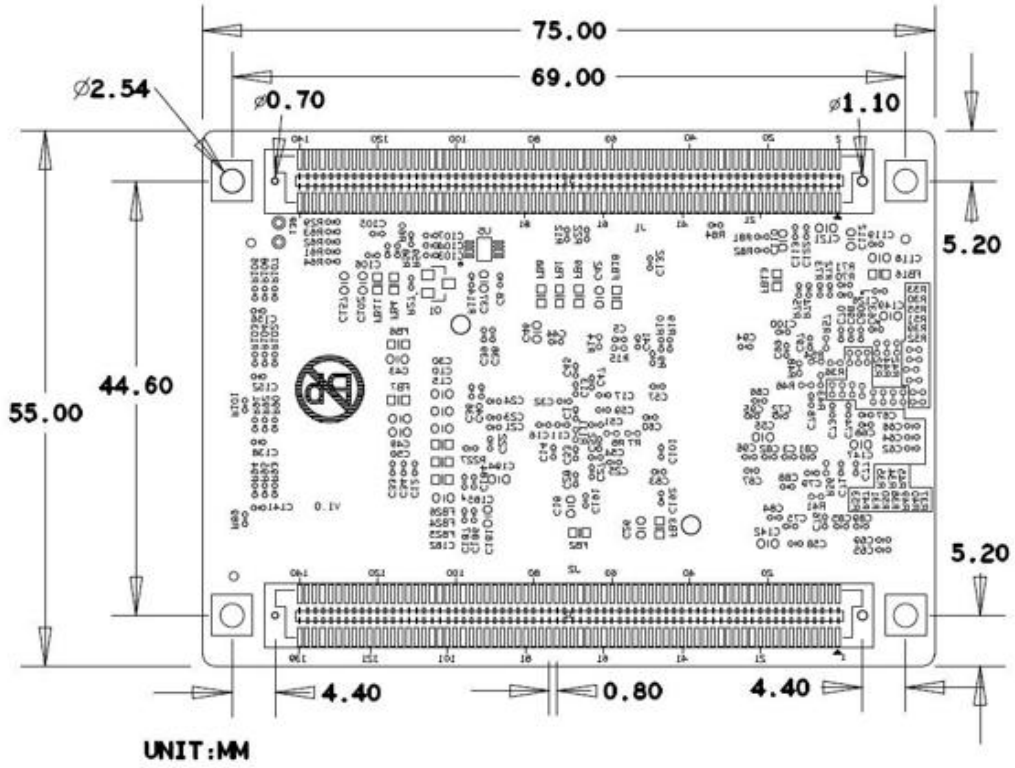


MYC-C7Z015 CPU Module Function Block Diagram

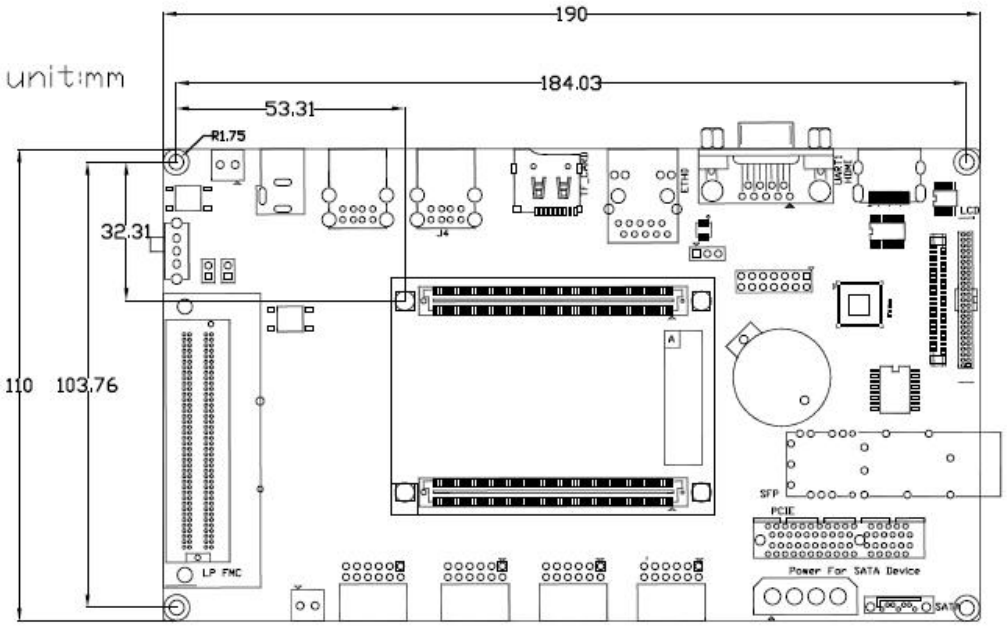


MYD-C7Z015 Development Board Function Block Diagram

Dimension Chart



Dimensions of MYC-C7Z015 CPU Module



Dimensions of MYD-C7Z015 Development Board

Software Features

The MYC-C7Z015 CPU Module is capable of running Linux 5.4.0. MYIR provides software package in product disk along with the goods delivery. The software package features as below:

Item	Features	Description	Remark
Cross compiler	gcc 9.2.0	arm-xilinx-linux-gnueabi-gcc (GCC) 9.2.0	
Boot program	BOOT.BIN	First boot program including FSBL, bitstream	Source code provided
	u-boot	Secondary boot program	Source code provided
Linux Kernel	Linux 5.4.0	Customized kernel for MYD-C7Z015	Source code provided
Drivers	USB Host	USB Host driver	Source code provided
	PCI-E	PCI-E driver	Source code provided
	SFP	SFP transceiver driver	Source code provided
	Ethernet	Gigabit Ethernet driver	Source code provided
	MMC/SD/TF	MMC/SD/TF card driver	Source code provided
	CAN	CAN driver	Source code provided
	LCD Controller	XYLON LCD driver	Source code provided
	HDMI	HDMI (SII902X chip) driver	Source code provided
	Button	Button driver	Source code provided
	UART	UART driver	Source code provided
	LED	LED driver	Source code provided
	GPIO	GPIO driver	Source code provided
	QSPI	QSPI Flash S25FL256S driver	Source code provided
	RTC	DS3231 RTC driver	Source code provided
	Resistive Touch	TSC2007 resistive touch screen driver	Source code provided
	Capacitive Touch	FT5X0X capacitive touch screen driver	Source code provided
	ADC	ADC driver	Source code provided
File System	Ramdisk	Ramdisk system image	
	RootFS	Build from buildroot tools, With Qt 5.11.3	
	Ubuntu Desktop 18.04	tar archive file and SD image	

Linux Software Package Features