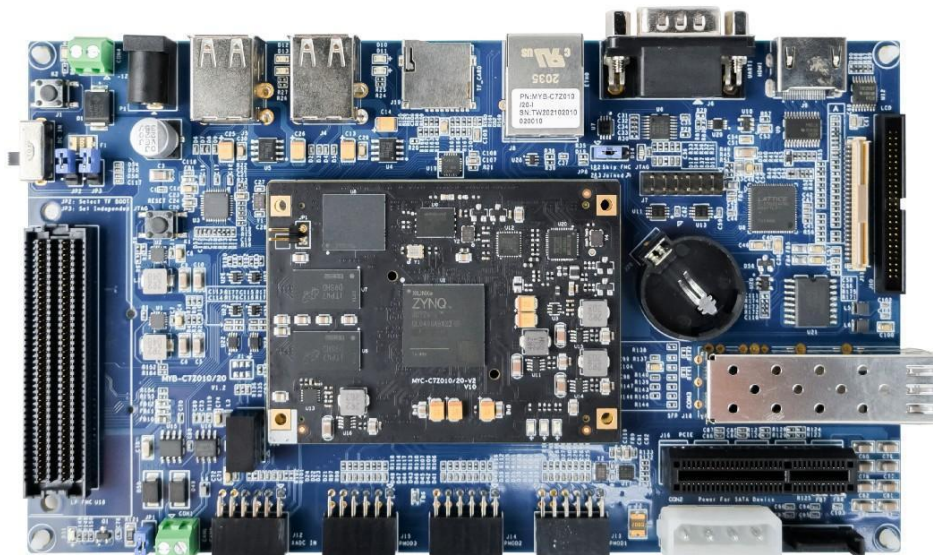




MYD-C7Z010/20-V2 Development Board Overview



- ✓ MYC-C7Z010/20-V2 CPU Module as Controller Board
- ✓ Two 0.8mm pitch 140-pin Connectors for Board-to-Board Connections
- ✓ Xilinx XC7Z010/20 Dual-core ARM Cortex-A9 Processor with Xilinx 7-series FPGA logic
- ✓ 1GB DDR3 SDRAM (2 x 512MB, 32-bit), 4GB eMMC, 32MB QSPI Flash
- ✓ Serial port, 4 x USB2.0 Host, Gigabit Ethernet, CAN, RTC, HDMI, LCD, TF
- ✓ 1 x XADC, 3 x PMoD, 1 x FMC
- ✓ Optional 4.3- or 7-inch LCD/TSP
- ✓ Ready-to-Run Linux 5.4.0

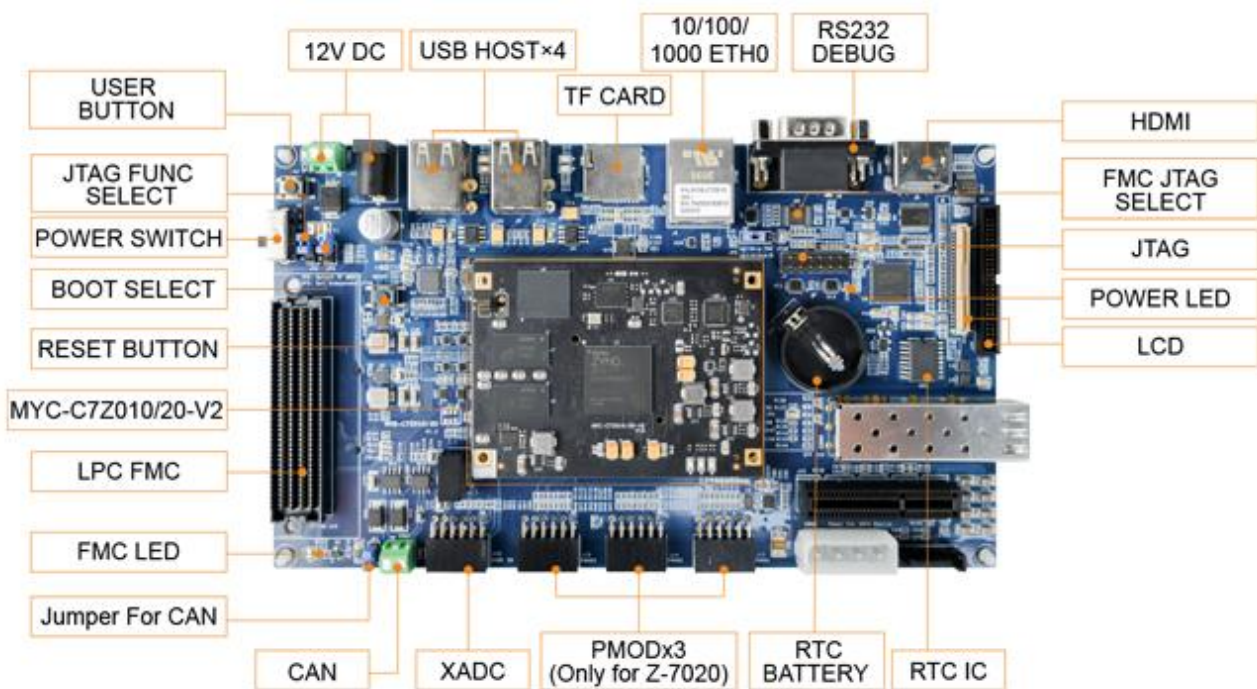


The **MYD-C7Z010/20-V2 development board** is built around the **MYC-C7Z010/20-V2 CPU Module** which is a compact Linux-ready ZYNQ-based SOM (System on Module). The MYC-C7Z010/20-V2 combines the Xilinx XC7Z010-1CLG400 or XC7Z020-2CLG400 SoC device, 1GB DDR3 SDRAM, 4GB eMMC, 32MB quad SPI Flash, a Gigabit Ethernet PHY, a USB PHY and external watchdog. It is connected to the MYD-C7Z010/20-V2 base board through two 0.8mm pitch 140-pin board-to-board connectors.

The **MYD-C7Z010/20-V2 development board** takes full features of the Zynq-7010 and Zynq-7020 SoCs ' powerful dual-core ARM Cortex-A9 processing system and Xilinx 7-series Field Programmable Gate Array (FPGA) logic unit to create a rich set of peripherals to the base board through headers and connectors including one RS232 serial port, four USB Host ports, one Gigabit Ethernet port, CAN, HDMI, LCD/Touch screen, TF card slot, RTC, one XADC header to allow you take advantage of Xilinx XADC; it has three PMoD headers to meet your I/O needs with PMoDs (only for 7020); it also has a low-pin count FMC connector to allow various FMC cards for custom I/O options. User can integrate a MYC-C7Z010-V2 or a MYC-C7Z020-V2 SOM on the same base board, thus making two variants of Zynq evaluation boards.

- *MYD-C7Z010-V2 Development Board* - with MYC-C7Z010-V2 CPU Module for Xilinx XC7Z010-1CLG400
- *MYD-C7Z020-V2 Development Board* - with MYC-C7Z020-V2 CPU Module for Xilinx XC7Z020-2CLG400

The **MYD-C7Z010/20-V2 development board** is delivered with necessary cable accessories and MYIR offers optional 4.3-inch and 7-inch LCD. The board is preloaded with Linux. It is a high-performance and low-cost development platform for evaluation and prototype based on Xilinx Zynq-7000 All Programmable SoC family.



MYD-C7Z010/20-V2 Development Board



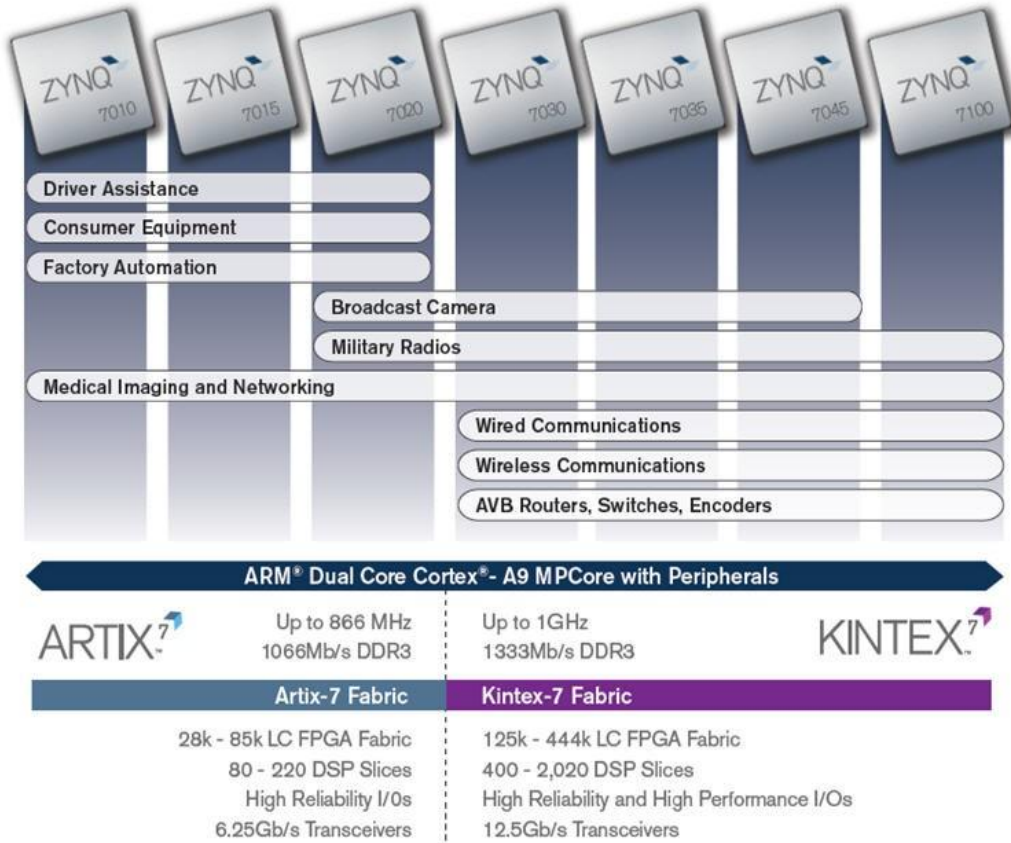
Hardware Specification

The Zynq™-7000 family of devices combines the software programmability of a Processor with the hardware programmability of an FPGA, resulting in unrivaled levels of system performance, flexibility, scalability while providing system benefits in terms of power reduction, lower cost with fast time to market. Unlike traditional SoC processing solutions, the flexible programmable logic of the Zynq-7000 devices enables optimization and differentiation, allowing designers to add peripherals and accelerators to adapt to a broad base of applications.

The Zynq-7000 AP SoC leverages the 28nm scalable optimized programmable logic used in Xilinx' s 7 series FPGAs. Each device is designed to meet unique requirements across many use cases and applications. The Z-7010, Z-7015, and Z-7020 leverage the Artix®-7 FPGA programmable logic and offer lower power and lower cost for high-volume applications. The Z-7030, Z-7035, Z-7045, and Z-7100 are based on the Kintex®-7 FPGA programmable logic for higher-end applications that require higher performance and high I/O throughput.

| | Z-7010 | Z-7015 | Z-7020 | Z-7030 | Z-7035 | Z-7045 | Z-7100 |
|----------------------|---------------------------------------------------------------------|-----------------|-----------------|---------------------|----------------------|----------------------|-------------------------|
| Processor Core | Dual ARM® Cortex™-A9 MPCore™ with CoreSight™ | | | | | | |
| Processor Extensions | NEON™ & Single / Double Precision Floating Point for each processor | | | | | | |
| L1 Cache | 32 KB Instruction, 32 KB Data per processor | | | | | | |
| L2 Cache | 512 KB | | | | | | |
| On-Chip Memory | 256 KB | | | | | | |
| Memory Interfaces | DDR3, DDR3L, DDR2, LPDDR2, 2x Quad-SPI, NAND, NOR | | | | | | |
| Peripherals | 2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO | | | | | | |
| Logic Cells | 28K Logic Cells | 74K Logic Cells | 85K Logic Cells | 125K Logic Cells | 275K Logic Cells | 350K Logic Cells | 444K Logic Cells |
| BlockRAM (Mb) | 240 KB | 380 KB | 560 KB | 1,060 KB | 2,000 KB | 2,180 KB | 3,020 KB |
| DSP Slices | 80 | 160 | 220 | 400 | 900 | 900 | 2,020 |
| Transceiver Count | | 4 (6.25 Gb/s) | | up to 4 (12.5 Gb/s) | up to 16 (12.5 Gb/s) | up to 16 (12.5 Gb/s) | up to 16 (10.3125 Gb/s) |

ZYNQ-7000 Devices



Zynq-7000 Devices

Mechanical Parameters

- Dimensions: 190mm x 110mm (base board), 75mm x 55mm (CPU Module)
- PCB layers: 4-layer design (base board), 10-layer design (CPU Module)
- Power supply: 12V/0.5A (base board), 5V/0.5A (CPU Module)
- Working temp.: 0~70 Celsius (commercial grade) or -40~85 Celsius (industrial grade)

The MYD-C7Z010/20-V2 Controller Board ([MYC-C7Z010/20-V2 CPU Module](#))



MYC-C7Z010/20-V2 Top-view



MYC-C7Z010/20-V2 CPU Bottom-view



SoC

- Xilinx XC7Z010-1CLG400C (Zynq-7010) or XC7Z020-1CLG400C (Zynq-7020)
 - 667MHz ARM® dual-core Cortex™-A9 MPCore processor (up to 866MHz)
 - Integrated Artix-7 class FPGA subsystem
 - with 28K logic cells, 17,600 LUTs, 80 DSP slices (for XC7Z010)
 - with 85K logic cells, 53,200 LUTs, 220 DSP slices (for XC7Z020)
 - NEON™ & Single / Double Precision Floating Point for each processor
 - Supports a Variety of Static and Dynamic Memory Interfaces

Memory

- 1GB DDR3 SDRAM (512MB*2)
- 4GB eMMC
- 32MB QSPI Flash (16MB is optional)

Peripherals and Signals Routed to Pins

- 10/100/1000M Ethernet PHY (YT8531SH)
- External watchdog
- Three LEDs
 - One blue LED for power indicator
 - One red LED for FPGA program done indicator
 - One green user LED
- Two 0.8mm pitch 140-pin board-to-board expansion connectors bring out below signals:
 - One Gigabit Ethernet
 - One USB OTG 2.0
 - Two Serial ports
 - Two I2C
 - Two CAN BUS
 - * Serial ports, I2C and CAN signals will be reused in PS part, or implemented through PL pins
 - Two SPI (can be implemented through PL pins)
 - ADC (one independent differential ADC, 16-channel ADC brought out through PL pins)
 - One SDIO

The MYD-C7Z010/20-V2 Base Board (MYB-C7Z010/20)



MYD-C7Z010/20-V2 Base Board for MYC-C7Z010/20-V2 CPU Module

**PS Unit**

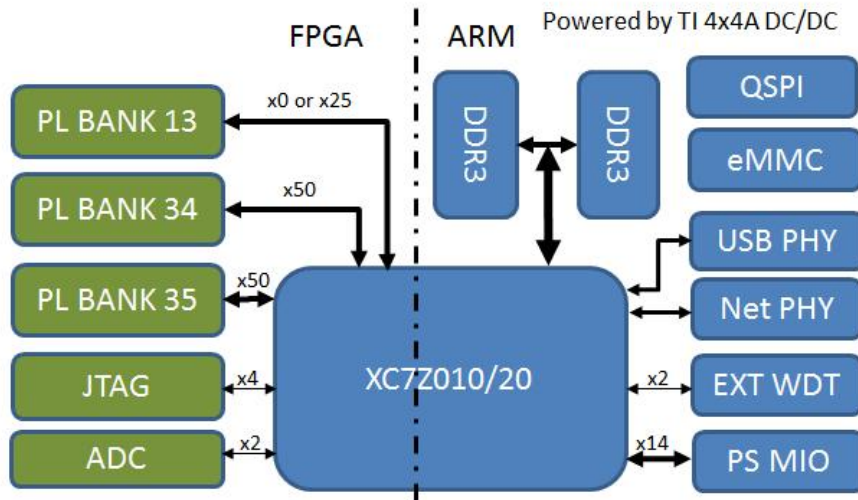
- Four USB 2.0 Host ports (through USB Hub)
- One RS232 (DB9 port)
- One TF card slot (bootable)
- One CAN interface
- One 10/100/1000M Ethernet
- One 2.54mm pitch 14-pin JTAG interface (PS, PL reused)
- Battery backed RTC
- One User Button (One I2C, can be connected to LCD and Resistive Touch Screen)
- Jumpers
 - One for booting selection from TF card or QSPI
 - One for JTAG selection for using PS and PL reused or independent JTAG configured through PL pins
 - One for selection if adding FMC module to JTAG

PL Unit

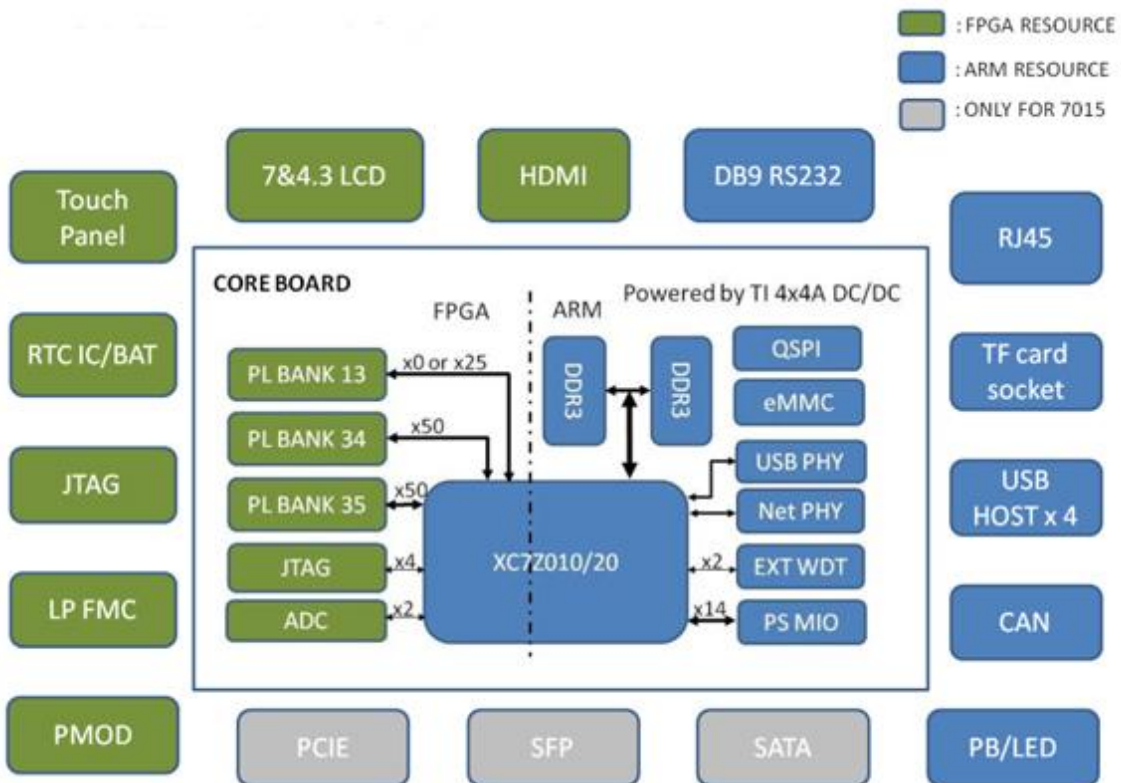
- One XADC interface
- One Xilinx standard LPFMC interface
- One HDMI interface (16-bit YCrCb, support 1080p display, do not support audio)
- LCD/Touch screen interface (16-bit RGB, signals reused with HDMI, supports resistive and capacitive touch screen)
- Two LEDS (one for FMC module detection, one for power indicator)
- Three-channel PMoD (only for XC7Z020)



Function Block Diagram



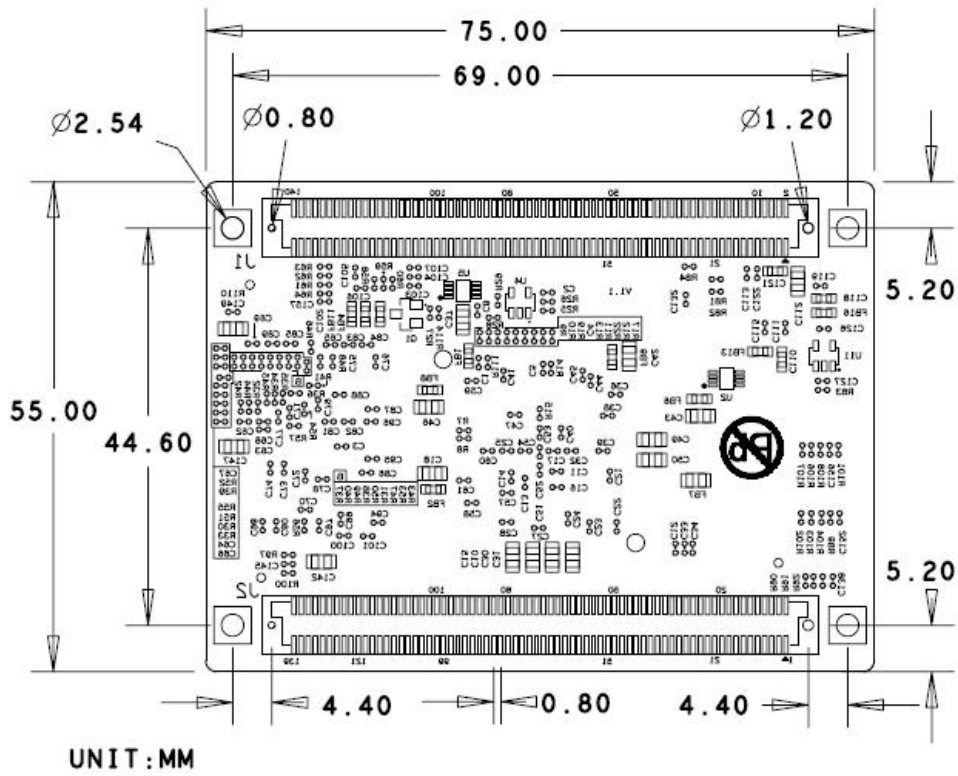
MYC-C7Z010/20-V2 CPU Module Function Block Diagram



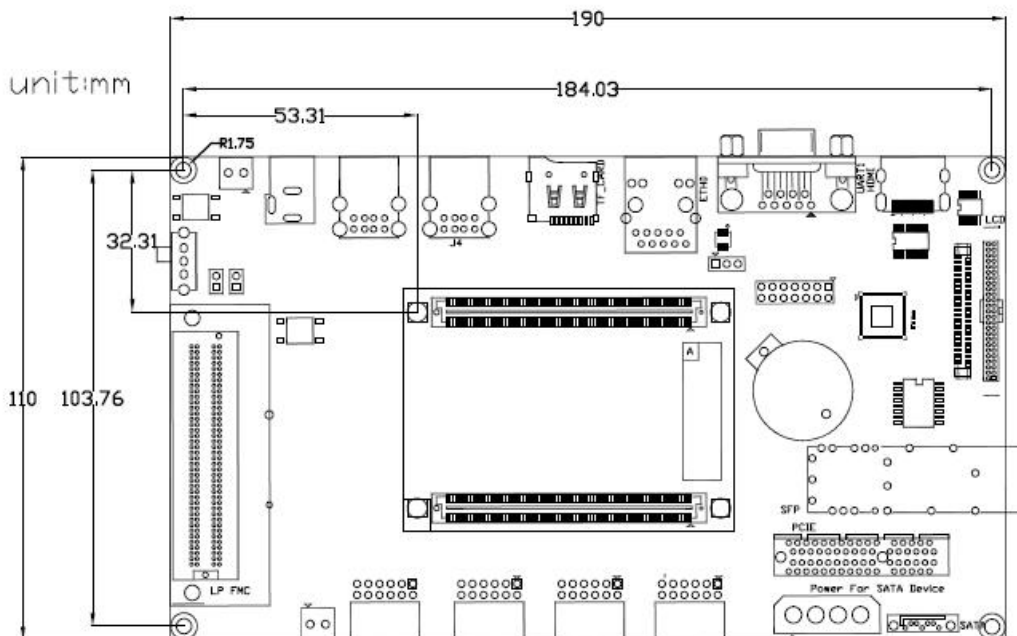
MYD-C7Z010/20-V2 Development Board Function Block Diagram



Dimension Chart



Dimensions of MYC-C7Z010/20-V2 CPU Module



Dimensions of MYD-C7Z010/20-V2 Development Board



Software Features

The MYC-C7Z010/20-V2 CPU Module is capable of running Linux 5.4.0. MYIR provides software package in product disk along with the goods delivery. The software package features as below:

| Item | Features | Description | Remark |
|----------------|------------------|----------------------------------------------|----------------------|
| Cross compiler | gcc 9.2.0 | arm-xilinx-linux-gnueabi-gcc (GCC) 9.2.0 | |
| Boot program | BOOT.BIN | First boot program including FSBL, bitstream | Source code provided |
| | u-boot | Secondary boot program | Source code provided |
| Linux Kernel | Linux 5.4.0 | Customized kernel for MYD-C7Z010/20-V2 | Source code provided |
| Drivers | USB Host | USB Host driver | Source code provided |
| | Ethernet | Gigabit Ethernet driver | Source code provided |
| | MMC/SD/TF | MMC/SD/TF card driver | Source code provided |
| | CAN | CAN driver | Source code provided |
| | LCD Controller | XYLON LCD driver | Source code provided |
| | HDMI | HDMI (SII902X chip) driver | Source code provided |
| | Button | Button driver | Source code provided |
| | UART | UART driver | Source code provided |
| | LED | LED driver | Source code provided |
| | GPIO | GPIO driver | Source code provided |
| | QSPI | QSPI Flash S25FL256S driver | Source code provided |
| | RTC | DS3231 RTC driver | Source code provided |
| | Resistive Touch | TSC2007 resistive touch screen driver | Source code provided |
| | Capacitive Touch | FT5X0X capacitive touch screen driver | Source code provided |
| ADC | ADC driver | Source code provided | |
| File System | Ramdisk | Ramdisk system image | |
| | Rootfs.tar | Tar file | |

Linux Software Package Features