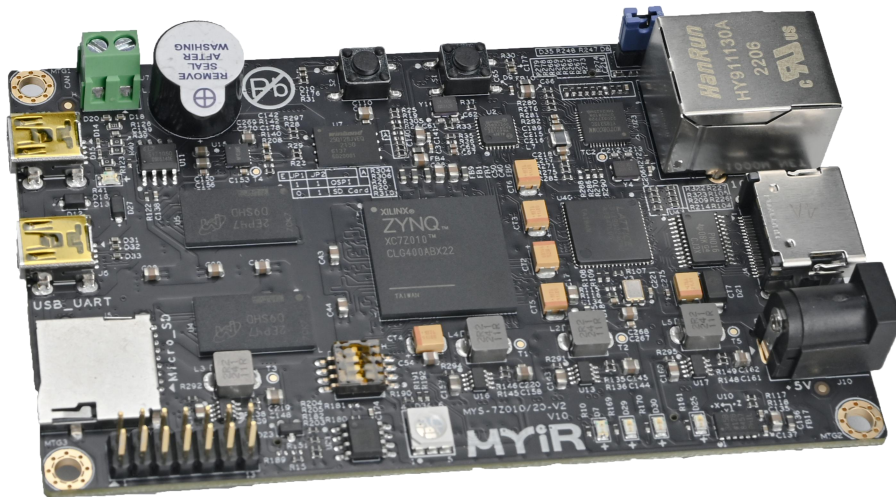




Z-turn Board V2 Overview



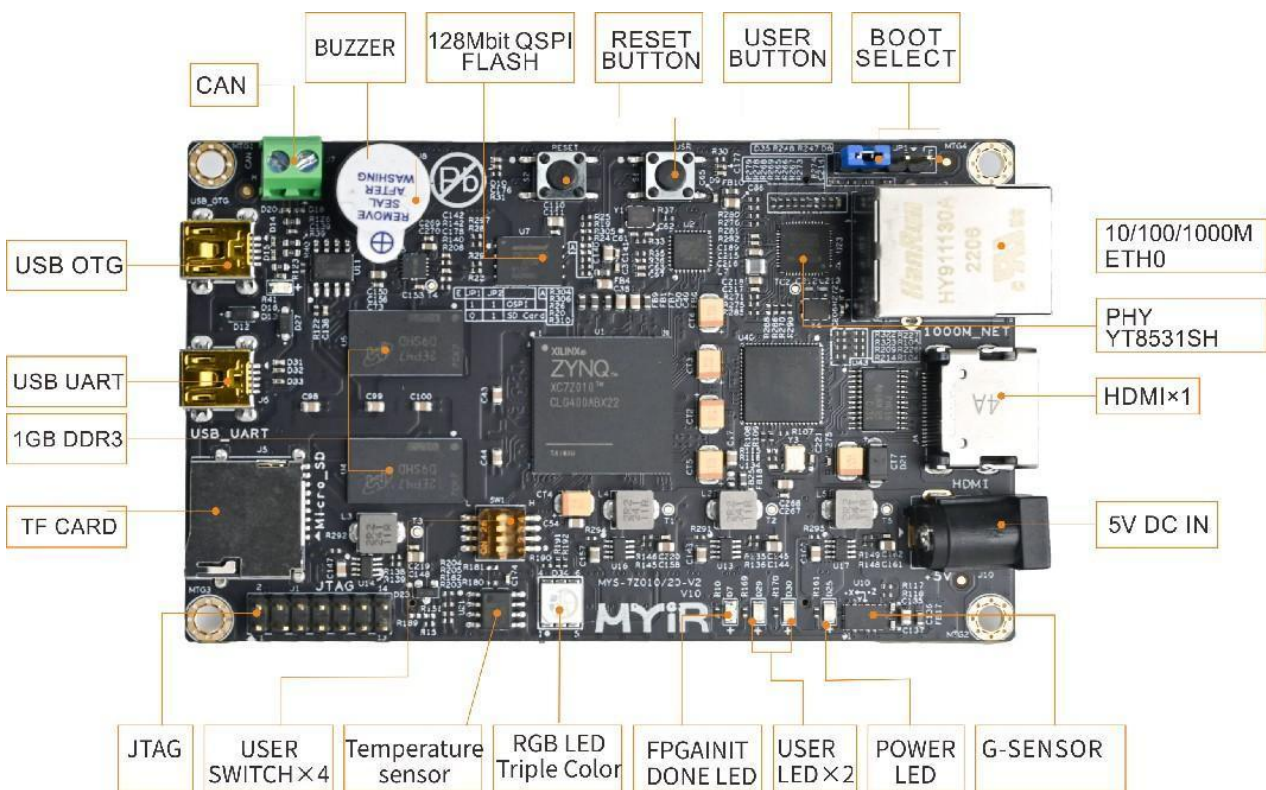
- ✓ 667MHz Xilinx XC7Z010/020 Dual-core ARM Cortex-A9 Processor with Xilinx 7-series FPGA logic
- ✓ 1GB DDR3 SDRAM (2 x 512MB, 32-bit), 16MB QSPI Flash, 64Kbit EEPROM
- ✓ USB_UART, USB2.0 OTG, 1 x 10/100/1000Mbps Ethernet, CAN, HDMI, TF, ...
- ✓ Onboard Three-axis Acceleration Sensor and Temperature Sensor
- ✓ Supports Optional Camera Module and Z-turn IO Cape
- ✓ Ready-to-Run Linux Single Board Computer
- ✓ Supports Python Development



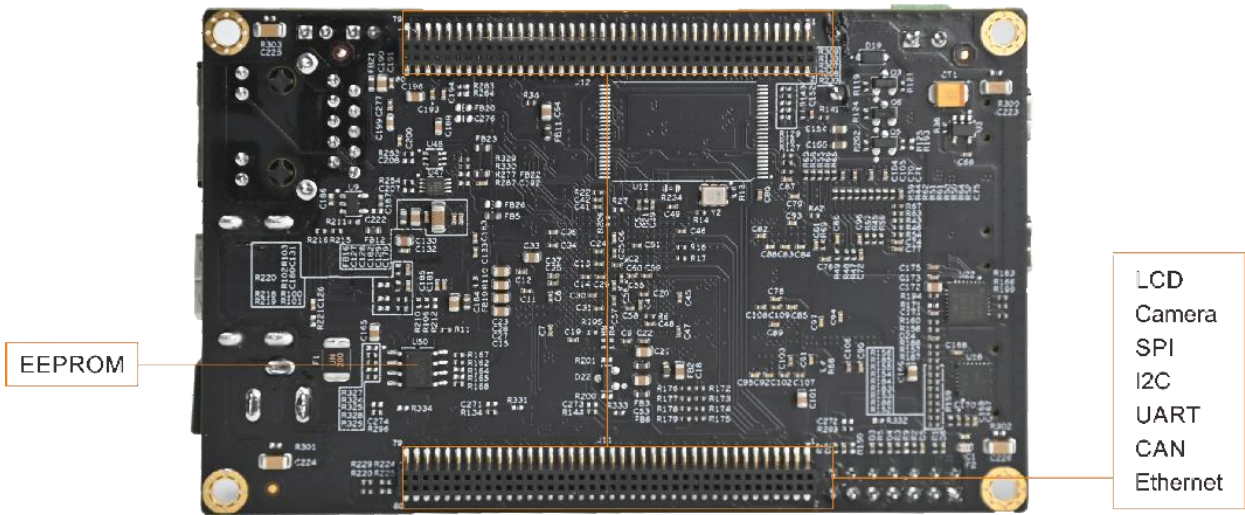
The [Z-turn Board V2](#) is a cost-optimized version for MYIR's popular [Z-turn Board](#). It is a high-performance Single Board Computer (SBC) built around the Xilinx Zynq-7010 (XC7Z010) or Zynq-7020 (XC7Z020) All Programmable System-on-Chip (SoC) which is among the Xilinx Zynq-7000 family, featuring integrated dual-core ARM Cortex-A9 processor with Xilinx 7-series Field Programmable Gate Array (FPGA) logic. Compared with the former version, the main differences are the IC parts as below:

IC on board	Z-turn Board	Z-turn Board V2
Gigabit Ethernet PHY	KSZ9031RXN	YT8531SH
Power IC	TLV62130RGTR	MP2143DJ-LF-Z
EEPROM	/	BL24C64A-PARC
DDR3	MT41K256M16HA-125:E	NT5CC256M16ER-EK

The [Z-turn Board V2](#) takes full features of the Zynq-7010 or 7020 SoC, it has 1GB DDR3, 16MB QSPI Flash and 64Kbit EEPROM on board and a set of rich peripherals including USB-to-UART, Mini USB OTG, 10/100/1000Mbps Ethernet, CAN, HDMI, TF, JTAG, Buzzer, G-sensor and Temperature sensor. On the rear of the board, there are two 1.27mm pitch 80-pin SMT female connectors to allow the availability of 96 (for 7010) or 106 (for 7020) user I/O and configurable as up to 39 LVDS pairs I/O.

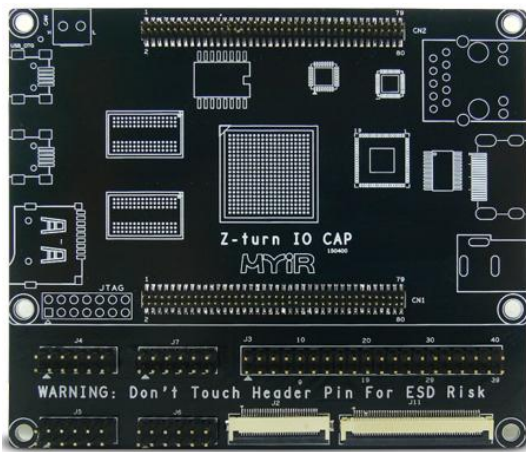


Z-turn Board V2 (Top-view)

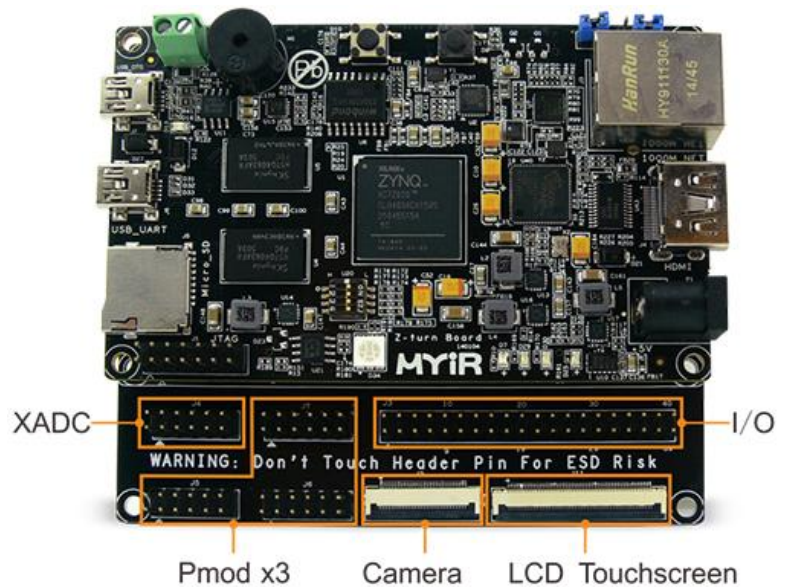


Z-turn Board V2 (Bottom-view)

The [Z-turn Board V2](#) is capable of running Linux operating system. MYIR has provided Linux 4.14.0 SDK, the kernel and many drivers are in source code. MYIR also provides a MYIR-PYNQ project to support Python development on the [Z-turn Board V2](#). The board is delivered with complete accessory kit including two USB cables, one Ethernet cable, one HDMI cable, one 16GB TF card and one 5V power adapter which enables you to start the development quickly when getting the board out-of-the-box. MYIR also offers optional USB camera module and an IO extension board [Z-turn IO Cape](#), which brings out many peripherals and signals like ADC, GPIO, LCD and camera interfaces to help you explore more functions from the Z-turn Board V2.



Z-turn IO Cape



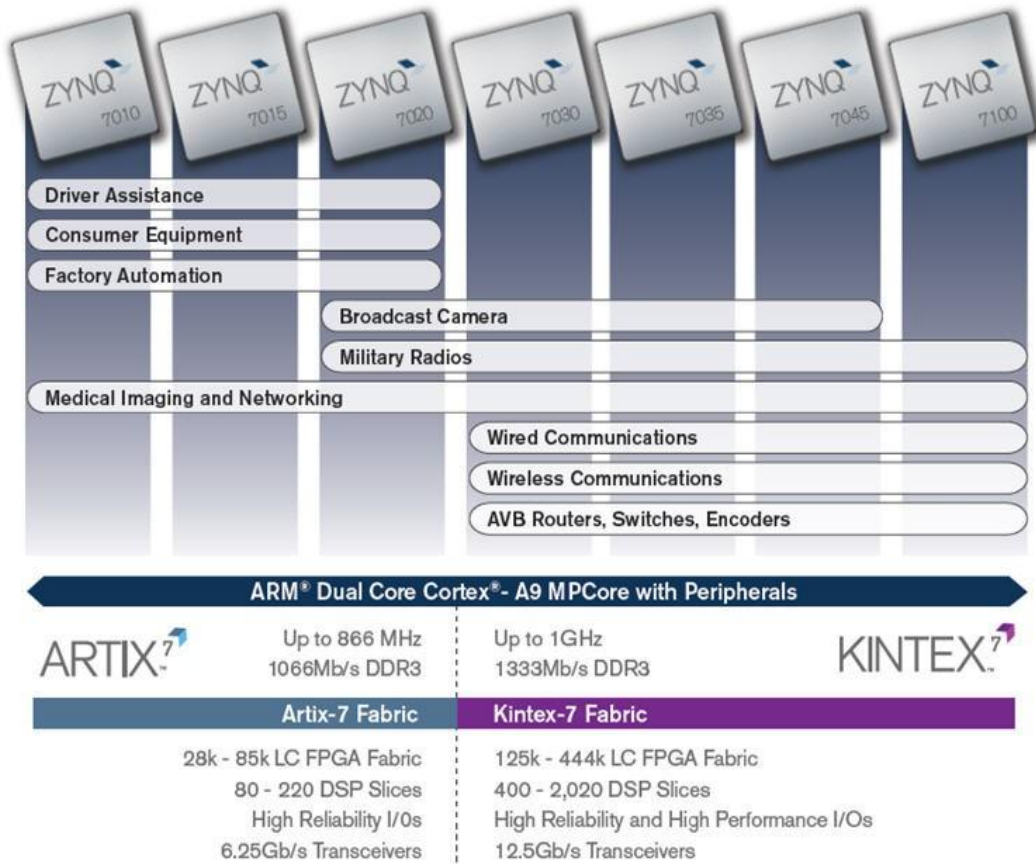
Z-turn Board V2 Mounted on Z-turn IO Cape

The [Z-turn Board V2](#) is an excellent development platform for evaluating and prototyping for Zynq-7000 SoC. It can also be used as a System-on-Module (SOM) for your next embedded design; typical applications are Industrial Automation, Test & measurement, Medical Equipment, Intelligent Video Surveillance, Aerospace and military, etc.



Hardware Specification

The Zynq-7000 AP SoC leverages the 28nm scalable optimized programmable logic used in Xilinx’s 7 series FPGAs. Each device is designed to meet unique requirements across many use cases and applications. The Z-7010, Z-7015, and Z-7020 leverage the Artix®-7 FPGA programmable logic and offer lower power and lower cost for high-volume applications. The Z-7030, Z-7035, Z-7045, and Z-7100 are based on the Kintex®-7 FPGA programmable logic for higher-end applications that require higher performance and high I/O throughput.



ZYNQ-7000 Device Family



The Z-turn Board V2 is based on the Xilinx Zynq-7010 or 7020 SoC and the hardware specification is as listed in following table:

Item	Features
SoC	Xilinx XC7Z010-1CLG400 (Zynq-7010) or XC7Z020-2CLG400 (Zynq-7020) - Up to 667MHz ARM® dual-core Cortex™-A9 MPCore processor - Integrated Artix-7 class FPGA subsystem with 28K logic cells, 17,600 LUTs, 80 DSP slices (for XC7Z010) with 85K logic cells, 53,200 LUTs, 220 DSP slices (for XC7Z020) - NEON™ & Single / Double Precision Floating Point for each processor - Supports a Variety of Static and Dynamic Memory Interfaces
Memory	1GB DDR3 SDRAM (2 x 512MB, 32-bit)
Storage	16MB QSPI Flash 64Kbit EEPROM TF card interface
Communications	1 x 10/100/1000M Ethernet 1 x CAN 1 x Mini USB2.0 OTG 1 x USB-UART debug interface
Display	1 x HDMI (supports 1080p resolution, MYIR offers reference design for HDMI and LCD display functions without limitation for its. The IP cores in the design are provided by Xilinx. MYIR will provide Vivado project and SDK testing programs.)
User I/O	Brought out via two 1.27mm pitch 80-pin SMT female connectors - 90/106 user I/O (7010/7020) - Configurable 33/ 39 LVDS pairs I/O (7010/7020)
Dimensions	63mm x 102mm x 1.6mm (8-layer PCB design)
Power supply	USB power supply or DC 5V/2A
Others	Onboard three-axis acceleration sensor and temperature sensor 1 x 2.54mm pitch 14-pin JTAG interface 2 x Buttons (1x Reset, 1 x User) 4-channel toggle switch 5 x LEDs (3 x User LEDs, 1 x Power indicator, 1 RGB LED) 1 x Buzzer

Z-turn Board V2 Hardware Specification



On the rear of the board, there are two 1.27mm pitch 80-pin SMT female connectors to allow the availability of 96 (for 7010) or 106 (for 7020) user I/O and configurable as up to 39 LVDS pairs I/O. The Pinouts information is as below:

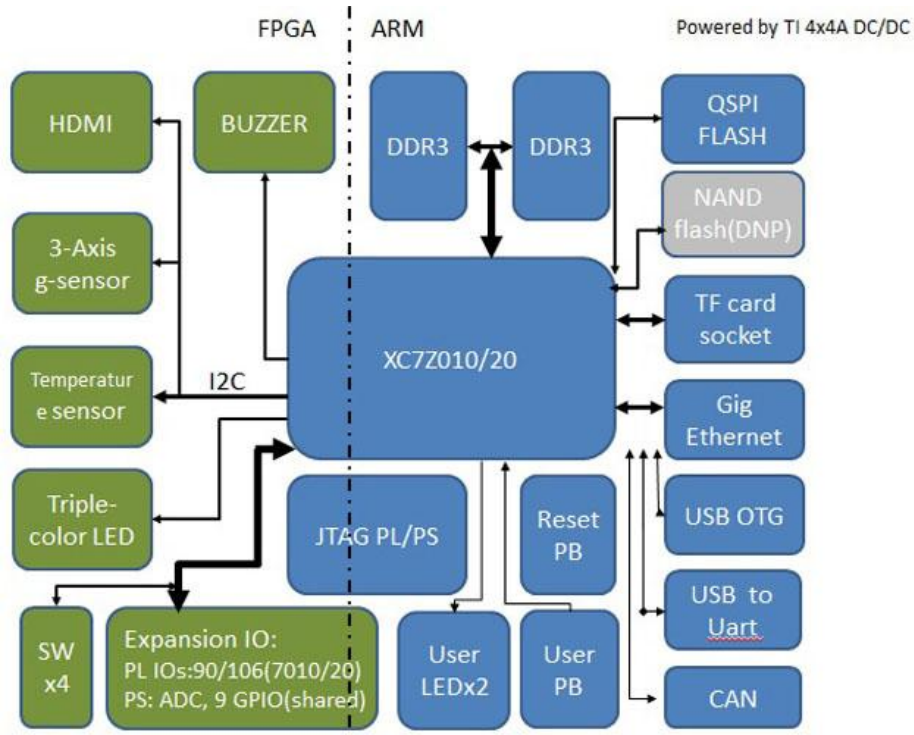
Default Function	BGA	Pin Name	CN1		Pin Name	BGA	Default Function
		VDD_5V	1	2	GND		
		VDD_3.3V	3	4	GND		
		VDD18_KEY_BACKUP	5	6	JTAG_TCK	F9	
	U7	IO_L11P_T1_13	7	8	JTAG_TMS	J6	
	V7	IO_L11N_T1_13	9	10	JTAG_TDI	G6	
	T9	IO_L12P_T1_13	11	12	JTAG_TDO	F6	
	U10	IO_L12N_T1_13	13	14	JTAG_NTRST		
		VDDIO_13_PL	15	16	IO_L14P_T2_13	Y9	
	Y7	IO_L13P_T2_13	17	18	IO_L14N_T2_13	Y8	
	Y6	IO_L13N_T2_13	19	20	IO_L21P_T3_13	V11	
	V8	IO_L15P_T2_13	21	22	IO_L21N_T3_13	V10	
	W8	IO_L15N_T2_13	23	24	GND		
		GND	25	26	IO_L1P_T0_34	T11	
	T12	IO_L2P_T0_34	27	28	IO_L1N_T0_34	T10	
	U12	IO_L2N_T0_34	29	30	IO_L3P_T0_34	U13	
	V12	IO_L4P_T0_34	31	32	IO_L3N_T0_34	V13	
	W13	IO_L4N_T0_34	33	34	GND		
		GND	35	36	IO_L5P_T0_34	T14	
	P14	IO_L6P_T0_34	37	38	IO_L5N_T0_34	T15	
RGB LED	R14	IO_L6N_T0_34	39	40	IO_L7P_T1_34	Y16	RGB LED
	W14	IO_L8P_T1_34	41	42	IO_L7N_T1_34	Y17	RGB LED
	Y14	IO_L8N_T1_34	43	44	GND		
12M	U14	IO_L11P_T1_34	45	46	IO_L10P_T1_34	V15	LCD_DATA2
	U15	IO_L11N_T1_34	47	48	IO_L10N_T1_34	W15	LCD_DATA3
		VDDIO_34_PL	49	50	IO_L13P_T2_34	N18	LCD_DATA6
LCD_DATA0	T16	IO_L9P_T1_34	51	52	IO_L13N_T2_34	P19	LCD_DATA7
LCD_DATA1	T20	IO_L15P_T2_34	53	54	GND		
LCD_DATA4	U18	IO_L12P_T1_34	55	56	IO_L15P_T2_34	T20	LCD_DATA10
LCD_DATA5	U19	IO_L12N_T1_34	57	58	IO_L15N_T2_34	U20	LCD_DATA11
LCD_DATA8	N20	IO_L14P_T2_34	59	60	IO_L17P_T2_34	Y18	LCD_DATA14
LCD_DATA9	P20	IO_L14N_T2_34	61	62	IO_L17N_T2_34	Y19	LCD_DATA15
LCD_DATA12	V20	IO_L16P_T2_34	63	64	IO_L19P_T3_34	R16	LCD_DE
LCD_DATA13	W20	IO_L16N_T2_34	65	66	IO_L19N_T3_34	R17	LCD_PCLK
		GND	67	68	GND		
LCD_HSYNC	W16	IO_L18N_T2_34	69	70	IO_L18P_T2_34	V16	LCD_VSYNC
I2S_SCLK	T17	IO_L20P_T3_34	71	72	IO_L20N_T3_34	R18	I2S_FSYNC_OUT
I2S_FSYNC_IN	V18	IO_L21N_T3_34	73	74	IO_L21P_T3_34	V17	I2S_Dout
I2S_Din	W18	IO_L22P_T3_34	75	76	IO_L24P_T3_34	P15	I2C0_SDA
HDMI_INT	W19	IO_L22N_T3_34	77	78	IO_L24N_T3_34	P16	I2C0_SCL
MEMS_INTn	N17	IO_L23P_T3_34	79	80	IO_L23N_T3_34	P18	BP

Pinouts of CN1

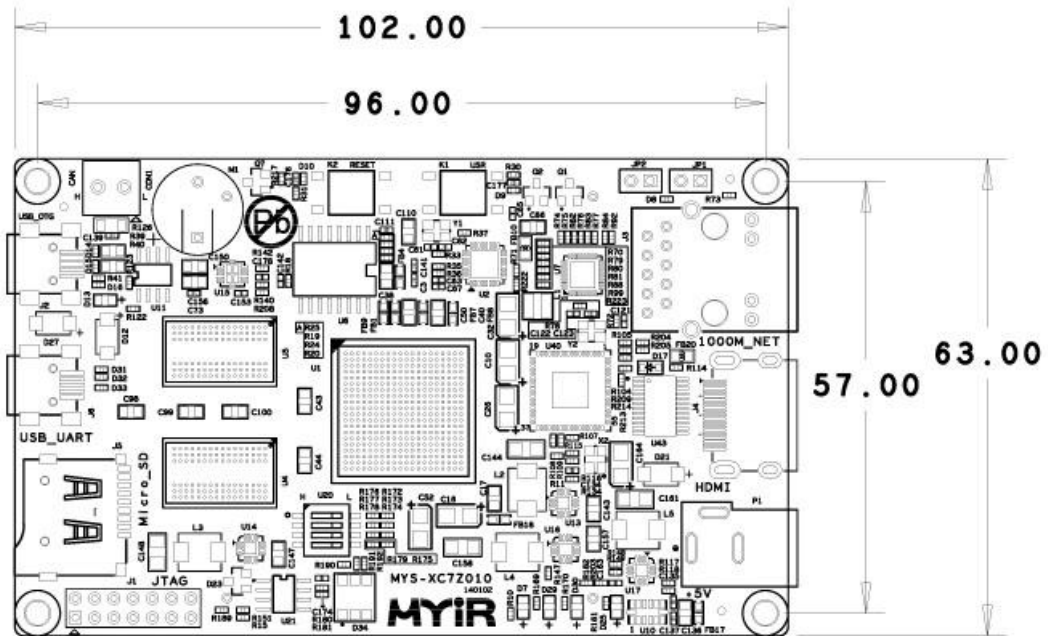


Default Function	BGA	Pin Name	CN2		Pin Name	BGA	Default Function
		VDD_5V	1	2	GND		
		VDD_3.3V	3	4	GND		
	K9	XADC_INP0	5	6	DXP_0	M9	
	L10	XADC_INN0	7	8	DXN_0	M10	
		XADC_VCC	9	10	GND		
PS_USER_LED1	E6	PS_MIO0_500	11	12	PS_MIO10_500	E9	UART0_RX
NAND_REn	D5	PS_MIO8_500	13	14	PS_MIO11_500	C6	UART0_TX
PS_USER_LED2	B5	PS_MIO9_500	15	16	PS_MIO14_500	C5	CAN0_RX
I2C1_CLK	D9	PS_MIO12_500	17	18	PS_MIO15_500	C8	CAN0_TX
I2C1_SDA	E8	PS_MIO13_500	19	20	GND		
		GND	21	22	IO_L2P_T0_35	B19	
	C20	IO_L1P_T0_35	23	24	IO_L2N_T0_35	A20	
	G20	IO_L18N_T2_35	25	26	IO_L4P_T0_35	D19	
	E17	IO_L3P_T0_35	27	28	IO_L4N_T0_35	D20	
	D18	IO_L3N_T0_35	29	30	GND		
		GND	31	32	IO_L6P_T0_35	F16	
	E18	IO_L5P_T0_35	33	34	IO_L6N_T0_35	F17	
	E19	IO_L5N_T0_35	35	36	IO_L8P_T1_35	M17	
	M19	IO_L7P_T1_35	37	38	IO_L8N_T1_35	M18	
	M20	IO_L7N_T1_35	39	40	GND		
		GND	41	42	IO_L10P_T1_35	K19	
	L19	IO_L9P_T1_35	43	44	IO_L10N_T1_35	J19	
	L20	IO_L9N_T1_35	45	46	IO_L12P_T1_35	K17	
	L16	IO_L11P_T1_35	47	48	IO_L12N_T1_35	K18	
	L17	IO_L11N_T1_35	49	50	GND		
		VDDIO_35_PL	51	52	IO_L14P_T2_35	J18	
	H16	IO_L13P_35	53	54	IO_L14N_T2_35	H18	
	H17	IO_L13N_35	55	56	IO_L16P_T2_35	G17	
	F19	IO_L15P_T2_35	57	58	IO_L16N_T2_35	G18	
	F20	IO_L15N_T2_35	59	60	GND		
		GND	61	62	IO_L18P_T2_35	G19	
	J20	IO_L17P_T2_35	63	64	IO_L18N_T2_35	G20	
	H20	IO_L17N_T2_35	65	66	IO_L20P_T3_35	K14	
	H15	IO_L19P_T3_35	67	68	IO_L20N_T3_35	J14	
	G15	IO_L19N_T3_35	69	70	GND		
		GND	71	72	IO_L22P_T3_35	L14	
	N15	IO_L21P_T3_35	73	74	IO_L22N_T3_35	L15	
	N16	IO_L21N_T3_35	75	76	IO_L24P_T3_35	K16	
	M14	IO_L23P_T3_35	77	78	IO_L24N_T3_35	J16	
	M15	IO_L23N_T3_35	79	80	GND		

Pinouts of CN2



Z-turn Board V2 Function Block Diagram



UNIT:MM

Z-turn Board V2 Dimension Chart



Software Features

Item	Features	Description	Remark
Cross compiler	gcc 6.2.1	gcc version 6.2.1 (Linaro GCC Snapshot 6.2-2016.11)	
Boot program	BOOT.BIN	First boot program including FSBL, bitstream and u-boot	Source code provided
Linux Kernel	Linux 4.14.0	Customized kernel for Z-turn Board V2	Source code provided
Drivers	USB OTG	USB OTG driver	Source code provided
	Ethernet	Gigabit Ethernet driver	Source code provided
	MMC/SD/TF	MMC/SD/TF card driver	Source code provided
	CAN	CAN driver	Source code provided
	LCD Controller	LCD driver	Source code provided
	HDMI	HDMI driver	Source code provided
	Button	Button driver	Source code provided
	UART	UART driver	Source code provided
	LED	LED driver	Source code provided
	GPIO	GPIO driver	Source code provided
	Buzzer	Buzzer driver	Source code provided
	G-Sensor	Three-axis acceleration sensor driver	Source code provided
Temperature Sensor	Temperature sensor driver	Source code provided	
File System	Ramdisk	Ramdisk system image	
	Ubuntu Desktop 18.04	Tar file and TF card image file	

Z-turn Board V2 Software Features