Boundary Devices
a Laird Connectivity™ company

Datasheet

Nitrogen8M Plus SMARC

Version 1.0

REVISION HISTORY

Version	Date	Notes	Contributors	Approver
0.1	20 April 2023	Preliminary Release	Gary Bisson	Dan Kephart
1.0	26 July 2023	Update RF Output section Update to R1 version of the schematics Update block diagram	Gary Bisson	Dan Kephart

CONTENTS

1 SCOPE

This document describes key hardware aspects of Boundary Device's Nitrogen8M Plus SMARC system-on-module which is based on the i.MX 8M Plus processor family and the Sterling™-LWB5+ Wi-Fi/BT combo radio. Data in this document is drawn from several sources and includes information found in the documentation for NXP's i.MX 8M Plus and our Sterling™-LWB5+.

Note: Information in this document is subject to change. Contact us for the most updated version of this document.

2 INTRODUCTION

The Nitrogen8M Plus SMARC is an integrated platform solution with Quad Cortex®-A53 processors operating up to 1.8 GHz and pre-certified dual-band 802.11 a/b/g/n/ac WLAN plus dual-mode Bluetooth® 5.2 Low Energy module.

Quad Arm® Cortex®-A53 processors are integrated with an NPU of 2.3 TOPS that greatly accelerates machine learning inference. The vision engine is composed of two MIPI-CSI camera inputs and an HDR-capable Image Signal Processor (ISP) capable of 375 MPixels/s. The advanced multimedia capabilities include several display interfaces, HDMI 2.0a (eARC), MIPI-DSI, and LVDS. These interfaces can utilize the onboard 1080p60 video encode and decode in H.265 and H.264 format, along with an onboard GPU that is a 3D and 2D graphic accelerator supporting 1 GPixel/s, OpenVG 1.1, Open GL ES3.1, Vulkan, and Open CL 1.2 FP. Multiple audio and microphone interfaces are available along with the audio processing capabilities of the HiFi 4 DSP operating at 800MHz for Immersive Audio and Voice systems.

The Nitrogen8M Plus SMARC features an Arm® Cortex®-M7 microcontroller running at 800 MHz for customer applications to offload the Cortex®-A53 processor for real time and low power operation. A variety of robust control networks for industrial applications are possible via CAN-FD interfaces, SPI, I2C, UART, USB 3.0, and dual Gb Ethernet.

The Nitrogen8M Plus SMARC includes the Sterling™-LWB5+ which is pre-calibrated and integrates the complete transmit/receive RF paths including diplexer, switches, reference crystal oscillator and power management units (PMU). One RF connector (MHF4) on the module provides the most flexibility of antenna selection and installation for the best antenna performance. Several high-performance antennas are certified with the Sterling™-LWB5+ onboard the Nitrogen8M Plus SMARC. A detailed antenna list is shown in the Certified Antennas section.

The Nitrogen8M Plus SMARC with the Sterling- provides IEEE 802.11 ac 1x1 SISO Wi-Fi capability with data rates up to MCS9 (433.3 Mbps) as well as a BT 5.2 radio solution. The radio interface is SDIO 3.0 for Wi-Fi and UART for Bluetooth for optimized power usage.

The Nitrogen8M Plus SMARC has several product SKUs providing different eMMC and LPDDR4 memory configurations, see Ordering Information section.

3 NITROGEN8M PLUS SMARC FEATURES SUMMARY

The Nitrogen8M Plus SMARC module is based on i.MX 8M Plus from NXP which offers a variety of interfaces and different memory configurations. Most of these interfaces are multiplexed and not able to be used simultaneously.

It complies with the SMARC v2.1 specification from SGET.

Key features of Nitrogen8M Plus SMARC are described in Table 1.

Table 1: Key Features of Nitrogen8M Plus SMARC

Feature	Description
CPU	Quad Cortex®-A53 processors operation up to 1.8 GHz ▪ 32 KB L1 Instruction Cache ▪ 32 KB L1 Data Cache ▪ 512 KB unified L2 cache Cortex®-M7 core platform operating up to 800 MHz ▪ 32 KB L1 Instruction Cache ▪ 32 KB L1 Data Cache ▪ 256 KB tightly coupled memory (TCM) ▪ ARM Neon™ extension
Image Sensor Processor (ISP)	▪ 375 Mpixel/s HDR ISP supporting configurations, such as 12MP@30fps, 4kp45, or 2x 1080p80
Memory interface	▪ On module: 32-bits LPDDR4 with inline ECC (size, please refer to Ordering Information) ▪ On module: 8-bits eMMC 5.1 with HS400 speed (size, please refer Ordering Information) ▪ SPI ▪ FlexSPI Flash with support for XIP (for Cortex®-M7 in low-power mode) and support for either one Octal SPI, or parallel read mode of two identical Quad SPI FLASH devices.
Graphic Processing Unit	GC7000UL with OpenCL and Vulkan support ▪ 2 shaders ▪ 166 million triangles/sec ▪ 1.0 giga pixel/sec ▪ 16 GFLOPs 32-bit ▪ Supports OpenGL ES 1.1, 2.0, 3.0, OpenCL 1.2, Vulkan ▪ Core clock frequency of 1000 MHz ▪ Shader clock frequency of 1000 MHz GC520L for 2D acceleration ▪ Render target compatibility between 3D and 2D GPU (super tile status buffer)
Video Processing Unit	Video Decode ▪ 1080p60 HEVC/H.265 Main, Main 10 (up to level 5.1) ▪ 1080p60 VP9 Profile 0, 2 ▪ 1080p60 VP8 ▪ 1080p60 AVC/H.264 Baseline, Main, High decoder Video Encode ▪ 1080p60 AVC/H.264 encoder ▪ 1080p60 HEVC/H.265 encoder
Neutral Processing Unit (NPU)	2.3 TOP/s Neural Network performance ▪ Keywords detect, noise reduction, beamforming ▪ Speech recognition (i.e., Deep Speech 2) ▪ Image recognition (i.e., ResNet-50)
HDMI 2.0a Tx	HDMI 2.0a Tx supporting one display ▪ Resolutions of 720x480p60, 1280x720p60, 1920x1080p60, 3840x2160p30 ▪ Pixel clock up to 297 MHz
LCDIF Display Controller	Supports up to 1920x1200p60 display per LCDIF if no more than 2 instances used simultaneously, or 2x 1080p60 + 1x 4kp30 on HDMI if all 3 instances used simultaneously. ▪ One LCDIF drives MIPI DSI, up to UWHD and WUXGA ▪ One LCDIF drives LVDS Tx, up to 1920x1080p60 ▪ One LCDIF drives HDMI Tx, up to 4kp30
Camera Interface	Two MIPI-CSI Interfaces ▪ 2x 4-lane MIPI-CSI interface (D-PHY v1.2, up to 1.5Gbps)

Feature	Description
	HDR ISP ▪ 2x ISP supporting 375 Mpixel/s aggregate performance and up to 3-exposure HDR processing. ▪ When one camera is used, supports up to 12MP@30fps or 4kp45 ▪ When two cameras are used, each supports up to 1080p80 ▪ Maximum resolution limited to resolutions achievable with a 250 MHz pixel clock and active pixel rate of 200 Mpixel/s with 24-bit RGB. This includes resolutions such as: – 1080p60 – WUXGA (1920X1200) at 60 Hz – 1920x1440 at 60 Hz – WHD (2560X1080) at 60 Hz – MIPI DSI: WQHD (2560x1440) can be supported by reduced blanking mode
Audio	▪ Cadence® Tensilica® HiFi 4 DSP, operating up to 800 MHz ▪ Two I2S (Optionally One as HAD) ▪ All ports support 49.152 MHz BCLK. ▪ ASRC supports processing 32 audio channels, 4 context groups, 8 kHz to 384 kHz sample rate, and 1/16 to 8x sample rate conversion ratio. ▪ eARC/ARC (HDMI)
Connectivity	▪ One PCI Express (PCIe) Gen3 Single Lane supporting Dual Mode Operation with PHY ▪ Two USB 3.0 Host interfaces (also supports USB 2.0) ▪ Two USB 2.0 Host interfaces (without integrated PHY) + One USB 2.0 OTG interface ▪ One Ultra Secure Digital Host Controller (uSDHC) interface ▪ Two Gigabit Ethernet controllers (both capable of simultaneous operation) ▪ Two Controller Area Network (FlexCAN) modules, each optionally supporting flexible data-rate (FD, available on Industrial parts only) **Note:** Flexible Data (FD) mode supports MB operation only with no RX FIFO or DMA support. ▪ Three Universal Asynchronous Receiver/Transmitter (UART) modules ▪ Five I2C modules ▪ Three SPI modules
Security	▪ Resource Domain Controller (RDC) ▪ Arm® TrustZone® (TZ) architecture ▪ On-chip RAM (OCRAM) secure region protection using OCRAM controller ▪ High Assurance Boot (HAB) ▪ Cryptographic Acceleration and Assurance Module (CAAM) ▪ Secure Non-Volatile Storage (SNVS) ▪ Secure JTAG Controller (SJC)
Debug Interface	▪ Secure JTAG Controller (SJC) ▪ Two Debug UART ports for Quad Cortex®-A53 processors and Cortex®-M7.
RF output	RF output with MHF4 connector provides flexible external antenna selection for optimized performance for both Wi-Fi and BT

4 Block Diagram

The figure below shows the block diagram of the Nitrogen8M Plus SMARC which contains the NXP i.MX 8M Plus processor, PMIC (PCA9450CHN) and the Sterling™-LWB5+ Wi-Fi/BT combo.

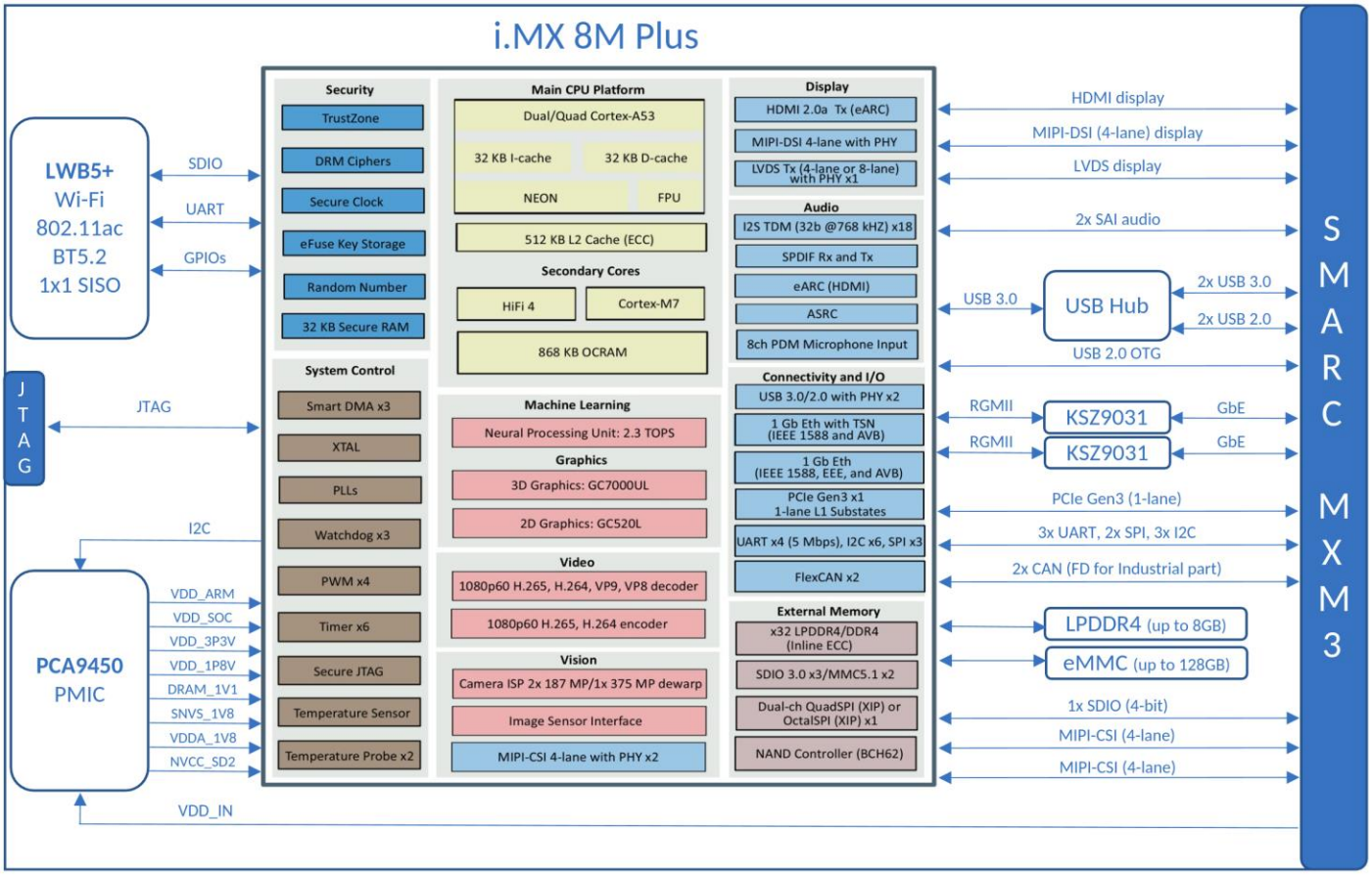


Figure 1: Nitrogen8MP SMARC block diagram

Detailed connections between the LWB5+ and the i.MX 8M Plus are detailed in Table 2 below.

Table 2: Sterling™-LWB5+ to i.MX 8M Plus Connections

	LWB5+	i.MX8M Plus
SDIO	SD_CLK/SD_CMD/SD_DATA0-3	SD3_CLK/SD3_CMD/SD3_DATA0-3
UART	UART_SOUT/UART_SIN/UART_CTSn/UART_RTSn	UART1_RXD/UART1_TXD/UART3_RXD/UART3_TXD
CLK	SUSCLK	CLKOUT1
BT_EN	BT_REG_ON	NAND_CE2
BT_IRQ	BT_HOST_WAKE	SAI5_RXD0
WL_EN	WL_REG_ON	NAND_CE3
WL_IRQ	GPIO_0	NAND_DQS

5 DC Power Tree

The Nitrogen8M Plus SMARC requires a primary 5V power supply (VSYS) input. This supply is the main power domain to the on-module NXP PCA9450CHN power management IC (PMIC), which generates all required supply voltages for the module

components. The PMIC has 32.768KHz crystal oscillator and buffer built-in which generates the real-time clock (RTC) for the NXP processor and Wi-Fi radio.

5.1 Power Modes Diagram

NXP PCA9450CHN has eight power modes: OFF, READY, SNVS, RUN, STANDBY, PWRDN, PWRUP and FAULT_SD. Below figure shows the state transition diagram showing the conditions to enter and exit each state.

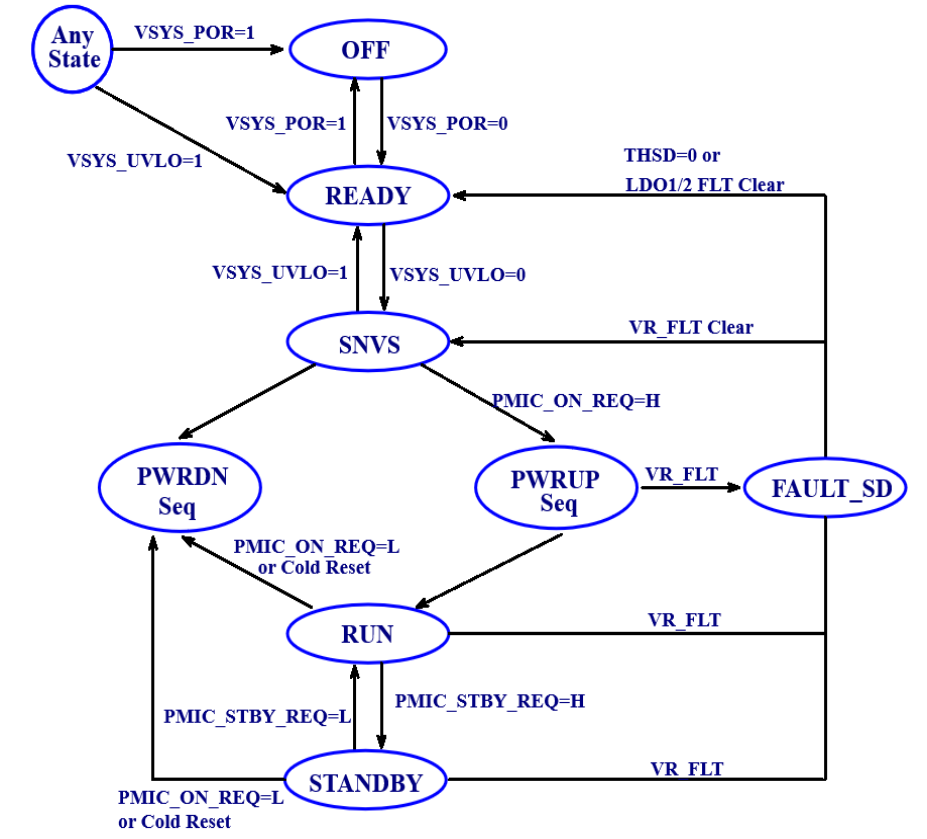


Figure 2: State transition diagram for PMIC

- **OFF mode:**
  PMIC will enter OFF mode from any state when the main power source VSYS_5V falls below V_{sys_POR} threshold (2.2 to 2.6V; typ.=2.4V). All regulators are OFF and all registers are reset in this mode.
- **READY Mode:**
  PMIC enters READY mode when VSYSY_5V is higher than V_{sys_POR}. The internal LDO VINT is enabled and loads the MTP data to registers. Once the MTP data loading is complete, the state machine is ready to transition to SNVS mode.
- **SNVS Mode:**
  PMIC will enter SNVS (Secure Non-Volatile Storage mode) when VSYS_5V exceeds the V_{sys_UVLO} threshold. LDO1 is powered up and the 32.778KHz buffer starts running. RTC_RESET_B is pulled high after both LDO1 and LDO2 voltage come up.

Note: PMIC_ON_REQ input is masked until RTC_RESET_B is released. PMIC will start power up sequence if PMIC_ON_REQ is asserted high in this mode.

- **PWRUP Mode:**
  After RTC_RESET_B is released in SNVS mode, the PMIC starts power up with a pre-defined sequence with PMIC_ON_REQ asserted high.

During PWRUP mode, PMIC_STBY_REQ signal is masked until POR_B is released. The PWRUP mode ends up releasing POR_B and the PMIC is transitioned to RUN mode.

- **PWRDN Mode:**
  When PMIC_ON_REQ is low in RUN or STANDBY mode, PMIC enters PWRDN mode, where it starts with pulling down POR_B. and then by turning off each power rail before transitioning to SNVS mode.
- **RUN Mode:**
  PMIC operates in RUN mode when PMIC_ON_REQ is driven high and PMIC_STBY_REQ is driven low. When PMIC_STBY_REQ is asserted high in this mode, it is transitioned to STANDBY mode. PMIC_ON_REQ is asserted low, it moves to PWRDN mode.
- **STANDBY Mode:**
  PMIC is transitioned to STANDBY mode from RUN mode when both PMIC_ON_REQ and PMIC_STBY_REQ are driven low. If PMIC_ON_REQ is asserted low, then it is transitioned to PWRDN mode. If PMIC_STBY_REQ is driven low, it is transitioned to RUN mode.

Power Mode	VSYS_5V	PMIC_ON_REQ	PMIC_STBY_REQ
OFF	VSYS_5V<V_{SYS_POR}	x	x
READY	VSYS_5V>V_{SYS_POR}	x	x
SNVS	VSYS_5V>V_{SYS_UVLO}	LOW	x
STANDBY	VSYS_5V>V_{SYS_UVLO}	HIGH	HIGH
RUN	VSYS_5V>V_{SYS_UVLO}	HIGH	LOW

- **FAULT_SD Mode:**
  PCA9450CHN has three kinds of Fault sources.
  - **Thermal shutdown**: Transition to SNVS mode or READY mode after Fault_SD mode.
    When junction temperature reaches 150℃, it enters FAULT_SD mode after 120 μ s where regulators are tuned off simultaneously. It stays at FAULT_SD mode until the junction temperature fall below 150℃, then move to READY state if any of LDO1 and LDO2 is fault is triggered. And it will move to SNVS mode if either LDO1 or LDO2 fault is triggered.
  - **Voltage regulator fault during power up:** Transition to READY mode after FAULT_SD mode.
    Any POK of voltage regulator doesn't come up within 10ms after regulator is enabled during power up sequence, it stops power-up sequence and then moves into FAULT_SD mode where all regulators are turned off.
  - **Voltage regulator fault in STBY and RUN MODE:** Move to FAULT_SD mode in 100ms after fault is detected. Transition to SNVS mode or READY mode after FAULT_SD mode.

6 BOOT MODE

The Nitrogen8M Plus SMARC module contains a switch (***SW1***) connected to BOOT_MODE0 thus allowing to switch from internal fuses boot (eMMC by default) to USB serial downloader.

The other boot mode signals (BOOT_MODE[1-3]) are exposed to the carrier to SMARC BOOT_SEL[0-2] signals.

This allows more combinations as shown in Table 3.

Table 3: Boot mode combinations

BOOT_MODE3	BOOT_MODE2	BOOT_MODE1	BOOT_MODE0	BOOT MODE
0	0	0	0	Boot from Internal Fuses
0	0	0	1	USB Serial Download
0	0	1	0	uSDHC3 (eMMC boot only, SD3 8-bit) Default.
0	0	1	1	uSDHC2 (SD boot, SD2)
0	1	0	0	NAND 8-bit single device 256 pages.
0	1	0	1	NAND 8-bit single device 512 pages
0	1	1	0	QSPI 3B Read
0	1	1	1	QSPI Hyperflash 3.3V
1	0	0	0	ECSPI Boot

BOOT_MODE3	BOOT_MODE2	BOOT_MODE1	BOOT_MODE0	BOOT MODE
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved (Boot on I2C connected to BOOT PIN[3:2]
1	1	0	1	Reserved
1	1	1	0	Infinite Loop Mode
1	1	1	1	Test Mode

Caution: BOOT_MODE0, BOOT_MODE1, BOOT_MODE2, BOOT_MODE3, JTAG_MOD and POR_B must be pulled to “111111” for i.MX8M Plus to enter Boundary Scan Mode.

7 Electrical Characteristic and Power Consumption

7.1 Absolute Maximum Ratings

Table 4 summarizes the absolute maximum ratings and Table 5 lists the recommended operating conditions for the Nitrogen8M Plus SMARC product series. Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Note: Maximum rating for signals follows the supply domain of the signals.

Table 4: Absolute maximum ratings

Symbol (Domain)	Parameter	Min.	Max	Unit
VSYS_5V	Input voltage for the SOM	-0.5	+6.0	V
I/O Input/output voltage range	Any I/O pin referred to VDD_1V8; VDDA_1V8; WI-FI_1V8; NVCC_SNVS_1V8	-0.3	+2.1	V
I/O Input/output voltage range	Any I/O pin referred to VDD_3V3; VSD_3V3; NVCC_SD2	-0.3	+3.6	V
$T_{STORAGE}$	Storage Temperature Range	-40	+125	°C
ANT0; ANT1	Maximum RF input (reference to 50-Ω input)	NA	+10	dBm
ESD	Electrostatic discharge tolerance	-2000	+2000	V

7.2 Recommended Operating Conditions

Table 5: Recommended Operating Conditions

Symbol (Domain)	Parameter	Min	Typ	Max	Unit
VSYS_5V	Input voltage for the SOM	3.3	5.0	5.5	V
I/O Input/output voltage range	Any I/O pin referred to VDD_1V8; VDDA_1V8; WI-FI_1V8; NVCC_SNVS_1V8	1.71	1.8	1.89	V
I/O Input/output voltage range	Any I/O pin referred to VDD_3V3; VSD_3V3; NVCC_SD2	3.0	3.3	3.6	V
T-ambient	Operating Ambient temperature	-40	25	85	°C

Note: The operating ambient temperature ratings are highly dependent on the design-case, such as the enclosure design, system design, processor activity, GPU/VPU activity, and peripherals used.

Running over 70° C ambient temperature typically requires the implementation of thermal management strategies such as passive (heatsink/spreader). Please contact Boundary Devices if you need information and guidance for thermal management.

7.3 DC current consumption

Several power saving modes are available and are listed in Table 6.

Table 6: Typical current consumption

Mode	Description	Current (Avg)
Power Saving mode	CPU is on, Stay on Wi-Fi connection only.	431mA
RAM suspend mode	CPU is on, memory and wireless connection are off.	7.7mA
Linux graceful power down mode	All circuits are off. Only the NVCC_SNVS_1V8 PMU is alive and ONOFF pin is accessible to allow turn on of the SOM.	154uA

8 MODULE PIN OUT AND PINMUX TABLE

Table 7 lists the pin multiplexing (PIN-MUX) of the Nitrogen8M Plus SMARC. Most of the pin names on the SOM are same as the pin names of the connected NXP processor. The "Pin Number " column shows the relationship of the SOM pin number to the NXP processor pin number.

PO = Power Output, PI = Power Input, DI = Digital Input, DO = Digital Output, DIO = Bi-directional Digital Port, GND = Ground

NXP process has configurable internal Pull-up (PU) and pull-down (PD) resistor whose values are listed below. During a reset condition, the PU and PD state are pre-defined and cannot be changed.

Table 7: Resistor characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Pull-up (PU) resistor	VDD=1.65 to 1.95V Temp=0 to 95℃	12	22	49	kΩ
Pull-down (PD) resistor		13	23	48	kΩ
Pull-up (PU) resistor	VDD=3.0 to 3.6V Temp=0 to 95℃	18	37	72	kΩ
Pull-down (PD) resistor		24	43	87	kΩ

Pin configuration for the i.MX is achieved using a suite of evaluation and configuration tools that assists users from initial evaluation to production software development. Users can download the tool from the NXP website: https://www.nxp.com/design/designs/config-tools-for-i-mx-applications-processors:CONFIG-TOOLS-IMX?tab=Design_Tools_Tab

Table 8: Pinout table for Nitrogen8M Plus SMARC edge connector (J2)

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
P1	SMB_ALERT#	**SAI**: SAI1_RXD0 **PDM**: PDM_BIT_STREAM00 **ENET1**: 1588_EVENT1_IN **GPIO**: GPIO4_IO02	DI	1.8 to 5 V	
P2	GND	NA	-	NA	
P3	CSI1_CK+	MIPI_CSI2_CLK_P	DO	1.8V	
P4	CSI1_CK-	MIPI_CSI2_CLK_N	DO	1.8V	
P5	GBE1_SDP	**GPIO**: GPIO4_IO01 **SAI**: SAI1_RXC **PDM**: PDM_CLK **ENET1**: 1588_EVENT0_OUT	DI/O	3.3V	
P6	GBE0_SDP	**GPIO**: GPIO1_IO09	DI/O	3.3V	

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
		ENET: 1588_EVENT0_OUT **PWM**: PWM2_OUT **ISP**: ISP_SHUTTER_OPEN_1 **USDHC**: USDHC3_RESET_B **DMA**: SDMA2_EXT_EVENT00			
P7	CSI1_RX0+	MIPI_CSI2_D0_P	DI	1.8V	
P8	CSI1_RX0-	MIPI_CSI2_D0_N	DI	1.8V	
P9	GND	NA	-	NA	
P10	CSI1_RX1+	MIPI_CSI2_D1_P	DI	1.8V	
P11	CSI1_RX1-	MIPI_CSI2_D1_N	DI	1.8V	
P12	GND	NA	-	NA	
P13	CSI1_RX2+	MIPI_CSI2_D2_P	DI	1.8V	
P14	CSI1_RX2-	MIPI_CSI2_D2_N	DI	1.8V	
P15	GND	NA	-	NA	
P16	CSI1_RX3+	MIPI_CSI2_D3_P	DI	1.8V	
P17	CSI1_RX3-	MIPI_CSI2_D3_N	DI	1.8V	
P18	GND	NA	-	NA	
P19	GBE0_MDI3-	TXRXM_D	DI/O	1.8V	From KSZ9031 (U8)
P20	GBE0_MDI3+	TXRXP_D	DI/O	1.8V	From KSZ9031 (U8)
P21	GBE0_LINK100#	LED1	DO	3.3V	From KSZ9031 (U8)
P22	GBE0_LINK1000#	LED2	DO	3.3V	From KSZ9031 (U8)
P23	GBE0_MDI2-	TXRXM_C	DI/O	1.8V	From KSZ9031 (U8)
P24	GBE0_MDI2+	TXRXP_C	DI/O	1.8V	From KSZ9031 (U8)
P25	GBE0_LINK_ACT#	LED1	DO	3.3V	From KSZ9031 (U8)
P26	GBE0_MDI1-	TXRXM_B	DI/O	1.8V	From KSZ9031 (U8)
P27	GBE0_MDI1+	TXRXP_B	DI/O	1.8V	From KSZ9031 (U8)
P28	GBE0_CTREF	TP28	-	NA	Test point
P29	GBE0_MDI0-	TXRXM_A	DI/O	1.8V	From KSZ9031 (U8)
P30	GBE0_MDI0+	TXRXP_A	DI/O	1.8V	From KSZ9031 (U8)
P31	SPI0_CS1#	**GPIO**: GPIO1_IO01 **PWM**: PWM1_OUT **ISP**: ISP_SHUTTER_TRIG_0 **CLK**: CCM_EXT_CLK2	DO	1.8V	
P32	GND	NA	-	NA	
P33	SDIO_WP	**USDHC**: USDHC2_WP **GPIO**: GPIO2_IO20 **DEBUG**: CORESIGHT_EVENTI	DI	1.8 or 3.3V	
P34	SDIO_CMD	**USDHC**: USDHC2_CMD **SPI**: ECSPI2_MOSI **UART**: UART4_DCE_TX **UART**: UART4_DTE_RX	DI/O	1.8 or 3.3V	

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
		PDM: AUDIOMIX_PDM_CLK **GPIO**: GPIO2_IO14			
P35	SDIO_CD#	**USDHC**: USDHC2_CD_B **GPIO**: GPIO2_IO12	DI	1.8 or 3.3V	
P36	SDIO_CK	**USDHC**: USDHC2_CLK **SPI**: ECSPI2_SCLK **UART**: UART4_DCE_RX **UART**: UART4_DTE_TX **PDM**: AUDIOMIX_PDM_CLK **GPIO**: GPIO2_IO13	DO	1.8 or 3.3V	
P37	SDIO_PWR_EN	**USDHC**: USDHC2_CD_B **GPIO**: GPIO2_IO12 **DEBUG**: SRC_SYSTEM_RESET	DO	3.3V	
P38	GND	NA	-	NA	
P39	SDIO_D0	**USDHC**: USDHC2_DATA0 **I2C**: I2C4_SDA **UART**: UART2_DCE_RX **UART**: UART2_DTE_TX **PDM**: AUDIOMIX_PDM_BIT_STREAM00 **GPIO**: GPIO2_IO15	DI/O	1.8 or 3.3V	
P40	SDIO_D1	**USDHC**: USDHC2_DATA1 **I2C**: I2C4_SCL **UART**: UART2_DCE_TX **UART**: UART2_DTE_RX **PDM**: AUDIOMIX_PDM_BIT_STREAM01 **GPIO**: GPIO2_IO16	DI/O	1.8 or 3.3V	
P41	SDIO_D2	**USDHC**: USDHC2_DATA2 **SPI**: ECSPI2_SS0 **SPDIF**: AUDIOMIX_SPDIF1_OUT **PDM**: AUDIOMIX_PDM_BIT_STREAM04 **GPIO**: GPIO2_IO17	DI/O	1.8 or 3.3V	
P42	SDIO_D3	**USDHC**: USDHC2_DATA3 **SPI**: ECSPI2_MISO **SPDIF**: AUDIOMIX_SPDIF1_IN **PDM**: AUDIOMIX_PDM_BIT_STREAM03 **GPIO**: GPIO2_IO18 **DEBUG**: SRC_EARLY_RESET	DI/O	1.8 or 3.3V	
P43	SPI0_CS0#	**SPI**: ECSPI1_SS0 **UART**: UART3_DCE_RTS **UART**: UART3_DTE_CTS **I2C**: I2C2_SDA **SAI**: AUDIOMIX_SAI7_TX_SYNC **GPIO**: GPIO5_IO09	DO	1.8V	
P44	SPI0_CK	**SPI**: ECSPI1_SCLK **UART**: UART3_DCE_RX **UART**: UART3_DTE_TX **I2C**: I2C1_SCL **SAI**: AUDIOMIX_SAI7_RX_SYNC **GPIO**: GPIO5_IO06	DO	1.8V	

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
P45	SPI0_DIN	**SPI**: ECSPI1_MISO **UART**: UART3_DCE_CTS **UART**: UART3_DTE_RTS **I2C**: I2C2_SCL **SAI**: AUDIOMIX_SAI7_RX_DATA00 **GPIO**: GPIO5_IO08	DI	1.8V	
P46	SPI0_DO	**SPI**: ECSPI1_MOSI **UART**: UART3_DCE_TX **UART**: UART3_DTE_RX **I2C**: I2C1_SDA **SAI**: AUDIOMIX_SAI7_RX_BCLK **GPIO**: GPIO5_IO07	DO	1.8V	
P47	GND	NA	-	NA	
P48	SATA_TX+	MIPI_CSI1_D2_P	DI	1.8V	SMARC exception
P49	SATA_TX-	MIPI_CSI1_D2_N	DI	1.8V	SMARC exception
P50	GND	NA	-	NA	
P51	SATA_RX+	MIPI_CSI1_D3_P	DI	1.8V	SMARC exception
P52	SATA_RX-	MIPI_CSI1_D3_N	DI	1.8V	SMARC exception
P53	GND	NA	-	NA	
P54	SPI1_CS0# / ESPI_CS0# / QSPI_CS0#	**SPI**: ECSPI2_SS0 **UART**: UART4_DCE_RTS **UART**: UART4_DTE_CTS **I2C**: I2C4_SDA **CLK**: CCM_CLK02 **GPIO**: GPIO5_IO13	DO	1.8V	
P55	SPI1_CS1# / ESPI_CS1# / QSPI_CS1#	**SAI**: AUDIOMIX_SAI1_MCLK **SAI**: AUDIOMIX_SAI1_TX_BCLK **ENET**: ENET1_TX_CLK **GPIO**: GPIO5_IO09	DO	1.8V	
P56	SPI1_CK / ESPI_CK / QSPI_CK	**SPI**: ECSPI2_SCLK **UART**: UART4_DCE_RX **UART**: UART4_DTE_TX **I2C**: I2C3_SCL **SAI**: AUDIOMIX_SAI7_TX_BCLK **GPIO**: GPIO5_IO10	DO	1.8V	
P57	SPI1_DIN / ESPI_IO_1 / QSPI_IO_1	**SPI**: ECSPI2_MISO **UART**: UART4_DCE_CTS **UART**: UART4_DTE_RTS **I2C**: I2C4_SCL **SAI**: AUDIOMIX_SAI7_MCLK **CLK**: CCM_CLK01 **GPIO**: GPIO5_IO12	DI	1.8V	
P58	SPI1_DO / ESPI_IO_0 / QSPI_IO_0	**SPI**: ECSPI2_MOSI **UART**: UART4_DCE_TX **UART**: UART4_DTE_RX **I2C**: I2C3_SDA **SAI**: AUDIOMIX_SAI7_TX_DATA00	DO	1.8V	

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
		GPIO: GPIO5_IO11			
P59	GND	NA	-	NA	
P60	USB0+	USB1_D_P	DI/O	3.3V	
P61	USB0-	USB1_D_N	DI/O	3.3V	
P62	USB0_EN_OC#	**GPIO**: GPIO1_IO13 **USB**: USB1_OTG_OC **PWM**: PWM2_OUT	DI	3.3V	
P63	USB0_VBUS_DET	USB1_VBUS	DI	5V	
P64	USB0_OTG_ID	USB1_ID	DI	3.3V	
P65	USB1+	USB2DN_DP2	DI/O	3.3V	From USB Hub (U9)
P66	USB1-	USB2DN_DM2	DI/O	3.3V	From USB Hub (U9)
P67	USB1_EN_OC#	PRT_CTL2	DI	3.3V	From USB Hub (U9)
P68	GND	NA	-	NA	
P69	USB2+	USB2DN_DP3	DI/O	3.3V	From USB Hub (U9)
P70	USB2-	USB2DN_DM3	DI/O	3.3V	From USB Hub (U9)
P71	USB2_EN_OC#	PRT_CTL3	DI	3.3V	From USB Hub (U9)
P72	RSVD	CLKOUT2	DO	1.8V	
P73	RSVD	NA	-	NA	
P74	USB3_EN_OC#	PRT_CTL1	DI	3.3V	From USB Hub (U9)
P75	PCIE_A_RST#	**SAI**: AUDIOMIX_SAI2_RX_SYNC **SAI**: AUDIOMIX_SAI5_TX_SYNC **SAI**: AUDIOMIX_SAI5_TX_DATA01 **SAI**: AUDIOMIX_SAI2_RX_DATA01 **UART**: UART1_DCE_TX **UART**: UART1_DTE_RX **GPIO**: GPIO4_IO21 **PDM**: AUDIOMIX_PDM_BIT_STREAM02	DO	1.8V	
P76	USB4_EN_OC#	PRT_CTL4	DI	3.3V	From USB Hub (U9)
P77	PCIE_B_CKREQ#	NA	-	NA	
P78	PCIE_A_CKREQ#	**SAI**: AUDIOMIX_SAI1_RX_SYNC **ENET**: ENET1_1588_EVENT0_IN **GPIO**: GPIO4_IO00	DI/O	3.3V	
P79	GND	NA	-	NA	
P80	PCIE_C_REFCK+	NA	-	NA	
P81	PCIE_C_REFCK-	NA	-	NA	
P82	GND	NA	-	NA	
P83	PCIE_A_REFCK+	PCIE_REF_PAD_CLK_P	DO	1.8V	
P84	PCIE_A_REFCK-	PCIE_REF_PAD_CLK_N	DO	1.8V	
P85	GND	NA	-	NA	
P86	PCIE_A_RX+	PCIE_RXN_P	DO	1.8V	

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
P87	PCIE_A_RX-	PCIE_RXN_N	DO	1.8V	
P88	GND	NA	-	NA	
P89	PCIE_A_TX+	PCIE_TXN_P	DO	1.8V	
P90	PCIE_A_TX-	PCIE_TXN_N	DO	1.8V	
P91	GND	NA	-	NA	
P92	HDMI_D2+ / DP1_LANE0+	HDMI_TX2_P	DO	1.8V	
P93	HDMI_D2- / DP1_LANE0-	HDMI_TX2_N	DO	1.8V	
P94	GND	NA	-	NA	
P95	HDMI_D1+ / DP1_LANE1+	HDMI_TX1_P	DO	1.8V	
P96	HDMI_D1- / DP1_LANE1-	HDMI_TX1_N	DO	1.8V	
P97	GND	NA	-	NA	
P98	HDMI_D0+ / DP1_LANE2+	HDMI_TX0_P	DO	1.8V	
P99	HDMI_D0- / DP1_LANE2-	HDMI_TX0_N	DO	1.8V	
P100	GND	NA	-	NA	
P101	HDMI_CK+ / DP1_LANE3+	HDMI_TXC_P	DO	1.8V	
P102	HDMI_CK- / DP1_LANE3-	HDMI_TXC_N	DO	1.8V	
P103	GND	NA	-	NA	
P104	HDMI_HPD / DP1_HPD	HDMI_HPD	DI	1.8V	
P105	HDMI_CTRL_CK / DP1_AUX+	HDMI_DDC_SCL	DI/O	1.8V	
P106	HDMI_CTRL_DAT / DP1_AUX-	HDMI_DDC_SDA	DI/O	1.8V	
P107	DP1_AUX_SEL	HDMI_CEC	DI/O	1.8V	SMARC exception
P108	GPIO0 / CAM0_PWR#	GPA0	DI/O	1.8V	From GPIO expander (U14)
P109	GPIO1 / CAM1_PWR#	GPA1	DI/O	1.8V	From GPIO expander (U14)
P110	GPIO2 / CAM0_RST#	GPA2	DI/O	1.8V	From GPIO expander (U14)
P111	GPIO3 / CAM1_RST#	GPA3	DI/O	1.8V	From GPIO expander (U14)
P112	GPIO4 / HDA_RST#	GPA4	DI/O	1.8V	From GPIO expander (U14)
P113	GPIO5 / PWM_OUT	**SPDIF**: AUDIOMIX_SPDIF1_OUT **PWM**: PWM3_OUT **I2C**: I2C5_SCL **TIMER**: GPT1_COMPARE1 **CAN**: CAN1_TX **GPIO**: GPIO5_IO03	DI/O	1.8V	
P114	GPIO6 / TACHIN	GPA6	DI/O	1.8V	From GPIO expander (U14)

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
P115	GPIO7	GPA7	DI/O	1.8V	From GPIO expander (U14)
P116	GPIO8	GPB1	DI/O	1.8V	From GPIO expander (U14)
P117	GPIO9	GPB2	DI/O	1.8V	From GPIO expander (U14)
P118	GPIO10	GPB3	DI/O	1.8V	From GPIO expander (U14)
P119	GPIO11	**SAI**: AUDIOMIX_SAI1_TX_DATA06 **SAI**: AUDIOMIX_SAI6_RX_SYNC **SAI**: AUDIOMIX_SAI6_TX_SYNC **ENET**: ENET1_RX_ER **GPIO**: GPIO4_IO18	DI/O	1.8V	
P120	GND	NA	-	NA	
P121	I2C_PM_CK	**I2C**: I2C4_CLK **PWM**: PWM2_OUT **PCI**: PCIE_CLKREQ_B **SPI**: ECSPI2_MISO **GPIO**: GPIO5_IO20	DI/O	1.8V	
P122	I2C_PM_DAT	**I2C**: I2C4_SDA **PWM**: PWM1_OUT **SPI**: ECSPI2_SS0 **GPIO**: GPIO5_IO21	DI/O	1.8V	
P123	BOOT_SEL0#	BOOT_MODE1	DI	1.8V	10k pull-down
P124	BOOT_SEL1#	BOOT_MODE2	DI	1.8V	10k pull-down
P125	BOOT_SEL2#	BOOT_MODE3	DI	1.8V	10k pull-down
P126	RESET_OUT#	GPB5	DI/O	1.8V	From GPIO expander (U14)
P127	RESET_IN#	POR_B	DI	1.8V	
P128	POWER_BTN#	ONOFF	DI	1.8 - 5V	
P129	SER0_TX	**UART**: UART4_DCE_TX **UART**: UART4_DTE_RX **UART**: UART2_DCE_RTS **UART**: UART2_DTE_CTS **TIMER**: GPT1_CAPTURE1 **I2C**: I2C6_SDA **GPIO**: GPIO5_IO29	DO	1.8V	
P130	SER0_RX	**UART**: UART4_DCE_RX **UART**: UART4_DTE_TX **UART**: UART2_DCE_CTS **UART**: UART2_DTE_RTS **PCI**: PCIE_CLKREQ_B **TIMER**: GPT1_COMPARE1 **I2C**: I2C6_SCL **GPIO**: GPIO5_IO28	DI	1.8V	
P131	SER0_RTS#	**NAND**: NAND_DATA03 **SPI**: FLEXSPI_A_DATA03 **SDHC**: USDHC3_WP **UART**: UART4_DCE_RTS **UART**: UART4_DTE_CTS **ISP**: ISP_FL_TRIG_1	DI	1.8V	

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
		GPIO: GPIO3_IO09 **DEBUG**: CORESIGHT_TRACE07			
P132	SER0_CTS#	**NAND**: NAND_DATA02 **SPI**: FLEXSPI_A_DATA02 **SDHC**: USDHC3_CD_B **UART**: UART4_DCE_CTS **UART**: UART4_DTE_RTS **I2C**: I2C4_SDA **GPIO**: GPIO3_IO08 **DEBUG**: CORESIGHT_TRACE06	DO	1.8V	
P133	GND	NA	-	NA	
P134	SER1_TX	**UART**: UART2_DCE_TX **UART**: UART2_DTE_RX **SPI**: ECPIS3_SS0 **TIMER**: GPT1_COMPARE2 **GPIO**: GPIO5_IO25	DO	1.8V	
P135	SER1_RX	**UART**: UART2_DCE_TX **UART**: UART2_DTE_RX **SPI**: ECPIS3_SS0 **TIMER**: GPT1_COMPARE2 **GPIO**: GPIO5_IO24	DI	1.8V	
P136	SER2_TX	**SPI**: ECPIS1_MOSI **UART**: UART3_DCE_TX **UART**: UART3_DTE_RX **I2C**: I2C1_SDA **SAI**: AUDIOMIX_SAI7_RX_BCLK **GPIO**: GPIO5_IO07	DO	1.8V	
P137	SER2_RX	**SPI**: ECPIS1_SCLK **UART**: UART3_DCE_RX **UART**: UART3_DTE_TX **I2C**: I2C1_SCL **SAI**: AUDIOMIX_SAI7_RX_SYNC **GPIO**: GPIO5_IO06	DI	1.8V	
P138	SER2_RTS#	NA	-	NA	
P139	SER2_CTS#	NA	-	NA	
P140	SER3_TX	NA	-	NA	
P141	SER3_RX	NA	-	NA	
P142	GND	NA	-	NA	
P143	CAN0_TX	**SAI**: AUDIOMIX_SAI5_RX_DATA01 **SAI**: AUDIOMIX_SAI1_TX_DATA03 **SAI**: AUDIOMIX_SAI1_TX_SYNC **SAI**: AUDIOMIX_SAI5_TX_SYNC **PDM**: AUDIOMIX_PDM_BIT_STREAM01 **GPIO**: GPIO3_IO22 **CAN**: CAN1_TX	DO	1.8V	
P144	CAN0_RX	**SAI**: AUDIOMIX_SAI5_RX_DATA02 **SAI**: AUDIOMIX_SAI1_TX_DATA04 **SAI**: AUDIOMIX_SAI1_TX_SYNC	DI	1.8V	

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
		SAI: AUDIOMIX_SAI5_TX_BCLK **PDM**: AUDIOMIX_PDM_BIT_STREAM02 **GPIO**: GPIO3_IO23 **CAN**: CAN1_RX			
P145	CAN1_TX	**SAI**: AUDIOMIX_SAI5_RX_DATA03 **SAI**: AUDIOMIX_SAI1_TX_DATA05 **SAI**: AUDIOMIX_SAI1_TX_SYNC **SAI**: AUDIOMIX_SAI5_TX_DATA00 **PDM**: AUDIOMIX_PDM_BIT_STREAM03 **GPIO**: GPIO3_IO24 **CAN**: CAN2_TX	DO	1.8V	
P146	CAN1_RX	**SAI**: AUDIOMIX_SAI5_MCLK **SAI**: AUDIOMIX_SAI1_TX_BCLK **PWM**: PWM1_OUT **I2C**: I2C5_SDA **GPIO**: GPIO3_IO25 **CAN**: CAN2_RX	DI	1.8V	
P147	VDD_IN	VSYS	A	3.0 - 5.25V	
P148	VDD_IN	VSYS	A	3.0 - 5.25V	
P149	VDD_IN	VSYS	A	3.0 - 5.25V	
P150	VDD_IN	VSYS	A	3.0 - 5.25V	
P151	VDD_IN	VSYS	A	3.0 - 5.25V	
P152	VDD_IN	VSYS	A	3.0 - 5.25V	
P153	VDD_IN	VSYS	A	3.0 - 5.25V	
P154	VDD_IN	VSYS	A	3.0 - 5.25V	
P155	VDD_IN	VSYS	A	3.0 - 5.25V	
P156	VDD_IN	VSYS	A	3.0 - 5.25V	
S1	CSI1_TX+ / I2C_CAM1_CK	SC1	DO	1.8V	From I2C expander (U13)
S2	CSI1_TX- / I2C_CAM1_DAT	SD1	DI/O	1.8V	From I2C expander (U13)
S3	GND	NA	-	NA	
S4	RSVD	NA	-	NA	
S5	I2C_CAM0_CK / CSI0_TX+	SC0	DO	1.8V	From I2C expander (U13)
S6	CAM_MCK	**GPIO**: GPIO1_IO15 **USB**: USB2_OC **USDHC**: USDHC3_WP **PWM**: PWM4_OUT **CCM**: CCM_CLKO2	DO	1.8V	
S7	I2C_CAM0_DAT / CSI0_TX-	SD0	DI/O	1.8V	From I2C expander (U13)
S8	CSI0_CK+	MIPI_CSI1_CLK_P	DO	1.8V	
S9	CSI0_CK-	MIPI_CSI1_CLK_N	DO	1.8V	
S10	GND	NA	-	NA	

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
S11	CSI0_RX0+	MIPI_CSI1_D0_P	DI	1.8V	
S12	CSI0_RX0-	MIPI_CSI1_D0_N	DI	1.8V	
S13	GND	NA	-	NA	
S14	CSI0_RX1+	MIPI_CSI1_D1_P	DI	1.8V	
S15	CSI0_RX1-	MIPI_CSI1_D1_N	DI	1.8V	
S16	GND	NA	-	NA	
S17	GBE1_MDI0+	TXRXP_A	DI/O	1.8V	From KSZ9031 (U16)
S18	GBE1_MDI0-	TXRXM_A	DI/O	1.8V	From KSZ9031 (U16)
S19	GBE1_LINK100#	LED1	DO	3.3V	From KSZ9031 (U16)
S20	GBE1_MDI1+	TXRXP_B	DI/O	1.8V	From KSZ9031 (U16)
S21	GBE1_MDI1-	TXRXM_B	DI/O	1.8V	From KSZ9031 (U16)
S22	GBE1_LINK1000#	LED2	DO	3.3V	From KSZ9031 (U16)
S23	GBE1_MDI2+	TXRXP_C	DI/O	1.8V	From KSZ9031 (U16)
S24	GBE1_MDI2-	TXRXM_C	DI/O	1.8V	From KSZ9031 (U16)
S25	GND	NA	-	NA	
S26	GBE1_MDI3+	TXRXP_D	DI/O	1.8V	From KSZ9031 (U16)
S27	GBE1_MDI3-	TXRXM_D	DI/O	1.8V	From KSZ9031 (U16)
S28	GBE1_CTREF	TP34	-	NA	Test point
S29	PCIE_D_TX+ / SERDES_0_TX+	NA	-	NA	
S30	PCIE_D_TX- / SERDES_0_TX-	NA	-	NA	
S31	GBE1_LINK_ACT#	LED1	DO	3.3V	
S32	PCIE_D_RX+ / SERDES_0_RX+	NA	-	NA	
S33	PCIE_D_RX- / SERDES_0_RX-	NA	-	NA	
S34	GND	NA	-	NA	
S35	USB4+	USB2DN_DP4	DI/O	3.3V	From USB Hub (U9)
S36	USB4-	USB2DN_DM4	DI/O	3.3V	From USB Hub (U9)
S37	USB3_VBUS_DET	NA	-	NA	
S38	AUDIO_MCK	**SAI**: AUDIOMIX_SAI3_MCLK **PWM**: PWM4_OUT **SAI**: AUDIOMIX_SAI5_MCLK **SPDIF**: AUDIOMIX_SPDIF1_OUT **GPIO**: GPIO5_IO02 **SPDIF**: AUDIOMIX_SPDIF1_IN	DO	1.8V	
S39	I2S0_LRCK	**SAI**: AUDIOMIX_SAI3_TX_SYNC **SAI**: AUDIOMIX_SAI2_TX_DATA01 **SAI**: AUDIOMIX_SAI5_RX_DATA01 **SAI**: AUDIOMIX_SAI3_TX_DATA01 **UART**: UART2_DCE_RX	DI/O	1.8V	

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
		UART: UART2_DTE_TX **GPIO**: GPIO4_IO31 **PDM**: AUDIOMIX_PDM_BIT_STREAM03			
S40	I2S0_SDOUT	**SAI**: AUDIOMIX_SAI3_TX_DATA00 **SAI**: AUDIOMIX_SAI2_TX_DATA03 **SAI**: AUDIOMIX_SAI5_RX_DATA03 **TIMER**: GPT1_CAPTURE2 **SPDIF**: AUDIOMIX_SPDIF1_EXT_CLK **GPIO**: GPIO5_IO01	DO	1.8V	
S41	I2S0_SDIN	**SAI**: AUDIOMIX_SAI3_RX_DATA00 **SAI**: AUDIOMIX_SAI2_RX_DATA03 **SAI**: AUDIOMIX_SAI5_RX_DATA00 **UART**: UART2_DCE_RTS **UART**: UART2_DTE_CTS **GPIO**: GPIO4_IO30 **PDM**: AUDIOMIX_PDM_BIT_STREAM01	DI	1.8V	
S42	I2S0_CK	**SAI**: AUDIOMIX_SAI3_TX_BCLK **SAI**: AUDIOMIX_SAI2_TX_DATA02 **SAI**: AUDIOMIX_SAI5_RX_DATA02 **TIMER**: GPT1_CAPTURE1 **UART**: UART2_DCE_TX **UART**: UART2_DTE_RX **GPIO**: GPIO5_IO00 **PDM**: AUDIOMIX_PDM_BIT_STREAM02	DI/O	1.8V	
S43	ESPI_ALERT0#	NA	-	NA	
S44	ESPI_ALERT1#	NA	-	NA	
S45	MDIO_CLK	NA	-	NA	
S46	MDIO_DAT	NA	-	NA	
S47	GND	NA	-	NA	
S48	I2C_GP_CK	**I2C**: I2C2_SCL **ENET**: ENET_QOS_1588_EVENT1_IN **SDHC**: USDHC3_CD_B **SPI**: ECSPI1_MISO **ENET**: ENET_QOS_1588_EVENT1_AUX_IN **GPIO**: GPIO5_IO16	DO	1.8V	
S49	I2C_GP_DAT	**I2C**: I2C2_SDA **ENET**: ENET_QOS_1588_EVENT1_OUT **SDHC**: USDHC3_WP **SPI**: ECSPI1_SS0 **GPIO**: GPIO5_IO17	DI/O	1.8V	
S50	I2S2_LRCK / HDA_SYNC	**SAI**: AUDIOMIX_SAI2_TX_SYNC **SAI**: AUDIOMIX_SAI5_TX_DATA01 **ENET**: ENET_QOS_1588_EVENT3_OUT **SAI**: AUDIOMIX_SAI2_TX_DATA01 **UART**: UART1_DCE_CTS **UART**: UART1_DTE_RTS **GPIO**: GPIO4_IO24 **PDM**: AUDIOMIX_PDM_BIT_STREAM02	DI/O	1.8V	

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
S51	I2S2_SDOUT / HDA_SDO	**SAI**: AUDIOMIX_SAI2_TX_DATA00 **SAI**: AUDIOMIX_SAI5_TX_DATA03 **ENET**: ENET_QOS_1588_EVENT2_IN **CAN**: CAN2_TX **ENET**: ENET_QOS_1588_EVENT2_AUX_IN **GPIO**: GPIO4_IO26	DO	1.8V	
S52	I2S2_SDIN / HDA_SDI	**SAI**: AUDIOMIX_SAI2_RX_DATA00 **SAI**: AUDIOMIX_SAI5_TX_DATA00 **ENET**: ENET_QOS_1588_EVENT2_OUT **SAI**: AUDIOMIX_SAI2_TX_DATA01 **UART**: UART1_DCE_RTS **UART**: UART1_DTE_CTS **GPIO**: GPIO4_IO23 **PDM**: AUDIOMIX_PDM_BIT_STREAM03	DI	1.8V	
S53	I2S2_CK / HDA_CK	**SAI**: AUDIOMIX_SAI2_TX_BCLK **SAI**: AUDIOMIX_SAI5_RX_BCLK **CAN**: CAN1_TX **UART**: UART1_DCE_RX **UART**: UART1_DTE_TX **GPIO**: GPIO4_IO22 **PDM**: AUDIOMIX_PDM_BIT_STREAM01	DI/O	1.8V	
S54	SATA_ACT#	NA	-	NA	
S55	USB5_EN_OC#	NA	-	NA	
S56	ESPI_IO_2 / QSPI_IO_2	GPA5	DI/O	1.8V	From GPIO expander (U14)
S57	ESPI_IO_3 / QSPI_IO_3	NA	-	NA	
S58	ESPI_RESET#	**SAI**: AUDIOMIX_SAI3_RX_BCLK **SAI**: AUDIOMIX_SAI2_RX_DATA02 **SAI**: AUDIOMIX_SAI5_RX_BCLK **TIMER**: GPT1_CLK **UART**: UART2_DCE_CTS **UART**: UART2_DTE_RTS **GPIO**: GPIO4_IO29 **PDM**: AUDIOMIX_PDM_CLK	DI/O	1.8V	<
S59	USB5+	NA	-	NA	
S60	USB5-	NA	-	NA	
S61	GND	NA	-	NA	
S62	USB3_SSTX+	USB3DN_TXDP1	DI/O	3.3V	From USB Hub (U9)
S63	USB3_SSTX-	USB3DN_TXDM1	DI/O	3.3V	From USB Hub (U9)
S64	GND	NA	-	NA	
S65	USB3_SSRX+	USB3DN_RXDP1	DI/O	3.3V	From USB Hub (U9)
S66	USB3_SSRX-	USB3DN_RXDM1	DI/O	3.3V	From USB Hub (U9)
S67	GND	NA	-	NA	
S68	USB3+	USB2DN_DP1	DI/O	3.3V	From USB Hub (U9)
S69	USB3-	USB2DN_DM1	DI/O	3.3V	From USB Hub (U9)

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
S70	GND	NA	-	NA	
S71	USB2_SSTX+	USB3DN_TXDP3	DI/O	3.3V	From USB Hub (U9)
S72	USB2_SSTX-	USB3DN_TXDM3	DI/O	3.3V	From USB Hub (U9)
S73	GND	NA	-	NA	
S74	USB2_SSRX+	USB3DN_RXDP3	DI/O	3.3V	From USB Hub (U9)
S75	USB2_SSRX-	USB3DN_RXDM3	DI/O	3.3V	From USB Hub (U9)
S76	PCIE_B_RST#	NA	-	NA	
S77	PCIE_C_RST#	NA	-	NA	
S78	PCIE_C_RX+ / SERDES_1_RX+	NA	-	NA	
S79	PCIE_C_RX- / SERDES_1_RX-	NA	-	NA	
S80	GND	NA	-	NA	
S81	PCIE_C_TX+ / SERDES_1_TX+	NA	-	NA	
S82	PCIE_C_TX- / SERDES_1_TX-	NA	-	NA	
S83	GND	NA	-	NA	
S84	PCIE_B_REFCK+	NA	-	NA	
S85	PCIE_B_REFCK-	NA	-	NA	
S86	GND	NA	-	NA	
S87	PCIE_B_RX+	NA	-	NA	
S88	PCIE_B_RX-	NA	-	NA	
S89	GND	NA	-	NA	
S90	PCIE_B_TX+	NA	-	NA	
S91	PCIE_B_TX-	NA	-	NA	
S92	GND	NA	-	NA	
S93	DP0_LANE0+	NA	-	NA	
S94	DP0_LANE0-	NA	-	NA	
S95	DP0_AUX_SEL	NA	-	NA	
S96	DP0_LANE1+	NA	-	NA	
S97	DP0_LANE1-	NA	-	NA	
S98	DP0_HPD	NA	-	NA	
S99	DP0_LANE2+	NA	-	NA	
S100	DP0_LANE2-	NA	-	NA	
S101	GND	NA	-	NA	
S102	DP0_LANE3+	NA	-	NA	
S103	DP0_LANE3-	NA	-	NA	
S104	USB3_OTG_ID	NA	-	NA	

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
S105	DP0_AUX+	NA	-	NA	
S106	DP0_AUX-	NA	-	NA	
S107	LCD1_BKLT_EN	**NAND**: NAND_CLE **SPI**: FLEXSPI_B_SCLK **SDHC**: USDHC3_DATA7 **UART**: UART4_DCE_RX **UART**: UART4_DTE_TX **GPIO**: GPIO3_IO05 **DEBUG**: CORESIGHT_TRACE03	DI/O	1.8V	
S108	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+	LVDS1_CLK_P	DO	1.8V	
S109	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-	LVDS1_CLK_N	DO	1.8V	
S110	GND	NA	-	NA	
S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	LVDS1_TX0_P	DO	1.8V	
S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-	LVDS1_TX0_N	DO	1.8V	
S113	eDP1_HPD / DSI1_TE	TP27	-	NA	Test point
S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	LVDS1_TX1_P	DO	1.8V	
S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-	LVDS1_TX1_N	DO	1.8V	
S116	LCD1_VDD_EN	**GPIO**: GPIO1_IO05 **M7**: M7_NMI **ISP**: ISP_FL_TRIG_1 **CLK**: CCM_PMIC_READY	DI/O	1.8V	
S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	LVDS1_TX2_P	DO	1.8V	
S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-	LVDS1_TX2_N	DO	1.8V	
S119	GND	NA	-	NA	
S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	LVDS1_TX3_P	DO	1.8V	
S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-	LVDS1_TX3_N	DO	1.8V	
S122	LCD1_BKLT_PWM	**TIMER**: GPT1_COMPARE3 **GPIO**: GPIO5_IO05 **SPDIF**: AUDIOMIX_SPDIF1_EXT_CLK **PWM**: PWM1_OUT	DO	1.8V	
S123	GPIO13	**GPIO**: GPIO1_IO00	DI/O	1.8V	

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
		CCM: CCM_ENET_PHY_REF_CLK_ROOT **ISP**: ISP_FL_TRIG_0 **SAI**: ANAMIX_REF_CLK_32K **CCM**: CCM_EXT_CLK1			
S124	GND	NA	-	NA	
S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	MIPI_DSI1_D0_P	DO	1.8V	
S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-	MIPI_DSI1_D0_N	DO	1.8V	
S127	LCD0_BKLT_EN	**NAND**: NAND_RE_B **SPI**: FLEXSPI_B_DQS **SDHC**: USDHC3_DATA4 **UART**: UART4_DCE_TX **UART**: UART4_DTE_RX **GPIO**: GPIO3_IO15 **DEBUG**: CORESIGHT_TRACE13	DO	1.8V	
S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	MIPI_DSI1_D1_P	DO	1.8V	
S129	LVDS0_1- / eDP0_TX1- / DSI0_D1-	MIPI_DSI1_D1_N	DO	1.8V	
S130	GND	NA	-	NA	
S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	MIPI_DSI1_D2_P	DO	1.8V	
S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-	MIPI_DSI1_D2_N	DO	1.8V	
S133	LCD0_VDD_EN	**SAI**: AUDIOMIX_SAI1_RX_DATA01 **PDM**: AUDIOMIX_PDM_BIT_STREAM01 **ENET**: ENET1_1588_EVENT1_OUT **GPIO**: GPIO4_IO03	DO	1.8V	
S134	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	MIPI_DSI1_CLK_P	DO	1.8V	
S135	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-	MIPI_DSI1_CLK_N	DO	1.8V	
S136	GND	NA	-	NA	
S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	MIPI_DSI1_D3_P	DO	1.8V	
S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-	MIPI_DSI1_D3_N	DO	1.8V	
S139	I2C_LCD_CK	NA	-	NA	
S140	I2C_LCD_DAT	NA	-	NA	
S141	LCD0_BKLT_PWM	**SPDIF**: AUDIOMIX_SPDIF1_IN	DI/O	1.8V	

SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
		PWM: PWM2_OUT **I2C**: I2C5_SDA **TIMER**: GPT1_COMPARE2 **CAN**: CAN1_RX **GPIO**: GPIO5_IO04			
S142	GPIO12	**NAND**: NAND_CE1_B **SPI**: FLEXSPI_A_SS1_B **USDHC**: USDHC3_STROBE **I2C**: I2C4_SCL **GPIO**: GPIO3_IO02 **DEBUG**: CORESIGHT_TRACE00	DI/O	1.8V	
S143	GND	NA	-	NA	
S144	eDP0_HPD / DSI0_TE	TP26	-	NA	Test point
S145	WDT_TIME_OUT#	WDOG_B	DO	1.8V	
S146	PCIE_WAKE#	**SAI**: AUDIOMIX_SAI3_RX_SYNC **SAI**: AUDIOMIX_SAI2_RX_DATA01 **SAI**: AUDIOMIX_SAI5_RX_SYNC **SAI**: AUDIOMIX_SAI3_RX_DATA01 **SPDIF**: AUDIOMIX_SPDIF1_IN **GPIO**: GPIO4_IO28 **PDM**: AUDIOMIX_PDM_BIT_STREAM00	DI	3.3V	
S147	VDD_RTC	NVCC_SNVS	A	1.8V	
S148	LID#	**GPIO**: GPIO1_IO11 **USB**: USB2_ID **PWM**: PWM2_OUT **SDHC**: USDHC3_VSELECT **CLK**: CCM_PMIC_READY	DI	1.8 - 5V	
S149	SLEEP#	**GPIO**: GPIO1_IO08 **ENET**; ENET_QOS_1588_EVENT0_IN **PWM**: PWM1_OUT **ISP**: ISP_PRELIGHT_TRIG_1 **ENET**: ENET_QOS_1588_EVENT0_AUX_IN **SDHC**: USDHC2_RESET_B	DI	1.8 - 5V	
S150	VIN_PWR_BAD#	PMIC_RST_B	DI	VDD_IN	
S151	CHARGING#	GPB6	DI	1.8 - 5V	From GPIO expander (U14)
S152	CHARGER_PRSNT#	**SAI**: AUDIOMIX_SAI1_TX_DATA07 **SAI**: AUDIOMIX_SAI6_MCLK **PDM**: AUDIOMIX_PDM_CLK **ENET**: ENET1_TX_ER **GPIO**: GPIO4_IO19	DI	1.8 - 5V	
S153	CARRIER_STBY#	**GPIO**: GPIO1_IO09 **ENET**: ENET_QOS_1588_EVENT0_OUT **PWM**: PWM2_OUT **ISP**: ISP_SHUTTER_OPEN_1 **SDHC**: USDHC3_RESET_B **DMA**: SDMA2_EXT_EVENT00	DO	1.8V	
S154	CARRIER_PWR_ON	**GPIO**: GPIO1_IO10 **USB**: USB1_ID	DO	1.8V	

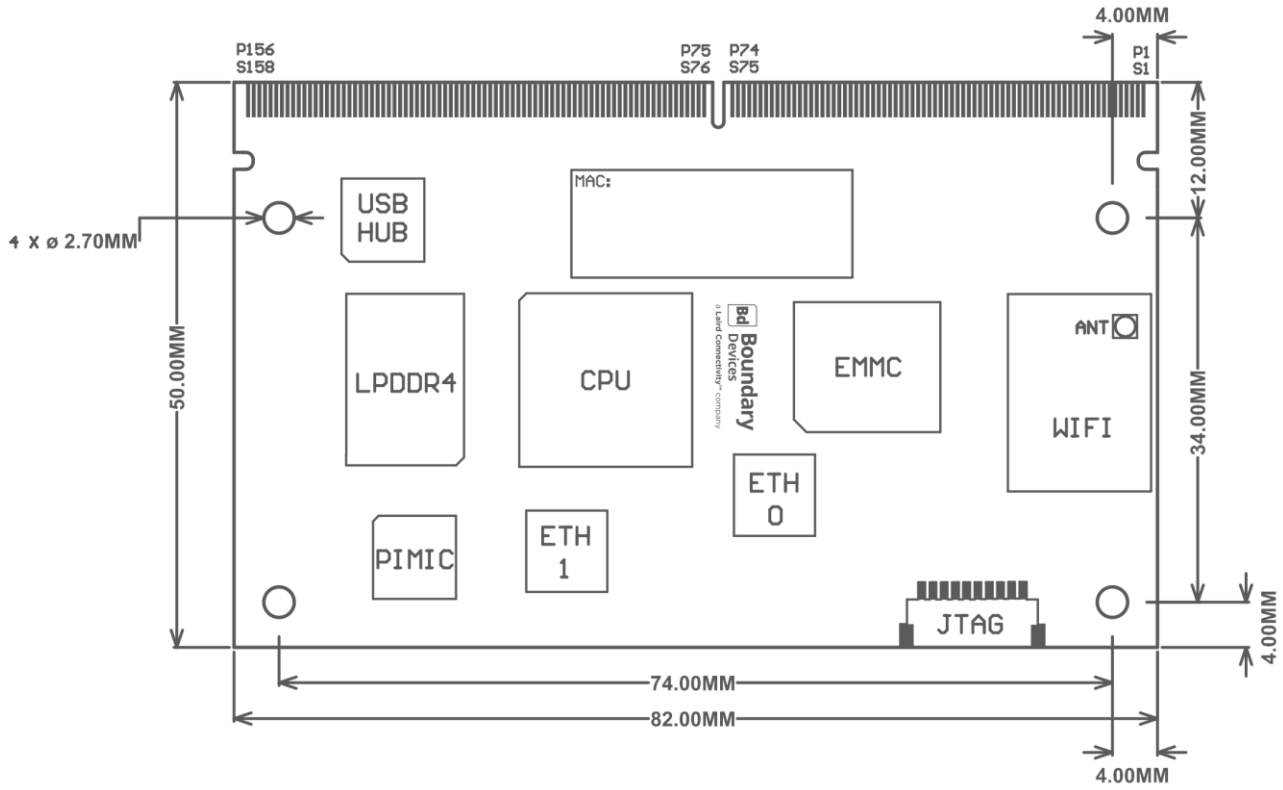
SMARCPin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
		PWM: PWM3_OUT			
S155	FORCE_RECOV#	BOOT_MODE0	DI	1.8V	High = USB recovery
S156	BATLOW#	GPB7	DI	1.8 - 5V	From GPIO expander (U14)
S157	TEST#	TP43	DI	1.8 - 5V	Test point
S158	GND	NA	-	NA	

Table 8: Pinout table for Nitrogen8M Plus SMARC JTAG connector (J1)

Pin #	Pin Name	CPU PIN / Multiplexing	I/O	I/O Level	Comments
1	VDD_JTAG	VDD_1P8V	DO	1.8V	
2	JTAG_TRST#	TP14	-	NA	Test point
3	JTAG_TMS	JTAG_TMS	DI	1.8V	
4	JTAG_TDO	JTAG_TDO	DO	1.8V	
5	JTAG_TDI	JTAG_TDI	DI	1.8V	
6	JTAG_TCK	JTAG_TCK	DI	1.8V	
7	JTAG_RTCK	TP15	DI	1.8V	
8	JTAG_RESET_IN#	GPB0	DI	1.8V	From GPIO expander (U14)
9	MFG_MODE#	NA	-	1.8V	
10	GND	GND	-	NA	

9 MECHANICAL AND PCB FOOTPRINT SPECIFICATION

Module dimensions of the Nitrogen8M Plus SMARC are 82 x 50 mm. Detail drawings are shown below.



10 STORAGE INSTRUCTIONS

Required Storage Conditions:

- **Prior to Opening the Dry Packing**
  The following are required storage conditions prior to opening the dry packing:
  - Normal temperature: 5~40℃
  - Normal humidity: 80% (Relative humidity) or less
  - Storage period: One year or less

11 REGULATORY

Regulatory IDs Summary

Model	US/FCC	Canada/IC	Japan
Nitrogen8M Plus SMARC	SQG-LWB5PLUS	3147A-LWB5PLUS	201-200402

12 CERTIFIED ANTENNAS

The Nitrogen8M Plus SMARC contains the Sterling LWSB5+ module, which was certified with the following antennas.

Manufacturer	Model	Laird Connectivity Part Number	Type	Connector	Peak Gain	
					2.4 GHz	5GHz
TE Connectivity	2.4/5.5 GHz Dipole Antenna	001-0009	Dipole	RP-SMA	2 dBi	2 dBi
Laird Connectivity	FlexPIFA	001-0021	PIFA	MHF4L	2.5 dBi	3 dBi
Laird Connectivity	Mini NanoBlade Flex	EMF2449A1-10MH4L	PCB Dipole	MHF4L	2.78 dBi	3.38 dBi
Laird Connectivity	NanoBlade	ENB2449A1-10MH4L	PCB Dipole	MHF4L	2 dBi	3.9 dBi
ACX	AD1608-A2455AAT/LF	N/A	Chip Antenna	MHF4L	1 dBi	4 dBi
Laird Connectivity	MHF4L Jumper	CARSMF10AMH4L-001	N/A	SMA to MHF4L		

13 Ordering Information

Order Model	Description
N8MP_SMARC_SOM_2r16eWB	SMARC SOM: i.MX8M Quad Plus / 2GB / 16GB eMMC / LWB5+
N8MP_SMARC_SOM_4r16eWB	SMARC SOM: i.MX8M Quad Plus / 4GB / 16GB eMMC / LWB5+
N8MP_SMARC_SOM_2r16eWB_i	SMARC SOM: i.MX8M Quad Plus / 2GB / 16GB eMMC / LWB5+ / Industrial Temp
N8MP_SMARC_SOM_4r16eWB_i	SMARC SOM: i.MX8M Quad Plus / 4GB / 16GB eMMC / LWB5+ / Industrial Temp
N8MP_SMARC_SOM_8r16eWB	SMARC SOM: i.MX8M Quad Plus / 8GB / 16GB eMMC / LWB5+ (MOQ requirements)
SMARC_CAR_BRD	Universal Carrier Board - SMARC (Note - SOM sold separately)