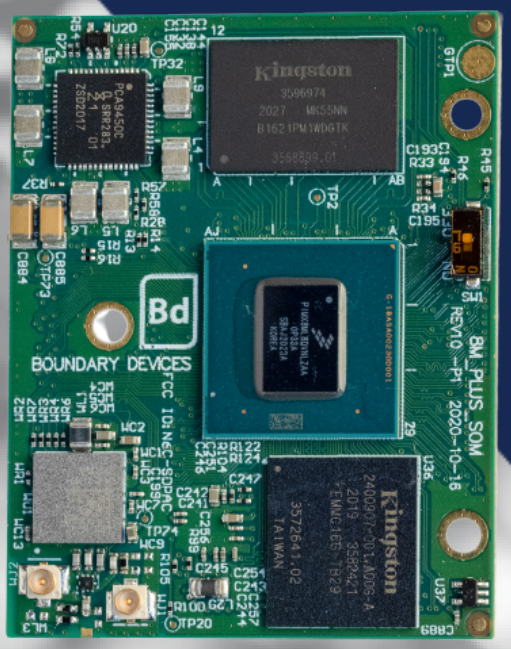
Nit8M_Plus_SOM

Product Manual

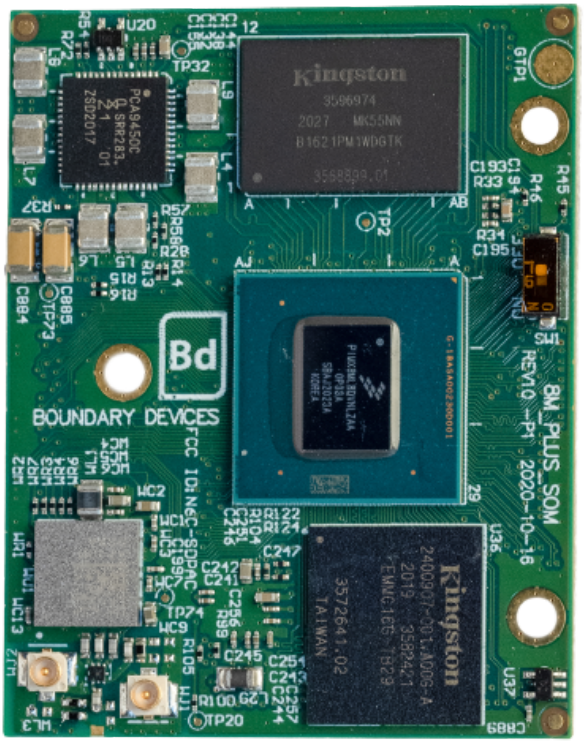


Boundary Devices

Nit8M_Plus_SOM

Product Manual

REVISION HISTORY		
Date	**Revision**	**Description**
7/17/2020	0.1	First Draft
1/5/2021	0.2	Minor Modifications
8/16/2021	0.3	Audio codec details - Boot mode addition
10/22/2021	0.4	Various Wi-Fi updates
4/21/2022	0.5	Update CPU freq + mechanical drawings
10/25/2022	0.6	Added 4GB version ordering information
02/01/2023	0.7	Fix J4-79 pin, add screw info



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1. OVERVIEW

1.1. GENERAL INFORMATION

The Nitrogen8 family of SBCs and SOMs are the latest in Boundary Device's i.MX based embedded computing solutions.

The different Nitrogen8 members of SBCs and SOMs are designed to best leverage the advantages of the i.MX8M, i.MX8M Mini, i.MX8M Nano, and i.MX8M Plus applications processors to fit a variety of embedded and IoT applications including: industrial automation, aviation & aerospace, HMI, industrial control, robotics, building control, digital displays, infotainment, telematics, Machine Learning, AI, and more.

The Nit8M_Plus_SOM is designed for mass production use with a guaranteed 10 year life span, FCC Pre-scan results, and a stable supply chain. Industrial temperature and conformal coating options are available.

1.2. SOFTWARE SUPPORT

Boundary Devices provides a full Board Support Package (BSP) for all Nitrogen boards.
The BSP includes boot loader, kernel and user-space components optimized for each platform.

The boards ship with U-Boot, Linux Kernel as well as an Ubuntu operating system.

Industry leading OS-Level support can be found on the Boundary Devices website via the Blog and Wiki. You can also find images for the latest versions of popular OS supported by the Nitrogen platforms including: Yocto, Buildroot, Ubuntu, Debian, Android, QNX, and FreeRTOS.

Boundary Devices does not provide application development or support, but does have a large list of software partners who can. You can browse our partners at https://boundarydevices.com/support.

1.2.1 U-BOOT CONFIGURATION

The U-Boot configuration isn't carrier specific, so it only depends on your SOM configuration:

- nitrogen8mp_2g_defconfig: for Nitrogen8M Plus SOM with 2G of LPDDR4
- nitrogen8mp_4g_defconfig: for Nitrogen8M Plus SOM with 4G of LPDDR4

For more information about the build process, please refer to this blog post:
https://boundarydevices.com/u-boot-2020-10-for-i-mx-platforms/

1.2.2 LINUX DEVICE TREE

Although the EVK and ENC carriers are close to each other, some features are only enabled on the ENC version of the device tree:

- imx8mp-nitrogen8mp.dts: default dts for EVK carrier
- imx8mp-nitrogen8mp-enc.dts: dts for ENC carrier

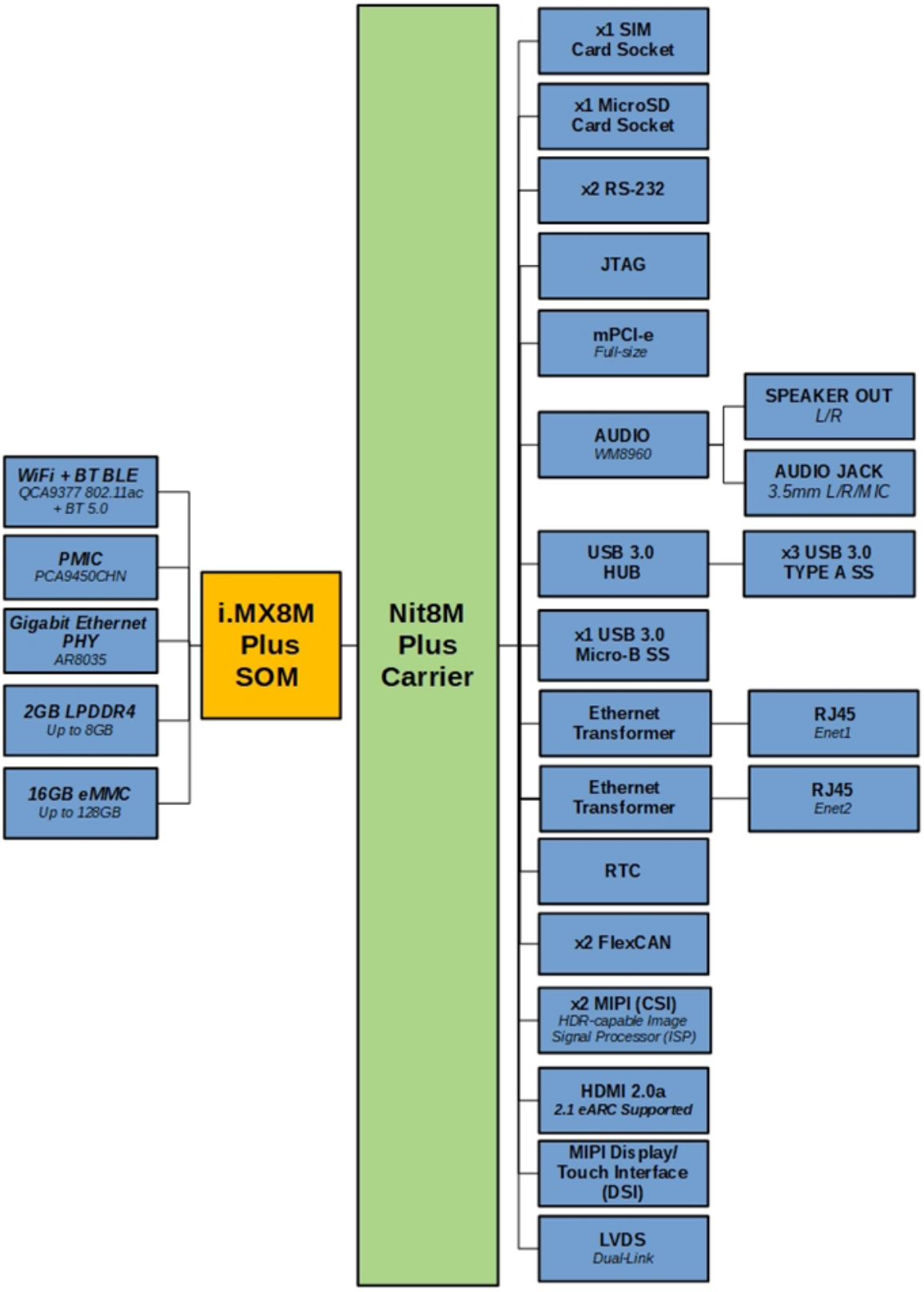
1.3. FEATURE SUMMARY

The Nit8M Plus System on Modules (SOM) is the latest in our line of i.MX based Nitrogen platform. Built with industry-leading audio, voice and video processing, the i.MX8M applications processor series of processors is ideal for applications scaling from consumer home audio to industrial building automation and mobile computers. The Nit8M Plus platform will include a robust set of populated attributes, allowing them to be embedded in a variety of applications.

Key Features of the Nit8M Plus Series:

- 4xCortex-A53 + Cortex-M7 integrated with a Neural Processing Unit (NPU) of 2.25 TOPS
    - Keyword detect, noise reduction, beamforming
    - Speech recognition (i.e. Deep Speech 2)
    - Image recognition (i.e. ResNet-50)
- 2-8GB of LPDDR4 RAM
- 16-128GB of eMMC
- Two 4-lane MIPI-CSI Camera Inputs
- HDR-capable Image Signal Processor (ISP), supporting up to two cameras:
    - When one camera is used, supports up to 12MP@30fps or 4kp45
    - When two cameras are used, each supports up to 1080p80
- One Dual-Link LVDS Interface (2 x 4lane)
- One 4-Lane MIPI-DSI Display (up to 1080p)
- HDMI 2.0a Tx up to 1080p60 or 4k30, 2.1 eARC supported
- High Performance GPU3D (GC7000UL), 2D Graphics (GC520L)
- Hifi4 Audio DSP, operating up to 800 MHz
- One PCI Express (PCIe): Single lane supporting PCIe Gen 3
- Two USB3.0 Host Controllers
    - Three USB 3.0 Host via USB Hub, USB 3.0 OTG (via Carrier)
- Three Ultra Secure Digital Host Controller (uSDHC) interfaces
    - 1 used for WiFi
    - 1 used for eMMC
    - 1 exposed to Carrier board
- Two Ethernet controllers, capable of simultaneous operation:
    - One Gigabit Ethernet controller with support for EEE, Ethernet AVB and IEEE1588
    - One Gigabit Ethernet controller with support for TSN, EEE, and Ethernet AVB
- Two Controller Area Network (FlexCAN) modules, each optionally supporting flexible data-rate (FD)
- Four universal asynchronous receiver/transmitter (UART) modules
- Six I2C modules

1.4. BLOCK DIAGRAM

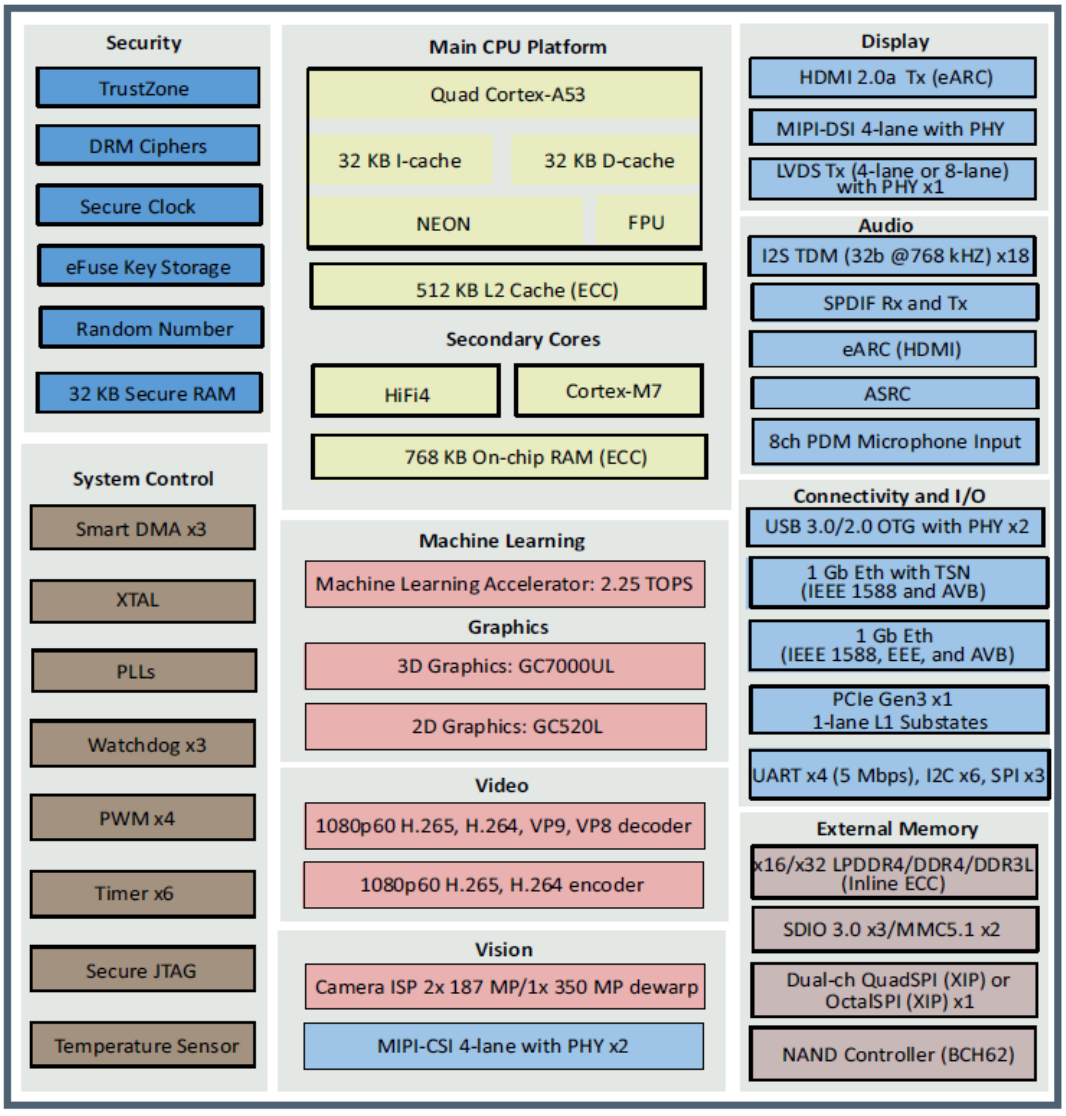


1.5. NXP I.MX 8M PLUS PROCESSOR

1.5.1. OVERVIEW

The i.MX 8M Plus is a powerful quad Arm® Cortex ®-A53 processor, with speed up to 1.8 GHz for C-Temp and 1.6 GHz for I-Temp, integrated with a Neural Processing Unit (NPU) of 2.25 TOPS that greatly accelerate machine learning inference. The vision engine is composed of two camera inputs and a HDR-capable Image Signal Processor (ISP) capable of 350 MPixels/s.The advanced multimedia capabilities include 1080p60video encode and decode H.265 and H.264. A 3D and 2D graphic acceleration supporting 1 GPixel/s, OpenVG 1.1, Open GL ES3.1, Vulkan, and Open CL 1.2 FP. Multiple audio and microphone interfaces for Immersive Audio and Voice systems. For industrial applications, real time control is enabled by an integrated 800 MHz Arm® Cortex®-M7. Robust control networks are possible via CAN-FD interfaces. And a dual Gb Ethernet, one supporting Time Sensitive Networking (TSN), drive gateway applications with low latency. High industrial system reliability for safety is leveraged by DRAM Inline ECC as well as ECC support on internal software-accessible SRAMs.

1.5.2. i.MX 8M PLUS BLOCK DIAGRAM



1.5.3. CPU

The i.MX 8M Plus applications processor represents NXP's latest video and audio experience combining state-of-the-art media-specific features with high-performance processing while optimized for lowest power consumption:

- Arm Cortex-A53 MPCore platform
- Quad symmetric Cortex-A53 processors :
  - 32 KB L1 Instruction Cache
  - 32 KB L1 Data Cache
  - Media Processing Engine (MPE) with NEON technology supporting the Advanced Single Instruction Multiple Data architecture:
  - Floating Point Unit (FPU) with support of the VFPv4-D16 architecture
  - Support of 64-bit Armv8-A architecture
  - 512 KB unified L2 cache

- Arm Cortex-M7 core platform operating up to 800MHz
  - 32 KB L1 Instruction Cache
  - 32 KB L1 Data Cache
  - 256 KB tightly coupled memory (TCM)

- Low power microcontroller available for customer application
  - Low power standby mode
  - IoT features including Weave
  - Manage IR or Wireless Remote
  - ML Applications

1.5.4. MEMORY

The on-chip memory system consists of the following:

- Boot ROM (256KB)
- On-chip RAM (512KB + 32KB) with ECC support

The external memory interfaces supported on this chip include:

- 16/32-bit DRAM Interface:
  - LPDDR4-3200 to 4266
- eMMC 5.1 FLASH (2 interfaces)
- SPI NOR FLASH (3 interfaces)
- 8-bit NAND FLASH, including support for Raw MLC/SLC devices, BCH ECC up to 62-bit, and ONFi3.2 compliance (clock rates up to 100 MHz and data rates up to 200 MB/sec)
- FlexSPI FLASH with support for XIP (for Cortex-M7 in low-power mode) and support for either one Octal SPI, or parallel read mode of two identical Quad SPI FLASH devices

The i.MX8M Plus supports the following boot devices:

- NAND FLASH (including SLC and MLC)
- SDIO / MMC / SDXC
- eSD 3.0/eMMC 5.1 (fast boot)
- SPI Serial Flash
- USB
- QSPI Ethernet (via plug-in mode)

1.5.5. DISPLAY

The chip has the following display support:

Three LCDIF Display Controllers:

- One LCDIF drives MIPI DSI
- One LCDIF drives LVDS Tx
- One LCDIF drives HDMI Tx
- Supports 8-bit / 16-bit / 18-bit / 24-bit / 32-bit pixel depth
- Supports up to 1080p60 display per LCDIF, if no more than 2 instances used
- simultaneously
- Supports 1x1080p60 + 2x720p60 if all 3 instances used simultaneously
- Supports one layer

MIPI Interface:

- One 4-lane MIPI DSI interface
- Two 4-lane MIPI CSI interface

Two 4-Lane LVDS Interfaces

ISI (Image Sensor Interface):

- The ISI is a simple camera interface that supports image processing and transfer via a bus master interface for up to 2 cameras

Two ISP supporting 375Mpixel/s aggregate performance and up to 3-exposure HDR processing:

- When one camera is used, supports up to 12MP@30fps or 4kp45
- When two cameras are used, each supports up to 1080p80

HDMI 2.0a

- HDMI 2.0a Tx supporting one display
- Resolutions of: 740x480p60, 720x480p60, 1280x720p60, 1920x1080p60, 4k30
- HDCP 2.2 and HDCP 1.4
    - Audio support
        - 32 channel audio output support
        - 1 S/PDIF audio eARC input support

1.5.6. GRAPHICS PROCESSING UNIT

The chip incorporates the following Graphics Processing Unit (GPU) features:

- 2D/3D acceleration
- Supports OpenGL ES 1.1, 2.0, 3.0
- Supports OpenCL 1.2
- Supports Vulkan
- Supports multi-source composition
- Supports one-pass filter
- Supports tile format

1.5.7. VIDEO PROCESSING UNIT

The chip incorporates the following Video Processing Unit (VPU) features:

- VP9 Profile 0, 2 (10 bit) decoder (VPU G2)
- HEVC/H.265 Main/Main10 Profile (up to level 5.1) decoder (VPU G2)
- AVC/H.264 Baseline, Main, High decoder (VPU G1)
- VP8 decoder (VPU G1)
- AVC/H.264 encoder
- HEVC/H.265 Encoder

1.5.8. MACHINE LEARNING: NPU (NEURAL PROCESSING UNIT)

- 2.25 TOP/s Neural Network performance available for user applications
  - Keyword detect, noise reduction, beamforming
  - Speech recognition (i.e. Deep Speech 2)
  - Image recognition (i.e. ResNet-50

2. CONNECTOR DETAILS

2.1. CUSTOM CONNECTORS

J4: 100 Pin Board to Carrier Board Connector Interface Connector P/N: Hirose - DF40C-100DP-0.4V(51) Mating Connector P/N: Hirose -DF40C-100DS-0.4V(51)				
PIN#	**SOM Signal**	**SOM Voltage Domain**	**Voltage Level**	**Comments**
1	GND	-	Ground	
2	GND	-	Ground	
3	CSI1_D3_P	VDD_MIPI_1P8	1.8V	CSI
4	CSI2_D0_P	VDD_MIPI_1P8	1.8V	CSI
5	CSI1_D3_N	VDD_MIPI_1P8	1.8V	CSI
6	CSI2_D0_N	VDD_MIPI_1P8	1.8V	CSI
7	GND	-	Ground	
8	GND	-	Ground	
9	CSI1_D2_P	VDD_MIPI_1P8	1.8V	CSI
10	CSI2_D1_P	VDD_MIPI_1P8	1.8V	CSI
11	CSI1_D2_N	VDD_MIPI_1P8	1.8V	CSI
12	CSI2_D1_N	VDD_MIPI_1P8	1.8V	CSI
13	GND	-	Ground	
14	GND	-	Ground	
15	CSI1_CK_P	VDD_MIPI_1P8	1.8V	CSI
16	CSI2_CK_P	VDD_MIPI_1P8	1.8V	CSI
17	CSI1_CK_N	VDD_MIPI_1P8	1.8V	CSI
18	CSI2_CK_N	VDD_MIPI_1P8	1.8V	CSI
19	GND	-	Ground	
20	GND	-	Ground	
21	CSI1_D1_P	VDD_MIPI_1P8	1.8V	CSI
22	CSI2_D2_P	VDD_MIPI_1P8	1.8V	CSI
23	CSI1_D1_N	VDD_MIPI_1P8	1.8V	CSI
24	CSI2_D2_N	VDD_MIPI_1P8	1.8V	CSI
25	GND	-	Ground	
26	GND	-	Ground	
27	CSI1_D0_P	VDD_MIPI_1P8	1.8V	CSI
28	CSI2_D3_P	VDD_MIPI_1P8	1.8V	CSI
29	CSI1_D0_N	VDD_MIPI_1P8	1.8V	CSI
30	CSI2_D3_N	VDD_MIPI_1P8	1.8V	CSI
31	GND	-	Ground	
32	GND	-	Ground	
33	PCIE_REFCLK_P	VDD_PCI_1P8	1.8V	PCIE
34	DSI_D3_P	VDD_MIPI_1P8	1.8V	
35	PCIE_REFCLK_N	VDD_PCI_1P8	1.8V	PCIE

36	DSI_D3_N	VDD_MIPI_1P8	1.8V	
37	GND	-	Ground	
38	GND	-	Ground	
39	PCIE_TX_P	VDD_PCI_1P8	1.8V	PCIE
40	DSI_D2_P	VDD_MIPI_1P8	1.8V	
41	PCIE_TX_N	VDD_PCI_1P8	1.8V	PCIE
42	DSI_D2_N	VDD_MIPI_1P8	1.8V	
43	GND	-	Ground	
44	GND	-	Ground	
45	PCIE_RX_P	VDD_PCI_1P8	1.8V	PCIE
46	DSI_CK_P	VDD_MIPI_1P8	1.8V	
47	PCIE_RX_N	VDD_PCI_1P8	1.8V	PCIE
48	DSI_CK_N	VDD_MIPI_1P8	1.8V	
49	GND	-	Ground	
50	GND	-	Ground	
51	USB2_TX_P	VDD_USB_3P3	3.3V	USB
52	DSI_D1_P	VDD_MIPI_1P8	1.8V	
53	USB2_TX_N	VDD_USB_3P3	3.3V	USB
54	DSI_D1_N	VDD_MIPI_1P8	1.8V	
55	GND	-	Ground	
56	GND	-	Ground	
57	USB2_RX_P	VDD_USB_3P3	3.3V	USB
58	DSI_D0_P	VDD_MIPI_1P8	1.8V	
59	USB2_RX_N	VDD_USB_3P3	3.3V	USB
60	DSI_D0_N	VDD_MIPI_1P8	1.8V	
61	GND	-	Ground	
62	GND	-	Ground	
63	USB2_D_P	VDD_USB_3P3	3.3V	USB
64	USB1_VBUS_3V3	VDD_USB_3P3	3.3V	USB
65	USB2_D_N	VDD_USB_3P3	3.3V	USB
66	USB1_ID	VDD_USB_3P3	3.3V	USB
67	GND	-	Ground	
68	GND	-	Ground	
69	USB2_VBUS_3V3	VDD_USB_3P3	3.3V	USB
70	USB1_TX_P	VDD_USB_3P3	3.3V	USB
71	USB2_ID	VDD_USB_3P3	3.3V	USB
72	USB1_TX_N	VDD_USB_3P3	3.3V	USB
73	GPIO1_IO11	NVCC_GPIO1	3.3V	
74	GND	-	Ground	
75	GPIO1_IO01	NVCC_GPIO1	3.3V	
76	USB1_RX_P	VDD_USB_3P3	3.3V	USB
77	GPIO1_IO07	NVCC_GPIO1	3.3V	

78	USB1_RX_N	VDD_USB_3P3	3.3V	USB
79	NC	-	NC	
80	GND	-	Ground	
81	GPIO1_IO04	NVCC_GPIO1	3.3V	
82	USB1_D_P	VDD_USB_3P3	3.3V	USB
83	GPIO1_IO10	NVCC_GPIO1	3.3V	
84	USB1_D_N	VDD_USB_3P3	3.3V	USB
85	GPIO1_IO13/USB1_OC	NVCC_GPIO1	3.3V	
86	GND	-	Ground	
87	GPIO1_IO12	NVCC_GPIO1	3.3V	
88	GPIO1_IO08	NVCC_GPIO1	3.3V	
89	GND	-	Ground	
90	GPIO1_IO09	NVCC_GPIO1	3.3V	
91	GPIO1_IO15/USB2_OC	NVCC_GPIO1	3.3V	
92	UART2_TXD	NVCC_I2C_UART	3.3V	
93	GPIO1_IO14	NVCC_GPIO1	3.3V	
94	UART2_RXD	NVCC_I2C_UART	3.3V	
95	GND	-	Ground	
96	GND	-	Ground	
97	GPIO1_IO05	NVCC_GPIO1	3.3V	
98	UART4_TXD	NVCC_I2C_UART	3.3V	
99	GPIO1_IO06	NVCC_GPIO1	3.3V	
100	UART4_RXD	NVCC_I2C_UART	3.3V	

J5: 100 Pin Board to Carrier Board Connector Interface Connector P/N: Hirose - DF40C-100DP-0.4V(51) Mating Connector P/N: Hirose -DF40C-100DS-0.4V(51)				
PIN#	SOM Signal	SOM Voltage Domain	Voltage Level	Comments
1	+5V	-	5V Power	
2	+5V	-	5V Power	
3	+5V	-	5V Power	
4	+5V	-	5V Power	
5	+5V	-	5V Power	
6	+5V	-	5V Power	
7	+5V	-	5V Power	
8	+5V	-	5V Power	
9	+5V	-	5V Power	
10	+5V	-	5V Power	
11	GND	-	Ground	
12	GND	-	Ground	
13	GND	-	Ground	
14	GND	-	Ground	

15	GND	-	Ground	
16	GND	-	Ground	
17	BOOT_MODE1	NVCC_JTAG	3.3V	
18	TP73	-	-	
19	SYS_RESETn	PMIC_RST_B	3.3V	
20	SAI1_RXFS	NVCC_SAI1_SAI5	3.3V	
21	I2C2_SCL	NVCC_I2C_UART	3.3V	
22	SAI1_RXC	NVCC_SAI1_SAI5	3.3V	
23	I2C2_SDA	NVCC_I2C_UART	3.3V	
24	SAI1_RXD0	NVCC_SAI1_SAI5	3.3V	
25	GND	-	Ground	
26	SAI1_RXD1	NVCC_SAI1_SAI5	3.3V	
27	I2C3_SCL	NVCC_I2C_UART	3.3V	
28	SAI1_RXD2	NVCC_SAI1_SAI5	3.3V	
29	I2C3_SDA	NVCC_I2C_UART	3.3V	
30	SAI1_RXD3	NVCC_SAI1_SAI5	3.3V	
31	I2C4_SCL	NVCC_I2C_UART	3.3V	
32	GND	-	Ground	
33	I2C4_SDA	NVCC_I2C_UART	3.3V	
34	SAI1_RXD4	NVCC_SAI1_SAI5	3.3V	
35	SAI5_RXFS	NVCC_SAI1_SAI5	3.3V	
36	SAI1_RXD5	NVCC_SAI1_SAI5	3.3V	
37	SAI5_RXC	NVCC_SAI1_SAI5	3.3V	
38	SAI1_RXD6	NVCC_SAI1_SAI5	3.3V	
39	GND	-	Ground	
40	SAI1_RXD7	NVCC_SAI1_SAI5	3.3V	
41	SAI5_MCLK	NVCC_SAI1_SAI5	3.3V	
42	GND	-	Ground	
43	GND	-	Ground	
44	SAI1_TXC	NVCC_SAI1_SAI5	3.3V	
45	SAI5_RXD3	NVCC_SAI1_SAI5	3.3V	
46	GND	-	Ground	
47	SAI5_RXD2	NVCC_SAI1_SAI5	3.3V	
48	SAI1_TXD0	NVCC_SAI1_SAI5	3.3V	
49	SAI5_RXD1	NVCC_SAI1_SAI5	3.3V	
50	SAI1_TXD1	NVCC_SAI1_SAI5	3.3V	
51	SAI5_RXD0	NVCC_SAI1_SAI5	3.3V	
52	SAI1_TXD2	NVCC_SAI1_SAI5	3.3V	
53	GND	-	Ground	
54	SAI1_TXD3	NVCC_SAI1_SAI5	3.3V	
55	SPDIF_TX	NVCC_SAI2_SAI3_SPDIF	3.3V	
56	SAI1_TXD4	NVCC_SAI1_SAI5	3.3V	

57	SPDIF_RX	NVCC_SAI2_SAI3_SPDIF	3.3V	
58	SAI1_TXD5	NVCC_SAI1_SAI5	3.3V	
59	GND	-	Ground	
60	SAI1_TXD6	NVCC_SAI1_SAI5	3.3V	
61	SPDIF_EXT_CLK	NVCC_SAI2_SAI3_SPDIF	3.3V	
62	SAI1_TXD7	NVCC_SAI1_SAI5	3.3V	
63	GND	-	Ground	
64	SAI1_TXFS	NVCC_SAI1_SAI5	3.3V	
65	EARC_P_UTIL	VDD_EARC_1P8	1.8V	
66	GND	-	Ground	
67	HDMI_DDC_SCL	NVCC_ECSPI_HDMI	3.3V	
68	SAI1_MCLK	NVCC_SAI1_SAI5	3.3V	
69	HDMI_DDC_SDA	NVCC_ECSPI_HDMI	3.3V	
70	GND	-	Ground	
71	HDMI_HPD	NVCC_ECSPI_HDMI	3.3V	
72	ECSPI2_MOSI	NVCC_ECSPI_HDMI	3.3V	
73	HDMI_CEC	NVCC_ECSPI_HDMI	3.3V	
74	ECSPI2_MISO	NVCC_ECSPI_HDMI	3.3V	
75	GND	-	Ground	
76	ECSPI2_CS0	NVCC_ECSPI_HDMI	3.3V	
77	HDMI_TXC_N	VDD_HDMI_1P8	1.8V	
78	GND	-	Ground	
79	HDMI_TXC_P	VDD_HDMI_1P8	1.8V	
80	ECSPI2_SCLK	NVCC_ECSPI_HDMI	3.3V	
81	GND	-	Ground	
82	GND	-	Ground	
83	HDMI_TX0_N	VDD_HDMI_1P8	1.8V	
84	EARC_AUX	VDD_EARC_1P8	1.8V	
85	HDMI_TX0_P	VDD_HDMI_1P8	1.8V	
86	EARC_N_HPD	VDD_EARC_1P8	1.8V	
87	GND	-	Ground	
88	GND	-	Ground	
89	HDMI_TX1_N	VDD_HDMI_1P8	1.8V	
90	UART3_RXD/ECSPI1_SCLK	NVCC_ECSPI_HDMI	3.3V	
91	HDMI_TX1_P	VDD_HDMI_1P8	1.8V	
92	GND	-	Ground	
93	GND	-	Ground	
94	UART3_TXD/ECSPI1_MOSI	NVCC_ECSPI_HDMI	3.3V	
95	HDMI_TX2_N	VDD_HDMI_1P8	1.8V	
96	UART3_CTS/ECSPI1_MISO	NVCC_ECSPI_HDMI	3.3V	
97	HDMI_TX2_P	VDD_HDMI_1P8	1.8V	
98	UART3_RTS/ECSPI1_CS0	NVCC_ECSPI_HDMI	3.3V	

99	GND	-	Ground	
100	GND	-	Ground	

J8: 100 Pin Board to Carrier Board Connector Interface Connector P/N: Hirose - DF40C-100DP-0.4V(51) Mating Connector P/N: Hirose -DF40C-100DS-0.4V(51)				
PIN#	**SOM Signal**	**SOM Voltage Domain**	**Voltage Level**	**Comments**
1	GND	-	Ground	
2	GND	-	Ground	
3	LVDS0_TX0_P	VDD_LVDS_1P8	1.8V	
4	LVDS1_TX0_P	VDD_LVDS_1P8	1.8V	
5	LVDS0_TX0_N	VDD_LVDS_1P8	1.8V	
6	LVDS1_TX0_N	VDD_LVDS_1P8	1.8V	
7	GND	-	Ground	
8	GND	-	Ground	
9	LVDS0_TX1_P	VDD_LVDS_1P8	1.8V	
10	LVDS1_TX1_P	VDD_LVDS_1P8	1.8V	
11	LVDS0_TX1_N	VDD_LVDS_1P8	1.8V	
12	LVDS1_TX1_N	VDD_LVDS_1P8	1.8V	
13	GND	-	Ground	
14	GND	-	Ground	
15	LVDS0_CLK_P	VDD_LVDS_1P8	1.8V	
16	LVDS1_CLK_P	VDD_LVDS_1P8	1.8V	
17	LVDS0_CLK_N	VDD_LVDS_1P8	1.8V	
18	LVDS1_CLK_N	VDD_LVDS_1P8	1.8V	
19	GND	-	Ground	
20	GND	-	Ground	
21	LVDS0_TX2_P	VDD_LVDS_1P8	1.8V	
22	LVDS1_TX2_P	VDD_LVDS_1P8	1.8V	
23	LVDS0_TX2_N	VDD_LVDS_1P8	1.8V	
24	LVDS1_TX2_N	VDD_LVDS_1P8	1.8V	
25	GND	-	Ground	
26	GND	-	Ground	
27	LVDS0_TX3_P	VDD_LVDS_1P8	1.8V	
28	LVDS1_TX3_P	VDD_LVDS_1P8	1.8V	
29	LVDS0_TX3_N	VDD_LVDS_1P8	1.8V	
30	LVDS1_TX3_N	VDD_LVDS_1P8	1.8V	
31	GND	-	Ground	
32	GND	-	Ground	
33	PMIC_ON_REQ	NVCC_S NVS_1P8	1.8V	
34	JTAG_TDO	N VCC_JTAG	3.3V	
35	ONOFF	NVCC_S NVS_1P8	1.8V	

36	JTAG_MOD	N VCC_JTAG	3.3V	
37	RSVD3	NVCC_NAND	1.8V	
38	JTAG_TMS	N VCC_JTAG	3.3V	
39	RSVD2	NVCC_NAND	1.8V	
40	JTAG_TDI	N VCC_JTAG	3.3V	
41	RSVD1	NVCC_NAND	1.8V	
42	JTAG_TCK	N VCC_JTAG	3.3V	
43	GND	-	Ground	
44	GND	-	Ground	
45	CLKIN1	NVCC_CLK	3.3V	
46	SD1_STROBE	NVCC_SD1	1.8V/3.3V	
47	GND	-	Ground	
48	SD1_RESET_B	NVCC_SD1	1.8V/3.3V	
49	CLKOUT1	NVCC_CLK	3.3V	
50	SD1_CMD	NVCC_SD1	1.8V/3.3V	
51	GND	-	Ground	
52	GND	-	Ground	
53	CLKIN2	NVCC_CLK	3.3V	
54	SD1_CLK	NVCC_SD1	1.8V/3.3V	
55	GND	-	Ground	
56	GND	-	Ground	
57	CLKOUT2	NVCC_CLK	3.3V	
58	SD1_DATA0	NVCC_SD1	1.8V/3.3V	
59	GND	-	Ground	
60	SD1_DATA1	NVCC_SD1	1.8V/3.3V	
61	SAI2_MCLK	NVCC_SAI2_SAI3_SPDIF	3.3V	
62	SD1_DATA2	NVCC_SD1	1.8V/3.3V	
63	GND	-	Ground	
64	SD1_DATA3	NVCC_SD1	1.8V/3.3V	
65	SAI2_RXD	NVCC_SAI2_SAI3_SPDIF	3.3V	
66	GND	-	Ground	
67	SAI2_TXC	NVCC_SAI2_SAI3_SPDIF	3.3V	
68	SD1_DATA4	NVCC_SD1	1.8V/3.3V	
69	SAI2_RXC	NVCC_SAI2_SAI3_SPDIF	3.3V	
70	SD1_DATA5	NVCC_SD1	1.8V/3.3V	
71	SAI2_TXD	NVCC_SAI2_SAI3_SPDIF	3.3V	
72	SD1_DATA6	NVCC_SD1	1.8V/3.3V	
73	SAI2_RXFS	NVCC_SAI2_SAI3_SPDIF	3.3V	
74	SD1_DATA7	NVCC_SD1	1.8V/3.3V	
75	SAI2_TXFS	NVCC_SAI2_SAI3_SPDIF	3.3V	
76	GND	-	Ground	
77	GND	-	Ground	

78	TRX0_P	-	Ethernet	
79	SAI3_MCLK	NVCC_SAI2_SAI3_SPDIF	3.3V	
80	TRX0_N	-	Ethernet	
81	GND	-	Ground	
82	GND	-	Ground	
83	SAI3_TXFS	NVCC_SAI2_SAI3_SPDIF	3.3V	
84	TRX1_P	-	Ethernet	
85	SAI3_RXD	NVCC_SAI2_SAI3_SPDIF	3.3V	
86	TRX1_N	-	Ethernet	
87	SAI3_RXC	NVCC_SAI2_SAI3_SPDIF	3.3V	
88	GND	-	Ground	
89	SAI3_TXD	NVCC_SAI2_SAI3_SPDIF	3.3V	
90	TRX2_P	-	Ethernet	
91	SAI3_RXFS	NVCC_SAI2_SAI3_SPDIF	3.3V	
92	TRX2_N	-	Ethernet	
93	SAI3_TXC	NVCC_SAI2_SAI3_SPDIF	3.3V	
94	GND	-	Ground	
95	RGMII_ACT		Ethernet	
96	TRX3_P	-	Ethernet	
97	RGMII_1000		Ethernet	
98	TRX3_N	-	Ethernet	
99	RGMII_10/100		Ethernet	
100	GND	-	Ground	

2.2. PIN MUXING

There are many pin muxing options on the i.MX8M Plus processor to change pins to GPIO, or other functions. If you need more GPIO, or need other signals, please contact us to discuss pin muxing options. Please also register on the NXP website to get the i.MX8M Plus reference manual.

3. SOM INTERFACES

3.1. DISPLAY INTERFACES

3.1.1 DSI

Nit8M_Plus_SOM MIPI DSI Host Controller supports One 4-lane MIPI DSI Interface

DSI SIGNALS (J4:100 PIN BOARD TO CARRIER BOARD CONNECTOR INTERFACE)

Pin #	Signal	Description
34	DSI_D3_P	Positive DSI Data3 Differential
36	DSI_D3_N	Negative DSI Data3 Differential
40	DSI_D2_P	Positive DSI Data2 Differential
42	DSI_D2_N	Negative DSI Data2 Differential
46	DSI_CK_P	Positive DSI Clock Differential
48	DSI_CK_N	Negative DSI Clock Differential
52	DSI_D1_P	Positive DSI Data1 Differential
54	DSI_D1_N	Negative DSI Data1 Differential
58	DSI_D0_P	Positive DSI Data0 Differential
60	DSI_D0_N	Negative DSI Data0 Differential

3.1.2 HDMI

HDMI SIGNALS (J5:100 PIN BOARD TO CARRIER BOARD CONNECTOR INTERFACE)

Pin #	Signal	Description
67	HDMI_DDC_SCL	Display Data Channel (DDC) Clock
69	HDMI_DDC_SDA	Display Data Channel (DDC) Data
71	HDMI_HPD	Hot Plug Detect (HPD)
73	HDMI_CEC	Consumer Electronics Control (CEC)
77	HDMI_TXC_N	Negative HDMI Clock
79	HDMI_TXC_P	Positive HDMI Clock
83	HDMI_TX0_N	Negative HDMI DATA0
85	HDMI_TX0_P	Positive HDMI DATA0
89	HDMI_TX1_N	Negative HDMI DATA1
91	HDMI_TX1_P	Positive HDMI DATA1
95	HDMI_TX2_N	Negative HDMI DATA2
97	HDMI_TX2_P	PositiveHDMI DATA2

3.1.3 LVDS

LVDS SIGNALS (J8:100 PIN BOARD TO CARRIER BOARD CONNECTOR INTERFACE)

Pin #	Signal	Description
3	LVDS0_TX0_P	Positive LVDS0 Data 0 Differential
4	LVDS1_TX0_P	Positive LVDS1 Data 0 Differential

5	LVDS0_TX0_N	Negative LVDS0 Data 0 Differential
6	LVDS1_TX0_N	Negative LVDS1 Data 0 Differential
9	LVDS0_TX1_P	Positive LVDS0 Data 1 Differential
10	LVDS1_TX1_P	Positive LVDS1 Data 1 Differential
11	LVDS0_TX1_N	Negative LVDS0 Data 1 Differential
12	LVDS1_TX1_N	Negative LVDS1 Data 1 Differential
15	LVDS0_CLK_P	Positive LVDS0 Clock Differential
16	LVDS1_CLK_P	Positive LVDS1 Clock Differential
17	LVDS0_CLK_N	Negative LVDS0 Clock Differential
18	LVDS1_CLK_N	Negative LVDS1 Clock Differential
21	LVDS0_TX2_P	Positive LVDS0 Data 2 Differential
22	LVDS1_TX2_P	Positive LVDS1 Data 2 Differential
23	LVDS0_TX2_N	Negative LVDS0 Data 2 Differential
24	LVDS1_TX2_N	Negative LVDS1 Data 2 Differential
27	LVDS0_TX3_P	Positive LVDS0 Data 3 Differential
28	LVDS1_TX3_P	Positive LVDS1 Data 3 Differential
29	LVDS0_TX3_N	Negative LVDS0 Data 3 Differential
30	LVDS1_TX3_N	Negative LVDS1 Data 3 Differential

3.2. CAMERA INTERFACES

3.2.1 MIPI CSI (Two instances of 4-lane MIPI CSI interface and HDR ISP)

MIPI CSI2 (four-lane)- This module provides one four-lane MIPI camera serial interfaces, which operates up to a maximum bit rate of 1.5 Gbps. The CSI-2 Host Controller is a digital core that implements all protocol functions defined in the MIPI CSI-2 specification, providing an interface between the system and the MIPI D-PHY, allowing communication with an MIPI CSI-2 compliant camera sensor.

MIPI CSI-2 SIGNALS (J4:100 PIN BOARD TO CARRIER BOARD CONNECTOR INTERFACE)

Pin #	Signal	Description
3	CSI1_D3_P	Positive CSI1 DATA3 Clock Differential
5	CSI1_D3_N	Negative CSI1 DATA3 Clock Differential
9	CSI1_D2_P	Positive CSI1 DATA2 Clock Differential
11	CSI1_D2_N	Negative CSI1 DATA2 Clock Differential
15	CSI1_CK_P	Positive Clock Differential
17	CSI1_CK_N	Negative Clock Differential
21	CSI1_D1_P	Positive CSI1 DATA1 Clock Differential
23	CSI1_D1_N	Negative CSI1 DATA1 Clock Differential
27	CSI1_D0_P	Positive CSI1 DATA0 Clock Differential
29	CSI1_D0_N	Negative CSI1 DATA0 Clock Differential

MIPI CSI-2 SIGNALS (J4:100 PIN BOARD TO CARRIER BOARD CONNECTOR INTERFACE)

Pin #	Signal	Description

4	CSI2_D0_P	Positive CSI2 DATA0 Clock Differential
6	CSI2_D0_N	Negative CSI2 DATA0 Clock Differential
10	CSI2_D1_P	Positive CSI2 DATA1 Clock Differential
12	CSI2_D1_N	Negative CSI2 DATA1 Clock Differential
16	CSI2_CK_P	Positive Clock Differential
18	CSI2_CK_N	Negative Clock Differential
22	CSI2_D2_P	Positive CSI2 DATA2 Clock Differential
24	CSI2_D2_N	Negative CSI2 DATA2 Clock Differential
28	CSI2_D3_P	Positive CSI2 DATA3 Clock Differential
30	CSI2_D3_N	Negative CSI2 DATA3 Clock Differential

3.3. GIGABIT ETHERNET

GIGABIT ETHERNET FEATURES:

Two Ethernet controllers (both capable of simultaneous operation):

- One Gigabit Ethernet controller with support for Energy Efficient Ethernet (EEE), Ethernet AVB, and IEEE 1588
- One Gigabit Ethernet controller with support for TSN in addition to EEE, Ethernet AVB

The Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. IEEE 1588 support can be added on the carrier board utilizing a different PHY than currently used on the Nit8MP_EVK_CAR. See the ENET and ENET_QOS chapters of the i.MX 8M Plus Applications Processor Reference Manual (IMX8MPRM) for details.

ENET_QOS Gigabit Ethernet:

Vendor	Part Number	Package
Qualcomm	AR8035-AL1A	PHY Transceiver (On SOM)
Amphenol	RJHSE-5381	RJ45 Ethernet Jack (On Carrier)
Link PP	LP5007NL	Ethernet Transformer (On Carrier)

ENET Gigabit Ethernet:

Vendor	Part Number	Package
Qualcomm	AR8035-AL1A	PHY Transceiver (On Carrier)
Amphenol	RJHSE-5381	RJ45 Ethernet Jack (On Carrier)
Link PP	LP5007NL	Ethernet Transformer (On Carrier)

ENET_QOS GIGABIT ETHERNET SIGNALS: (J8:100 PIN BOARD TO CARRIER BOARD CONNECTOR INTERFACE)

Pin #	Signal
78	TRX0_P
80	TRX0_N

84	TRX1_P
86	TRX1_N
90	TRX2_P
92	TRX2_N
95	RGMII_ACT
96	TRX3_P
97	RGMII_1000
98	TRX3_N
99	RGMII_10/100

ENET GIGABIT ETHERNET SIGNALS: (J5:100 PIN BOARD TO CARRIER BOARD CONNECTOR INTERFACE)

Pin #	Signal
28	SAI1_RXD2
30	SAI1_RXD3
34	SAI1_RXD4
36	SAI1_RXD5
38	SAI1_RXD6
40	SAI1_RXD7
44	SAI1_TXC
50	SAI1_TXD1
52	SAI1_TXD2
54	SAI1_TXD3
56	SAI1_TXD4
58	SAI1_TXD5
62	SAI1_TXD7
64	SAI1_TXFS
68	SAI1_MCLK

3.4. WI-FI & BLUETOOTH

The Nit8M_Plus_SOM contains WiFi+BT directly on the SOM using Silex SX-SDPAC package based upon the Qualcomm QCA9377-3 advanced 1x1 dual-band 802.11ac Wi-Fi + Bluetooth 5.0.

Features:

- IEEE802.11a/b/g/n/ac compatible (2.4 GHz, 5 GHz)
  - 5 GHz : Support 20/40/80 MHz bandwidth mode (Link rate 433 Mbps)
  - 2.4 GHz : Support 20/40 MHz bandwidth mode (Link rate 200 Mbps)
- Bluetooth 5.0 BR/EDR/LE Smart Ready compatible. Backward-compatible to BT 1.x, 2.x, 3.0, 4.0
- SDIO3.0 as the Wireless LAN host interface
- UART as the Bluetooth host interface
- u.FL connector for external antenna
- Worldwide acceptance: FCC (USA), IC (Canada), ETSI (Europe)
- Modular certification allows reuse of FCC ID and ETSI certification without repeating the expensive testing on end product

Note that both Wi-Fi and BT signals go through the WJ1 antenna connector.

3.5. USB 3.0

The USB module is a USB 3.0-compliant serial interface engine for implementing a USB interface. This module may be connected to an external port. Collectively the module and external port are called the USB 3.0 interface. USB 3.0 supports super-speed (SS), high-speed (HS), full-speed (FS), and low-speed (LS) operations.

The USB 3.0 module includes the following features:

- Complies with USB specification rev 3.0 (xHCI compatible)
- Supports operation as a standalone USB host controller
- USB dual-role operation and can be configured as host or device
- Super-speed (5 Gbit/s), high-speed (480 Mbit/s), full-speed (12 Mbit/s), and lowspeed (1.5 Mbit/s) operations.
- Supports operation as a standalone single port USB
- Supports four programmable, bidirectional USB endpoints
- OTG (on-the-go) 2.0 compliant, which includes both device and host capability. Super-speed operation is not supported when OTG is enabled.
- Supports system memory interface with -bit addressing capability

USB1 SIGNALS: (J4:100 PIN BOARD TO CARRIER BOARD CONNECTOR INTERFACE)

Pin #	Signal	Description
64	USB1_VBUS_3V3	USB1 3.0 VBUS Indicator (3.3V)
66	USB1_ID	USB1 ID /3.3V
70	USB1_TX_P	USB1 Transmit Data Positive
72	USB1_TX_N	USB1 Transmit Data Negative
76	USB1_RX_P	USB1 Receive Data Positive
78	USB1_RX_N	USB1 Receive Data Negative
82	USB1_D_P	Positive USB1 Data
84	USB1_D_N	Negative USB1 Data
85	GPIO1_IO13/USB1_OC	USB1 OTG Over Current

***Note*: On Boundary Devices Carrier board USB1 is configured as USB OTG**

USB 2 SIGNALS: (J4:100 PIN BOARD TO CARRIER BOARD CONNECTOR INTERFACE)

Pin #	Signal	Description
51	USB2_TX_P	USB2 Transmit Data Positive
53	USB2_TX_N	USB2 Transmit Data Negative
57	USB2_RX_P	USB2 Receive Data Positive
59	USB2_RX_N	USB2 Receive Data Negative
63	USB2_D_P	Positive USB2Data
65	USB2_D_N	Negative USB2Data
69	USB2_VBUS_3V3	USB2 3.0 VBUS Indicator (3.3V)
71	USB2_ID	USB2 ID /3.3V
91	GPIO1_IO15/USB2_OC	USB Over Current

***Note:* On Boundary Devices Carrier board USB2 is configured as USB HOST**

3.6. MMC/SD/SDIO

All the MMC/SD/SDIO controller IPs are based on the uSDHC IP.

They are designed to support:

- SD/SDIO standard, up to version 3.0.
- MMC standard, up to version 5.1.
- Support for SDXC (extended capacity)
- 1.8 V and 3.3 V operation, but do not support 1.2 V operation.
- 1-bit/4-bit SD and SDIO modes, 1-bit/4-bit/8-bit MMC mode.

Two uSDHC controllers (SDHC1 and SDHC3) can support up to an 8-bit interface, the other controller (SDHC2) can only support up to a 4-bit interface.

SDMMC1 SIGNALS: (J8:100 PIN BOARD TO CARRIER BOARD CONNECTOR INTERFACE)

Pin #	Signal	Description
46	SD1_STROBE	SD1 Data Strobe (SD1_CD)
48	SD1_RESET_B	Connect to SD2 Reset Pin on SD CARD
50	SD1_CMD	CMD Line Connect to Card
54	SD1_CLK	Clock
58	SD1_DATA0	SD1 Data 0 Line
60	SD1_DATA1	SD1 Data 1 Line
62	SD1_DATA2	SD1 Data 2 Line
64	SD1_DATA3	SD1 Data 3 Line
68	SD1_DATA4	SD1 Data 4 Line
70	SD1_DATA5	SD1 Data 5 Line
72	SD1_DATA6	SD1 Data 6 Line
74	SD1_DATA7	SD1 Data 7 Line

***Note:* SDIO does not require pull-ups**

3.7. AUDIO

The Nit8M_Plus_SOM features six external Synchronous Audio Interfaces (SAI) with different TX/RX lines supported. By default 1 SAI3 RX and TX is muxed:

AUDIO SIGNALS:(J8:100 PIN BOARD TO CARRIER BOARD CONNECTOR INTERFACE)

Pin #	Signal	Description
79	SAI3_MCLK	GPIO or SAI Audio 3.3V
83	SAI3_TXFS	GPIO or SAI Audio 3.3V
85	SAI3_RXD	GPIO or SAI Audio 3.3V
89	SAI3_TXD	GPIO or SAI Audio 3.3V
93	SAI3_TXC	GPIO or SAI Audio 3.3V

Our carriers include a WM8960CGEFL/V codec interfaces offering:

- Stereo HP out
- Lineout L/R
- Built-In 2W Amplifier

3.8. UART INTERFACES

All four UART interfaces are supported based on pin mux configurations of the UART interface.

UART Features:

- High-speed TIA/EIA-232-F compatible, up to Mbit/s
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s)
- 9-bit or Multidrop mode (RS-485) support (automatic slave address detection)
- 7 or 8 data bits for RS-232 characters, or 9 bit RS-485 format
- 1 or 2 stop bits
- Programmable parity (even, odd, and no parity)
- Hardware flow control support for request to send (RTS_B) and clear to send (CTS_B) signals
- RS-485 driver direction control via CTS_B signal
- Edge-selectable RTS_B and edge-detect interrupts
- Status flags for various flow control and FIFO states
- Voting logic for improved noise immunity (16x oversampling)
- Transmitter FIFO empty interrupt suppression
- UART internal clocks enable/disable
- Auto baud rate detection (up to 115.2 Kbit/s)
- Receiver and transmitter enable/disable for power saving
- RX_DATA input and TX_DATA output can be inverted respectively in RS-232/ RS-485 mode
- DCE/DTE capability
- RTS_B, IrDA asynchronous wake (AIRINT), receive asynchronous wake (AWAKE) interrupts wake the processor from STOP mode
- Maskable interrupts
- Two DMA Requests (TxFIFO DMA Request and RxFIFO DMA Request)
- Escape character sequence detection
- Software reset (SRST_B)
- Two independent, 32-entry FIFOs for transmit and receive
- The peripheral clock can be totally asynchronous with the module clock. The module clock determines baud rate. This allows frequency scaling on peripheral clock (such as during DVFS mode) while remaining the module clock frequency and baud rate

UART1 Signals: UART1 is RESERVED FOR BT Interface

Pin #	Signal	Description
-	UART1_RXD	BT_UART_TXD
-	UART1_TXD	BT_UART_RXD
-	UART1_CTS	BT_UART_CTS
-	UART_RTS	BT_UART_RTS

UART2 SIGNALS: (J4:100 PIN BOARD TO CARRIER BOARD CONNECTOR INTERFACE)

Pin #	Signal	Description
92	UART2_TXD	UART2 Transmit
94	UART2_RXD	UART2 Receive

***Note:* UART2 is used as default boot debug port. (Console/Debug Port)**

UART3 SIGNALS: (J5:100 PIN BOARD TO CARRIER BOARD CONNECTOR INTERFACE)

Pin #	Signal	Description
90	UART3_RXD/ECSPI1_SCLK	UART3 Receive
94	UART3_TXD/ECSPI1_MOSI	UART3 Transmit
96	UART3_CTS/ECSPI1_MISO	UART3 HW Flow Control CTS
98	UART3_RTS/ECSPI1_CS0	UART3 HW Flow Control RTS

UART4 SIGNALS:(J4:100 PIN BOARD TO CARRIER BOARD CONNECTOR INTERFACE)

Pin #	Signal	Description
98	UART4_TXD	UART4 Transmit
100	UART4_RXD	UART4 Receive

3.9. FLEXIBLE SPI

FlexSPI Flash with support for XIP (for Cortex®-M7 in low-power mode) and support for either one Octal SPI, or parallel read mode of two identical Quad SPI FLASH devices. It also supports both Serial NOR and Serial NAND flash using the FlexSPI.

FlexSPI block supports following features:

- Flexible sequence engine (LUT table) to support various vendor devices
- Serial NOR Flash or other device with similar SPI protocol as Serial NOR Flash
- Serial NAND Flash
- HyperBus device (HyperFlash/HyperRAM)
- FPGA device
- Flash access mode
- Single/Dual/Quad/Octal mode
- SDR/DDR mode
- Individual/Parallel mode
- Supports sampling clock mode:
- Internal dummy read strobe loopbacked internally
- Internal dummy read strobe loopbacked from pad
- Flash provided read strobe
- Automatic Data Learning to select correct sample clock phase
- Memory mapped read/write access by AHB Bus
- AHB RX Buffer implemented to reduce read latency. Total AHB RX Buffer size: 256 * 64 Bits
- 16 AHB masters supported with priority for read access
- 8 flexible and configurable buffers in AHB RX Buffer
- AHB TX Buffer implemented to buffer all write data from one AHB burst. AHB
- TX Buffer size: 8 * 64 Bits
- All AHB masters share this AHB TX Buffer. No AHB master number limitation for Write Access.
- Software triggered Flash read/write access by IP Bus
- IP RX FIFO implemented to buffer all read data from External device. FIFO size: 64 * 64 Bits
- IP TX FIFO implemented to buffer all Write data to External device. FIFO size: 128 * 64 Bits
- DMA support to fill IP TX FIFO
- DMA support to read IP RX FIFO

- SCLK stopped when reading flash data and IP RX FIFO is full
- SCLK stopped when writing flash data and IP TX FIFO is empty

3.10. ECSPI KEY FEATURES

The Enhanced Configurable Serial Peripheral Interface (ECSPI) is a Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. Configurable to support Master/Slave modes.

Key features of the ECSPI include:

- Full-duplex synchronous serial interface
- Master/slave configurable
- One chip select (SS) signal
- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 64-entry FIFO for both transmitting and receiving data
- Polarity and phase of the chip select (SS) and SPI clock (SCLK) are configurable
- Direct Memory Access (DMA)support
- Refer to the product data sheet for the maximum operating frequency

SPI IS MUXED WITH SD2 AND IS SUPPORTED AS FOLLOWS:

Signal	USDHC1	USDHC2	USDHC3
CD_B	GPIO1_IO06.alt5	SD2_CD_B.alt0	NAND_DATA02.alt2
CLK	SD1_CLK.alt0	SD2_CLK.alt0	NAND_WE_B.alt2
CMD	SD1_CMD.alt0	SD2_CMD.alt0	NAND_WP_B.alt2
DATA0	SD1_DATA0.alt0	SD2_DATA0.alt0	NAND_DATA04.alt2
DATA1	SD1_DATA1.alt0	SD2_DATA1.alt0	NAND_DATA05.alt2
DATA2	SD1_DATA2.alt0	SD2_DATA2.alt0	NAND_DATA06.alt2
DATA3	SD1_DATA3.alt0	SD2_DATA3.alt0	NAND_DATA07.alt2
DATA4	SD1_DATA4.alt0	-	NAND_RE_B.alt2
DATA5	SD1_DATA5.alt0	-	NAND_CE2_B.alt2
DATA6	SD1_DATA6.alt0	-	NAND_CE3_B.alt2
DATA7	SD1_DATA7.alt0	-	NAND_CLE.alt2
RESET_	SD1_RESET_B.alt0	SD2_RESET_B.alt0	GPIO1_IO09.alt4
STROBE	SD1_STROBE.alt0	-	NAND_CE1_B.alt2
VSELECT	GPIO1_IO03.alt1	GPIO1_IO04.alt1	GPIO1_IO11.alt4
WP	GPIO1_IO07.alt5	SD2_WP.alt0	NAND_DATA03.alt2

3.11. PCIE

Nit8M_Plus_SOM PCI Express functionality has the following parts:

- One PCIe Express (PCIe) Single Lane supporting PCIe Gen3
- Dual Mode operation to function as root complex or endpoint
- Integrated PHY interface
- Supports L1 low power sub-state

This PCI Express dual mode (DM) controller provides a solution to implement a PCI Express port for a PCI Express root complex or endpoint application. A complete PCI Express port solution includes the controller, an analog PHY macro, and application logic to source and sink data.

PCIE SIGNALS: (J8:100 PIN BOARD TO CARRIER BOARD CONNECTOR INTERFACE)

Pin #	Signal	Description
71	SAI3_RXD/PCIE_DIS	Disable PCIE Signal 3.3V
87	SAI2_RXC/PCIE_RST	Reset PCIE Module 3.3V

PCIE SIGNALS: (J4:100 PIN BOARD TO CARRIER BOARD CONNECTOR INTERFACE)

Pin #	Signal	Description
33	PCIE_REFCLK_P	Positive PCIE Clock
35	PCIE_REFCLK_N	Negative PCIE Clock
39	PCIE_TX_P	Positive PCI TX Differential
41	PCIE_TX_N	Negative PCI TX Differential
45	PCIE_RX_P	Positive PCI RX Differential
47	PCIE_RX_N	Negative PCI RX Differential

3.12. I2C

Six I2C Interface connectivity peripherals provide serial interface for external devices.

The I2C operates primarily in two functional modes: Standard mode and Fast mode.

- In Standard mode, I2C supports the data transfer rates up to 100 kbits/s.
- In Fast mode, data transfer rates up to 400 kbits/s can be achieved. Per blockoperation, there is no special configuration required for Fast or Standard mode. It is the data transfer rate that distinguishes Standard and Fast mode.

I2C1 SIGNALS: I2C1 IS RESERVED FOR PMIC

I2C2 SIGNALS: (J5:100 PIN BOARD TO CARRIER BOARD CONNECTOR INTERFACE)

Pin #	Signal	Description
21	I2C2_SCL	I2C Signal
23	I2C2_SDA	I2C Signal

I2C3 SIGNALS: (J5:100 PIN BOARD TO CARRIER BOARD CONNECTOR INTERFACE)

Pin #	Signal	Description
27	I2C3_SCL	I2C Signal
29	I2C3_SDA	I2C Signal

I2C4 SIGNALS: (J5:100 PIN BOARD TO CARRIER BOARD CONNECTOR INTERFACE)

Pin #	Signal	Description
31	I2C4_SCL	I2C Signal
33	I2C4_SDA	I2C Signal

I2C5 SIGNALS:SIGNALS NOT EXPOSED ON NIT8M_PLUS_CARRIER

***Note:** Please contact us for pin muxing options*

I2C6 SIGNALS:SIGNALS NOT EXPOSED ON NIT8M_PLUS_CARRIER

***Note:** Please contact us for pin muxing options*

3.13. GENERAL PURPOSE I/O

Most of the SOM's IO pins can be used as GPIOs. If you need more GPIO, or need other signals, please contact us to discuss pin muxing options.

3.14. GENERAL SYSTEM CONTROL

3.14.1. RESET

'0' logic will reset Nit8M_Plus_SOM

3.14.2. BOOT MODE

The SW1 switch on the SoM forces the USB Serial Download boot mode (BOOT_MODE[0]).
Make sure to read this article when using that mode: Recovery i.MX platforms using UUU.

3.15. REFERENCE CLOCK OUT

Nit8M_Plus_SOM output clock is controlled by the i.MX8 Plus CCM module. Please refer to the i.MX8 Plus User Manual regarding the configuration option for this clock.

3.16. POWER

3.16.1. POWER SUPPLY

Pin #	Signal	Description
1, 2, 3, 4, 5, 6, 7, 8, 9, 10	5VIN	DC Supply Voltage (5 Volt)

3.16.2. GROUND

GROUND: (J4:100 PIN BOARD TO CARRIER BOARD CONNECTOR INTERFACE)

Pin #	Signal	Description
1, 2, 7, 8, 13, 14, 19, 20, 25, 26, 31, 32, 37, 38, 43, 44, 49, 50, 55, 56, 61, 62, 67, 68, 74, 80, 86, 89, 95, 96	GND	Digital Ground

GROUND: (J5:100 PIN BOARD TO CARRIER BOARD CONNECTOR INTERFACE)

Pin #	Signal	Description
11, 12, 13, 14, 15, 16, 25, 32, 39, 42, 43, 46, 53, 59, 63, 66, 70, 75, 78, 81, 82, 87, 88, 92, 93, 99, 100	GND	Digital Ground

GROUND: (J8:100 PIN BOARD TO CARRIER BOARD CONNECTOR INTERFACE)

Pin #	Signal	Description
1, 2, 7, 8, 13, 14, 19, 20, 25, 26, 31, 32, 43, 44, 47, 51, 52, 55, 56, 59, 63, 66, 76, 77, 81, 82, 88, 94, 100	GND	Digital Ground

4. OPERATIONAL CHARACTERISTICS

4.1. POWER SUPPLY

Description	Signal	Description	Typical	Tolerance	Unit
Main Power Supply, DC-IN	5VIN	DC Supply Voltage	5	+/- 5%	V

4.2. POWER CONSUMPTION

Parameter	Min	Typical	Max	Unit
Main Input Voltage	-	5	-	V
Power Consumption*	-	TBD	TBD	mW
CPU Clock	-	-	1.8	Ghz

Reference the NXP Website to get the i.MX8 Plus reference manual for power consumption and CPU clock speed specifications

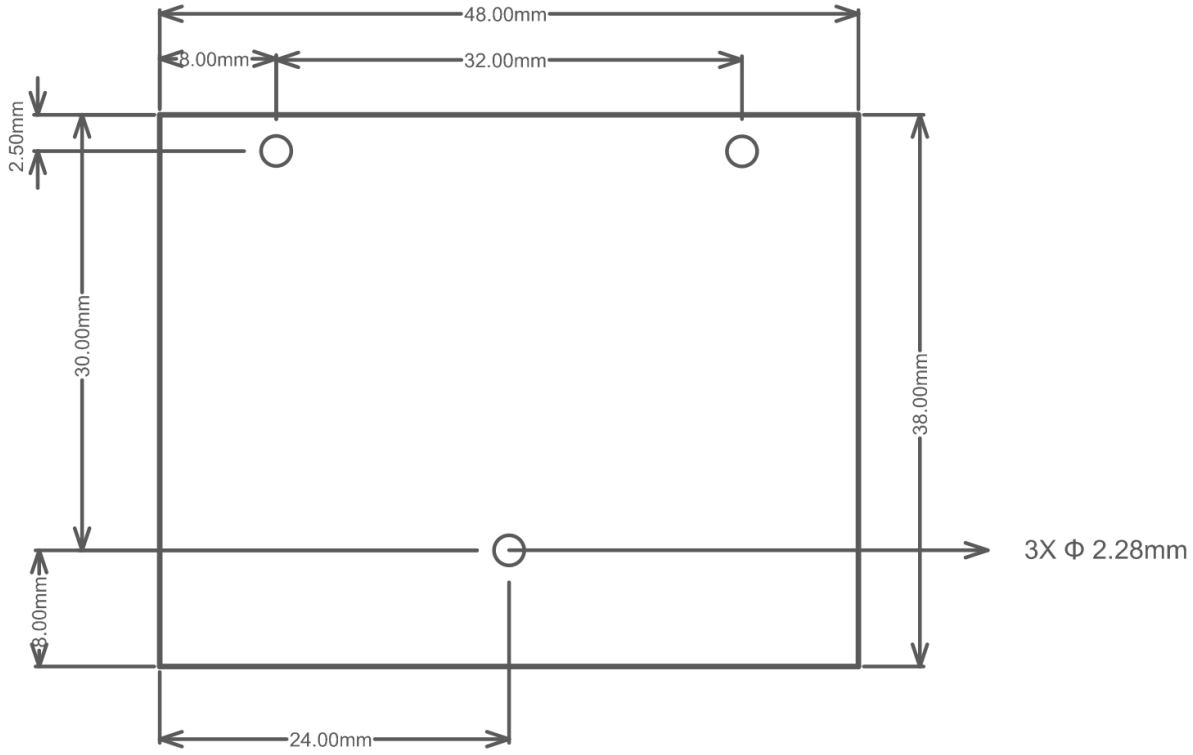
5. ENVIRONMENTAL SPECIFICATIONS

Operating Rating	Min. Temperature	Max. Temperature
Commercial Operating Temperature Range	0 °C	+70 °C
Industrial Operating Temperature Range*	-40 °C	+85 °C

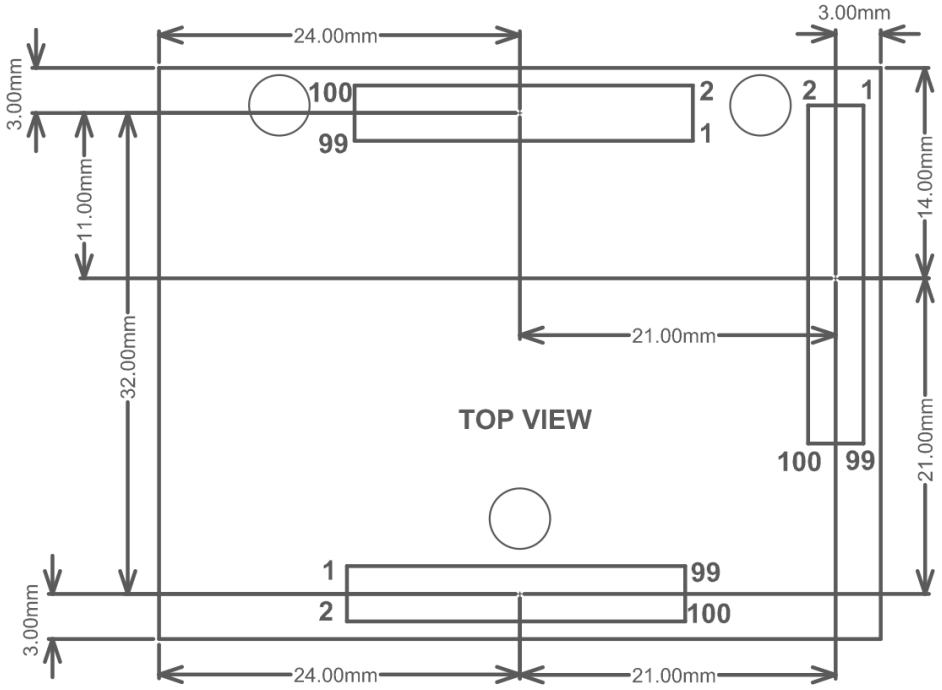
***Note:** Commercial and Industrial Temperature is based on the operating temperature grade of the SOM components. Customers should consider specific thermal design for the final product based upon the specific environmental and operational conditions. WiFi+BT module is only rated to -20 to +70C.*

6. MECHANICAL DRAWINGS

TOP VIEW



TOP VIEW (with connectors)



Recommended screws for the SOM are M2 x 4mm.

7. ORDERABLE PART NUMBERS

SKU	CPU	LPDDR4 Memory	eMMC Size	Operating Rating	Operating Temperature Range
N8MP_SOM_2r16e	i.MX8M Quad Plus	2GB	16GB	Commercial	0° to 70°C
N8MP_SOM_2r16eWB	i.MX8M Quad Plus (Wifi+BT)	2GB	16GB	Commercial	0° to 70°C
N8MP_SOM_4r16eWB	i.MX8M Quad Plus (Wifi+BT)	4GB	16GB	Commercial	0° to 70°C
N8MP_SOM_2r16e_i	i.MX8M Quad Plus	2GB	16GB	Industrial	-40° to 85°C
N8MP_SOM_2r16eWB_i	i.MX8M Quad Plus (Wifi+BT)	2GB	16GB	Industrial	-40° to 85°C *
N8MP_SOM_4r16eWB_i	i.MX8M Quad Plus (Wifi+BT)	4GB	16GB	Industrial	-40° to 85°C *

** Wi-Fi + BT module is only rated to -20C to +70C*

Note: Please contact us to discuss other custom options