

# NAFE13388

NAFE13388 Universal  $\pm 25$  V 8-input low-power AFE with excitation sources

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Product data sheet

## Document information

Information	Content
Keywords	NAFE13388, 8-channel, analog front-end (AFE), 24-bit ADC resolution, excitation source
Abstract	Highly configurable multichannel precision AFE for industrial applications.



## 1 General description

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The NAFE13388 is a highly configurable industrial-grade multichannel universal input analog front-end (AFE) that meets high-precision measurement requirements. The device integrates low-leakage, high-voltage (HV) fast multiplexers, low-offset and low-drift programmable gain amplifier (PGA) and buffers, high data-rate 24-bit Delta-Sigma analog-to-digital converter (ADC), precise voltage and current excitation source, and low-drift voltage reference. All of the HV analog pins are diode-protected internally for electromagnetic compatibility (EMC) and miswiring scenarios. The NAFE13388 is equipped with various diagnostic and supplies supervisory circuitry for condition monitoring and anomaly detection. Two precise calibration voltage sources are made available for ease of end-to-end system self-calibration and predictive maintenance.

The NAFE13388 family of products is designed for programmable logic controllers (PLCs), I/O modules, data loggers, instrumentation, and high-precision sensor and data acquisition systems.

## 2 Features and benefits

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- Eight configurable HV inputs
  - Single-ended or differential, with ranges up to  $\pm 25$  V
  - Independent configurations for voltage, current, resistance, resistance temperature detector (RTD), thermocouple
  - Overvoltage protected up to  $\pm 36$  V for less than one hour
- Programmable gain: x0.2 to x16
- Fast data rates
  - 7.5 SPS to 288 kSPS
  - Simultaneous 50 Hz/60 Hz line rejection
  - ENOB: 17-bit at 72 kSPS
- High accuracy
  - 0.005 %FS accuracy at room after user calibration
  - 0.1 %FS accuracy over  $-25$  °C to  $105$  °C
- System calibration
  - End-to-end calibration with integrated precise voltage sources
  - Accurate factory-calibrated products available
- $\pm 3$  °C internal temperature sensor
- Precise excitation voltage and current sources
- 0.2% internal oscillator accuracy at room temperature
- Diagnostic system for faults detection and prediction
- CRC error detection
- Ten GPIOs
- 32 MHz SPI interface
- Robust 7.5 kV HBM ESD and IEC61000-4-5 2 kV surge protection
- Power supply: HV:  $\pm 7$  V to  $\pm 24$  V, LV: 3.3 V
- 150 mW low power consumption
- Operating temperature range  $T_A$ :  $-40$  °C to  $+125$  °C
- Package: 64 pin, 9 mm x 9 mm x 0.85 mm HVQFN

### 3 Applications

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- Data acquisition system
- PLC, DCS I/O modules
- Industrial automation and process control

## 4 Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
NAFE13388 B40BS	NAFE13388 B40BS	HVQFN64	Plastic, thermal-enhanced very thin quad flatpack; no leads; 64 terminals; 0.5 mm pitch; 9 mm x 9 mm x 0.85 mm body	SOT804-3(D) <a href="https://www.nxp.com/packages/SOT804-3(D)">https://www.nxp.com/packages/SOT804-3(D)</a>

### 4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
NAFE13388 B40BS	NAFE13388 B40BSMP	HVQFN64	Reel 13" Q2/T1 *Standard mark SMD dry pack	1000	TA = -40 °C to +125 °C
NAFE13388 B40BS	NAFE13388 B40BSE	HVQFN64	1 + 1 Tray *Standard mark SMD dry pack	260	TA = -40 °C to +125 °C
NAFE13388 B40BS	NAFE13388 B40BSK	HVQFN64	5+1 Tray *Standard mark SMD dry pack	1300	TA = -40 °C to +125 °C

### 4.2 Product family

The NAFE family is optimized for power and speed, with highly integrated functional features and modes for offloading the host processor to achieve higher performance and low power consumption of overall system.

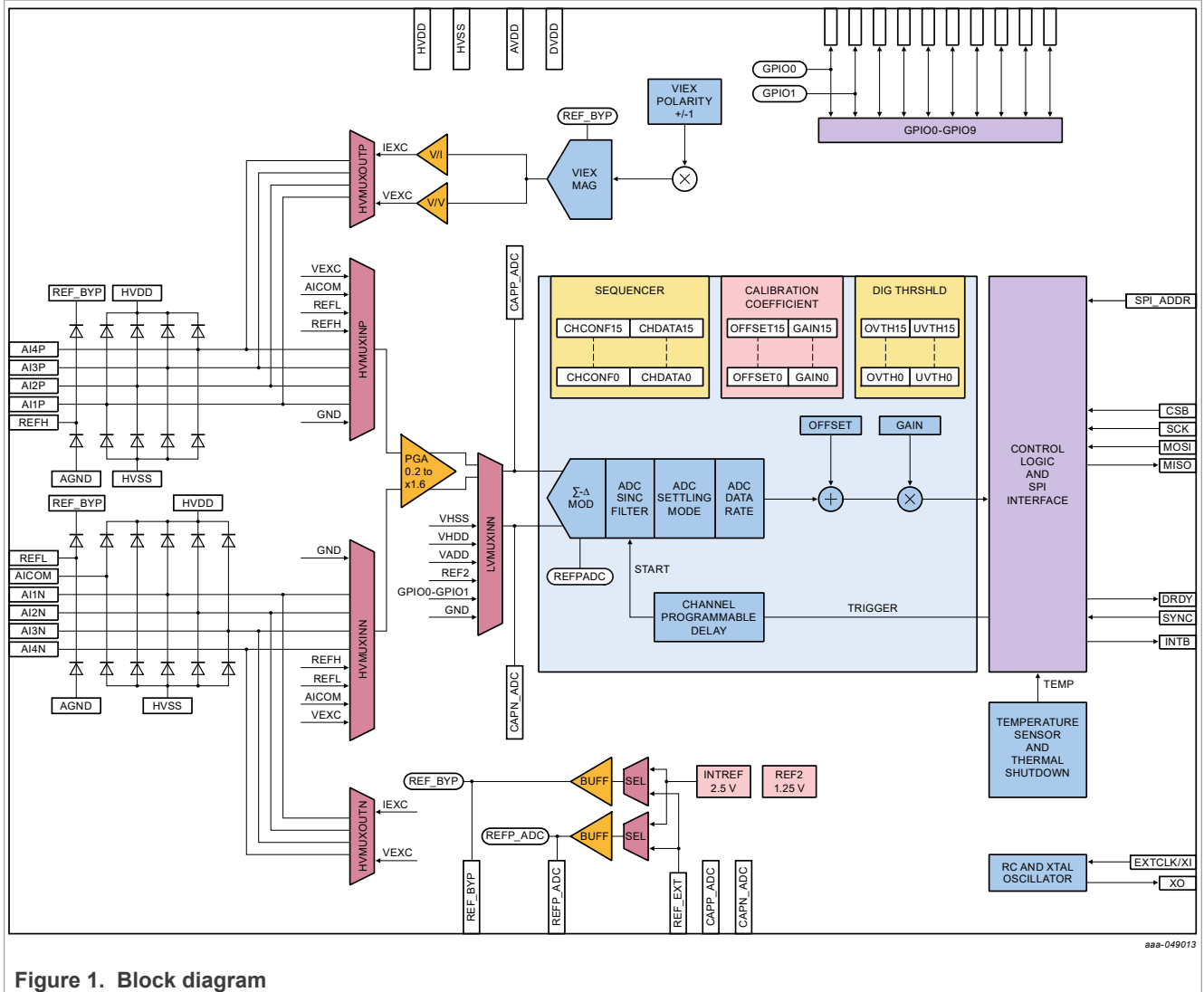
In addition, the NXP analog input AFE family of products is pin-to-pin, software-compatible, and well-suited in scalable applications of analog I/O modules and data acquisition systems.

[Table 3](#) shows the possible features to select for each family member. Contact the NXP factory or an NXP sales representative to get further information and availability of appropriate configurations.

Table 3. Part numbers

Part number	VI excitation source	Low-power high-speed	Resolution 16-bit/24-bit	#Input	Factory calibrated
NAFE13388B40BS	Yes	Low power	24	8	Yes
NAFE73388B40BS	Yes	High speed	24	8	Yes
NAFE13188B40BS	Yes	Low power	24	8	No

5 Block diagram



aaa-049013

Figure 1. Block diagram

## 6 Pinning information

### 6.1 Pinning

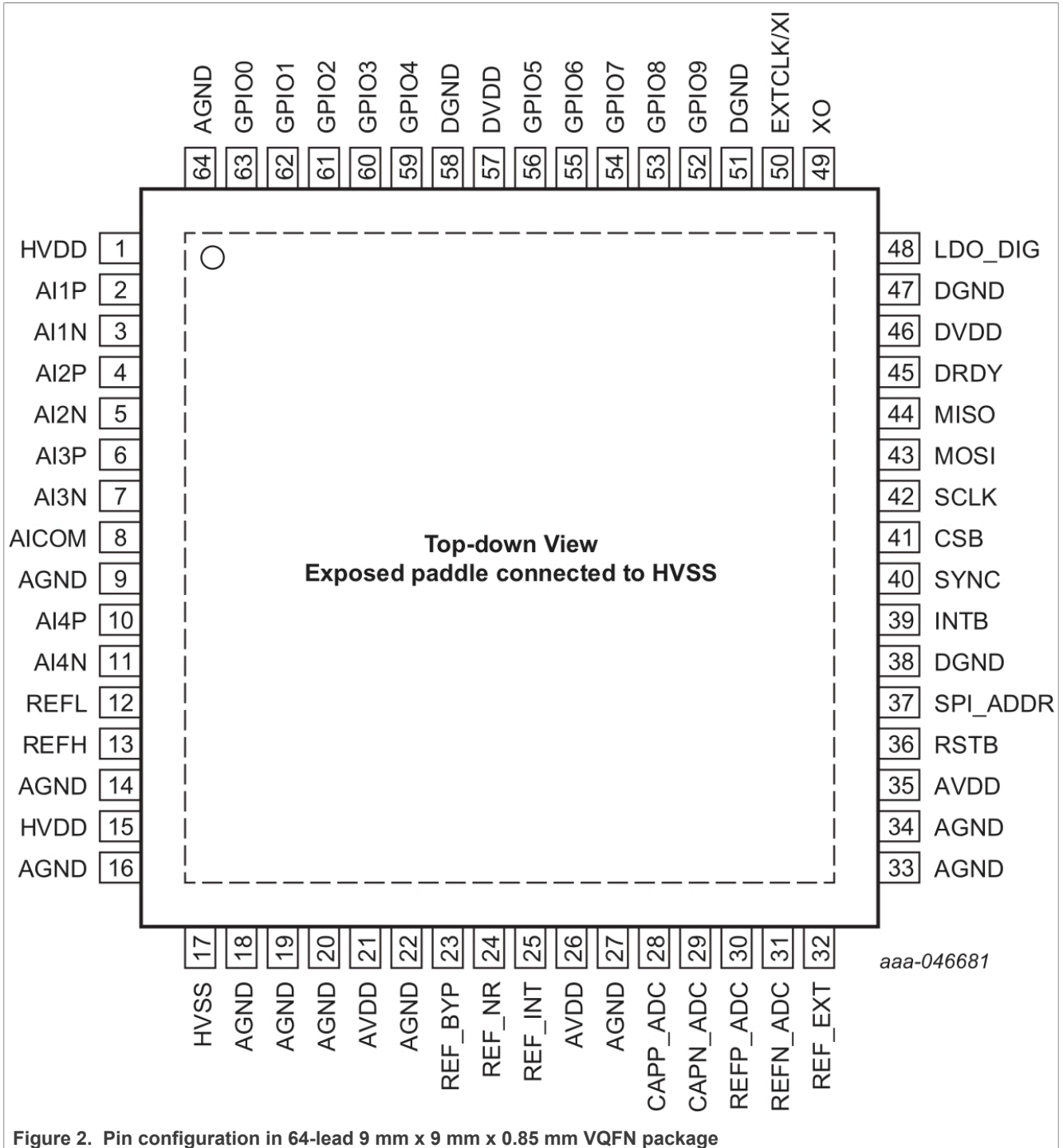


Figure 2. Pin configuration in 64-lead 9 mm x 9 mm x 0.85 mm VQFN package

## 6.2 Pin description

Table 4. Pin description

Pin	Name	I/O	Functional description
1	HVDD	Supply	High-voltage positive supply, 0.1 µF    4.7 µF to AGND, optional: install 28 V Zener to AGND for protection
2	AI1P	AI	Analog Input in series with external 2.5 kΩ resistor with 1 nF or 10 nF cap to AGND
3	AI1N	AI	Analog Input in series with external 2.5 kΩ resistor with 1 nF or 10 nF cap to AGND
4	AI2P	AI	Analog Input in series with external 2.5 kΩ resistor with 1 nF or 10 nF cap to AGND
5	AI2N	AI	Analog Input in series with external 2.5 kΩ resistor with 1 nF or 10 nF cap to AGND
6	AI3P	AI	Analog Input in series with external 2.5 kΩ resistor with 1 nF or 10 nF cap to AGND
7	AI3N	AI	Analog Input in series with external 2.5 kΩ resistor with 1 nF or 10 nF cap to AGND
8	AICOM	AI	Analog GND or common input in series with external 2.5 kΩ resistor with 1 nF or 10 nF cap to AGND
9	AGND	Ground	Analog ground
10	AI4P	AI	Analog Input in series with external 2.5 kΩ resistor with 1 nF or 10 nF cap to AGND
11	AI4N	AI	Analog Input in series with external 2.5 kΩ resistor with 1 nF or 10 nF cap to AGND
12	REFL	AO	0.2 V unbuffered internal voltage source, 10 nF cap to AGND
13	REFH	AO	2.3 V unbuffered internal voltage source, 10 nF cap to AGND
14	AGND	Ground	Analog ground
15	HVDD	Supply	High-voltage positive supply, 0.1 µF    4.7 µF cap to AGND
16	AGND	Ground	Analog ground
17	HVSS	Supply	High-voltage negative supply, 0.1 µF    4.7 µF cap to AGND. (internally shorted to exposed pad) Zener to AGND for protection.
18	AGND	Ground	Analog ground
19	AGND	Ground	Analog ground
20	AGND	Ground	Analog ground
21	AVDD	Supply	3.3 V analog power supply, 0.1 µF    4.7 µF cap to AGND.
22	AGND	Ground	Analog ground
23	REF_BYP	AO	Buffered voltage reference bypass, 100 pF (max loading) cap to AGND
24	REF_NR	AI	Voltage reference noise reduction, 0.47 µF cap to AGND
25	REF_INT	AO	Internal voltage reference output bypass, 0.47 µF
26	AVDD	Supply	3.3 V analog power supply, 0.1 µF    4.7 µF cap to AGND
27	AGND	Ground	Analog ground
28	CAPP_ADC	AO	ADC buffer positive output, 1 nF C0G cap to CAPN
29	CAPN_ADC	AO	ADC buffer negative output, 1 nF C0G cap to CAPP
30	REFP_ADC	AO	ADC positive reference bypass, 0.1 µF    1 µF X7R cap to REFN_ADC
31	REFN_ADC	AI	ADC ground reference, 0.1 µF    1 µF X7R cap to REFP_ADC
32	REF_EXT	AI	External 2.5 V reference voltage Input. 0.1 µF cap to AGND
33	AGND	Ground	Analog ground
34	AGND	Ground	Analog ground
35	AVDD	Supply	Connect 0.1 µF    4.7 µF cap to AGND (pin-34) close to the AVDD pin
36	RSTB	DI	Chip reset, active-low (CMOS push-pull or open drain with internal 100 kΩ pullup).
37	SPI_ADDR	DI	SPI address 0 (with internal 100 kΩ pulldown).
38	DGND	Ground	Digital ground
39	INTB	DO	Active low interrupt output (CMOS push-pull or open drain internally pulled up)
40	SYNC	DI	ADC sync pulse input
41	CSB	DI	Chip select input, active-low (with internal 100 kΩ pullup)
42	SCLK	DI	SPI clock input



Table 4. Pin description...continued

Pin	Name	I/O	Functional description
43	MOSI	DI	SPI data input
44	MISO	DO	SPI data output
45	DRDY	DO	ADC data ready output, active-high
46	DVDD	Supply	3.3 V digital power supply, 0.1 $\mu$ F    4.7 $\mu$ F cap to DGND.
47	DGND	Ground	Digital ground
48	LDO_DIG	AO	Internal 1.8 V LDO bypass, 0.1 $\mu$ F    4.7 $\mu$ F uF cap to DGND.
49	XO	DI	18.432 MHz crystal XOUT with loading cap (< 20 pF). No-connect or float if crystal is not used
50	EXTCLK/XI	DI	External clock input or 18.432 MHz crystal XIN with loading cap(< 20 pF)
51	DGND	Ground	Digital ground
52	GPIO9	DI, DO	General-purpose digital input/output or system clock output
53	GPIO8	DI, DO	General-purpose digital input/output
54	GPIO7	DI, DO	General-purpose digital input/output
55	GPIO6	DI, DO	General-purpose digital input/output
56	GPIO5	DI, DO	General-purpose digital input/output
57	DVDD	Supply	3.3 V digital power supply, 0.1 $\mu$ F    4.7 $\mu$ F cap to DGND.
58	DGND	Ground	Digital ground
59	GPIO4	DI, DO	General-purpose digital input/output
60	GPIO3	DI, DO	General-purpose digital input/output
61	GPIO2	DI, DO	General-purpose digital input/output
62	GPIO1	DI, DO, AI	General-purpose digital I/O or ADC differential analog input: GPIO0-GPIO1
63	GPIO0	DI, DO, AI	General-purpose digital I/O or ADC differential analog input: GPIO0-GPIO1
64	AGND	Ground	Analog ground
	EP		Exposed pad is connected to HVSS internally. Exposed pad should be tied to HVSS on PCB.

## 7 Functional description

### 7.1 Overview

The NAFE13388 is a highly configurable, universal eight-input AFE with various integrated diagnostic features. At HV analog inputs, the low-leakage pins could be configured anywhere from eight single-ended to four differential signals, with external common input AICOM or internal AGND reference. Eight selectable PGA gain settings of 0.2 V/V to 16 V/V provide a wide range of differential input range from  $\pm 25$  V to  $\pm 312.5$  mV for variety of applications. In general, all of the HV input characteristics are specified to the linear (nominal) input ranges for all of the channel gain settings, which is 80 % of the full input range. In addition to the differential signals at PGA output, one auxiliary differential input GPIO0-GPIO1, four low-voltage diagnostic signals are also multiplexed to ADC: power supplies AVDD, HVDD, HVSS, and an independent coarse voltage reference (REF\_coarse).

The voltage reference (VREF) derived voltage sources REFH and REFL are available through pins for external measurement. These two voltage sources are also connected as inputs to high-voltage multiplexer (HVMUX). They could be used for on-chip self-calibration or self-diagnostic purposes, regardless of the voltage reference sources, which can be either external, internal, or mixed. When supplied with the factory-calibrated coefficients, REFH and REFL facilitate routine calibrations without the need for additional accurate components.

The device includes a configurable voltage or current excitation source. The configurable source provides required voltage or current to sensors, such as RTD.

An independent on-chip temperature sensor is included for continuous die temperature monitoring with a 16-bit readout. This temperature reading is also used to trigger an overtemperature warning at 145 °C, auto-shutdown at 165 °C, or the user-programmable temperature alarm.

The NAFE13388 comes with ten GPIOs that satisfy most of the needs for monitoring and control in typical applications. The selectable clock sources could be either the internal oscillator or a crystal oscillator, or external clock. In addition, a data and conversion synchronization is available via SYNC and DRDY pins, and the last falling edge of the SPI clock.

Succeeding to 24-bit  $\Delta\Sigma$  modulator, a multistage digital filter was designed to offer a wide range of data rates with a selectable cascade of SINC filters and the option of Single-Cycle Settling mode versus Normal Settling mode. In multichannel, fast-switching applications, the user may trade off speed/accuracy and fine-tune the effective data rate. Simultaneous 50 Hz and 60 Hz line rejection is available in lower data rates.

The software-configurable sequencer enables high data-rate input channel scanning at system level.

Five efficient reading modes are available for ADC data conversion: single-channel single-reading (SCSR), single-channel continuous-reading (SCCR), multichannel single-reading (MCSR), multichannel multireading (MCMR), and multi-channel continuous-reading (MCCR). The user may issue command CMD\_BURST\_DATA to read back multiple channels data in a single SPI transaction. See [Table 19](#) for conversion start commands.

### 7.2 Precise and fast data acquisition

The NAFE13388 is suitable for data acquisition of high-precision and high-speed analog inputs.

The NAFE13388 integrates an input multiplexer (MUX), high gain bandwidth (GBW) programmable gain amplifier (PGA), and a high-resolution 24-bit sigma-delta ADC. The optimized architecture of the MUX, PGA, and ADC provides fast input-scanning with flexible output data rates, which are comparable with SAR ADC architecture used in fast response-time system.

Programmable ADC output data rate range:

- 288 ksp/s to 7.5 sp/s in Normal Settling mode
- 72 ksp/s to 1.5 sp/s in Single-Cycle Settling mode

Figure 3 shows the scanning time required when HV MUX switches from one input to another (effectively presenting a step function), and PGA follows to settle with limited bandwidth and the required ADC conversion time at a specified data rate.

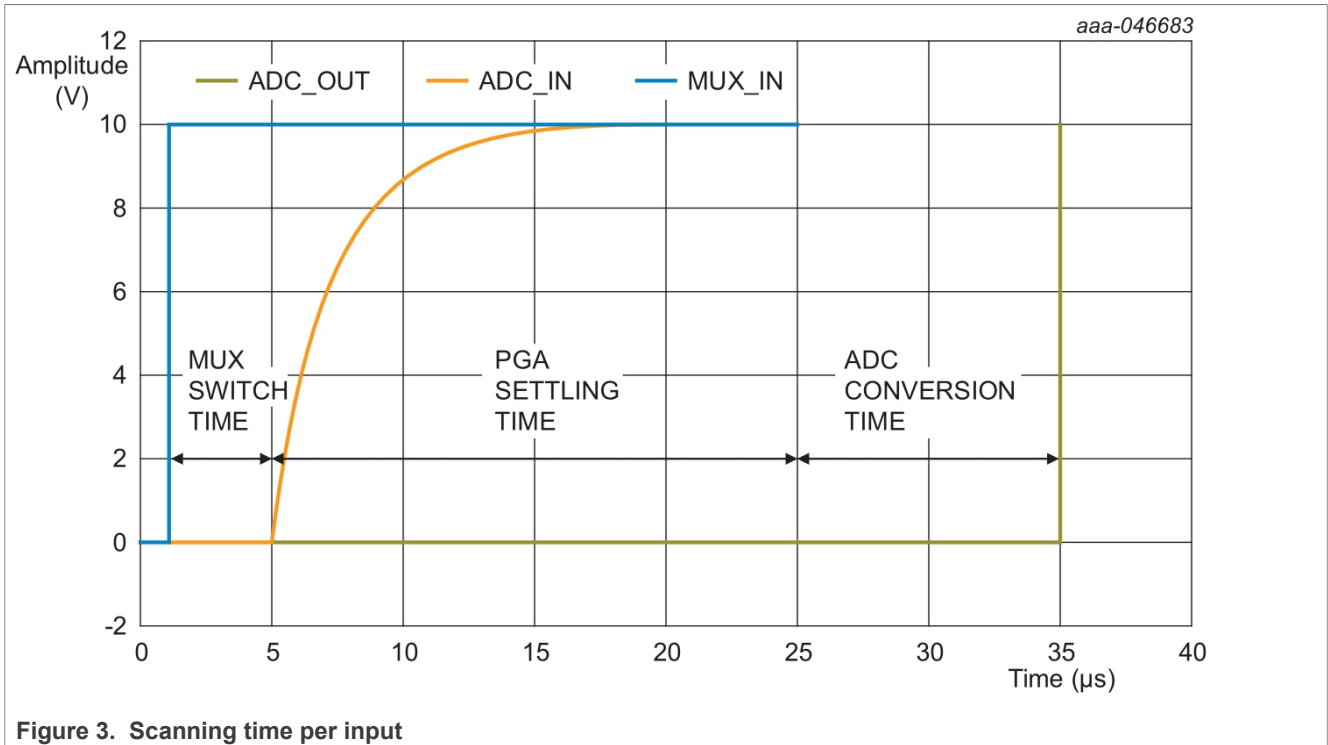


Figure 3. Scanning time per input

### 7.3 Detailed description

This section describes the building blocks integrated in the NAFE13388.

#### 7.3.1 Architecture block diagram

The NAFE13388 can be grouped into eight sections: high-voltage multiplexer, PGA, low-voltage multiplexer, ADC, digital calibration, voltage reference, VIEX (voltage/current excitation), and clock sources as shown in Figure 1.

#### 7.3.2 High-voltage multiplexer — HVMUX

The high-voltage analog input section serves as an externally accessible input and internal input.

The external inputs are: AI1P, AI2P, AI3P, AI4P, AI1N, AI2N, AI3N, AI4N, AICOM

- AI1P, AI2P, AI3P, AI4P are connected to the positive high-voltage multiplexer HVMUXINP input.
- AI1N, AI2N, AI3N, AI4N are connected to the negative high-voltage multiplexers HVMUXINN input.

AICOM, REFH, REFL, and AGND (internal ground) are connected to both positive and negative high-voltage input multiplexers HVMUXINP and HMMUXINN, respectively.

##### 7.3.2.1 Analog input protection diodes and clamping

As shown in Figure 4, the external analog input pins of the NAFE are followed by clamping circuits for electrostatic discharge (ESD) and surge protection.

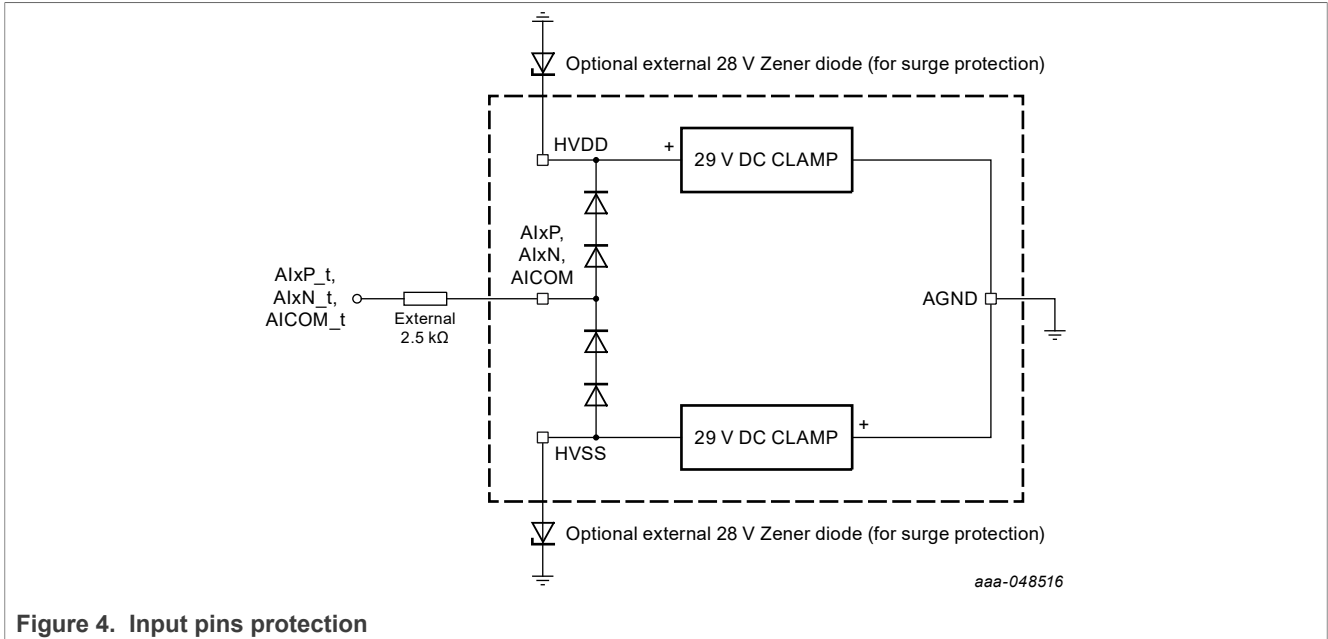


Figure 4. Input pins protection

Each HV input pin is equipped with input protection diodes connected to HVDD, HVSS.

It is recommended that an external series 2.5 kΩ resistor with 1 nF or 10 nF capacitor to AGND is installed for each HV input pin for reliability. See [Section 11.1](#).

The integrated clamping circuits, shown in [Figure 4](#), protect the NAFE inputs from possible surge voltage and from ESD events occurring during the manufacturing process and during printed-circuit board (PCB) assembly.

If an analog input is driven below HVSS, or above HVDD, the internal protection diodes may conduct current. A 2.5 kΩ or greater external series resistor is required to limit the input current to the specified value.

### 7.3.2.2 HV input multiplexer - HVMUXIN

The NAFE uses two independent HV input multiplexers to measure the differential, pseudo-differential, and single-ended signal. When the input is used in differential or pseudo-differential mode, the NAFE provides high common-mode rejection.

The differential configuration is obtained by connecting the positive wire of signal to any of the AlxP inputs and the negative wire of signal to any of the AlxN inputs and via software configuration selecting the respective inputs of HVMUX.

The pseudo-differential configuration is obtained by connecting the positive wire of signal to any of the AlxP or AlxN inputs and the negative wire of signal to AICOM input and via software configuration selecting the respective inputs of HVMUX.

The single-ended configuration is achieved by connecting the positive signal to any of the AlxP or AlxN inputs and the negative wire of signal to AICOM.

The selected input to positive and negative HVMUX should be configured appropriately to match the physical connections. When CH\_CHOP = 1 is set, two ADC conversions will be performed. Therefore the final ADC output is the average of the difference of these two ADC intermediate outputs. As such, the channel offset is canceled and the effective output data rate is half of the programmed value.

**Note:** The ADC output polarity sign is inverted internally and automatically whenever AlxP input is connected to AICOM or GND while AlxN input is AI1N..AI4N, REFH, REFL.

### 7.3.2.2.1 Analog common input (AICOM)

To ensure precise single-ended measurements, AICOM pin should be connected in series with a 2.5 k $\Omega$  resistor and connected to an external GND reference physically close to the measured positive signal on the printed-circuit board (PCB).

### 7.3.2.2.2 REFH and REFL

REFH and REFL provide stable and accurate voltage sources derived from VREF\_BYP. REFH and REFL are 92 % and 8 %, of VREF\_BYP, with a nominal value of 2.3 V and 0.2 V, respectively.

REFH and REFL are connected to inputs of both HVMUXINP and HVMUXINN multiplexer.

REFH and REFL could be used for system-level self-calibration on the field, failure prediction, and predictive maintenance. Factory OPT\_COEF1 and OPT\_COEF2 is available for REFH and REFL on optional part numbers.

### 7.3.2.2.3 Low-leakage circuit

The NAFE13388 provides a high-input impedance of 1 G $\Omega$  and low-input leakage current less than 5 nA at 105  $^{\circ}$ C. In combination with its low-noise and low-offset drift PGA, the device is well-suited for precision temperature measurement with RTD and TC.

The NAFE13388 provides a precise programmable current excitation source to enable the measurement of resistance and the RTD sensor.

### 7.3.2.3 HV output multiplexer - HVMUXOUT

The AFE uses two independent HV output multiplexers to connect the voltage or current excitation VIEX source to the desired input pin. This enables the device to measure resistance, RTD, to detect open and short circuit at the input, and implement readback monitoring for diagnostic testing.

## 7.3.3 Programmable gain amplifier

The programmable gain amplifier (PGA) is a low-noise, programmable gain, differential input, differential output amplifier. The PGA operates in Gain or Attenuation mode, depending on the gain selected. Typically, the PGA is programmed to utilize the input range of the ADC to the full-scale input signal. Available PGA gains are 0.2, 0.4, 0.8, 1, 2, 4, 8, 16 V/V.

7.3.3.1 PGA input operating ranges

Table 5 shows the HV input nominal ranges, the max and min values, full-scale range, and resolution for the different types of input signals and PGA gain setting.

Table 5. HV input ranges and resolutions

Nominal range values (V)								
Type	PGA gain setting							
	0.2	0.4	0.8	1	2	4	8	16
Bipolar DIFF	±20.00000	±10.00000	±5.00000	±4.00000	±2.00000	±1.00000	±0.50000	±0.25000
BipolarSE	±10.00000	±5.00000	±2.50000	±2.00000	±1.00000	±0.50000	±0.25000	±0.12500
Unipolar DIFF	±10.00000	±5.00000	±2.50000	±2.00000	±1.00000	±0.50000	±0.25000	±0.12500
Unipolar SE	±10.00000	±5.00000	±2.50000	±2.00000	±1.00000	±0.50000	±0.25000	±0.12500
Min and max values (V)								
Type	PGA gain setting							
	0.2	0.4	0.8	1	2	4	8	16
Bipolar DIFF	±25.00000	±12.50000	±6.25000	±5.00000	±2.50000	±1.25000	±0.62500	±0.31250
BipolarSE	±12.50000	±6.25000	±3.12500	±2.50000	±1.25000	±0.62500	±0.31250	±0.15625
Unipolar DIFF	±12.50000	±6.25000	±3.12500	±2.50000	±1.25000	±0.62500	±0.31250	±0.15625
Unipolar SE	±12.50000	±6.25000	±3.12500	±2.50000	±1.25000	±0.62500	±0.31250	±0.15625
Full range scale (V)								
Type	PGA gain setting							
	0.2	0.4	0.8	1	2	4	8	16
Bipolar DIFF	50	25	12.5	10	5	2.5	1.25	0.625
BipolarSE	25	12.5	6.25	5	2.5	1.25	0.625	0.3125
Unipolar DIFF	25	12.5	6.25	5	2.5	1.25	0.625	0.3125
Unipolar SE	12.5	6.25	3.125	2.5	1.25	0.625	0.3125	0.15625
Resolution (V)								
Type	PGA gain setting							
	0.2	0.4	0.8	1	2	4	8	16
Bipolar DIFF	3.0E-6	1.5E-6	745.1E-9	596.0E-9	298.0E-9	149.0E-9	74.5E-9	37.3E-9
BipolarSE	3.0E-6	1.5E-6	745.1E-9	596.0E-9	298.0E-9	149.0E-9	74.5E-9	37.3E-9
Unipolar DIFF	3.0E-6	1.5E-6	745.1E-9	596.0E-9	298.0E-9	149.0E-9	74.5E-9	37.3E-9
Unipolar SE	3.0E-6	1.5E-6	745.1E-9	596.0E-9	298.0E-9	149.0E-9	74.5E-9	37.3E-9

7.3.3.2 PGA input common mode ranges

PGA input common mode voltage range depends on PGA gain.

For cases with fully differential input voltages, the maximum allowable input common mode voltage can be calculated as:

If  $V_{in+} = VCM + \frac{V_{DIFF}}{2}$  and  $V_{in-} = VCM - \frac{V_{DIFF}}{2}$

Then,  $VCM_{max} = A \cdot \left( V_{REF} - CH_{GAIN} \cdot \frac{V_{DIFF}}{2} \right)$

Where,  $A = 1$  for  $CH_{GAIN} = 1, 2, 4, 8, 16$ .

$A = 5$  for  $CH_{GAIN} = 0.2, 0.4, 0.8$ .

And  $V_{REF} = 2.5 V$  with internal reference voltage.

7.3.4 Low-voltage multiplexer - LVMUX

The internal node voltages (scaled HVDD and HVSS, AVDD, VREF\_Coarse, GPIO0-GPIO1) and PGA outputs are routed to the ADC input via a low-voltage multiplexer controlled by register bit HVSEL.

**Note:** The associated HV\_AIP and HV\_AIN setting for each LVSIG\_IN signal selection in [Table 6](#). For example, LVSIG\_IN = 3 (VADD), the setting for CH\_CONFIG0 is 0xCC07 when CH\_GAIN = 0 and TCC\_OFF = 1.

Table 6. CONFIG0 Setting for using LVMUX signals

HV_AIP	HV_AIN	CH_GAIN	HVSEL	LVSIG_IN	TCC_OFF
9	9	X	0	0:REF2	X
A	A	X	0	1:GPIO01	X
B	B	X	0	2:REF_Coarse	X
C	C	X	0	3:VADD	X
D	D	X	0	4:VHDD	X
E	E	X	0	5:VHSS	X

7.3.5 Analog-to-digital converter

7.3.5.1 ADC buffer

The ADC buffer is used to drive the sampling circuit of the ADC, where its differential output pins, CAPP and CAPN, are to be loaded with external C0G type capacitor.

7.3.5.2 Sigma delta ADC

The ADC is based on sigma delta architecture that provides low-noise and high-speed acquisition in Single-Channel and Multichannel mode. The sigma delta architecture includes a sigma delta modulator followed by a configurable digital filter.

The ADC modulator is a third-order ΣΔ modulator. The modulator samples the analog input voltage at a high-sample rate (fMOD = fsys\_clk / 2) and converts the analog input to a bit stream that is processed by the following digital filter.

The digital filter processes the modulator output data to produce the high-resolution conversion result. The digital filter filters and decimates the data. Software selection of a certain digital filter depends on the trade-off between resolution, data rate, and line-cycle rejection acceptable in a system.

The ADC digital filter consists of two SINC filter stages. The first stage is a variable decimation SINC4 filter followed by the second stage variable-decimation, variable-order SINC filters. The optimized high-speed SINC4 filter averages and down-samples the modulator data to produce high-speed data rates from 288 ksps to 6 ksps.

The low-speed digital filter performs additional filtering and decimation to produce data rates of 4.5 ksps to 7.5 sps. The low-speed stage is a programmable-order SINC filter as SINC1, SINC2, SINC3, SINC4.

The data rate is programmed by the CH\_CONFIG1.ADC\_DATA\_RATE bits.

The digital filters are controlled by CH\_CONFIG1.ADC\_SINC bits.

**Note:** SINCx filter has settling time of x clock cycles, where x is the order. To manage the SINC filter settling, the NAFE13388 offers two different Conversion modes.

The Single-Cycle Settling mode is suggested for a multichannel system to avoid the settling error. The Normal Settling mode is suggested for single channel to get a faster data rate or lower noise.

### 7.3.5.3 Frequency response

The low-pass filtering effect of the SINC filters sets the overall frequency response of the ADC.

In Normal Settling mode, the frequency response of data rates, 6000 sps to 288000 sps, is determined by the transfer function of the first stage SINC4 filter. The frequency response of data rates, 7.5 sps to 4500 sps, is the product of the transfer function of the first digital filter stage (SINC4) and the selected digital filter of the second stage (SINC1, SINC2, SINC3, SINC4).

Figure 5 shows an example of filter response for data rate 6000 sps with first stage SINC4 filter; and for data rate 3000 sps with second stage SINC4 filter.

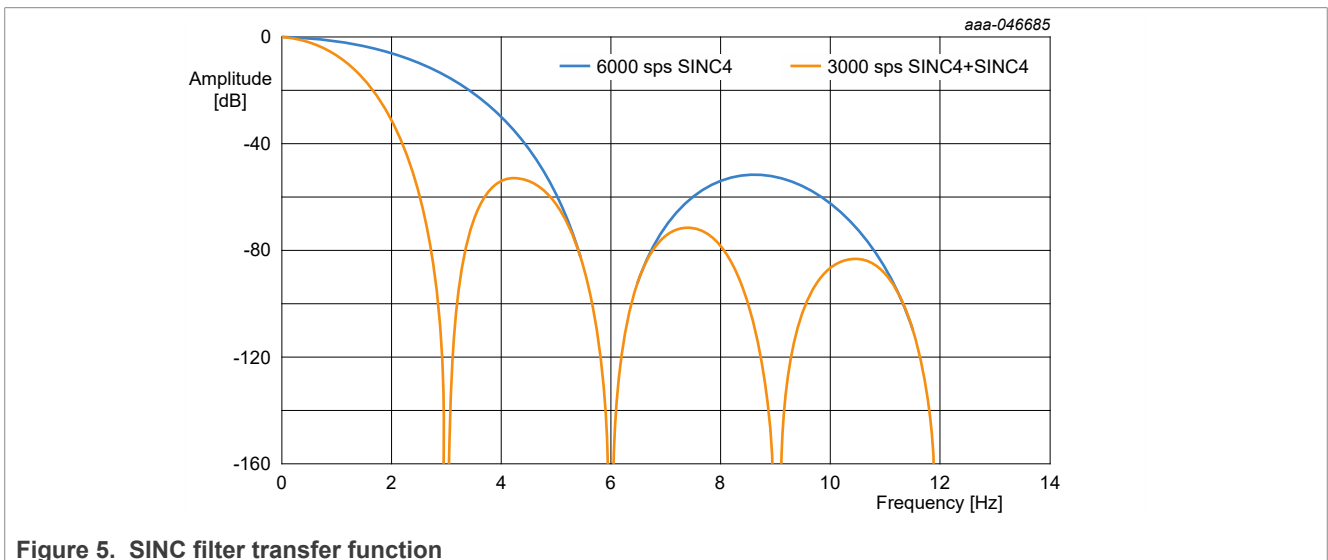
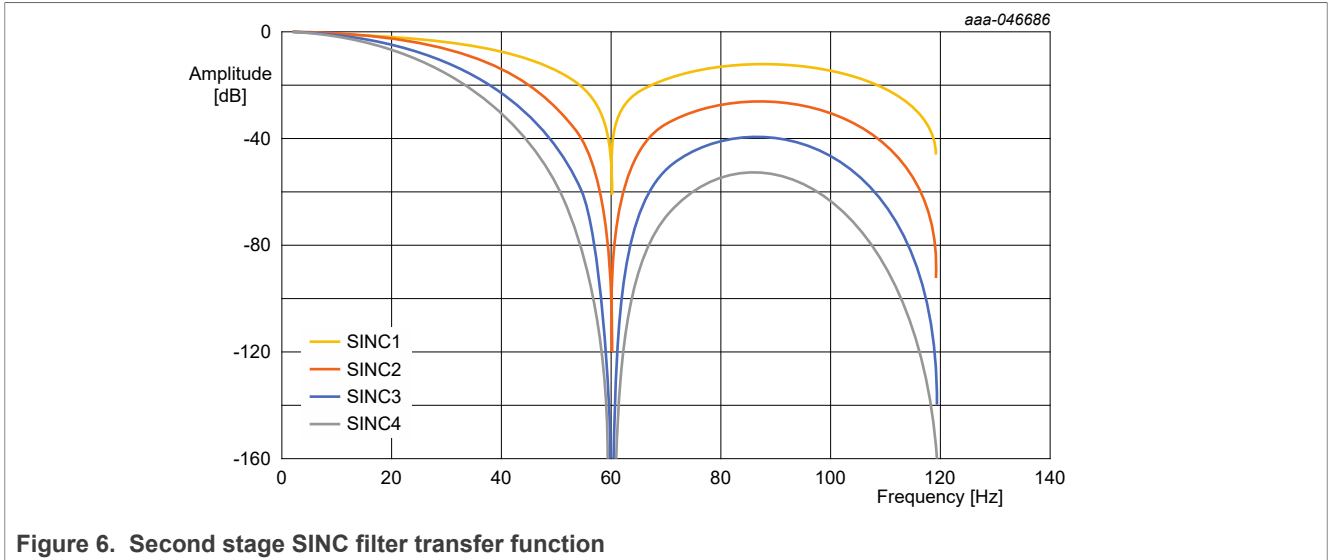


Figure 6 shows the frequency responses of the second stage SINC1, SINC2, SINC3, and SINC4 filter.

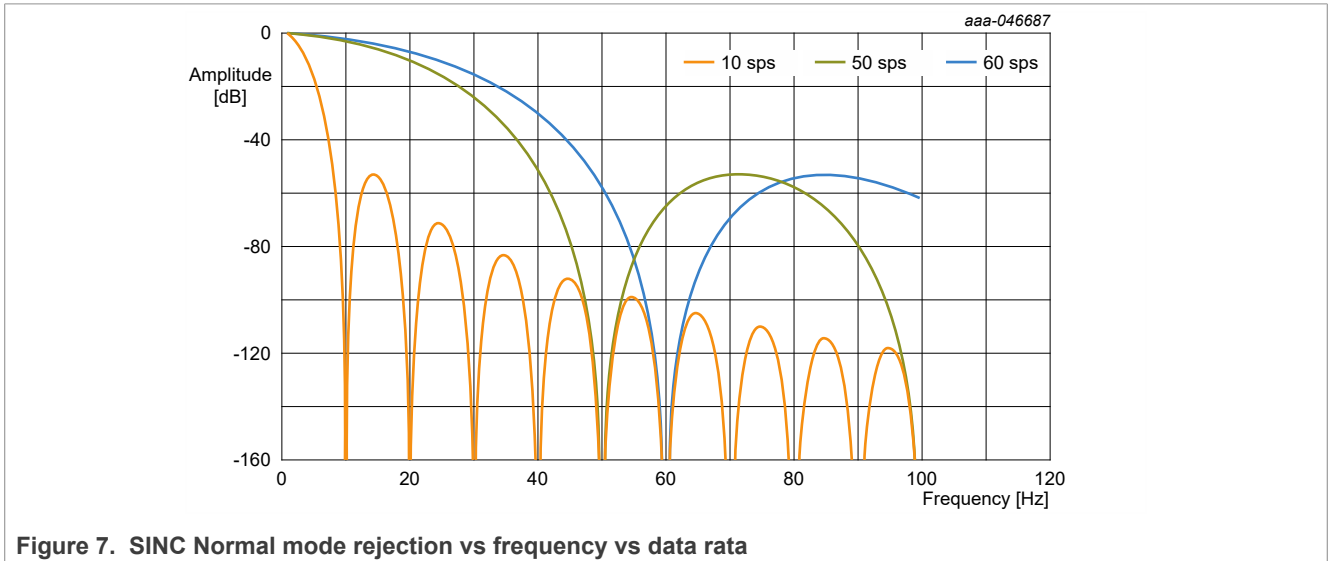




### 7.3.5.4 50 Hz/60 Hz Normal mode noise rejection

The NAFE13388 features a digital filter that provides a 50 Hz and 60 Hz Normal mode rejection (NMR).

Figure 7 shows the SINC4 filter NMR at the data rate of 10 sps, 50 sps, and 60 sps.



### 7.3.5.5 Step response

The NAFE13388 could be configured for the following settling mode:

- **Normal settling:** Fits better for single-channel reading, providing lower noise measurements.
- **Single-cycle settling:** Fits better for multichannel reading, providing settled output.

Figure 8 shows the relative settling time of the digital filter for the normal settling for different orders of SINC filter.

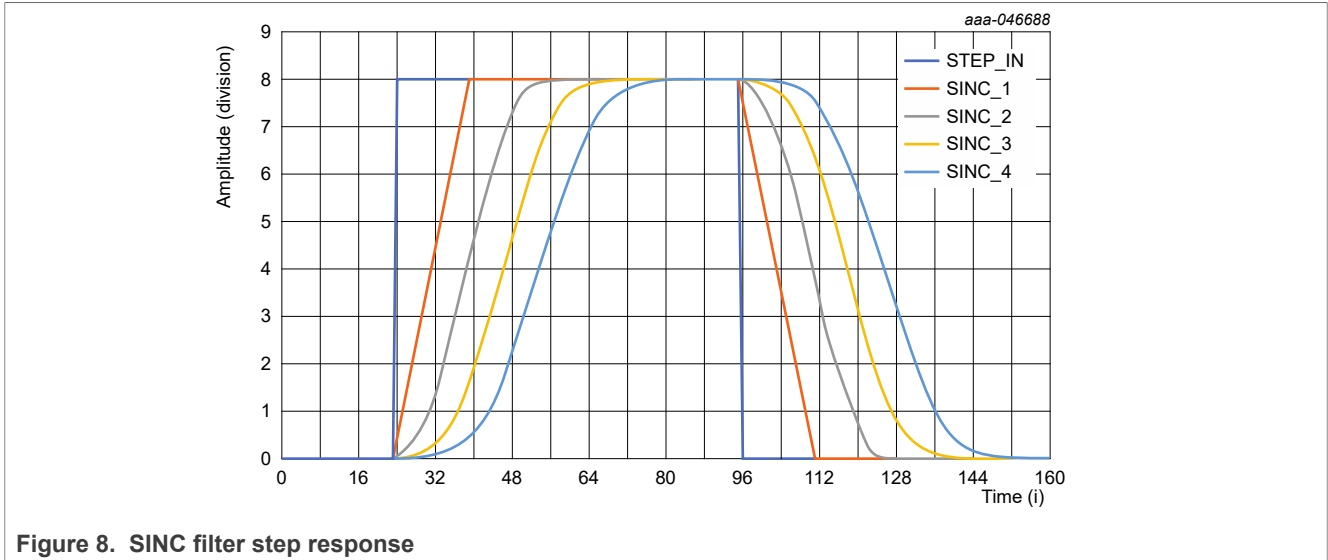


Figure 8. SINC filter step response

7.3.5.5.1 Normal settling vs. single-cycle settling

Figure 9 shows a 100 Hz digitized square wave sampled at 36 ksp/s. The digital filter is SINC4 and the settling mode is set to normal. During the square wave transition from low to high, the output takes four samples to settle.

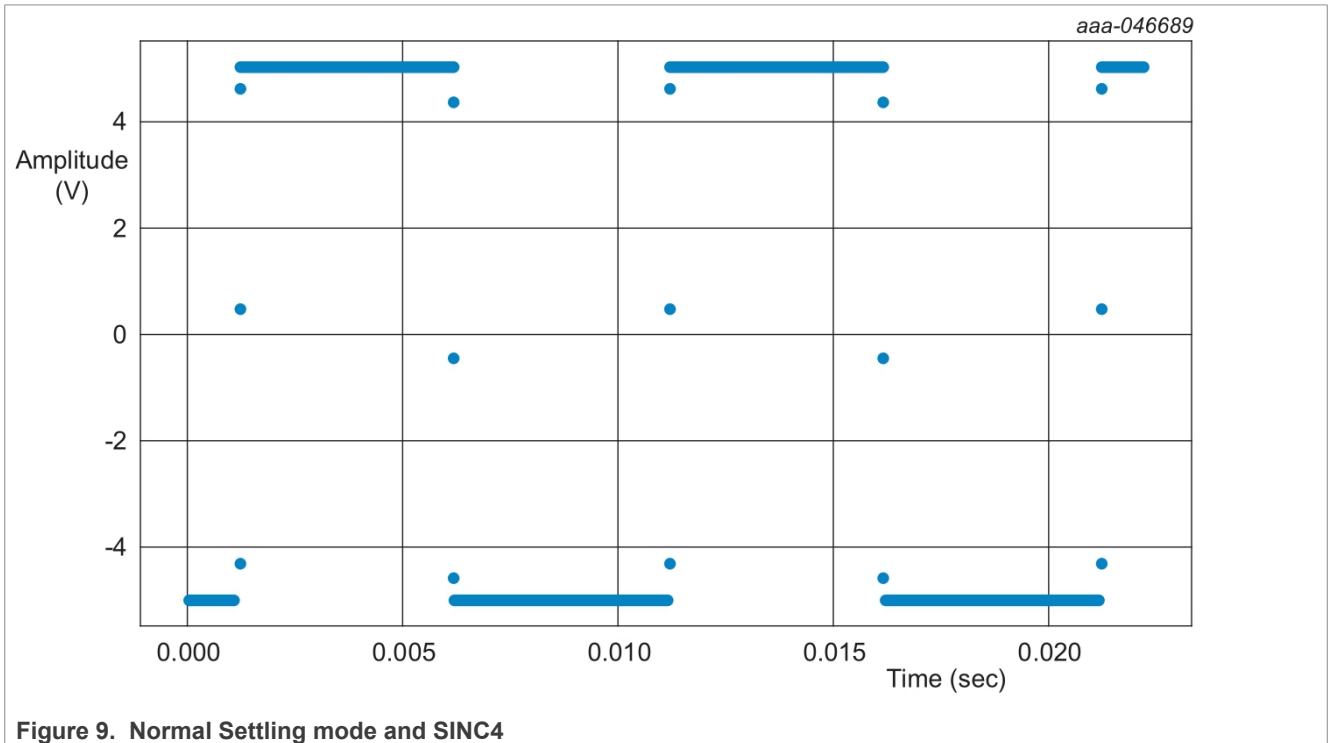


Figure 9. Normal Settling mode and SINC4

Instead, Figure 10 shows a 100 Hz digitized square wave with Settling mode set to single-cycle. The waveform is sampled at 9 ksp/s and the digital filter is SINC4. In Single-Cycle Settling mode, during the square wave transition from low to high, the output takes one sample to settle.

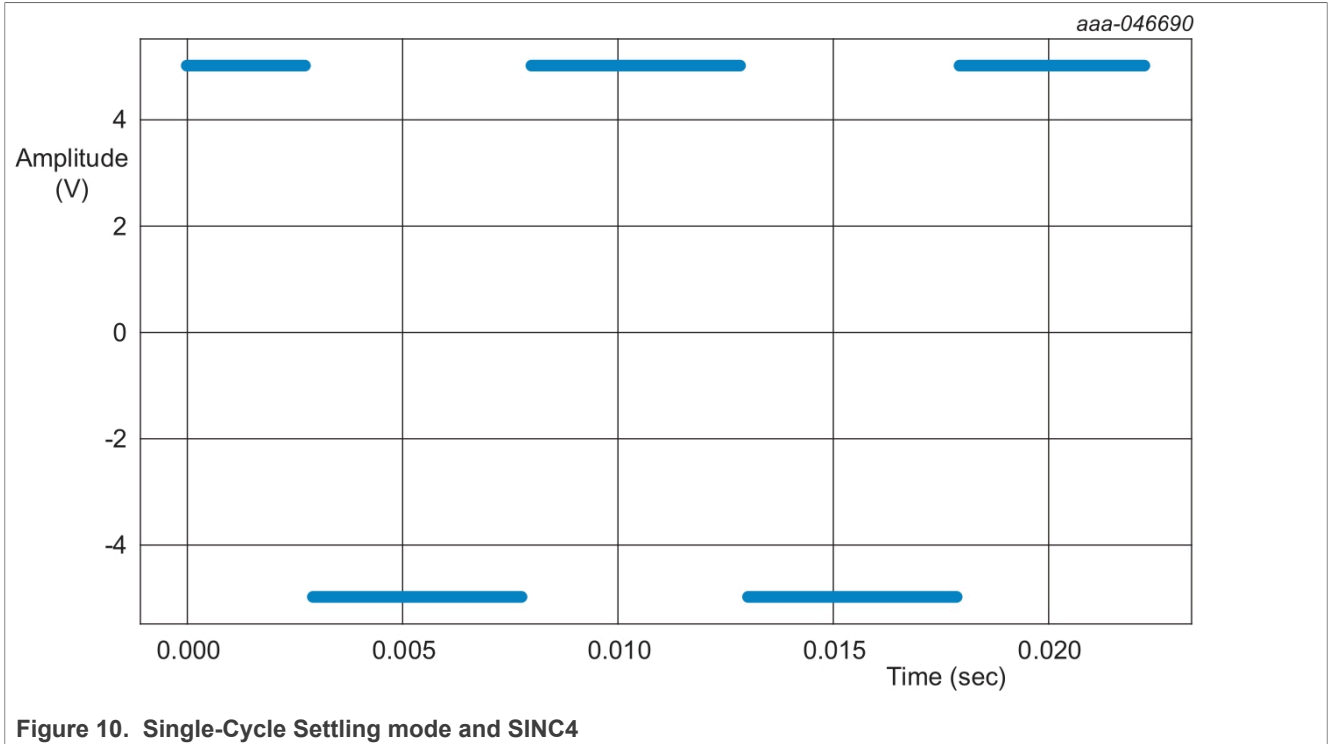


Figure 10. Single-Cycle Settling mode and SINC4

7.3.5.6 ADC data rate

Table 7 shows the programmable data rates for different SINC digital filters and Settling modes.

A total of 29 programmable data rates is available. The rates are set by channel-based CH\_CONFIG1 register bits ADC\_DATA\_RATE[4:0]. The highest data rate codes (DRO = 0..11) are with second-stage SINC filter bypassed, ADC\_SINC[2:0]=0. Moreover, data rates with Single-Cycle Settling modes are four times slower with respect to Normal Settling mode, CH\_CONFIG2 register bit ADC\_NORMAL\_SETTLING = 1. The final effective data rate, in Single-Cycle Settling mode, could be further reduced by CH\_DELAY[5:0]. The details are described in Section 7.5.3.3.

Although all conversions are from the 24-bit ADC, the data may be read out in 24-bit or 16-bit format by setting ADC\_DATA\_OUT\_16BIT bit in SYS\_CONFIG0 register.

Table 7. Data rate (system clock: 4.608 MHz)

DRO code	OSR	Normal settling					Single-cycle settling				
		SINC4	SINC4+ SINC1	SINC4+ SINC2	SINC4+ SINC2	SINC4+ SINC4	SINC4	SINC4+ SINC1	SINC4+ SINC2	SINC4+ SINC2	SINC4+ SINC4
0	8	288000					72000				
1	12	192000					48000				
2	16	144000					36000				
3	24	96000					24000				
4	32	72000					18000				
5	48	48000					12000				
6	64	36000					9000				
7	96	24000					6000				
8	128	18000					4500				
9	192	12000					3000				
10	256	9000					2250				

Table 7. Data rate (system clock: 4.608 MHz)...continued

11	384	6000					1500				
12	512		4500.00	4500.00	4500.00	4500.00		2250.00	1500.00	1125.00	900.00
13	768		3000.00	3000.00	3000.00	3000.00		1500.00	1000.00	750.00	600.00
14	1024		2250.00	2250.00	2250.00	2250.00		1125.00	750.00	562.50	450.00
15	2048		1125.00	1125.00	1125.00	1125.00		562.50	375.00	281.25	225.00
16	4096		562.50	562.50	562.50	562.50		281.25	187.50	140.63	112.50
17	5760		400.00	400.00	400.00	400.00		200.00	133.33	100.00	80.00
18	7680		300.00	300.00	300.00	300.00		150.00	100.00	75.00	60.00
19	11520		200.00	200.00	200.00	200.00		100.00	66.67	50.00	40.00
20	23040		100.00	100.00	100.00	100.00		50.00	33.33	25.00	20.00
21	38400		60.00	60.00	60.00	60.00		30.00	20.00	15.00	12.00
22	46080		50.00	50.00	50.00	50.00		25.00	16.67	12.50	10.00
23	76800		30.00	30.00	30.00	30.00		15.00	10.00	7.50	6.00
24	92160		25.00	25.00	25.00	25.00		12.50	8.33	6.25	5.00
25	115200		20.00	20.00	20.00	20.00		10.00	6.67	5.00	4.00
26	153600		15.00	15.00	15.00	15.00		7.50	5.00	3.75	3.00
27	230400		10.00	10.00	10.00	10.00		5.00	3.33	2.50	2.00
28	307200		7.50	7.50	7.50	7.50		3.75	2.50	1.88	1.50

The highest data rate is achieved with the lowest OSR, SINC4 only in Normal Settling mode.

7.3.5.7 Noise performance vs data rate

The NAFE13388 noise performance depends on the device configuration: data rate, PGA gain, digital filter order, and Settling mode configuration. Two settings that affect noise performance are data rate and PGA gain. Decreasing the data rate results in a proportional decrease of total noise because the equivalent noise bandwidth of the digital filter is reduced proportionally with the data rate. Increasing the gain reduces input referred noise of the NAFE13388 because the noise of the PGA is lower than the noise of the ADC. Noise performance also depends on the shape of the digital filter because the order of the digital filter decreases the equivalent noise bandwidth, which results in lower noise.

The table below lists the typical noise performance of gain equal to 0.2 to 16 V/V (corresponding input full-scale ranges of ±25 V to ±0.3125 V) as input-referred values.

The noise performance data are in units of μVRMS (RMS = root mean square) under the conditions listed.

The data shown in the noise performance tables represent typical performance in normal settling at TA = 25 °C and internal 2.5 V reference voltage. The noise data are acquired with inputs shorted and is based on continuous ADC readings for a period of ten seconds or 1024 samples, whichever occurs first. Repeated noise measurements may yield higher or lower noise performance results because of the statistical nature of the noise.

The following tables in this section report the noise performance versus data rate and PGA gain setting.

Effective number of bits (ENOB) is calculated from the RMS noise applying the following formula:

$$ENOB = \text{MIN}(\text{LOG}(\text{Full\_Scale\_Range} / \text{Noise\_RMS}, 2), 24)$$

$$\text{Full Scale Range} = \frac{10}{PGAGAIN}$$

7.3.5.7.1 Noise 24-bit option

Table 8. Noise  $\mu\text{Vrms}$  (24-bit)

Code	Data rate	2,304,000	Estimate noise ( $\mu\text{Vrms}$ ) vs. gain setting							
		OSR	0.2	0.4	0.8	1	2	4	8	16
0	288000	8	27946.8	13973.4	6986.7	5589.4	2794.7	1397.4	698.7	349.45
1	192000	12	7546.0	3773.0	1886.5	1509.2	754.6	377.4	188.8	94.62
2	144000	16	2984.2	1492.1	746.1	596.9	298.5	149.3	74.9	37.85
3	96000	24	818.1	409.1	204.6	163.7	82.0	41.2	21.1	11.50
4	72000	32	343.5	171.8	86.0	68.8	34.6	17.8	9.7	6.26
5	48000	48	137.2	68.7	34.5	27.7	14.2	7.8	5.1	4.09
6	36000	64	98.8	49.5	24.9	20.0	10.4	5.9	4.1	3.45
7	24000	96	76.3	38.2	19.2	15.5	8.1	4.6	3.2	2.80
8	18000	128	65.7	32.9	16.6	13.3	7.0	4.0	2.8	2.42
9	12000	192	53.6	26.8	13.5	10.9	5.7	3.3	2.3	1.98
10	9000	256	46.4	23.2	11.7	9.4	4.9	2.8	2.0	1.71
11	6000	384	37.9	19.0	9.6	7.7	4.0	2.3	1.6	1.40
12	4500	512	32.8	16.4	8.3	6.7	3.5	2.0	1.4	1.21
13	3000	768	26.8	13.4	6.8	5.4	2.8	1.6	1.1	0.99
14	2250	1024	23.2	11.6	5.9	4.7	2.5	1.4	1.0	0.86
15	1125	2048	16.4	8.2	4.1	3.3	1.7	1.0	0.7	0.61
16	562.5	4096	11.6	5.8	2.9	2.4	1.2	0.7	0.5	0.43
17	400	5760	9.8	4.9	2.5	2.0	1.0	0.6	0.4	0.36
18	300	7680	8.5	4.3	2.2	1.7	0.9	0.5	0.4	0.31
19	200	11520	7.0	3.5	1.8	1.4	0.7	0.4	0.3	0.26
20	100	23040	5.0	2.5	1.3	1.0	0.5	0.3	0.2	0.18
21	60	38400	3.9	2.0	1.0	0.8	0.4	0.2	0.2	0.14
22	50	46080	3.6	1.8	0.9	0.7	0.4	0.2	0.2	0.13
23	30	76800	2.9	1.4	0.7	0.6	0.3	0.2	0.1	0.10
24	25	92160	2.7	1.3	0.7	0.5	0.3	0.2	0.1	0.09
25	20	115200	2.4	1.2	0.6	0.5	0.3	0.1	0.1	0.08
26	15	153600	2.2	1.1	0.5	0.4	0.2	0.1	0.1	0.07
27	10	230400	1.9	0.9	0.5	0.4	0.2	0.1	0.1	0.06
28	7.5	307200	1.7	0.9	0.4	0.3	0.2	0.1	0.1	0.05

**7.3.5.7.2 ENOB 24-bit option**

**Table 9. ENOB (24-bit)**

Code	Data rate	2,304,000	Estimate noise (uVrms) vs. gain setting							
		OSR	0.2	0.4	0.8	1	2	4	8	16
0	288000	8	10.8	10.8	10.8	10.8	10.8	10.8	10.8	10.8
1	192000	12	12.7	12.7	12.7	12.7	12.7	12.7	12.7	12.7
2	144000	16	14.0	14.0	14.0	14.0	14.0	14.0	14.0	14.0
3	96000	24	15.9	15.9	15.9	15.9	15.9	15.9	15.8	15.6
4	72000	32	17.1	17.1	17.1	17.1	17.1	17.1	16.9	16.4
5	48000	48	18.4	18.4	18.4	18.4	18.4	18.2	17.7	16.9
6	36000	64	18.9	18.9	18.9	18.9	18.8	18.6	18.0	17.2
7	24000	96	19.3	19.3	19.3	19.2	19.2	18.9	18.3	17.5
8	18000	128	19.5	19.5	19.5	19.5	19.4	19.1	18.5	17.7
9	12000	192	19.8	19.8	19.8	19.8	19.7	19.4	18.8	18.0
10	9000	256	20.0	20.0	20.0	20.0	19.9	19.6	19.0	18.2
11	6000	384	20.3	20.3	20.3	20.3	20.2	19.9	19.3	18.5
12	4500	512	20.5	20.5	20.5	20.5	20.4	20.1	19.5	18.7
13	3000	768	20.8	20.8	20.8	20.7	20.7	20.4	19.8	19.0
14	2250	1024	21.0	21.0	21.0	21.0	20.9	20.6	20.0	19.2
15	1125	2048	21.5	21.5	21.5	21.5	21.4	21.1	20.5	19.7
16	562.5	4096	22.0	22.0	22.0	22.0	21.9	21.6	21.0	20.2
17	400	5760	22.2	22.2	22.2	22.2	22.1	21.8	21.3	20.4
18	300	7680	22.4	22.4	22.4	22.4	22.3	22.1	21.5	20.6
19	200	11520	22.7	22.7	22.7	22.7	22.6	22.3	21.8	20.9
20	100	23040	23.2	23.2	23.2	23.2	23.1	22.8	22.3	21.4
21	60	38400	23.2	23.2	23.2	23.2	23.1	22.8	22.3	21.4
22	50	46080	23.7	23.7	23.7	23.6	23.6	23.3	22.8	21.9
23	30	76800	24.0	24.0	24.0	24.0	23.9	23.7	23.1	22.3
24	25	92160	24.0	24.0	24.0	24.0	24.0	23.8	23.2	22.4
25	20	115200	24.0	24.0	24.0	24.0	24.0	23.9	23.4	22.6
26	15	153600	24.0	24.0	24.0	24.0	24.0	24.0	23.6	22.8
27	10	230400	24.0	24.0	24.0	24.0	24.0	24.0	23.9	23.1
28	7.5	307200	24.0	24.0	24.0	24.0	24.0	24.0	24.0	23.9

7.3.5.7.3 Noise 16-bit option

Table 10. Noise (16-bit)

Code	Data rate	2,304,000	Estimate ENOB vs PGA gain setting							
		OSR	0.2	0.4	0.8	1	2	4	8	16
0	288000	8	27948.3	13974.1	6987.1	5589.7	2794.9	1397.5	698.8	349.54
1	19200	12	7551.2	3775.6	1887.8	1510.3	755.2	377.7	189.0	94.85
2	14400	16	2997.3	1498.7	749.4	599.5	299.8	150.1	75.4	38.32
3	96000	24	864.1	432.1	216.1	172.9	86.7	43.7	22.6	12.64
4	72000	32	441.7	220.9	110.6	88.5	44.5	22.8	12.4	7.93
5	48000	48	309.0	154.5	77.4	62.0	31.2	16.1	9.0	6.04
6	36000	64	293.6	146.8	73.5	58.8	29.6	15.2	8.4	5.45
7	24000	96	286.4	143.2	71.7	57.4	28.8	14.7	7.9	4.86
8	18000	128	283.6	141.8	71.0	56.8	28.5	14.5	7.6	4.55
9	24000	192	280.8	140.4	70.2	56.2	28.2	14.2	7.4	4.21
10	9000	256	279.5	139.7	69.9	55.9	28.0	14.1	7.3	4.03
11	6000	384	278.1	139.1	69.5	55.6	27.9	14.0	7.1	3.84
12	4500	512	277.4	138.7	69.4	55.5	27.8	13.9	7.1	3.75
13	2250	1024	276.3	138.2	69.1	55.3	27.7	13.9	7.0	3.60
14	1125	2048	275.8	137.9	69.0	55.2	27.6	13.8	6.9	3.52
15	562.5	4096	275.6	137.8	68.9	55.1	27.6	13.8	6.9	3.48
16	300	7680	275.4	137.7	68.9	55.1	27.5	13.8	6.9	3.46
17	225	10240	275.4	137.7	68.9	55.1	27.5	13.8	6.9	3.46
18	150	15360	275.4	137.7	68.8	55.1	27.5	13.8	6.9	3.45
19	100	23040	275.3	137.7	68.8	55.1	27.5	13.8	6.9	3.45
20	50	46080	275.3	137.7	68.8	55.1	27.5	13.8	6.9	3.44
21	30	76800	275.3	137.7	68.8	55.1	27.5	13.8	6.9	3.44
22	25	92160	275.3	137.7	68.8	55.1	27.5	13.8	6.9	3.44
23	15	153600	275.3	137.7	68.8	55.1	27.5	13.8	6.9	3.44
24	12.5	184320	275.3	137.7	68.8	55.1	27.5	13.8	6.9	3.44
25	10	230400	275.3	137.7	68.8	55.1	27.5	13.8	6.9	3.44
26	5	460800	275.3	137.7	68.8	55.1	27.5	13.8	6.9	3.44
27	2.5	921600	275.3	137.7	68.8	55.1	27.5	13.8	6.9	3.44
28	1.25	1843200	275.3	137.7	68.8	55.1	27.5	13.8	6.9	3.44

7.3.5.7.4 ENOB 16-bit option

Table 11. ENOB (16-bit)

Code	Data rate	2,304,000	Estimate ENOB vs gain setting							
		OSR	0.2	0.4	0.8	1	2	4	8	16
0	288000	8	10.8	10.8	10.8	10.8	10.8	10.8	10.8	10.8
1	19200	12	12.7	12.7	12.7	12.7	12.7	12.7	12.7	12.7
2	14400	16	14.0	14.0	14.0	14.0	14.0	14.0	14.0	14.0
3	96000	24	15.8	15.8	15.8	15.8	15.8	15.8	15.8	15.6
4	72000	32	16.0	16.0	16.0	16.0	16.0	16.0	16.0	16.0
5	48000	48	16.0	16.0	16.0	16.0	16.0	16.0	16.0	16.0
6	36000	64	16.0	16.0	16.0	16.0	16.0	16.0	16.0	16.0
7	24000	96	16.0	16.0	16.0	16.0	16.0	16.0	16.0	16.0
8	18000	128	16.0	16.0	16.0	16.0	16.0	16.0	16.0	16.0
9	24000	192	16.0	16.0	16.0	16.0	16.0	16.0	16.0	16.0
10	9000	256	16.0	16.0	16.0	16.0	16.0	16.0	16.0	16.0
11	6000	384	16.0	16.0	16.0	16.0	16.0	16.0	16.0	16.0
12	4500	512	16.0	16.0	16.0	16.0	16.0	16.0	16.0	16.0
13	2250	1024	16.0	16.0	16.0	16.0	16.0	16.0	16.0	16.0
14	1125	2048	16.0	16.0	16.0	16.0	16.0	16.0	16.0	16.0
15	562.5	4096	16.0	16.0	16.0	16.0	16.0	16.0	16.0	16.0
16	300	7680	16.0	16.0	16.0	16.0	16.0	16.0	16.0	16.0
17	225	10240	16.0	16.0	16.0	16.0	16.0	16.0	16.0	16.0
18	150	15360	16.0	16.0	16.0	16.0	16.0	16.0	16.0	16.0
19	100	23040	16.0	16.0	16.0	16.0	16.0	16.0	16.0	16.0
20	50	46080	16.0	16.0	16.0	16.0	16.0	16.0	16.0	16.0
21	30	76800	16.0	16.0	16.0	16.0	16.0	16.0	16.0	16.0
22	25	92160	16.0	16.0	16.0	16.0	16.0	16.0	16.0	16.0
23	15	153600	16.0	16.0	16.0	16.0	16.0	16.0	16.0	16.0
24	12.5	184320	16.0	16.0	16.0	16.0	16.0	16.0	16.0	16.0
25	10	230400	16.0	16.0	16.0	16.0	16.0	16.0	16.0	16.0
26	5	460800	16.0	16.0	16.0	16.0	16.0	16.0	16.0	16.0
27	2.5	921600	16.0	16.0	16.0	16.0	16.0	16.0	16.0	16.0
28	1.25	1843200	16.0	16.0	16.0	16.0	16.0	16.0	16.0	16.0

7.3.6 Gain and offset calibration

All NAFE family products include 46 user-accessible calibration coefficient registers divided into three groups:

- **Gain:** GAIN\_COEF0[23:0] to GAIN\_COEF15[23:0]
- **Offset:** OFFSET\_COEF0[23:0] to OFFSET\_COEF15[23:0]



- **Optional:** OPT\_COEF0[23:0] to OPT\_COEF15[23:0]

To reduce the calibration error, the bit-width of gain, offset, and self-calibration coefficient registers are 24-bit wide, the same as main ADC.

The above user-calibration coefficients can be read and written by the user. During device power up or reset, the factory calibrated coefficients stored in NVM are loaded into the preset registers, if available. The user may overwrite with different calibration coefficients as needed.

In general, there are three categories of calibration coefficients:

- System offset and gain calibration coefficients for voltage or current input
- System offset and gain calibration coefficients for resistance and RTD input
- Self-calibration values
  - 2.5 V VREF
  - 2.3 V REFH and 0.2 V REFL

These features enable accurate dynamic self-calibration without external voltage sources and advanced predictive maintenance.

[Table 12](#) describes the calibration gain/offset coefficient pair, addressable by coefficient pointer CH\_CONFIG1.CH\_CAL\_GAIN\_OFFSET.

**Note:** The gain and offset coefficients are channel-gain setting dependent.

**Table 12. System gain and offset calibration registers**

Pointer	Gain register	ADDR \h	Offset register	ADDR \h	NVM stored coefficient and setting
0	GAIN_COEF0[23:0]	80	OFFSET_COEF0[23:0]	90	Gain = 0.2 V/V, single-ended Alxx-AICOM
1	GAIN_COEF1[23:0]	81	OFFSET_COEF1[23:0]	91	Gain = 0.4 V/V, single-ended Alxx-AICOM
2	GAIN_COEF2[23:0]	82	OFFSET_COEF2[23:0]	92	Gain = 0.8 V/V, single-ended Alxx-AICOM
3	GAIN_COEF3[23:0]	83	OFFSET_COEF3[23:0]	93	Gain = 1 V/V, single-ended Alxx-AICOM
4	GAIN_COEF4[23:0]	84	OFFSET_COEF4[23:0]	94	Gain = 2 V/V, single-ended Alxx-AICOM
5	GAIN_COEF5[23:0]	85	OFFSET_COEF5[23:0]	95	Gain = 4 V/V, single-ended Alxx-AICOM
6	GAIN_COEF6[23:0]	86	OFFSET_COEF6[23:0]	96	Gain = 8 V/V, single-ended Alxx-AICOM
7	GAIN_COEF7[23:0]	87	OFFSET_COEF7[23:0]	97	Gain = 16 V/V, single-ended Alxx-AICOM
8	GAIN_COEF8[23:0]	88	OFFSET_COEF8[23:0]	98	-
9	GAIN_COEF9[23:0]	89	OFFSET_COEF9[23:0]	99	-
10	GAIN_COEF10[23:0]	8A	OFFSET_COEF10[23:0]	9A	-
11	GAIN_COEF11[23:0]	8B	OFFSET_COEF11[23:0]	9B	-
12	GAIN_COEF12[23:0]	8C	OFFSET_COEF12[23:0]	9C	-
13	GAIN_COEF13[23:0]	8D	OFFSET_COEF13[23:0]	9D	-
14	GAIN_COEF14[23:0]	8E	OFFSET_COEF14[23:0]	9E	-
15	GAIN_COEF15[23:0]	8F	OFFSET_COEF15[23:0]	9F	-

**Table 13. Optional and RTD calibrated coefficients register**

CAL REGISTER	NVM stored parameter	Nominal value	Stored format	Setting description
OPT_COEF0[23:0]	VREFP_ADC	2.496 V	(VREF/5)*2^24	Factory measured voltage across pins REFP_ADC - REFN_ADC
OPT_COEF1[23:0]	REFH - GND	2.29632 V	(REFH/5)*2^24	ADC converted voltage after factory CAL. gain = 0.8 V/V, TCC_OFF = 1, CH_CHOP = 1
OPT_COEF2[23:0]	REFL - GND	0.19968 V	(REFL/5)*2^24	ADC converted voltage after factory CAL. gain = 16 V/V, TCC_OFF = 1, CH_CHOP = 1.

Table 13. Optional and RTD calibrated coefficients register...continued

CAL REGISTER	NVM stored parameter	Nominal value	Stored format	Setting description
OPT_COEF3[23:0]	RTD_OFFSET1	0		Factory CAL coefficient for gain = 16 V/V, VIEX_VI = 1, VIEX_MAG = 9ld (250 uA)
OPT_COEF4[23:0]	RTD_GAIN1	1	G = 2 <sup>24</sup> /4	Factory CAL coefficient for gain = 16 V/V, VIEX_VI = 1, VIEX_MAG = 9ld (250 uA)
OPT_COEF5[23:0]	RTD_OFFSET2	0		Factory CAL coefficient for gain = 8 V/V, VIEX_VI = 1, VIEX_MAG = 11ld (500 uA)
OPT_COEF6[23:0]	RTD_GAIN2	1	G = 2 <sup>24</sup> /4	Factory CAL coefficient for gain = 8 V/V, VIEX_VI = 1, VIEX_MAG = 11ld (500 uA)
OPT_COEF7[23:0]	RTD_OFFSET3	0		Factory CAL coefficient for gain = 4 V/V, VIEX_VI = 1, VIEX_MAG = 13ld (1 mA)
OPT_COEF8[23:0]	RTD_GAIN3	1	G = 2 <sup>24</sup> /4	Factory CAL coefficient for gain = 4 V/V, VIEX_VI = 1, VIEX_MAG = 13ld (1 mA)
OPT_COEF9[23:0]	RTD_OFFSET4	0		Factory CAL coefficient for gain = 0.8 V/V, VIEX_VI = 1, VIEX_MAG = 13ld (1 mA)
OPT_COEF10[23:0]	RTD_GAIN4	1	G = 2 <sup>24</sup> /4	Factory CAL coefficient for gain = 0.8 V/V, VIEX_VI = 1, VIEX_MAG = 13ld (1 mA)
OPT_COEF11[23:0]				
OPT_COEF12[23:0]				
OPT_COEF13[23:0]				
OPT_COEF14[23:0]				
OPT_COEF15[23:0]				

**Note:** Units used in nominal value: voltage (V), gain (V/V), offset (V)

7.3.6.1 Gain and offset calibration coefficients

The NAFE product family includes 16 pairs of offset and gain calibration registers and internal adder and multiplier for offset and gain compensation.

Offset calibration registers are 24-bit wide. Their values are in two’s complement format with a minimum negative value equal to 80\_0000h and a maximum positive value equal to 7F\_FFFFh. A register value of 00\_0000h has no offset correction.

$$Offset = \left( \frac{10}{2^{24}} \right) \cdot \frac{1}{GAIN} \cdot \left( mod(hex2dec(COEF) + 2^{23}, 2^{24}) - 2^{23} \right)$$

Gain calibration registers are 24-bit wide. Their values are straight binary format. The registers map a gain range from 0 to 3.99999976158142. The unity gain value is 40\_0000h. Table 14 shows the full range of gain factor correction.

$$Gain = \frac{COEF}{2^{22}}$$

The NAFE13388 output equation with internal digital calibration is as follows:

$$AFE_{OUT} = ( ADCOUT - CAL\_OFFSET ) \cdot CAL\_GAIN$$

Table 14. Gain calibration coefficient and factor

Gain calibration coefficient (Hexadecimal)	Gain calibration coefficient (Decimal)	Gain calibration factor = Gain_coeff./(2 <sup>22</sup> )
FFFFFF	16777215	3.9999998
800000	8388608	2.0000000
400001	4194305	1.0000002

Table 14. Gain calibration coefficient and factor...continued

Gain calibration coefficient (Hexadecimal)	Gain calibration coefficient (Decimal)	Gain calibration factor = Gain_coeff./(2^22)
400000	4194304	1.0000000
3FFFFFF	4194303	0.9999998
200000	2097152	0.5000000
000000	0	0.0000000

Table 15. Offset calibration coefficient and factor

Offset calibration coefficient (Hexadecimal)	Offset calibration coefficient (Decimal)	Offset calibration PGA = 0.2 (V)
7FFFFFF	8388607	24.9999970
400000	4194304	12.5000000
000001	1	0.0000030
000000	0	0.0000000
FFFFFFF	-1	-0.0000030
C00000	-4194304	-12.5000000
800000	-8388608	-25.0000000

7.3.6.2 Factory calibrated coefficients

NAFE13388 products come with a factory calibration option that is supplemented with factory digitally calibrated coefficients (CAL) stored in the internal NVM register. The calibrated gain/offset coefficient pairs are accessible through the calibration registers, GAIN\_COEF0[23:0].. GAIN\_COEF 15[23:0] and OFFSET\_COEF0[23:0]..OFFSET\_COEF15[23:0]. At the power up, the calibrated coefficients are uploaded from the NVM to the user-calibration coefficients registers.

**Note:** The coefficients stored in NVM are loaded into their respective registers every time upon power up, reset or CMD\_RELOAD.

As the registers for gain (GAIN\_COEFi[23:0]) and offset (OFFSET\_COEFi[23:0]) coefficient pairs are read/write accessible, the user may shuffle the location of the calibrated coefficient pairs as necessary.

**Note:** There is only one register, CH\_CONFIG1.CH\_CAL\_GAIN\_OFFSET[3:0], to address the calibrated coefficient pair to be used for each channel setup.

The gain and offset coefficient pair is programmed to use one of the 16 gain/offset registers with the same index or the address with matching 4-bit in the lowest nibble. That is, GAIN\_COEF0(0x80) is to be paired with OFFSET\_COEF0(0x90). Similarly GAIN\_COEF1(0x81) is paired with OFFSET\_COEF1(0x91), and GAIN\_COEF15(0x8F) is paired with OFFSET\_COEF15(0x9F).

7.3.6.3 Loading and use

Upon chip power up, the factory calibration coefficients are uploaded from NVM to user-calibration coefficient registers GAIN\_COEFi[23:0], OFFSET\_COEFi[23:0], OPT\_COEFi[23:0]. When CHIP\_READY bit in SYS\_STATUS0 register is asserted to 1, that indicates the chip is ready to perform conversion.

For ADC conversion on the logical channel (default is channel 0, CH0), a pair of offset and gain coefficients is mated with each logical channel by register CH\_CONFIG1.CH\_CAL\_GAIN\_OFFSET[3:0]. Before the

conversion takes place, the value in the designated pair of offset and gain coefficient will be latched into the internal registers to be used for compensating internal gain and offset errors. The user may shuffle GAIN\_COEF and OFFSET\_COEF when setting up the logical channel after initialization or power up. For example, setting channel CH0 to gain = 0.8 V/V, the user will need to set GAIN\_COEF0[23:0] and OFFSET\_COEF0[23:0] with the calibrated coefficient to gain = 0.8 V/V and so forth. See [Table 12](#) for the stored location of each gain-dependent coefficients.

The selected channel for read/write register configuration is indicated by using the pointer position. The position is displayed in bit CONFIG\_CH\_PTR[3:0]. Similarly, the active ADC conversion on channel-pointer position is shown in bit ADC\_CONV\_CH[3:0]

SPI command CMD\_RELOAD will reload the factory calibrated coefficients from internal non-volatile memory into registers GAIN\_COEF, OFFSET\_COEF and OPT\_COEF. This will overwrite previously modified values. When CMD\_RELOAD is issued, the status bit SYS\_STATUS0.CHIP\_READY will be deasserted. It will then be asserted when NVM data reloading is complete.

### 7.3.7 Temperature coefficient correction

TCC\_OFF = 0 enables a temperature coefficient correction that reduces the temperature drift error. Set this bit to 1 to disable the TCC feature for any of the following three situations:

- REF\_EXT is used
- The ratiometric measurement is used with internal reference (SYS\_CONFIG0.REF\_SEL[1:0] = 00h)
- The following input signals are used: REFH (= VREF\*0.92), REFL (= VREF\*0.08), VIEX\_VI (excitation voltage or current source)

### 7.3.8 Voltage reference

#### 7.3.8.1 Low-drift voltage reference 1

The NAFE13388 integrates a voltage reference with calibrated TCC coefficients to reduce the drift error over temperature. Set register bits TCC\_OFF = 0 to apply TCC coefficients for non-ratiometric measurement. If external voltage reference is used as ADC reference, set TCC\_OFF = 1.

#### 7.3.8.2 Coarse voltage reference 2

The NAFE13388 includes a second and independent internal coarse voltage reference for diagnostic purpose.

#### 7.3.8.3 Voltage reference selector

The voltage reference selector enables the selection of either internal or external reference, or a combination of internal and external reference by setting register bits REF\_SEL[1:0]. External 2.5 V voltage reference is applied at REF\_EXT pin when required. See [Table 31](#).

### 7.3.9 Excitation source

The NAFE13388 includes two programmable excitation DAC outputs, a voltage source and a current source. Different magnitudes, polarities, and output pins can be selected using CH\_CONFIG3 register bits accordingly.

The programmable excitation sources can be used for input impedance measurement, biasing of RTD, self-calibration, built-in self-test (BIST) and self-monitoring channel readback.

Because the excitation source is shared, the HVMUXOUT multiplexers are enabled to route voltage/current excitation to appropriate HVMUX inputs. For persistent V/I source connection to a particular input, the corresponding HVMUXOUT needs to be selected and VI\_MAG set to a value greater than zero.

If the voltage reference for the V/I source DAC and ADC are common, the measurement associated with it is ratiometric. This is desirable as the absolute value of VREF is less of a concern.

[Table 16](#) shows the DAC code and the corresponding voltage or current output values. The polarity bit sets the voltage and current output polarity.

**Table 16. Programmable excitation V/I source: DAC code, magnitude, and polarity**

Polarity bit = 0			Polarity bit = 1		
DAC code	VEXC Magnitude (V)	IEXC Magnitude (A)	DAC code	VEXC Magnitude (V)	IEXC Magnitude (A)
0	0.000	000.0E+0	0	0.000	000.0E+0
1	0.006	977.0E-9	1	-0.006	-977.0E-9
2	0.012	2.0E-6	2	-0.012	-2.0E-6
3	0.023	3.9E-6	3	-0.023	-3.9E-6
4	0.047	7.8E-6	4	-0.047	-7.8E-6
5	0.094	15.6E-6	5	-0.094	-15.6E-6
6	0.188	31.3E-6	6	-0.188	-31.3E-6
7	0.375	62.5E-6	7	-0.375	-62.5E-6
8	0.750	125.0E-6	8	-0.750	-125.0E-6
9	1.500	250.0E-6	9	-1.500	-250.0E-6
10	2.250	375.0E-6	10	-2.250	-375.0E-6
11	3.000	500.0E-6	11	-3.000	-500.0E-6
12	4.500	750.0E-6	12	-4.500	-750.0E-6
13	6.000	1.0E-3	13	-6.000	-1.0E-3
14	9.000	1.5E-3	14	-9.000	-1.5E-3
15	12.000	2.0E-3	15	-12.000	-2.0E-3

**7.3.9.1 Voltage current sources polarity switching**

If VIEX\_CHOP bit is set, two ADC conversions will be performed, such that the first conversion will take on the current polarity set by VIEX\_POL and the second conversion will follow with the opposite polarity. The final ADC output is an average of the difference of two conversions. The DAC value will be reverted to the initial value at the end of the second conversion. This VIEX chop enables the cancellation of any internal and external systematic offset presented in the signal path.

Use of VIEX\_POL for polarity change of the output voltage or current source, the Common mode voltage of the sensing circuitry could be removed by averaging the difference of two ADC conversions. The input Common mode voltage could be removed.

**7.3.9.2 Calibrated resistance measurement**

To provide end-to-end resistance calibration, additional sets of factory gain and offset calibration coefficients are also provided. See [Table 13](#) for further details.

7.3.9.3 Open detection current (ODC)

NAFE13388 includes a dedicated 65 nA current source, see ODC in [Figure 1](#), for open detection on the selected AI channel. Selection of ODC supersedes the the VIEX\_VI selection as mentioned in [Table 29](#).

7.3.10 Temperature sensor

The NAFE13388 includes a temperature sensor to monitor the IC junction temperature and provides temperature alarm with user-programmable threshold. Overtemperature warning and shutdown factory defaults are 145 °C and 165 °C, respectively.

7.3.11 General-purpose input/output

The NAFE13388 includes ten GPIOs. The operating input and output voltage ranges are 0 V to VDD when pins GPIO0..9 are configured as GPIO.

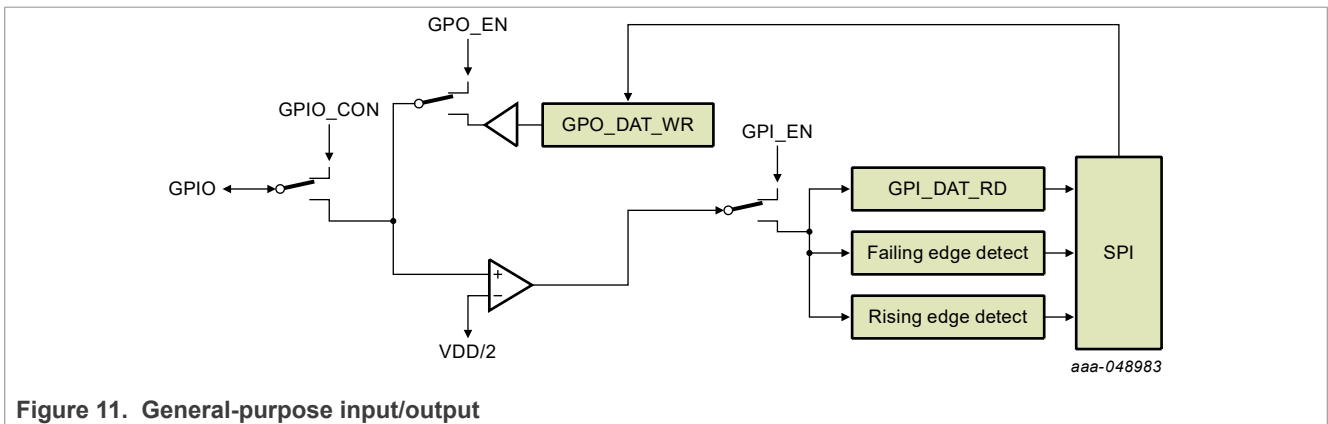


Figure 11. General-purpose input/output

The GPIO control and data registers are organized in the following registers, right-aligned in 16-bit space:

GPI\_DATA (0x29\h): Read (R) only register. It detects input logic level signal at the corresponding pin.

GPIO\_CONFIG0 (0x2A\h): Read/Write (R/W) GPO\_EN register. It enables an output path.

GPIO\_CONFIG1(0x2B\h): R/W GPIO\_CON register. It connects the internal circuitry to GPIO pins for either out or input function as programmed by user.

GPIO\_CONFIG2 (0x2C\h): R/W GPI\_ENABLE. It enables the input path to allow reading data from PAD, looping back from GPO\_DATA register and/or GPIO edges detection.

GPIO double edge detection (low-to-high and high-to-low) results in 2x10-bit register GPI\_EDGE\_POS(0x2D) for positive and GPI\_EDGE\_NEG(0x2E) for negative, respectively, are implemented as follows.

While GPIO\_CONFIG2.GPI\_ENABLE[i] and GPIO\_CONFIG1.GPIO\_CON[i] = 1, any transition from 0 -> 1 (positive edge) or 1 -> 0 (negative edge) the edge detection register is set to 1. These edge detection registers, GPI\_POS\_EDGE and GPI\_NEG\_EDGE, are defined as a sticky by nature and requires the host to clear it by writing 1 to the bit that is set to 1 (W1C) by the previous event.

Some GPIOs, such as GPIO0, GPIO1, GPIO2, and GPIO9 serve dual functions.

The GPIO0 and GPIO1, in addition to general-purpose digital input and output function, serve as differential analog input GPIO0-GPIO1 by selecting the appropriate input in LVMUXIN multiplexer. The input common voltage range is from 0.5 V to 2.5 V.

The GPIO9 can output the system clock for synchronization by writing '1' to SYS\_CONFIG0.MCLK\_OUT\_ENABLE.

GPIO2 can provide CRC\_ERROR status flag by writing '1' to SYS\_CONFIG0.CRC\_EN.

**7.3.12 Clock sources**

The NAFE13388 provides flexible and configurable clocking modes. It can function with three different clock sources: internal RC oscillator, oscillator with external crystal, external oscillator.

Figure 12 shows the clock architecture.

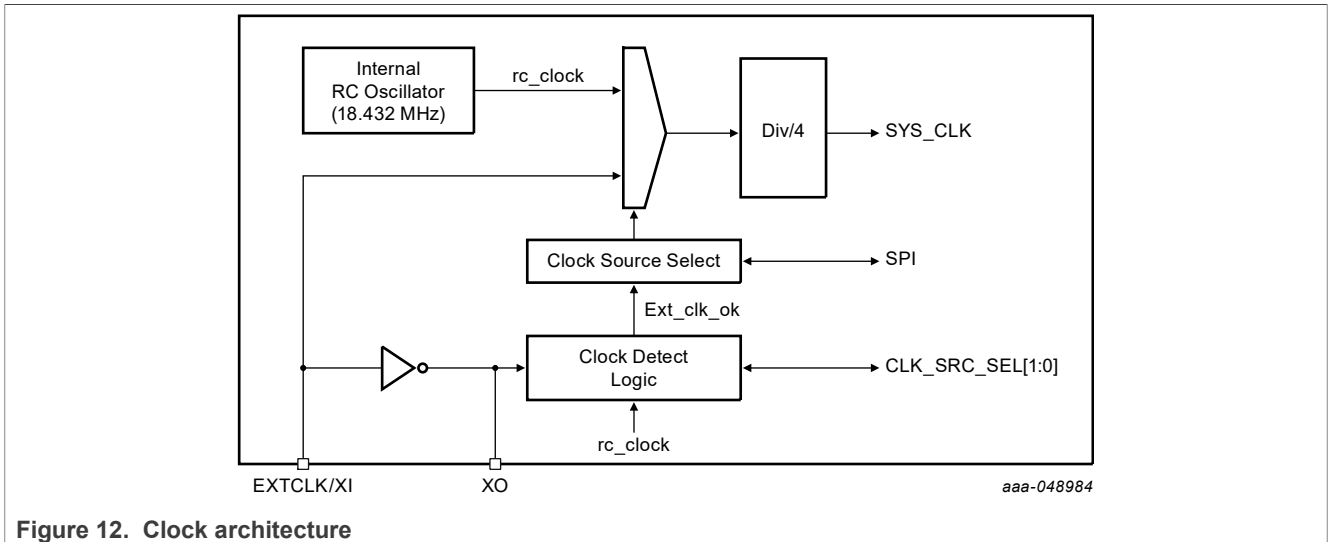


Figure 12. Clock architecture

**7.3.12.1 Internal RC oscillator**

The NAFE13388 integrates an internal oscillator to allow autonomous and cost-effective operation without support of any external clock source.

The internal oscillator nominal frequency is 18.432 MHz.

**7.3.12.2 Oscillator with external crystal**

The oscillator with external crystal enables all the applications that require more accurate and stable clock frequency.

The 18.432 MHz external crystal is installed between pins EXTCLK/XI and XO with the appropriate loading caps.

**7.3.12.3 External oscillator**

The NAFE13388 can operate with an external oscillator. Operating in this manner enables applications that require synchronization between the NAFE13388 and the host, as well as coherent sampling of the input signal.

The external oscillator should be applied to pin EXTCLK/XI.

**7.3.12.4 Clock selection**

The NAFE13388 provides two mechanisms for system clock source selection:

- Auto-selection upon power on
- User selection via system register configuration

### 7.3.12.5 Auto-selection of clock source

The automatic clock selection detects the presence of either the crystal oscillator or an external clock pulse upon power up and switches over to the available clock source.

The first phase detects if the clock is present at XI pin, by expecting at least 256 clock pulses within a 1 ms window. If the first detection phase is true, then the second detection is skipped and the logic sets the SRC\_SEL[1:0] to 2'b10. Detection is complete at this point with the external clock used as the system clock.

When the first phase detection is not true, the second phase is set to detect if the crystal is installed. The logic looks for at least 256 clock pulses within a 31 ms window. If the second phase detection is true, the logic sets the SRC\_SEL[1:0] to 2'b11. Detection is complete at this point with the external crystal set as the system clock.

If both phases of detection are not true, the SRC\_SEL [1:0] is not updated. It remains at the default 2'b00, which implies the internal clock is used. Then, CLK\_DET\_DONE is asserted 1 when both phases are complete. After CLK\_DET\_DONE = 1, the internal digital CHIP\_RDY is asserted to 1.

### 7.3.12.6 User selection of clock sources

The user selection option allows the user to select the desired clock after power on. The clock source can be selected by writing to the clock source system configuration register.

Check the presence of the external clock while making external clock selection in system configuration register to ensure proper functioning of the NAFE13388. If the external clock is detected and the NAFE13388 switches to the external clock, the system status register is updated accordingly. If the external clock is not detected, the NAFE13388 maintains the previous clock configuration.

### 7.3.12.7 Clock period drift detection

Whenever SRC\_SEL[1:0] is set to 2'b11 or 2'b10 by the user or by the auto-detect logic, one-time switch over at power-on reset (POR), the clock period monitoring circuit is activated to continuously measure the clock period difference between the external clock and internal RC Oscillator.

The typical value of clock period difference is set to 20 % at POR. The clock comparison logic issues an alarm when the running average clock count difference is greater than 20 %. The internal oscillator clock is the main reference. The alarm status bit for clock variation is user accessible via SPI register. The average time window is ~128 ms. If external clock is selected to be used as the system clock source and while EXTCLK\_FREQ\_ALARM bit is enabled, the external clock alarm interrupt triggers (EXTCLK\_FREQ\_INT = 1) whenever the EXTCLK is over the 20 % period difference.

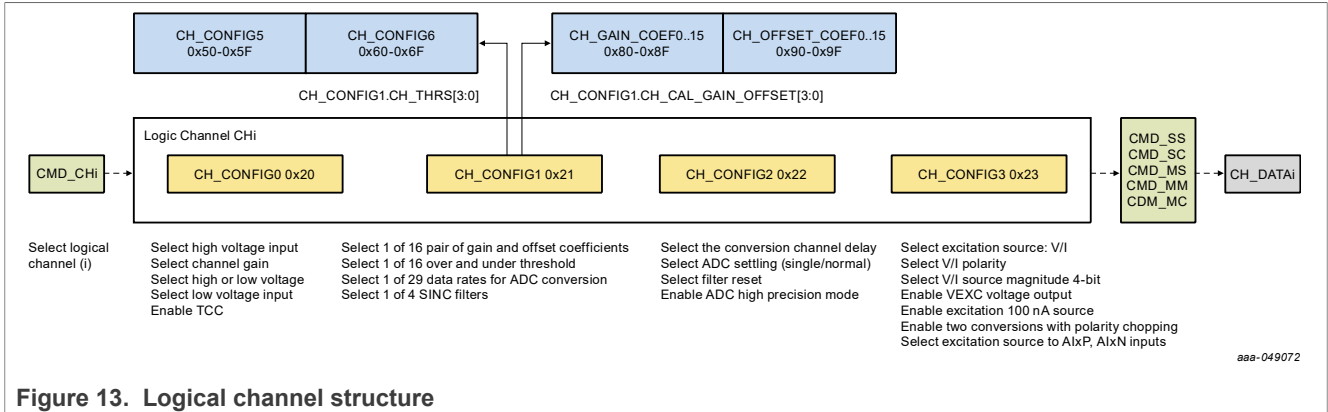
## 7.4 Channel configuration and multichannel sequencer

### 7.4.1 Channel configuration

The NAFE13388 has eight HV configurable analog inputs, LV diagnostic signals, and on-chip scaled reference voltages for built-in self-test (BIST), self-calibration, and a channel-based excitation V/I source. Coupling the various inputs with channel-based ADC configurations allows a highly flexible analog input configuration. With the channel-based configurations, the user may switch among the configured channels seamlessly, and without the need to perform multiple SPI transactions to set up various configurations before each ADC conversion. The 16 configurable logical channels are all independent and the associated registers. [Figure 13](#) shows structure of one logic channel:



NAFE13388 Universal ±25 V 8-input low-power AFE with excitation sources



- Channel configuration registers: CH\_CONFIG0, CH\_CONFIG1, CH\_CONFIG2, and CH\_CONFIG3.
  - CH\_CONFIG0 (0x20h)
    - Select input channel, either high voltage (HV\_AIP/HV\_AIN, HV\_SEL=1) or low voltage (LVSIG\_IN[2:0], HV\_SEL = 0).
    - Select one of the eight channel gains if high-voltage input is selected.
    - Disable/enabled the channel temperature coefficients correction (TCC\_OFF = 1).
  - CH\_CONFIG1 (0x21h)
    - Set the pointer (CH\_CAL\_GAIN\_OFFSET[3:0]) to select one of the 16 calibrated gain and offset coefficient pairs in the calibrated channel coefficient registers: GAIN\_COEF0...15 and OFFSET\_COEF0...15.
    - Set the pointer (CH\_THRS[3:0]) to select one of the 16 channel over- and under-range threshold pairs: CH\_CONFIG5.OVR\_THRS0...15 and CH\_CONFIG6.UDR\_THRS0...15.
    - Select one of 29 possible data rates: ADC\_DATA\_RATE[4:0].
    - Select one of the five possible filter options for second-stage SINC filter: ADC\_SINC[2:0].
  - CH\_CONFIG2 (0x22h)
    - Select one of the 64 possible preset channel delays before ADC start conversion: CH\_DELAY[5:0].
    - Select ADC Settling mode, single-cycle, or normal: ADC\_NORMAL\_SETTLING.
    - Select to reset ADC digital filters at the start of every ADC conversion: ADC\_FILTER\_RESET.
    - Select to enable input channel level chopping with two ADC conversions (Precision mode): CH\_CHOP = 1.
  - CH\_CONFIG3 (0x23h)
    - Select excitation source: voltage or current (V/I).
    - Select V/I polarity: positive or negative.
    - Excitation V/I source magnitude 4 bits.
    - Enable voltage source to direct route to HVMUX as one of the selectable inputs for ADC conversion.
    - Enable 65 nA source current for open detection.
    - Enable VIEX chopping with two conversions (see VIEX\_CHOP section).
    - Select one of the AIxP or AIxN pins for excitation V/I output.
- Channel gain coefficients: GAIN\_COEF0..15 [23:0] (0x80 – 0x8F)
  - These 16 24-bit calibrated gain coefficients are used to correct the gain error for the selected logic channel. The uncalibrated default is equivalent to 1 V/V.
- Channel offset coefficients: OFFSET\_COEF0..15[23:0] (0x90 – 0x9F)
  - These 16 24-bit calibrated offset coefficients are used to correct the offset error for the selected logic channel. The uncalibrated default offset value is 0 V.
- Channel input range detect threshold
  - CH\_CONFIG5 (0x50..0x5F): Over-range 24-bit threshold setting

These 16 24-bit registers are used to set the over-range threshold values.

- CH\_CONFIG6 (0x60..0x6F): Under-range 24-bit threshold setting

These 16 24-bit registers are used to set the under-range threshold values.

- Channel output data
  - CH\_DATA $[i]$ [23:0]: Holds ADC converted output data as selected by CMD\_CH $i$ . CH0 data is address 0x40 and CH15 data address is 0x4F.
- Channel status
  - CH\_STATUS0 $[i]$ : Over-range status bit. CH0 status is in bit[0] and CH15 is in bit[15].
  - CH\_STATUS1 $[i]$  - Under-range status bit. CH0 status is in bit[0] and CH15 is in bit[15].

Upon startup, chip reset, and register clear, each of the logical channels is to be reconfigured once. Channel gain/offset coefficients are preloaded from the on-chip NVM after POR. The user could overwrite these coefficients after the POR.

Channel select, CMD\_CH $i$  :

- SPI command CMD\_CH $i$  is used to select the logic channel CH $i$ , and the CH\_DATA $i$ , where  $i = 0..15$  is the channel index.
- Channel configuration is activated after the conversion command is issued.
- The activated logical channel is indicated by reading CONFIG\_CH\_PTR[3:0] in SYS\_STATUS0 register.

For single-channel conversion, the host will issue (CMD\_SS, CMD\_SC), then wait for DRDY signal asserted high where ADC data is ready for the host to read. Figure 14 shows a typical sequence before CMD\_SS or CMD\_SC is issued.

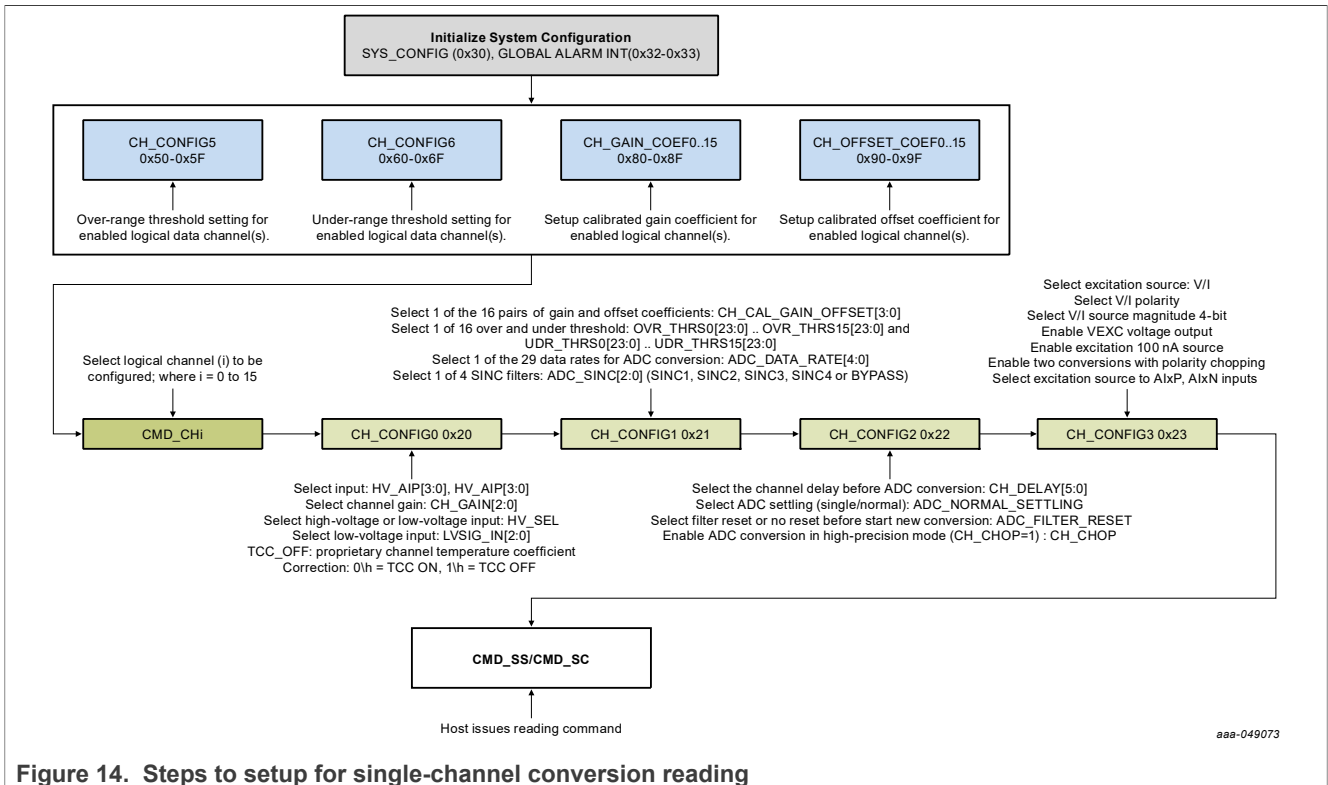


Figure 14. Steps to setup for single-channel conversion reading

**Example code sequence**

For example, setup a single conversion using `CMD_SS` command with the following setup and the conversion result will be stored at `CH_DATA5`.

Example how to select, config, enable, run, read data.

```

hv_aip = 1; // 4-bit
hv_ain = 1; // 4-bit
hvlv_sel = 1;
CH_GAIN = 0; // 3-bit
AIIP = 10.35 V;
AIIN = -10.72 V;
ADC_SINGLE_NORMAL = 0; // Single cycle settling
ADC_DATA_RATE = 2; //
CH_CAL_GAIN_OFFSET = 0; // 4-bit pointer points to GAIN_COEF0 & OFFSET_COEF0
CH_THRS = 0; // 4-bit pointer points to OVR_THRS0 & UDR_THRS0
ADC_SINC = 0; // 3-bit, SINC4 bypass stage 2
ADC_FILTER_RESET = 1; // filter reset at start of ADC conversion
CH_CHOP = 0; // disable precision mode
CONV_DELAY = 1; //
write_cmd_ch(5) ; // CMD_WR_POINTER5 - set conversion pointer to 5
write_reg16("CH_CONFIG0", { hv_aip, hv_ain, CH_GAIN, hvlv_sel, 4'b0000}); // TCC
is enabled
write_reg16("CH_CONFIG1", {CH_CAL_GAIN_OFFSET, CH_THRS, ADC_DATA_RATE,
ADC_SINC} );
write_reg16("CH_CONFIG2", {CONV_DELAY, ADC_SINGLE_NORMAL,
ADC_FILTER_RESET, CH_CHOP, 7'b000_0000});
write_cmd_ss() ; // CMD_SS - issue single ADC conversion command
wait_rise_edge (DRDY);
CH_DATA5 = read_reg24("CH_DATA5"); // read the conversion data at logical
channel 5

```

**7.4.2 Working with multichannel sequencer**

The sequencer will step through CH0 to CH15 (or current channel to CH15) to execute the enabled channels (`CH_CONFIG4.MCH_EN[15:0]`) and store ADC output in the corresponding `ADC_DATA` output register (`CH_DATA0.CH_DATA15`).

ADC conversion can be set either to Single-Cycle Settling mode or Normal Settling mode with `CH_CONFIG4.ADC_SINGLE_NORMAL = 0` or `1`, respectively. However, single-cycle settling is typically preferable in many applications.

When `CMD_MM` or `CMD_MC` command is issued, the sequencer will begin ADC conversions on the enabled channels and stop upon completing the conversion of the last enabled channel. At the end of the Sequencer mode, `SYS_STATUS0.ADC_CONV_CH[3:0]` is set to CH0. The `DRDY` pin will transition from 0 to 1 when `ADC_DATA` is ready for the host to read. The register `SYS_STATUS0.ADC_CONV_CH[3:0]` can be used for tracking the current ADC channel. ADC busy status is indicated in either status bit `SYS_STATUS0.SINGLE_CH_ACTIVE` or `SYS_STATUS0.MULTI_CH_ACTIVE`.

See [Section 7.5.9](#), [Section 7.5.10](#), [Section 7.5.11](#) in modes (MM, MC, MS) for the expected behavior of the sequencer with the use of `SYNC` pulse and reading command as triggers.

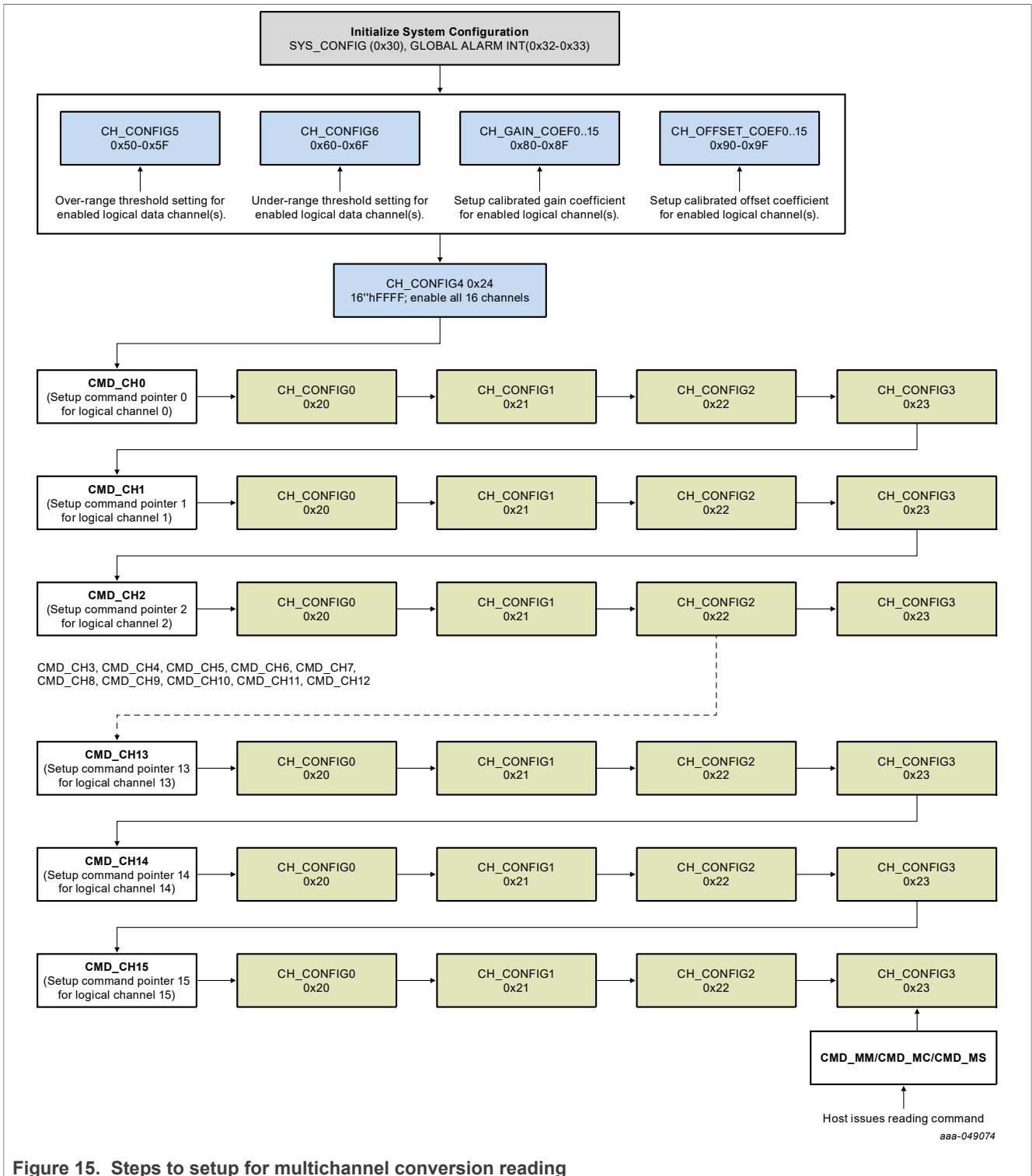


Figure 15. Steps to setup for multichannel conversion reading

7.4.2.1 Channel enable

CH\_CONFIG4[15:0] = MCH\_EN[15:0] is an index-based channel enable bit for ADC conversion for multichannel reading. If MCH\_EN = 0xFFFF, all 16 channels are enabled in multichannel sequencer conversions.

When single-conversion, single-reading (CMD\_SS) or single-conversion continuous-reading (CMD\_SC) is used, channel enable CH\_CONFIG4[15:0] is ignored. This register is only used in multichannel reading, sequencer conversions. MCH\_EN = 0xFFFF, all 16 channels are enabled in multichannel sequencer conversions.

#### 7.4.2.2 On-the-fly channel configuration

Any of the 16 logical channels are configurable on-the-fly and could be modified while the sequencer is **running**.

**Note:** Any register setting changes on ADC active channel (SINGLE\_CH\_ACTIVE or MULTI\_CH\_ACTIVE) will not be taken into effect until next ADC conversion command CMD\_ is issued.

### 7.5 ADC Conversion and Reading modes

The NAFE13388 reading process starts when a start event is received, and finishes with an event that signals the completion of reading. The reading process includes four main steps:

1. Reading start event received.
2. Wait a period equal to the configured programmable delay.
3. Execute one or more analog-to-digital conversions.
4. Send the DRDY signal when the reading process is complete.

#### 7.5.1 Reading start event

The NAFE13388 provides two types of reading start event to fit simplicity and performance.

One reading event is command based. It is intrinsic in the SPI command transaction. The other is triggered through SYNC pin.

The SPI reading process starts on the last falling edge of the SPI command clock. The SYNC reading process begins on the rising edge of the SYNC pulse at the SYNC pin.

#### 7.5.2 Reading process stop event

The reading process can be stopped by the host issuing either SPI commands or a SYNC pulse. This command is useful if the host wants to stop an infinite reading process executed autonomously by the NAFE13388.

The SPI commands to stop reading in progress are CMD\_ABORT or CMD\_END.

##### 7.5.2.1 CMD\_ABORT

While the NAFE reading period is active and the ADC is converting, if a CMD\_ABORT command is received, the ongoing conversion is aborted, and the device returns to its initial waiting state. The corresponding CH\_DATA register will not be updated.

##### 7.5.2.2 CMD\_END

While the NAFE reading period is active and the ADC is converting, if CMD\_END is received, ADC conversion is allowed to complete (contrary to CMD\_ABORT) and CH\_DATA register is updated with new results before device returns to its initial waiting state.

#### 7.5.3 Reading period

The reading period is defined as the time interval between the reading start event and the reading end event.

If `SYS_CONFIG0.ADC_SYNC = 0`, the conversion start event is the last falling edge of the SPI command clock. If `SYS_CONFIG0.ADC_SYNC = 1`, the conversion start event is the rising edge of the SYNC pulse. The reading completion event is the rising edge of the DRDY signal.

The reading period is a function of system clock, reading mode, fixed delay, data rate and programmable delay. Also, the fixed delay is different for the first reading and the readings after first reading.

#### Reading modes:

- Single-channel single-reading (SCSR)
- Single-channel continuous-reading (SCCR)
- Multichannel single-reading (MCSR)
- Multichannel multireading (MCMR)
- Multichannel continuous reading (MCCR)

The system clock frequency is 4.608 MHz. The period of system ( $T_{\text{sys\_clk}}$ ) is  $1/(4.608 \text{ MHz}) = 217 \text{ ns}$  with the master clock at 18.432 MHz.

Table 17. Channel programmable delay

Master clock		18,432,000
System clock		4,608,000
Prog delay code	Prog delay (# sysclk)	Programmable delay
0	0	000.000E+0
1	2	434.028E-9
2	4	868.056E-9
3	6	1.302E-6
4	8	1.736E-6
5	10	2.170E-6
6	12	2.604E-6
7	14	3.038E-6
8	16	3.472E-6
9	18	3.906E-6
10	20	4.340E-6
11	28	6.076E-6
12	38	8.247E-6
13	40	8.681E-6
14	42	9.115E-6
15	56	12.153E-6
16	64	13.889E-6
17	76	16.493E-6
18	90	19.531E-6
19	128	27.778E-6
20	154	33.420E-6
21	178	38.628E-6
22	204	44.271E-6

Table 17. Channel programmable delay...continued

		Master clock	18,432,000
		System clock	4,608,000
23	224		48.611E-6
24	256		55.556E-6
25	358		77.691E-6
26	512		111.111E-6
27	716		155.382E-6
28	1024		222.222E-6
29	1664		361.111E-6
30	3276		710.938E-6
31	7680		1.667E-3
32	19200		4.167E-3
33	23040		5.000E-3

7.5.3.1 Calculate the effective reading period

The general reading period formula is:

$$T_{\text{reading}} = T_{\text{fixed}} + T_{\text{prog\_delay}} + T_{\text{conv}}$$

For all Reading modes, due to internal setup requirements, the fixed delay is always built into the first sample reading time. The subsequent readings are free of this setup time overhead. Because the Single-Reading modes produce only one sample, the effective data rate is  $1/(T_{\text{conv}} + T_{\text{fixed}})$ , if  $T_{\text{prog\_delay}} = 0$ . Some reading period examples are provided in the Reading mode sections.

7.5.3.2 Fastest reading period in SCCR mode

The fastest reading period is achievable in Single-Channel Continuous-Reading mode with the ADC digital filter set in Normal Settling mode. In particular, after the first reading, it is possible to achieve a data rate up to 288 ksps.

7.5.3.3 Effective output data rate with CH\_DELAY

In addition to the programmable data rate provided by the ADC, the NAFE offers further data rate output availability with the combination of ADC conversion period and programmable delay, CH\_CONFIG2.CH\_DELAY[5:0].

Table 18 shows examples of the most common reading periods.

Table 18. Popular reading periods

System clock = 4,608,000						
ADC data rate (sps)	ADC conversion period(s)	Fixed delay (# sysclk)	Prog delay (# sysclk)	Prog delay(s)	Actual reading period(s)	Target reading period(s)
288000.00	3.472E-6	0	0	000.000E+0	3.5E-6	4.0E-6
288000.00	3.472E-6	0	2	434.028E-9	3.9E-6	4.0E-6
192000.00	5.208E-6	0	4	868.056E-9	6.1E-6	6.0E-6
192000.00	5.208E-6	0	6	1.302E-6	6.5E-6	6.7E-6
144000.00	6.944E-6	0	4	868.056E-9	7.8E-6	8.0E-6

NAFE13388 Universal ±25 V 8-input low-power AFE with excitation sources

Table 18. Popular reading periods...continued

System clock = 4,608,000						
144000.00	6.944E-6	0	14	3.038E-6	10.0E-6	10.0E-6
96000.00	10.417E-6	0	8	1.736E-6	12.2E-6	12.0E-6
96000.00	10.417E-6	0	12	2.604E-6	13.0E-6	13.3E-6
96000.00	10.417E-6	0	16	3.472E-6	13.9E-6	14.0E-6
72000.00	13.889E-6	0	10	2.170E-6	16.1E-6	16.0E-6
72000.00	13.889E-6	0	18	3.906E-6	17.8E-6	18.0E-6
72000.00	13.889E-6	0	28	6.076E-6	20.0E-6	20.0E-6
48000.00	20.833E-6	0	20	4.340E-6	25.2E-6	25.0E-6
48000.00	20.833E-6	0	42	9.115E-6	29.9E-6	30.0E-6
36000.00	27.778E-6	0	56	12.153E-6	39.9E-6	40.0E-6
24000.00	41.667E-6	0	38	8.247E-6	49.9E-6	50.0E-6
18000.00	55.556E-6	0	20	4.340E-6	59.9E-6	60.0E-6
18000.00	55.556E-6	0	90	19.531E-6	75.1E-6	75.0E-6
18000.00	55.556E-6	1	204	44.271E-6	99.8E-6	100.0E-6
12000.00	83.333E-6	0	76	16.493E-6	99.8E-6	100.0E-6
9000.00	111.111E-6	0	40	8.681E-6	119.8E-6	120.0E-6
9000.00	111.111E-6	0	64	13.889E-6	125.0E-6	125.0E-6
9000.00	111.111E-6	0	178	38.628E-6	149.7E-6	150.0E-6
9000.00	111.111E-6	0	224	48.611E-6	159.7E-6	160.0E-6
6000.00	166.667E-6	0	154	33.420E-6	200.1E-6	200.0E-6
4500.00	222.222E-6	0	128	27.778E-6	250.0E-6	250.0E-6
4500.00	222.222E-6	0	358	77.691E-6	299.9E-6	300.0E-6
2250.00	444.444E-6	0	256	55.556E-6	500.0E-6	500.0E-6
2250.00	444.444E-6	0	716	155.382E-6	599.8E-6	600.0E-6
1125.00	888.889E-6	0	512	111.111E-6	1.0E-3	1.0E-3
1125.00	888.889E-6	0	1,664	361.111E-6	1.3E-3	1.3E-3
1125.00	888.889E-6	0	3,276	710.938E-6	1.6E-3	1.6E-3
562.50	1.778E-3	0	1,024	222.222E-6	2.0E-3	2.0E-3
400.00	2.500E-3	0	0	000.000E+0	2.5E-3	2.5E-3
200.00	5.000E-3	0	0	000.000E+0	5.0E-3	5.0E-3
100.00	10.000E-3	0	0	000.000E+0	10.0E-3	10.0E-3
60.00	16.667E-3	0	0	000.000E+0	16.7E-3	16.7E-3
50.00	20.000E-3	0	0	000.000E+0	20.0E-3	20.0E-3
30.00	33.333E-3	0	0	000.000E+0	33.3E-3	33.3E-3
30.00	33.333E-3	0	19,200	4.167E-3	37.5E-3	37.5E-3
25.00	40.000E-3	0	0	000.000E+0	40.0E-3	40.0E-3
25.00	40.000E-3	0	23,040	5.000E-3	45.0E-3	45.0E-3
20.00	50.000E-3	0	0	000.000E+0	50.0E-3	50.0E-3
15.00	66.667E-3	0	0	000.000E+0	66.7E-3	66.6E-3
10.00	100.000E-3	0	0	000.000E+0	100.0E-3	100.0E-3
7.50	133.333E-3	0	0	000.000E+0	133.3E-3	133.3E-3
7.50	133.333E-3	0	7,680	1.667E-3	135.0E-3	135.0E-3
7.50	133.333E-3	0	8,191	1.778E-3	135.1E-3	360.0E-3



7.5.4 ADC synchronization

Generally, the NAFE13388 supports four different types of synchronization:

- Synchronize multi NAFE with SYNC pulse at SYNC pin
- Synchronize the NAFE to host for conversion start by SYNC pulse
- Synchronize the host to the NAFE through DRDY signal
- Synchronize the NAFE and the host clock to the same clock, by one of the following methods:
  - Configure the NAFE to use external clock and apply 18.432 MHz clock pulses at EXTCLK/XI pin
  - Configure the NAFE to output its system clock to GPIO9

7.5.4.1 ADC\_SYNC bit

When bit `SYS_CONFIG0.ADC_SYNC = 1`, a detection of the rising edge at the SYNC pin starts a new conversion. If there is an ongoing conversion and the rising edge of the SYNC is received, the ongoing conversion is aborted. Then, a new conversion is restarted. In this case, `CMD_xy` is used to select the Conversion mode. The conversion start is only triggered by a rising edge at the SYNC pin.

SYNC pulse width should be greater or equal to two system clock periods,  $2 \times T_{sys\_clk}$  and `SYS_CONFIG0.ADC_SYNC` is set to 1.

If bit `SYS_CONFIG0.ADC_SYNC = 0`, the SYNC pulse is ignored. The conversion start is triggered by the last SPI clock falling edge of SPI conversion commands. In this case, the `CMD_xy` has two functions:

- Select the Reading mode
- Trigger the conversion start

The conversion start with SYNC pulse is supported in all Reading modes. [Table 19](#) summarizes the Reading mode and start commands.

Table 19. Reading mode and start commands

		Conversion start trigger	
		ADC_SYNC = 0	ADC_SYNC = 1
Reading modes	SCSR	CMD_SS	SYNC pin
	SCCR	CMD_SC	SYNC pin
	MCSR	CMD_MS	SYNC pin
	MCMR	CMD_MM	SYNC pin
	MCCR	CMD_MC	SYNC pin
Trigger event on <code>CMD_xy</code> is the last SPI command falling edge check			
Trigger event on SYNC pin is the pulse rising edge			

7.5.4.2 Synchronize multi-NAFE with SYNC pulse at SYNC pin

The SYNC pin function enables the synchronization of multiple NAFE13388s connected to the same SYNC signal generated by the host. When the host issues the SYNC pulse, all the connected devices start the conversion on the rising edge of the SYNC pulse.

7.5.4.3 Synchronize NAFE to host with SYNC pin

The SYNC input enables the host to control the start conversion of the NAFE. Consequently, this provides a synchronization mechanism driven by the host.

7.5.4.4 Synchronize the host to the NAFE through DRDY signal

DRDY rising edge can be used to synchronize the host with the NAFE13388 data rate output (DRO). This enables the host to estimate the effective DRO and to be synchronized with the device on fetching the data at the correct time. This function is critical for synchronizing the reading time for an infinite reading loop.

7.5.4.5 Synchronize the NAFE and host to the same clock

The NAFE13388 offers two options to synchronize the NAFE and the host to the same clock:

- Apply an external 18.432 MHz master clock to XI/EXTCLK pin and set SYS\_CONFIG0.CK\_SRC\_SEL[1:0] = 1. This enables coherent measurements and the possibility to synchronize the SPI data fetching using this clock as a timer.
- Use internal 4.608 MHz system clock at GPIO9 pin configuring SYS\_CONFIG0.MCLK\_OUT\_ENABLE = 1 in SYS\_CONFIG0 register. This implementation enables synchronization to the NAFE so the host can synchronize the SPI data fetching using this clock as a timer.

7.5.4.6 Reading conversion start - SYNC pulse

If SYS\_CONFIG0.ADC\_SYNC = 1, a new ADC conversion will start at each rising edge of the SYNC pulse at the pin.

SYNC pulse width should be a minimum of two system clock cycles.

Figure 16 shows an ADC conversion triggered by a pulse at the SYNC pin in Single-Channel Continuous-Reading mode (CMD\_SC). The Continuous Reading mode, in combination with SYNC, allows the fastest reading mode, while requiring only one SYNC pulse to collect many or infinite reading samples. In addition, it mitigates the timing requirements for fetching channel data on the SPI bus. The fetching period is close to the reading period for the second reading and beyond.

SYNC pulse triggers the conversion start for all the reading modes.

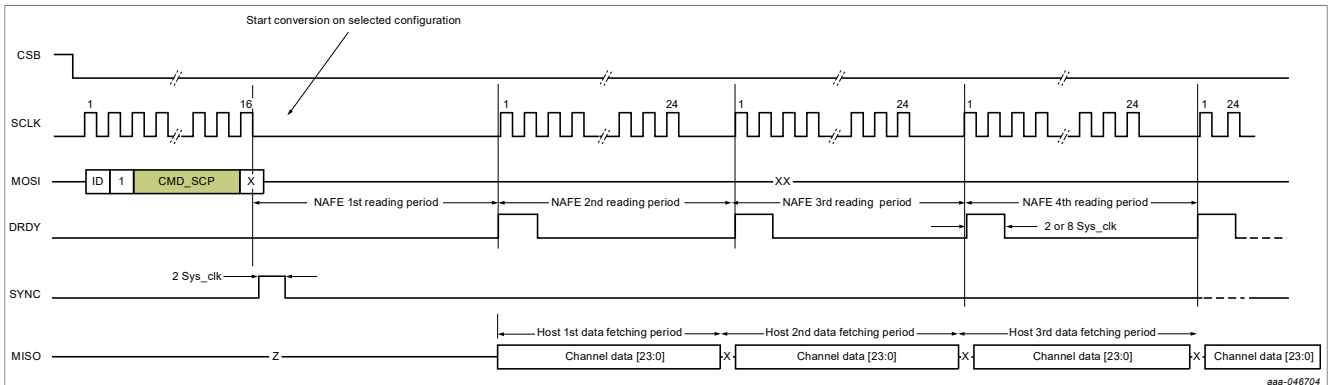


Figure 16. Conversion start

7.5.5 Reading modes

NAFE13388 provides five reading (conversion) modes:

1. Single-channel single-reading (SCSR) set by the CMD\_SS command
2. Single-channel continuous-reading (SCCR) set by the CMD\_SC command
3. Multichannel single-reading (MCSR) set by the CMD\_MS command
4. Multichannel multireading (MCMR) set by the CMD\_MM command
5. Multichannel continuous-reading (MCCR) set by the CMD\_MC command

The following sections describe the reading modes in details.

7.5.6 Reading sequence

In general, the ADC follows a five-step sequence to complete a reading (conversion) process. The reading (conversion) process is initiated by either SPI start command or SYNC pulse.

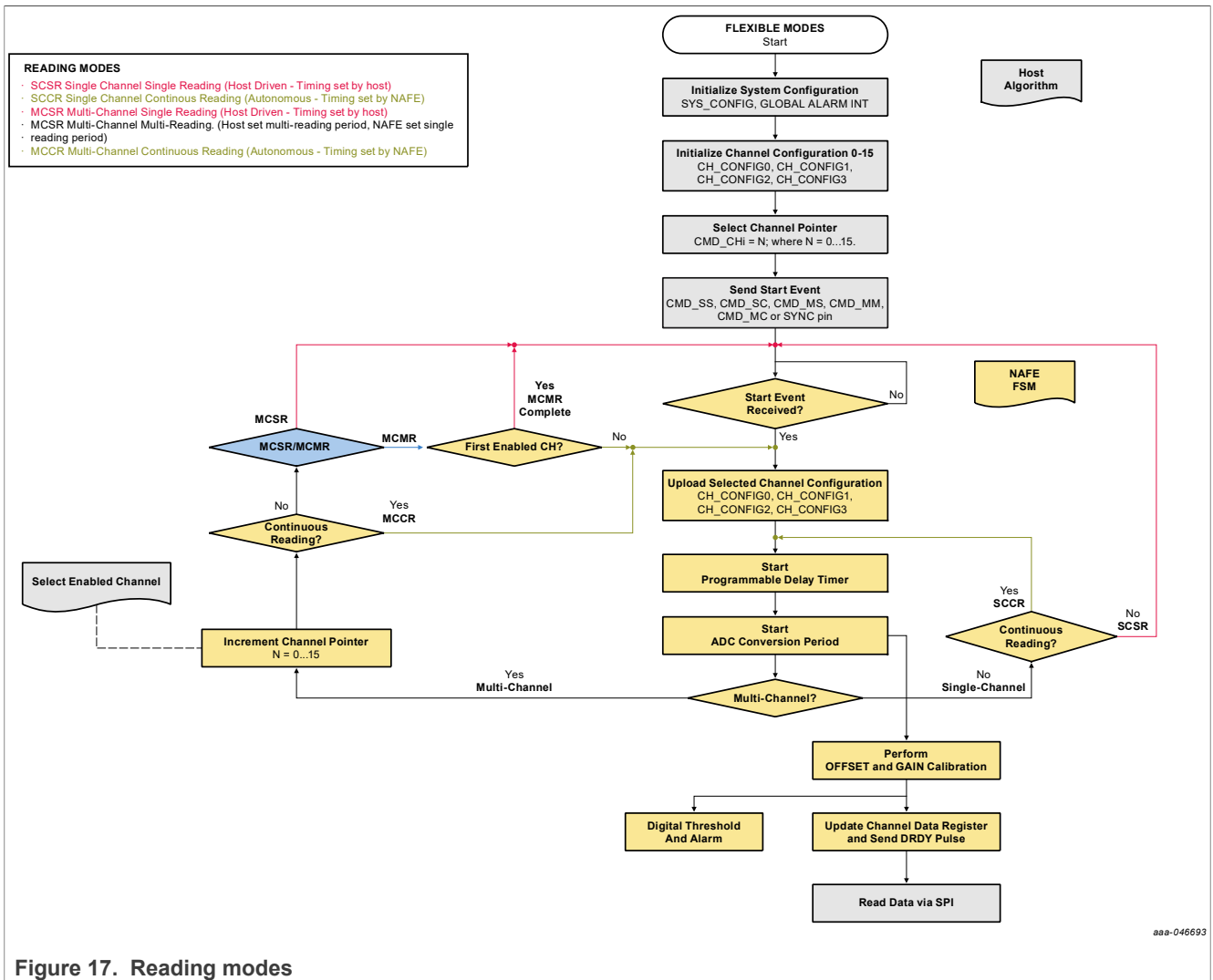


Figure 17. Reading modes

Reading sequence:

1. Idle state. Wait for a start event: SPI start command or SYNC pulse
2. Update the active channel configuration and pointer location (as needed)
3. Wait for the timer of programmable delay to expire
4. Start and complete ADC conversion on the selected channel, check active converting channel pointer with register bits ADC\_CONV\_CH[3:0]
  - a. In Multichannel Reading mode MCSR, MCMR, and MCCR, the active converting channel pointer is automatically incremented to the next enabled channel after the conversion is complete.
5. Loop increment for Continuous-Reading and Multireading modes:
  - a. In Single-Reading modes: SCSR and MCSR - ADC returns to [Step 1](#), idle state

- b. In Continuous-Reading modes: SCCR, MCCR – ADC jumps to [Step 2](#) and repeats the sequence until interrupted
- c. In Multireading mode: MCMR – ADC jumps to [Step 2](#) until the reading completion of the last enabled channel defined in CH\_CONFIG4.MCH\_EN[15:0]. The loop is then broken and ADC returns to [Step 1](#).

In Single-Reading mode SS mode, the host issues the conversion start by sending CMD\_SS if SYS\_CONFIG0.ADC\_SYNC = 0, or the SYNC pulse if SYS\_CONFIG0.ADC\_SYNC = 1. After the NAFE completes the reading conversion process, it returns to idle and waits for the next instruction command or next SYNC pulse.

In Continuous-Reading SCCR and MCCR modes, the host issues the conversion start by sending CMD\_SC, CMD\_MC, or the SYNC pulse (when SYS\_CONFIG0.ADC\_SYNC = 1 is set). After the NAFE completes first reading conversion process, it jumps to [Step 2](#) and continues the reading process forever or until is interrupted.

There are three ways to interrupt an ADC conversion:

1. CMD\_END: Stop ADC conversion reading process after the current conversion is completed.
2. CMD\_ABORT: Abort the ADC conversion reading process immediately.
3. Conversion start event:
  - a. If SYS\_CONFIG0.ADC\_SYNC = 0, the last falling edge of SPI command restarts a new conversion. A pulse at the SYNC pin is ignored.
  - b. If SYS\_CONFIG0.ADC\_SYNC = 1, a rising edge signal at SYNC pin will trigger ADC a new conversion start.

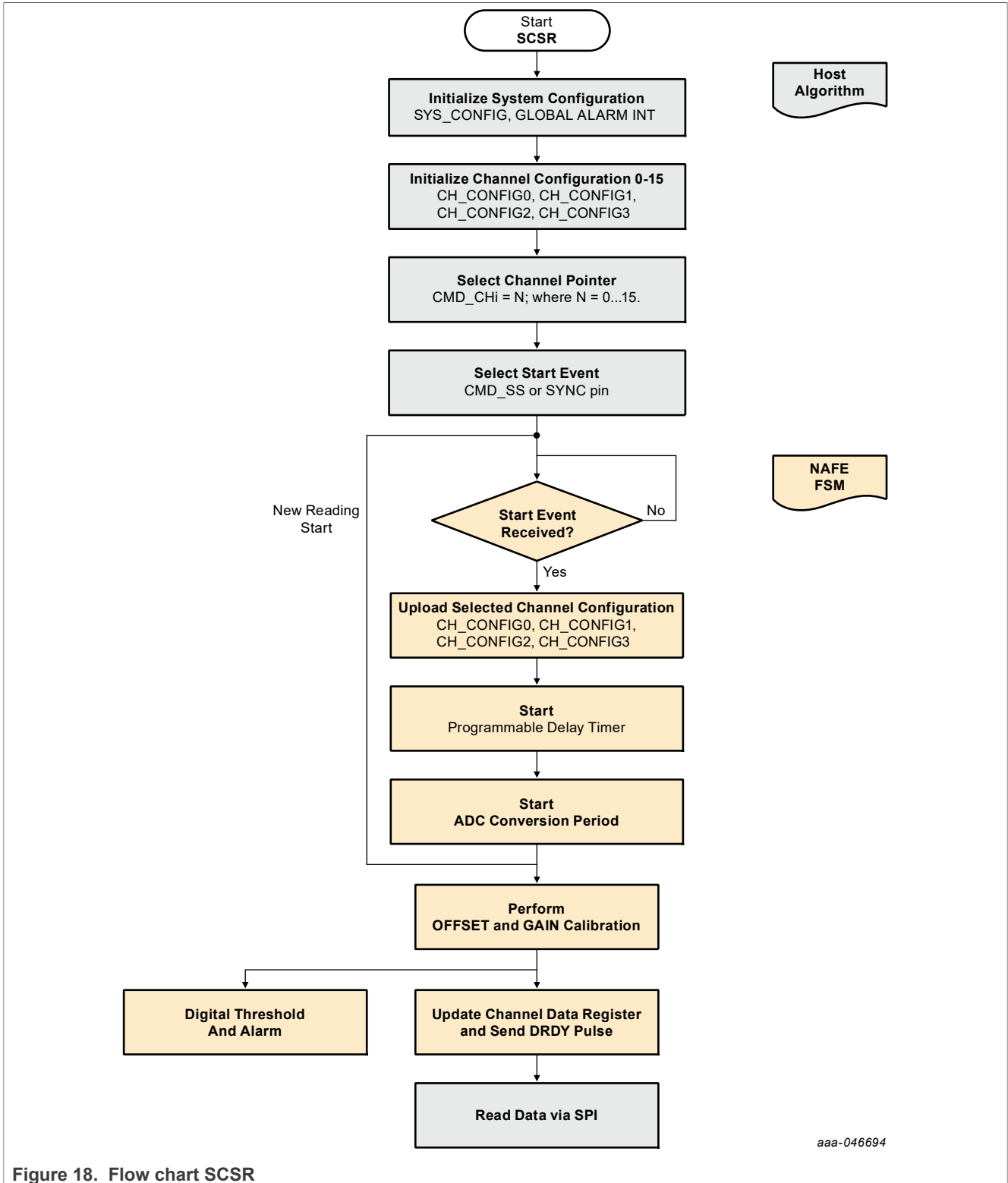
### 7.5.7 CMD\_SS (single-channel single-reading)

Start Single-Channel Single-Reading (conversion) mode.

If SYS\_CONFIG0.ADC\_SYNC = 0, the conversion start is triggered by this SPI command at the last SPI clock falling edge. If SYS\_CONFIG0.ADC\_SYNC = 1, the conversion start is triggered by SYNC rising edge. In both cases, the conversion is executed on the selected channel. After the conversion is complete, the device returns to its waiting state.

Data can be read serially via the MISO pin after the DRDY pin asserts high, or after the reading process is complete.

7.5.7.1 Flow chart - SCSR



aaa-046694

Figure 18. Flow chart SCSR

7.5.7.2 Timing diagram - SCSR

The host can fetch single-channel data after the NAFE reading period by two methods:

- Keep the CSB low after the command was issued. Then wait for DRDY assert high. Data is available at the MISO pin at every rising of SCLK. MSB outputs first.
- Deassert the CSB high, then wait until the DRDY goes high and read the channel data.

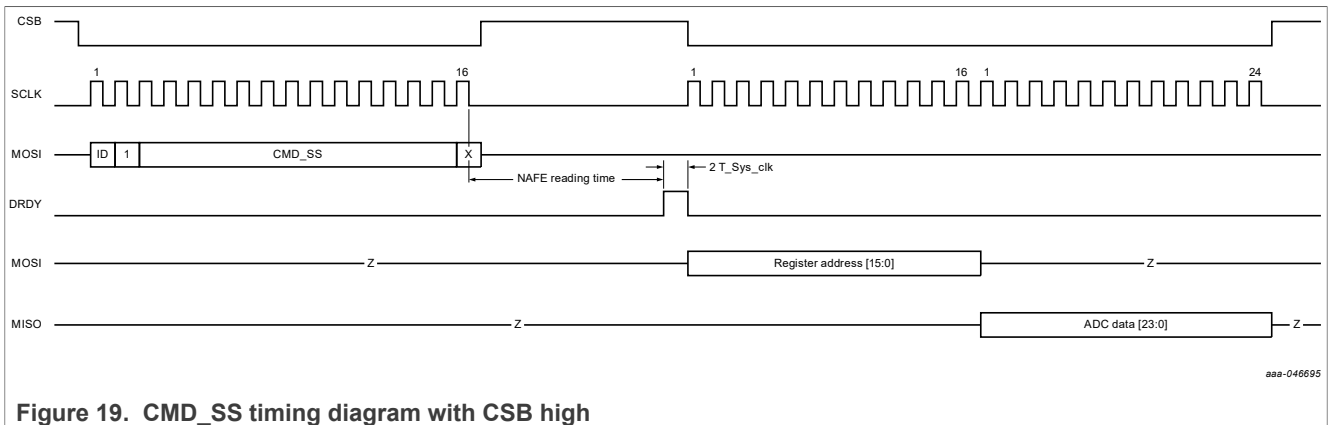


Figure 19. CMD\_SS timing diagram with CSB high

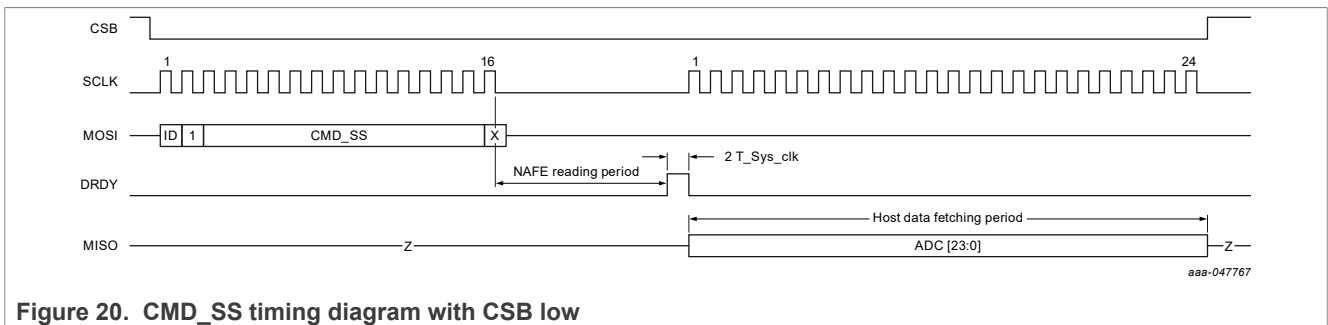


Figure 20. CMD\_SS timing diagram with CSB low

7.5.7.3 Code example - SCSR

```

Reg_Read ('SYS_STATUS0) ; to clear INTB
Reg_write ('SYS_CONFIG, sys_config_data); //
Reg_write ('CH_CONFIGi, ch_config_datai); // i = 0..15
Send CMD_CHi;
Send CMD_SS;
Send SYNC Pulse (if SYNC_BIT = 1);
    
```

7.5.7.4 Reading period for SCSR

SS Reading period:  $T_{reading} = T_{fixed} + T_{prog\_delay} + T_{conv}$

On single reading,  $T_{fixed} = (2 \times T_{sys\_clk}) \pm 1 \times T_{sys\_clk}$

For example,

Set  $CH\_DELAY[5:0]=17\text{d}$ ; #delay 76 sys\_clk

Set  $ADC\_DATA\_RATE[4:0] = 5\text{d}$ ; #DRO is 12000 sps

Set  $ADC\_NORMAL\_SETTLING = 0\text{d}$ ; #Single-cycle mode

$T_{\text{sys\_clk}} = 1/\text{sys\_clk} = 1/4608000 = 0.217 \text{ us}$

$T_{\text{prog\_delay}} = 76 * T_{\text{sys\_clk}}$  #Table Channel Programmable Delay

$T_{\text{conv}} = 1/12000 = 83.3 \text{ us}$  #Table Data Rate

Hence,

On single reading,  $T_{\text{reading}} = 0.217 \text{ us} * (2 \pm 1 + 76) + 83.33 \text{ us} = 100.3 \pm 0.217 \text{ us}$ .

### 7.5.8 CMD\_SC (single-channel continuous-reading)

Start Single-Channel Continuous-Reading (conversion) mode.

If bit `SYS_CONFIG0.ADC_SYNC` = 0, the conversion start is triggered by this SPI command at the last clock falling edge.

If bit `SYS_CONFIG0.ADC_SYNC` = 1, the conversion start is triggered by SYNC rising edge.

In both cases, the conversion is executed on the selected channel until it is interrupted or restarted. The conversion could be interrupted by `CMD_ABORT` or `CMD_END`, or could be aborted and restarted by a SYNC pulse if `SYS_CONFIG0.ADC_SYNC` = 1 or any conversion command if `SYS_CONFIG0.ADC_SYNC` = 0.

Data can be read serially via the MISO pin after the DRDY pin asserts high or after the reading is completed.

7.5.8.1 Flow chart - SCCR

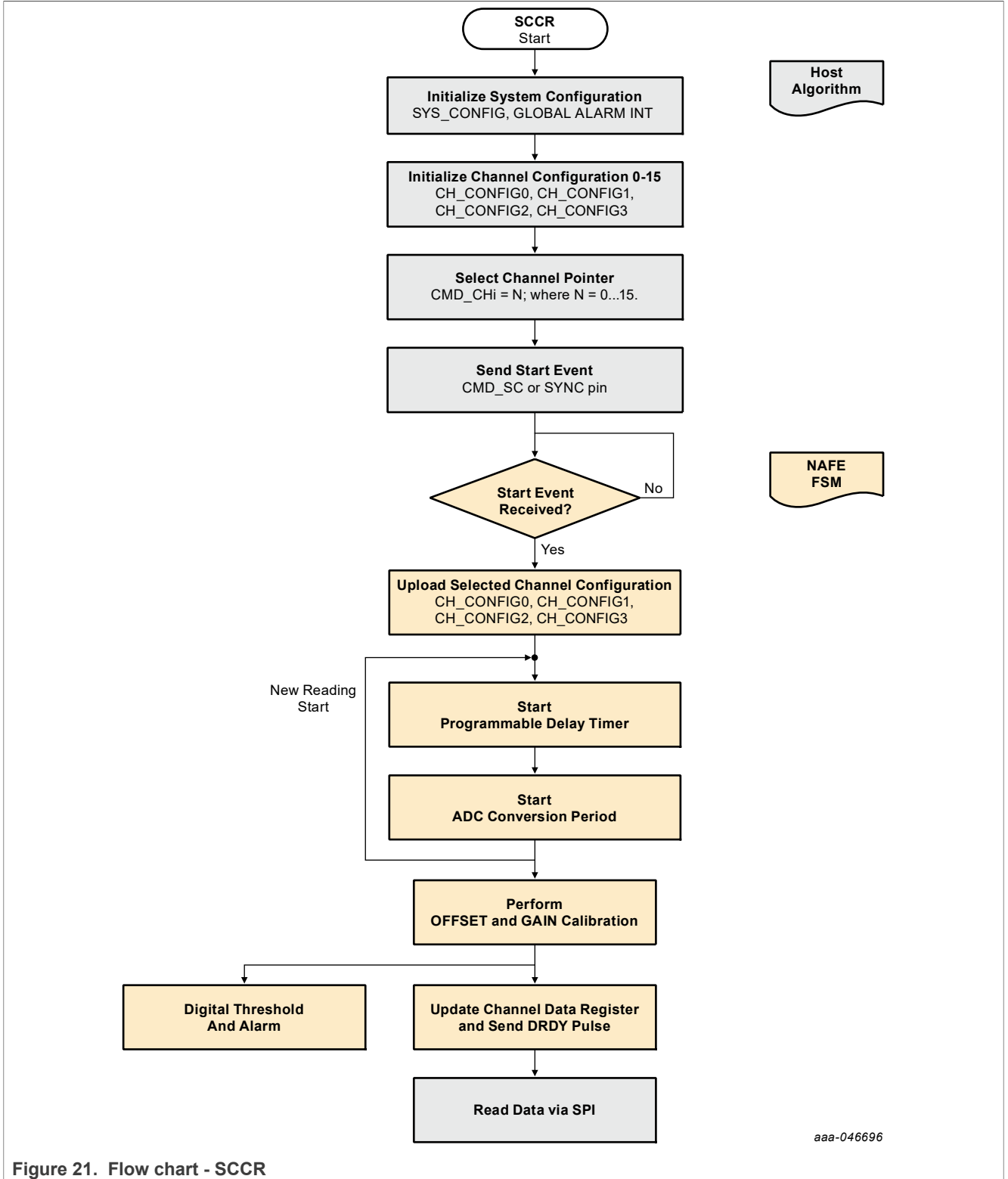


Figure 21. Flow chart - SCCR



7.5.8.2 Timing diagram - SCCR

The host can fetch single-channel data after the NAFE reading period by the two methods:

- Keep the CSB low after the command was issued. Then wait for DRDY pin assert high and read the channel data. Data is available at MISO pin at every rising of SCLK. MSB outputs first.
- De-assert the CSB high, then wait until the DRDY goes high and read the channel data.

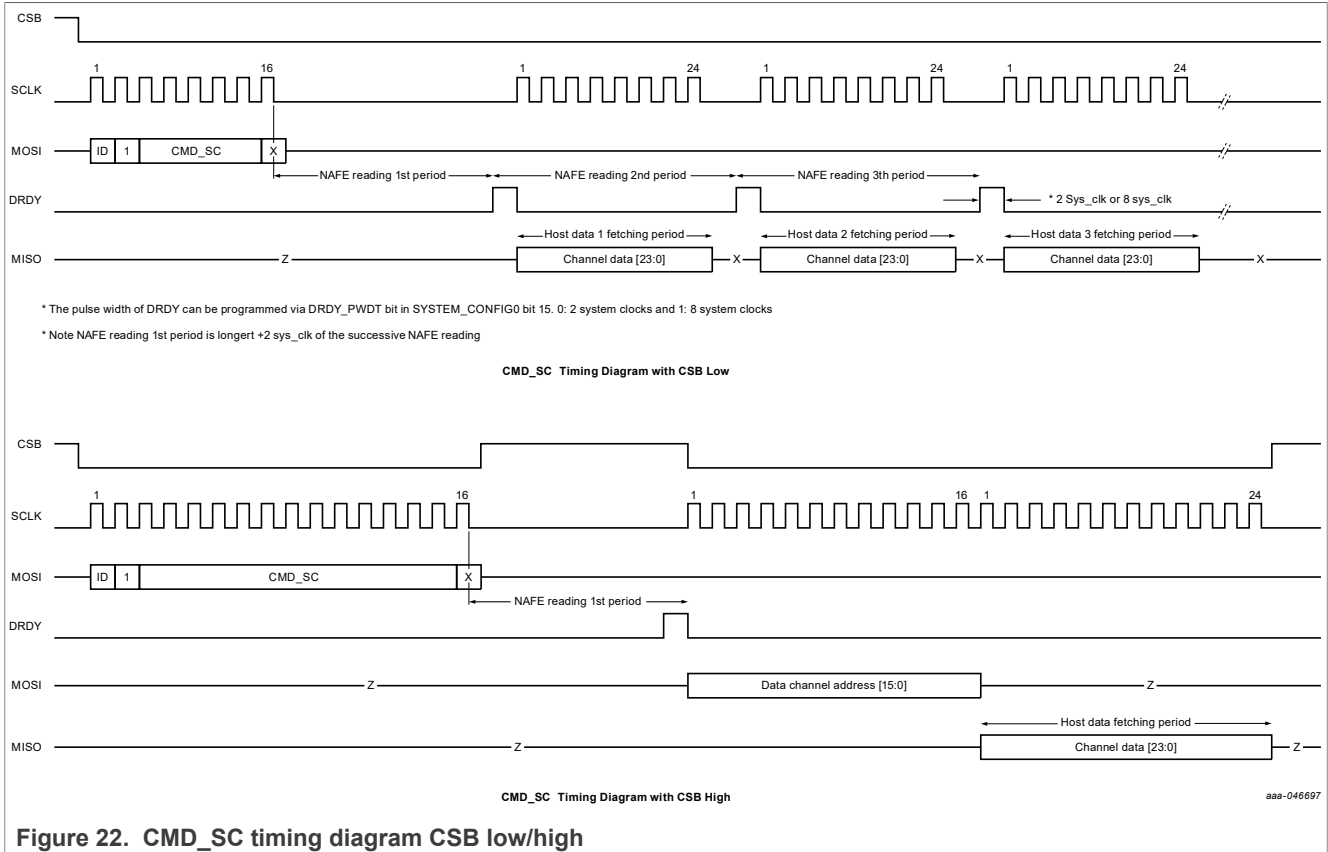


Figure 22. CMD\_SC timing diagram CSB low/high

7.5.8.3 Code example - SCCR

```

Reg_Read ('SYS_STATUS0) ; to clear INTB
Reg_write ('SYS_CONFIG, sys_config_data); //
Reg_write ('CH_CONFIGi, ch_config_datai); // i = 0...15
Send CMD_CHi;
Send CMD_SC;
Send SYNC Pulse (if SYNC_BIT = 1);
    
```

7.5.8.4 Reading period for SCCR

SC Reading period:  $T_{reading} = T_{fixed} + T_{prog\_delay} + T_{conv}$

On first reading,  $T_{fixed} = (2 \times T_{sys\_clk}) \pm 1 \times T_{sys\_clk}$

On subsequent readings,  $T_{fixed} = 0$ .

For example,

Set  $CH\_DELAY[5:0] = 17\backslash d; \#delay\ 76\ sys\_clk$

Set ADC\_DATA\_RATE[4:0] = 5\; #DRO is 12000 sps

Set ADC\_NORMAL\_SETTLING = 0\; #Single-cycle mode

$T_{\text{sys\_clk}} = 1/\text{sys\_clk} = 1/4608000 = 0.217 \text{ us}$

$T_{\text{prog\_delay}} = 76 * T_{\text{sys\_clk}}$  #Table Channel Programmable Delay

$T_{\text{conv}} = 1/12000 = 83.3 \text{ us}$  #Table Data Rate

Hence,

On first reading,  $T_{\text{reading}} = 0.217 \text{ us} * (2 + 1 + 76) + 83.33 \text{ us} = 100.3 \pm 0.217 \text{ us}$

On subsequent readings,  $T_{\text{reading}} = 0.217 \text{ us} * (0 + 76) + 83.33 \text{ us} = 99.83 \text{ us}$ .

### 7.5.9 CMD\_MM (multichannel multireading)

Start Multichannel Multireading (conversion) mode.

If SYS\_CONFIG0.ADC\_SYNC = 0, the conversion start is triggered by this SPI command at the last clock falling edge.

If SYS\_CONFIG0.ADC\_SYNC = 1, the conversion start is triggered by SYNC rising edge.

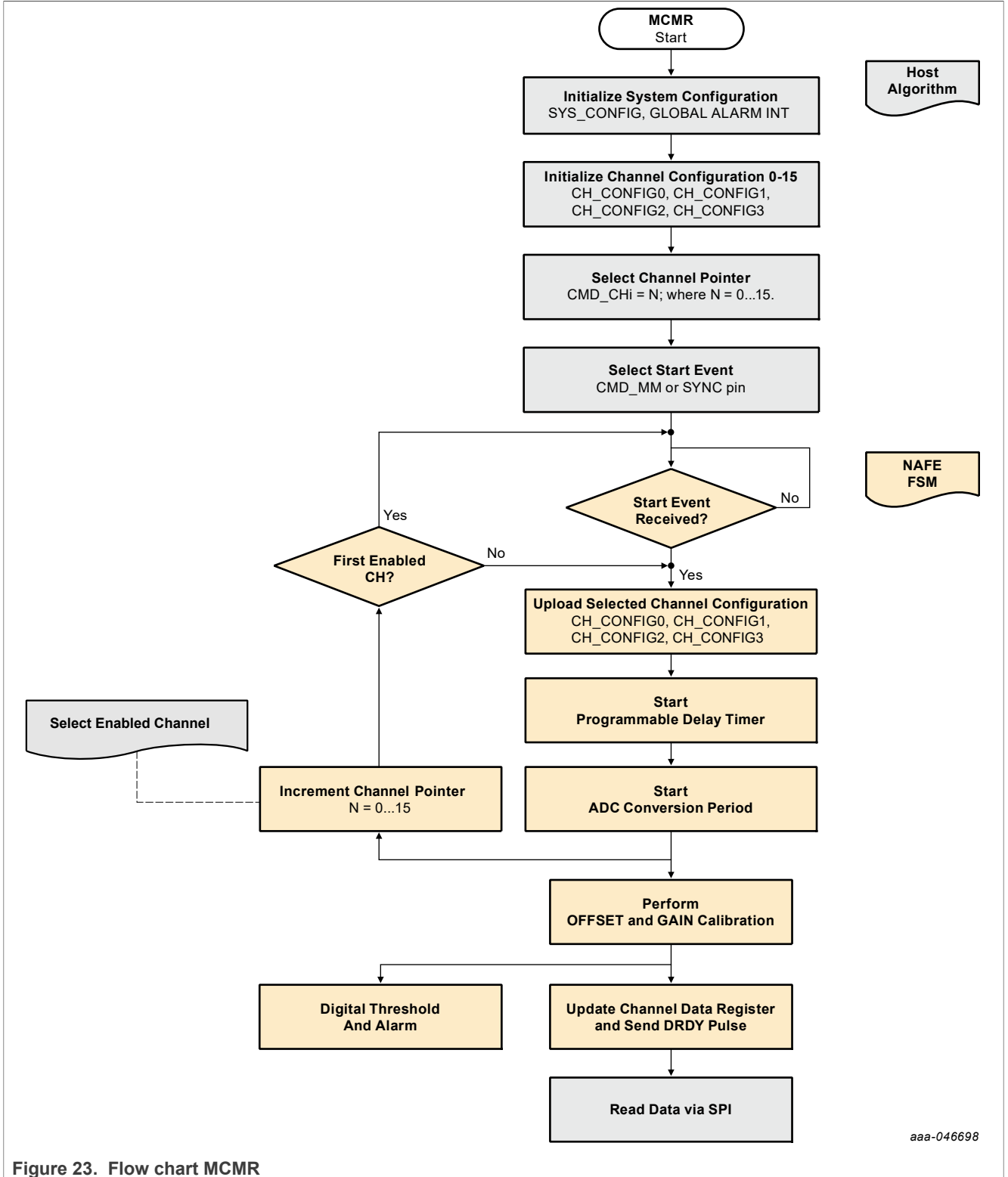
After first conversion, the sequencer will start conversion by sequencing on the enabled channel set via CH\_CONFIG4.MCH\_EN[15:0] register, from CH0 to CH15. Upon the completion of the last enabled channel, the device returns to waiting state.

The conversion could be interrupted by CMD\_ABORT or CMD\_END, or could be aborted and restarted by SYNC pulse if SYS\_CONFIG0.ADC\_SYNC = 1 or any conversion command if ADC\_SYNC = 0.

If an SPI conversion command or a SYNC pulse is issued before completion of the current conversion, ADC aborts the conversion immediately and restarts the conversion starting from first enabled channel.

Data can be read serially via the MISO pin after the DRDY pin asserts high or after the reading is completed.

7.5.9.1 Flow chart - MCMR



aaa-046698

Figure 23. Flow chart MCMR

7.5.9.2 Timing diagram - MCMR

In this example, channels 0, 4, 8, and 12 are enabled in multichannel conversion as shown in Figure 24, CH\_CONFIG4.MCH\_EN[15:0] = 0001\_0001\_0001\_0001. The sequencer generates four conversions results based on the four configurations stored at these respective locations 0, 4, 8, and 12 in the sequencer table.

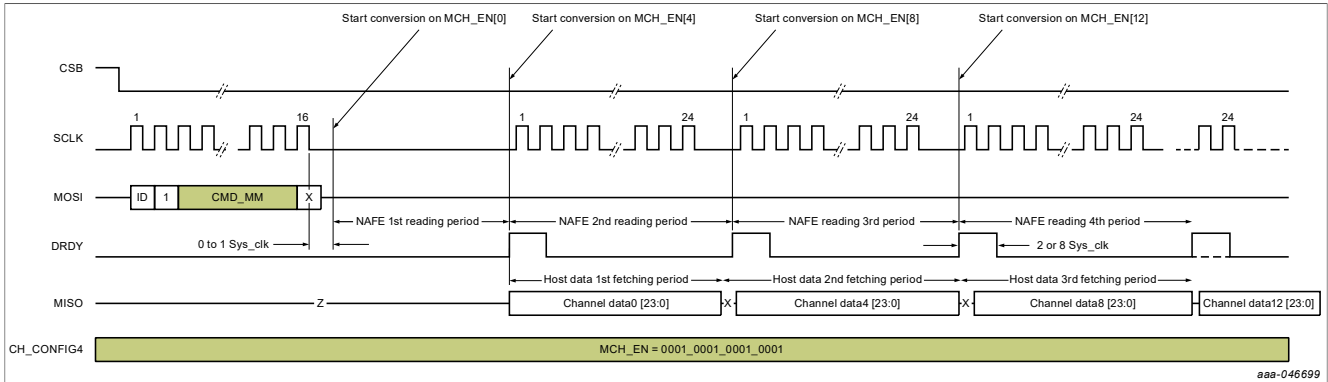


Figure 24. Timing diagram - MCMR

7.5.9.3 Code example - MCMR

```

Reg_Read ('SYS_STATUS0) ; to clear INTB
Reg_write ('SYS_CONFIG, sys_config_data);
Reg_write ('CH_CONFIGi, ch_config_datai); // i = 0...15
Send CMD_CHi;
Send CMD_MM;
Send SYNC Pulse (if SYNC_BIT = 1);
    
```

7.5.9.4 Reading period for MCMR

MM Reading period:  $T_{reading} = T_{fixed} + T_{prog\_delay} + T_{conv}$

On first reading,  $T_{fixed} = (2 \times T_{sys\_clk}) \pm 1 \times T_{sys\_clk}$

On subsequent reading,  $T_{fixed} = 0$

For example,

Set CH\_DELAY[5:0]=17\; #delay 76 sys\_clk

Set ADC\_DATA\_RATE[4:0]=5\; #DRO is 12000 sps

Set ADC\_NORMAL\_SETTLING=0\; #Single-cycle mode

$T_{sys\_clk} = 1/sys\_clk = 1/4608000 = 0.217 \text{ us}$

$T_{prog\_delay} = 76 * T_{sys\_clk}$  #Table Channel Programmable Delay

$T_{conv} = 1/12000 = 83.3 \text{ us}$  #Table Data Rate

Hence,

On first reading,  $T_{reading} = 0.217 \text{ us} * (2 \pm 1 + 76) + 83.33 \text{ us} = 100.3 \pm 0.217 \text{ us}$

On subsequent readings,  $T_{reading} = 0.217 \text{ us} * (0 + 76) + 83.33 \text{ us} = 99.83 \text{ us}$ .

### 7.5.10 CMD\_MC (multichannel continuous-reading)

Start Multichannel Continuous-Reading (conversion) autonomous mode.

The CMD\_MC is similar to CMD\_MM with infinite loop until it is interrupted or restarted.

CMD\_MC sets multichannel continuous-reading (conversion) mode.

If SYS\_CONFIG0.ADC\_SYNC = 0, the conversion start is triggered by this SPI command at the last clock falling edge.

If SYS\_CONFIG0.ADC\_SYNC = 1, the conversion start is triggered by SYNC rising edge.

After first conversion, the sequencer will start conversion by sequencing on the enabled channel set via CH\_CONFIG4.MCH\_EN[15:0] register, from CH0 to CH15. After the conversion completion of the last enabled channel, the device restarts a new cycle in an infinite loop.

The conversion could be interrupted by CMD\_ABORT or CMD\_END; or could be aborted and restarted by SYNC pulse if SYS\_CONFIG0.ADC\_SYNC = 1 or any conversion command if SYS\_CONFIG0.ADC\_SYNC = 0.

If an SPI conversion command or a SYNC pulse is issued before completion of the current conversion, ADC aborts the conversion immediately and restarts the conversion, starting from first enabled channel.

Data can be read serially via the MISO pin after the DRDY pin asserts high or after the reading is completed.

7.5.10.1 Flow chart - MCCR

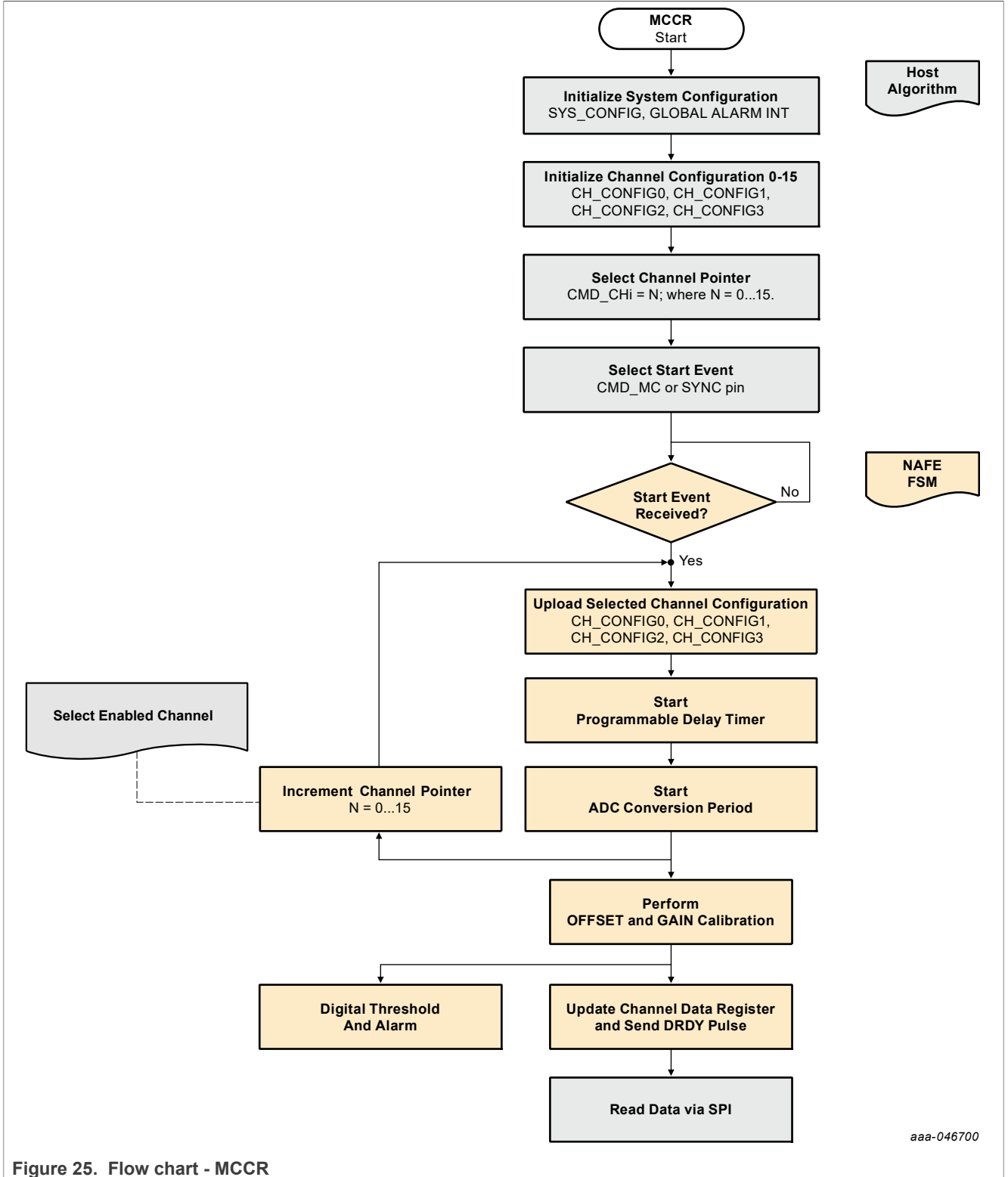


Figure 25. Flow chart - MCCR

7.5.10.2 Timing diagram - MCCR

The timing diagram for a multichannel continuous reading is shown in Figure 26, where Channels 0 and 12 are enabled by setting CH\_CONFIG4.MCH\_EN = 0001\_0000\_0000\_0001. For CMD\_MC command, the sequencer generates looping through two conversions based on the two configurations stored at these respective locations, 0 and 12, in the sequencer table. The conversions keep running through the loop until CMD\_ABORT or CMD\_END is issued.

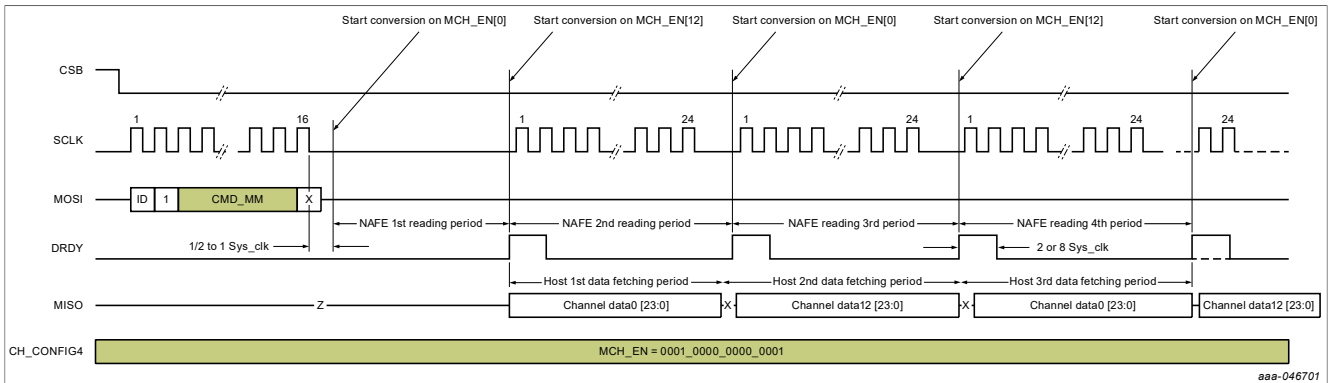


Figure 26. Timing diagram - MCCR

7.5.10.3 Code example - MCCR

```

Reg_Read ('SYS_STATUS0) ; to clear INTB
Reg_write ('SYS_CONFIG, sys_config_data); //
Reg_write ('CH_CONFIGi, ch_config_datai); // i = 0...15
Send CMD_CHi;
Send CMD_MC;
Send SYNC Pulse (if SYNC_BIT = 1);
    
```

7.5.10.4 Reading period for MCCR

MC Reading period:  $T_{reading} = T_{fixed} + T_{prog\_delay} + T_{conv}$

On first reading,  $T_{fixed} = (2 \times T_{sys\_clk}) \pm 1 \times T_{sys\_clk}$

On subsequent readings,  $T_{fixed} = 0$ .

For example,

Set CH\_DELAY[5:0] = 17\; #delay 76 sys\_clk

Set ADC\_DATA\_RATE[4:0] = 5\; #DRO is 12000 sps

Set ADC\_NORMAL\_SETTLING = 0\; #Single-cycle mode

$T_{sys\_clk} = 1/sys\_clk = 1/4608000 = 0.217 \text{ us}$

$T_{prog\_delay} = 76 * T_{sys\_clk}$  #Table Channel Programmable Delay

$T_{conv} = 1/12000 = 83.3 \text{ us}$  #Table Data Rate

Hence,

On first reading,  $T_{reading} = 0.217 \text{ us} * (2 \pm 1 + 76) + 83.33 \text{ us} = 100.3 \pm 0.217 \text{ us}$

On subsequent readings,  $T_{reading} = 0.217 \text{ us} * (0 + 76) + 83.33 \text{ us} = 99.83 \text{ us}$ .

### 7.5.11 CMD\_MS (multichannel single-reading)

Start Multichannel Single-Reading (conversion) mode.

If `SYS_CONFIG0.ADC_SYNC = 0`, the conversion start is triggered by this SPI command at the last clock falling edge.

If `SYS_CONFIG0.ADC_SYNC = 1`, the conversion start is triggered by SYNC rising edge.

Upon completion of each ADC conversion, the logic channel pointer is auto-incremented to the next enabled channel and awaits the arrival of a conversion start trigger. The ADC loops back to the first enabled channel when the last enabled channel is complete.

This reading mode could be terminated by issuing the `CMD_END` or `CMD_ABORT`.

If SYNC pulse or same conversion command is issued before completion of the conversion on the current channel, ADC aborts the conversion immediately and restarts the conversion on the current channel. (This is different from MM and MC modes, which restart on the first enabled channel)

Data can be read serially via the MISO pin after the DRDY pin asserts high or after the reading is completed.



7.5.11.1 Flow chart - MCSR

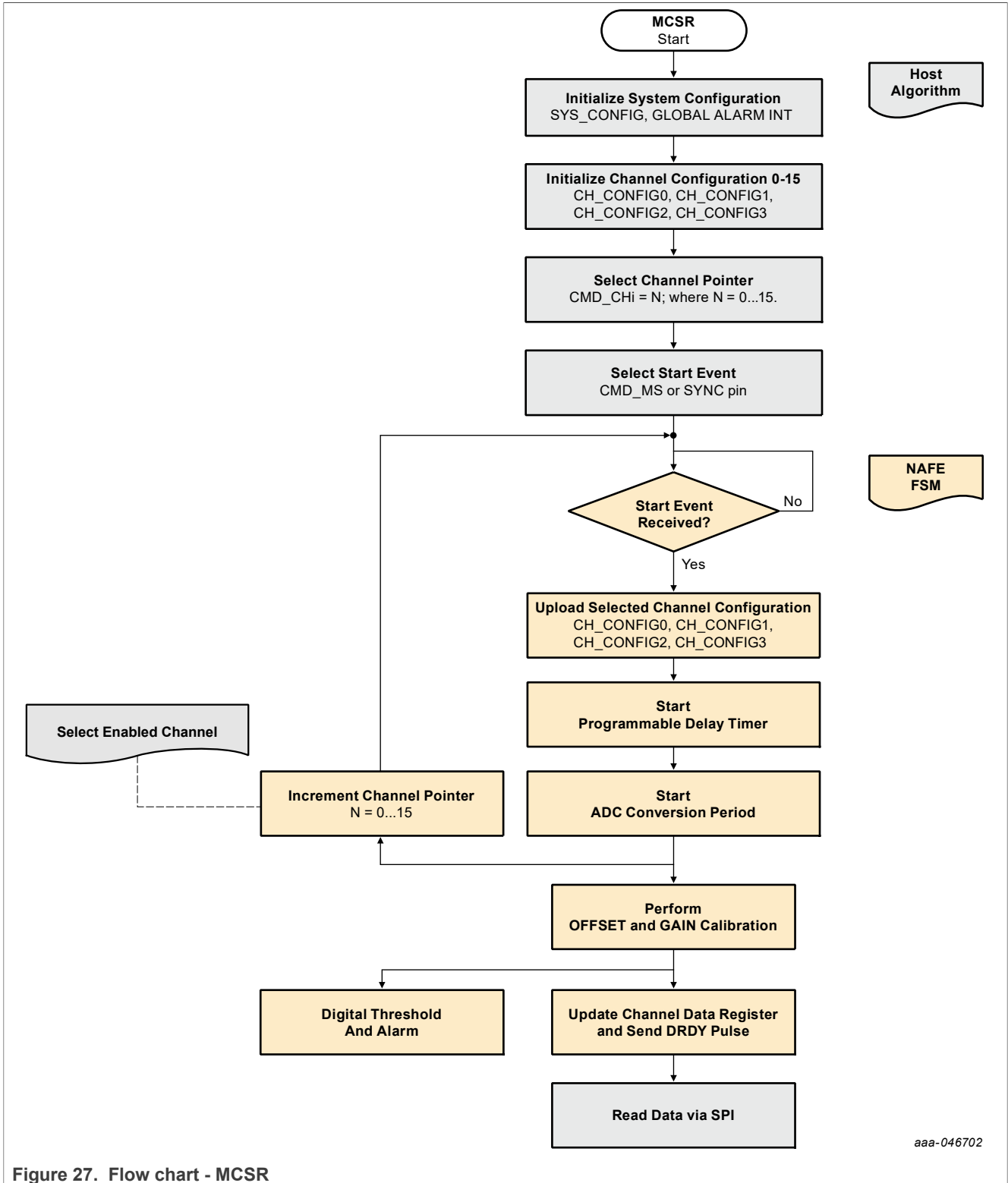


Figure 27. Flow chart - MCSR

7.5.11.2 Timing diagram - Flow chart - MCSR



Figure 28. Timing diagram - Flow chart - MCSR

7.5.11.3 Code example - Flow chart - MCSR

```

Reg_Read ('SYS_STATUS0) ; to clear INTB
Reg_write ('SYS_CONFIG, sys_config_data); //
Reg_write ('CH_CONFIGi, ch_config_datai); // i = 0...15
Send CMD_CHi;
Send CMD_MS;
Send SYNC Pulse (if SYNC_BIT = 1);
    
```

7.5.11.4 Reading period for MCSR

MS Reading period:  $T_{reading} = T_{fixed} + T_{prog\_delay} + T_{conv}$

On single reading,  $T_{fixed} = (2 \times T_{sys\_clk}) \pm 1 \times T_{sys\_clk}$

For example,

Set CH\_DELAY[5:0] = 17\; #delay 76 sys\_clk

Set ADC\_DATA\_RATE[4:0] = 5; #DRO is 12000 sps

Set ADC\_NORMAL\_SETTLING = 0; #Single-cycle mode

$T_{sys\_clk} = 1 / sys\_clk = 1 / 4608000 = 0.217\ \mu s$

$T_{prog\_delay} = 76 * T_{sys\_clk}$  #Table Channel Programmable Delay

$T_{conv} = 1 / 12000 = 83.3\ \mu s$  #Table Data Rate

Hence,

On single reading,  $T_{reading} = 0.217\ \mu s * (2 \pm 1 + 76) + 83.33\ \mu s = 100.3 \pm 0.217\ \mu s$ .

### 7.6 ADC code to voltage translation

ADC code output can be translated to voltage with the simple formula provided in [Table 20](#).

**Note:** For HVMUX inputs, the readout voltage is scaled by PGA gain setting and the LVMUX diagnostic voltage readout is scaled with a fixed gain of 2.5.

24-bit ADC hexadecimal code maximum (most positive) is 7F\_FFFFh and minimum (most negative) is 80\_0000h. The equivalent max- and min-signed decimal are 8,388,607 and -8,388,608 respectively.

The temperature sensor 16-bit code continuous readout is independent of main the ADC. The code to temperature translation is provided in [Table 20](#).

Table 20. ADC code conversion formulas

Description	Gain	Formula
24-bit Hex to signed Decimal, sINT <sub>24</sub>	-	$sINT_{24} = [ (\text{hex2dec}(\text{Hex}) + 2^{23}) \% 2^{24} ] - 2^{23}$
16-bit Hex to signed Decimal, sINT <sub>16</sub>	-	$sINT_{16} = [ (\text{hex2dec}(\text{Hex}) + 2^{15}) \% 2^{16} ] - 2^{15}$
24-bit ADC scaled voltage	Gain	$VG = 10 / 2^{24} * (sINT_{24} / GAIN)$
16-bit ADC scaled voltage	Gain	$VG = 10 / 2^{16} * (sINT_{16} / GAIN)$
HV inputs	0.2, 0.4, 0.8	$V_{HV} = VG$
LV: GPIO0-GPIO1	2.5	$V_{GPIO} = 1 * (VG + 0)$
LV: REF2	2.5	$V_{REF2} = 2 * (VG + 1.5)$
LV: AVDD	2.5	$V_{AVDD} = 2 * (VG + 1.5)$
LV: HVDD	2.5	$V_{HVDD} = 32 * (VG + 0.25)$
LV: HVSS	2.5	$V_{HVSS} = -32 * (VG - 0.25)$
Temperature, DIE_TEMP[15:0]	-	$T (^{\circ}C) = sINT_{16} / 64$

### 7.7 Diagnostic features

The NAFE13388 is equipped with temperature and voltage condition monitoring and anomaly detection circuitries for system and self diagnostics. These flexible and configurable global alarms to allow the user to configure for various applications and needs. Useful, programmable-input signal monitoring and interrupt is also made available, as described in the following sections.

Table 21. Alarm and interrupt

Register	Bit order	Bit name	RW	Reset	Description
GLOBAL ALARM ENABLE 0x32\h	15	OVER_TEMP_ALARM	RW	0x0	Overtemperature warning at 145 °C
	14	HVDD_ALARM	RW	0x0	Enable alarm for HVDD supply detect below preset threshold.
	13	HVSS_ALARM	RW	0x0	Enable alarm for HVSS supply detect above preset threshold.
	12	ADVDD_ALARM	RW	0x0	Enable alarm for DVDD supply detect below preset threshold.
	11	reserved	RW	0x0	reserved
	10	GPI_POS_ALARM	RW	0x0	Enable alarm for rising edge detected at any GPI pins.
	9	GPI_NEG_ALARM	RW	0x0	Enable alarm for falling edge detected at any GPI pins.
	8	CONFIG_ERROR_ALARM	RW	0x0	Enable alarm for register configuration error.
	7	OVRNRNG_ALARM	RW	0x0	Enable alarm when one or more data channels is over-range
	6	UNDRNG_ALARM	RW	0x0	Enable alarm when one or more data channels is under-range.
	5	OVRLOAD_ALARM	RW	0x0	Enable alarm when one or more data channels is overloaded or underloaded.
	4	EXTCLK_FREQ_ALARM	RW	0x0	Enable alarm when EXTCLK or XTAL clock period deviates > 20 % from 18.432 MHz INTOSC.
	3	reserved			reserved
	2	VIEX_OVLD_ALARM	RW	0x0	Enable alarm for excitation voltage source is overloaded.
	1	VIEX_OI_ALARM	RW	0x0	Enable alarm for excitation current source is overloaded.
	0	TEMP_ALARM	RW	0x0	Enable programmable temperature alarm. The triggering threshold is set in THRS_TEMP register bit.
GLOBAL ALARM INT ERRUPT 0x33\h	15	OVER_TEMP_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALARM_STICKY
	14	HVDD_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALARM_STICKY.
	13	HVSS_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALARM_STICKY.
	12	ADVDD_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALARM_STICKY.
	11	reserved	R	0x0	reserved
	10	GPI_POS_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALARM_STICKY.
	9	GPI_NEG_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALARM_STICKY.
	8	CONFIG_ERROR_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALARM_STICKY.
	7	OVRNRNG_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALARM_STICKY.
	6	UNDRNG_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALARM_STICKY.
	5	OVRLOAD_ALARM	RW	0x0	Bit clear behavior controlled by GLOBAL_ALARM_STICKY.
	4	EXTCLK_FREQ_ALARM	RW	0x0	Bit clear behavior controlled by GLOBAL_ALARM_STICKY.
	3	reserved	RW	0x0	reserved
	2	VIEX_OV_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALARM_STICKY.
	1	VIEX_OI_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALARM_STICKY.
	0	TEMP_ALARM	RW	0x0	Bit clear behavior controlled by GLOBAL_ALARM_STICKY.

The alarm clearing behavior is determined by GLOBAL\_ALARM\_STICKY.

See [Section 7.9.2](#) for address, bit order, and description of various global alarm configurations available.

### 7.7.1 Input under-range and over-range

Each of the 16 configured channels is paired with its own channel-based programmable thresholds for under- or over-range detection based on its ADC output.

These channel-based over-range (OVRNRNG\_ALARM) and under-range (UNDRNG\_ALARM) conditions could also be set as INTB pin interrupt with register bit OVRNRNG\_INT = 1 and UNDRNG\_INT = 1, respectively.

If the ADC detects a max or min value generates an over-load (OVRLOAD\_ALARM) which could be set as INTB pin interrupt with register bit OVRLOAD\_ALARM\_INT = 1

### 7.7.2 REFH and REFL for diagnostic

REFL and REFH are two unbuffered, precise voltage sources connected to the analog input of HVMUXP and HVMUXN. With appropriate channel gain setting, it could be used as a reference channel or channel self-test in the field.

### 7.7.3 Voltage supply rail monitoring

The NAFE13388 can measure and monitor its own power supplies: HVDD, HVSS, and VDD.

When these values are read, a global alarm is issued if the read value is out of the user-programmed threshold. HVDD, HVSS, VDD (AVDD = DVDD) also have dedicated circuits with the undervoltage lockout (UVLO) to allow the device to operate above POR level at preset threshold.

### 7.7.4 Thermal monitoring and thermal shutdown

The NAFE13388 integrates a temperature sensor that allows continuous monitoring of die temperature by reading the DIE\_TEMP(0x34) register. In addition, a user-programmable alarm threshold THRS\_TEMP(0x37) can provide early over-temperature warning interrupt, TEMP\_INT.

The NAFE includes a thermal shutdown circuit to protect the device from overheating. The thermal monitoring circuit asserts an alarm if the temperature is in the range 145 °C. The circuit resets the chip when the junction temperature reaches 165 °C.

### 7.7.5 Alarm

EXTCLK\_FREQ\_ALARM is triggered when the period deviation of external clock to internal oscillator clock is more than 20 %.

INTB alarms for detected input rising or falling edge at GPIO pins (GPI\_POS\_INT and GPI\_NEG\_INT) could also be used with configured setting on GPIO\_CON, GPI\_ENABLE, GPI\_EDGE\_POS, GPI\_EDGE\_NEG.

### 7.7.6 Interrupts

The INTB pin of the chip is a NOR function of the internal 14-bit of global alarm interrupt (GAI) registers. Each of these GAI registers' bits can be written 1 or 0 to enable or disable independently by SPI's register write command to global alarm enable register (address = 0x32\h).

**Note:** When all the CH\_DATA readback is enabled, the readback data could be prepended with channel-specific status byte, by enabling SYS\_CONFIG0.STATUS\_EN. Each of the status bit is OR's of all 16 channels.

The logic equivalence is shown in [Figure 29](#).

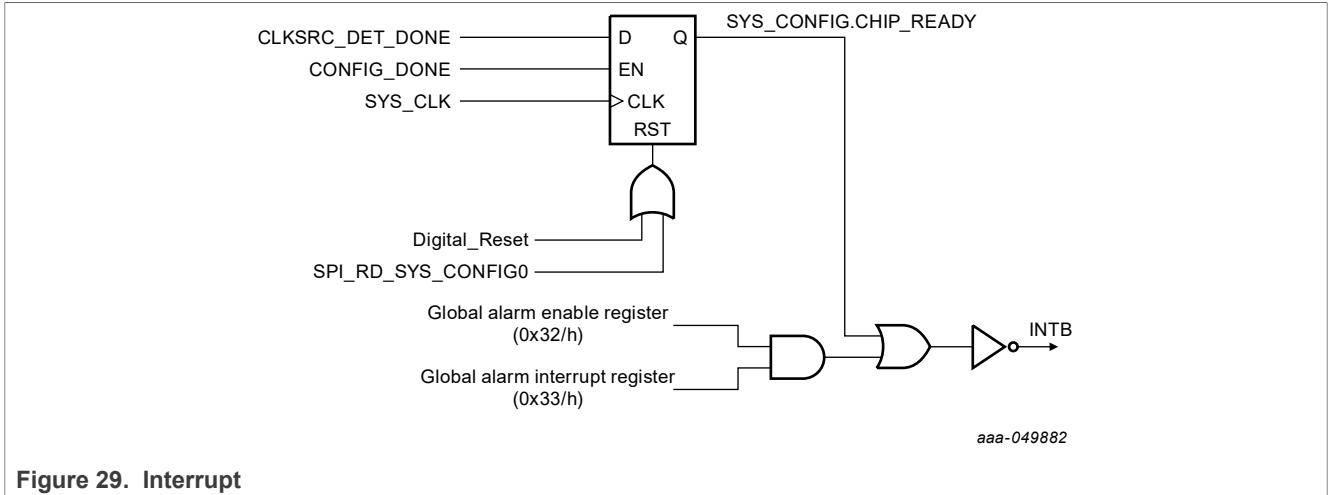


Figure 29. Interrupt

**Note:** The status byte is only prepended when reading out the ADC data with `SYS_CONFIG0.STATUS_EN=1`. Each individual status bit is concatenated in single byte listed in [Table 22](#).

Table 22. Status byte description

Status bit function	Representation Base		Bit index
	channel	global	
ADC underloaded or overloaded	√		7
ADC over user set threshold	√		6
ADC under user set threshold	√		5
VIEX_OV_ALARM or VIEX_OI_ALARM	√		4
PGA is overloaded	√		3
Current die temperature over user-set threshold		√	2
Clock alarm error		√	1
Result of 3-bit logical OR of HVDD_ALARM, HVSS_ALARM, and AVDD_ALARM signals		√	0

These status bits behave independently of the `SYS_CONFIG0.GLOBAL_ALARM_STICKY` state. They behave depending on what `CMD_xy` was issued:

Command `CMD_SS`: Status become sticky until host initiates another conversion then the status updates accordingly. Host can clear this channel-based status by issuing `CMD_CLEAR_DATA` or `CMD_CLEAR_REG`.

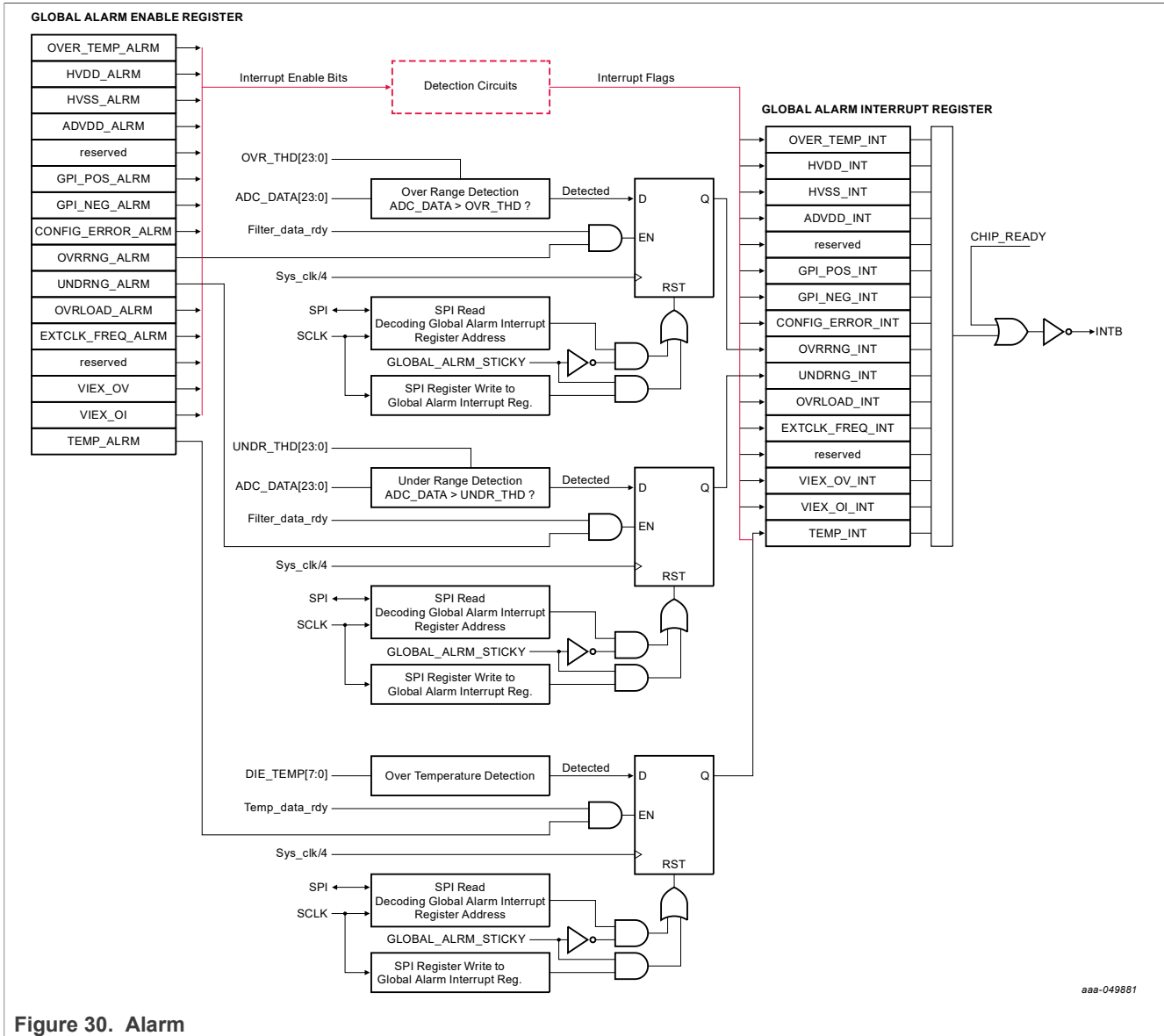
Commands `CMD_MM`, `CMD_MC`, `CMD_MS`, and `CMD_SC`: During multichannel or continuous conversions these status bits are updated live for each channel. For commands `CMD_MM` and `CMD_MS`, the last conversion channel status bits will not be cleared until the host issues `CMD_CLEAR_DATA` or `CMD_CLEAR_REG`.

This behavior applies for channel-based status during active conversion. The 5-MSB status bits are ADC underload/overflow, ADC over-range, ADC under-range, VIEX over/under, and PGA overload.

Global alarm interrupt (GAI) register (address `0x33\h`) can be configured non-sticky or sticky behavior by programming. `SYS_CONFIG0.GLOBAL_ALARM_STICKY = 0` or `SYS_CONFIG0.GLOBAL_ALARM_STICKY = 1`, respectively. When the sticky option is selected, each GAI register bit is set by hardware if an interrupt event occurs with respect to each functional bit described in the GAI register. The host needs to clear whatever bit is already set in the GAI register by writing 1 to the respective bit locations to see the next interrupt event.

**Note:** Writing 1 to the bit that is 0 in GAI register, will not alter it to 1.

7.7.7 Behavior of sticky v. non-sticky alarms



aaa-049881

Figure 30. Alarm

When the non-sticky option is selected, the content of the GAI register reflects the current chip or channel conversion status at the time the host reads this register. The functionality of the INTB pin depends on how the host program `SYS_CONFIG0.GLOBAL_ALARM_STICKY` bit. For example, `GLOBAL_ALARM_STICKY = 1`, sticky, INTB is de-asserted low until all interrupts are clear, whereas `SYS_CONFIG0.GLOBAL_ALARM_STICKY = 0`, non-sticky, INTB is low whenever there is an interrupt occurring and high whenever there is no interrupt. INTB might be toggling, meaning interrupt comes and goes regardless of GAI register read or not.

7.7.8 Configuration or loading error

When a user configuration error or chip error is detected, `GLOBALALARMINTERRUPT.CONFIG_ERROR_INT` will be asserted 1. A chip configuration error could be triggered by command `CMD_RELOAD`, at POR or pulling low on RSTB pin. If any of these events take place, on-chip NVM module loads the information to the shadow's trim registers and the data integrity is checked at this time. If the data was found to be corrupted or inconsistent, the configuration error would be set to 1.

## 7.8 SPI interface and controls

### 7.8.1 SPI signal pins

The SPI-compatible serial interface is used to read the conversion data, internal register content and to configure the device and control the ADC. The serial interface consists of four signals: CSB, SCLK, MOSI, and MISO. One external pin, SPI\_ADDR, is used as SPI address such that the host can address two devices without using a separate CSB pin. In addition, DRDY and SYNC signals allow the handshaking and data synchronization between the host and the device. The conversion data are provided with an optional CRC code for improved data integrity. 24-bit ADC word can be read with and without 8-bit CRC appended at the end of data.

The SPI pin functions are described in the following sub-sections.

#### 7.8.1.1 CSB (active low)

CSB is an input pin that enables the communication between the host and the chip. CSB must remain low for the entire data transaction. When CSB is set to high, the serial interface is reset, SCLK input and command inputs are ignored.

#### 7.8.1.2 SCLK

SCLK is the serial interface clock that operates up to 32 MHz. It is a noise-filtered, Schmitt-triggered input used to clock data in and out of the chip. Serial input data is latched in the falling edge of SCLK and serial data outputs from the chip are updated on the rising edge of SCLK.

#### 7.8.1.3 MOSI

MOSI is the serial data input to the chip. MOSI is used to input commands and register data to the chip.

#### 7.8.1.4 MISO

MISO is the serial data output from the chip. MISO data contains: internal registers data, ADC results, status byte, and/or 8-bit CRC if CRC\_EN and/or STATUS\_EN are set to 1, respectively. When CSB is high, MISO is in high-impedance. When CSB is low, MISO is updated on the rising edge of the SCLK.

#### 7.8.1.5 SPI\_ADDR

SPI\_ADDR is an additional input pin used to address a second device with a single CSB to reduce the number of chip select signals required.

#### 7.8.1.6 DRDY

DRDY (rising edge) is an output pin that indicates the conversion status. DRDY is driven to high when the new conversion result is stored in the SPI buffer and ready for reading.

DRDY pulse stays high for  $2 \times T_{\text{sys\_clk}}$  if SYS\_CONFIG0.DRDY\_PWDT bit = 0. Otherwise, the pulse stays high for  $8 \times T_{\text{sys\_clk}}$  if DRDY\_PWDT bit = 1.

#### 7.8.1.7 SYNC

SYNC is an external pin used to synchronize the data conversion to external events. The user can start any conversion mode either by using SPI command or asserting low to high transition on the SYNC pin given that the SYS\_CONFIG0.ADC\_SYNC bit = 1.



The minimum width of SYNC pulse should be  $2 \times T_{\text{sys\_clk}}$ .

7.8.1.8 INTB (active low)

INTB (active low) is an output pin that notifies when a global alarm interrupt has occurred. The driver can be programmed as open-drain with internal pullup or CMOS output.

7.8.2 SPI communication protocols

This section describes the user SPI communication protocols. The SPI host must always start with DEV\_AD bit either 0 or 1 to match the device ADDR0's pin to initiate the communication with that device. The following bits are: RW\_L bit (read or write transaction), 13 RA bits (addressable up to 8192 locations), and D is data from the host to the device or the device to the host depending on write or read operation, respectively. RW\_L should be set to 0 for write, whereas it should be 1 for read.

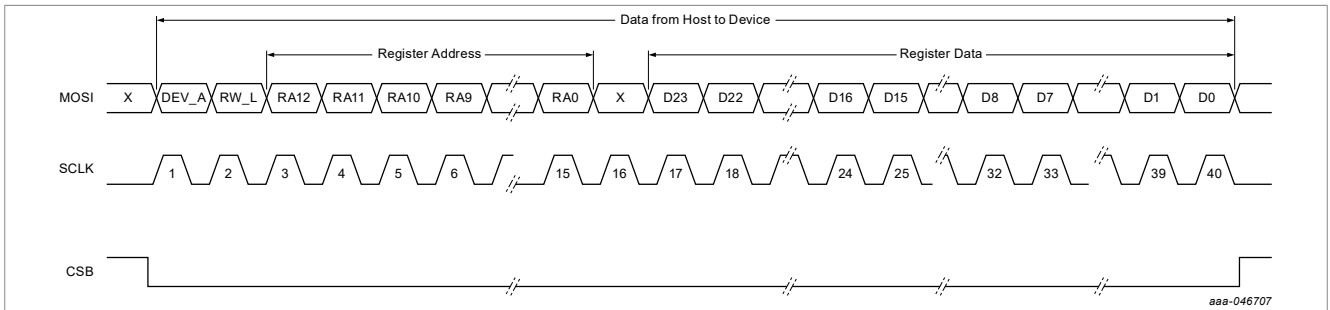


Figure 31. SPI write timing

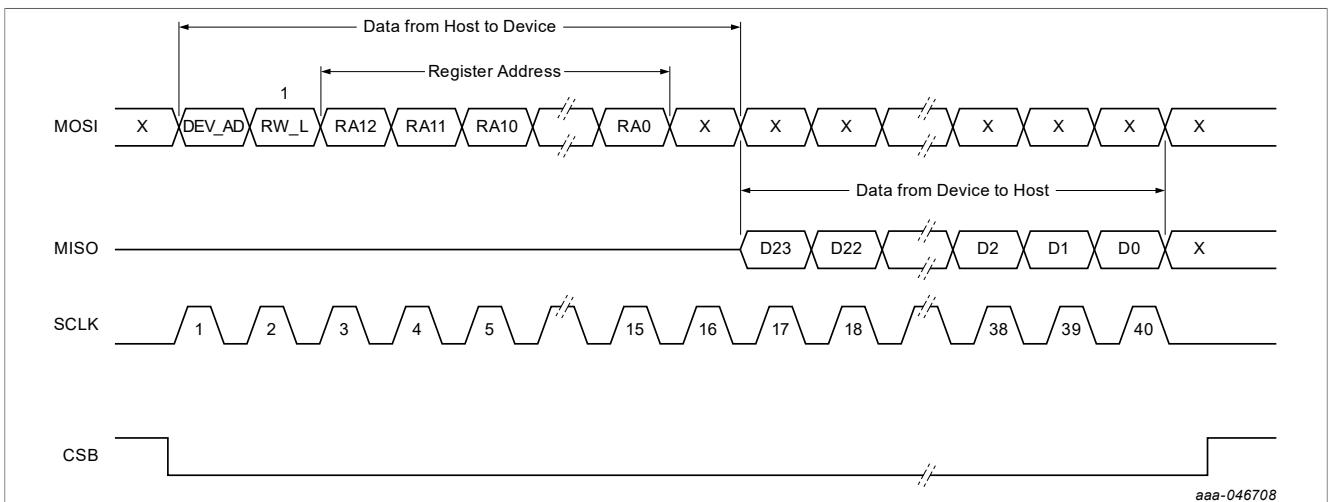
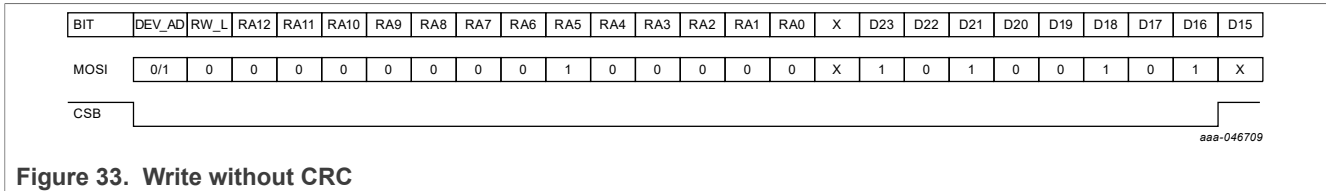


Figure 32. SPI read timing

7.8.2.1 Write without CRC

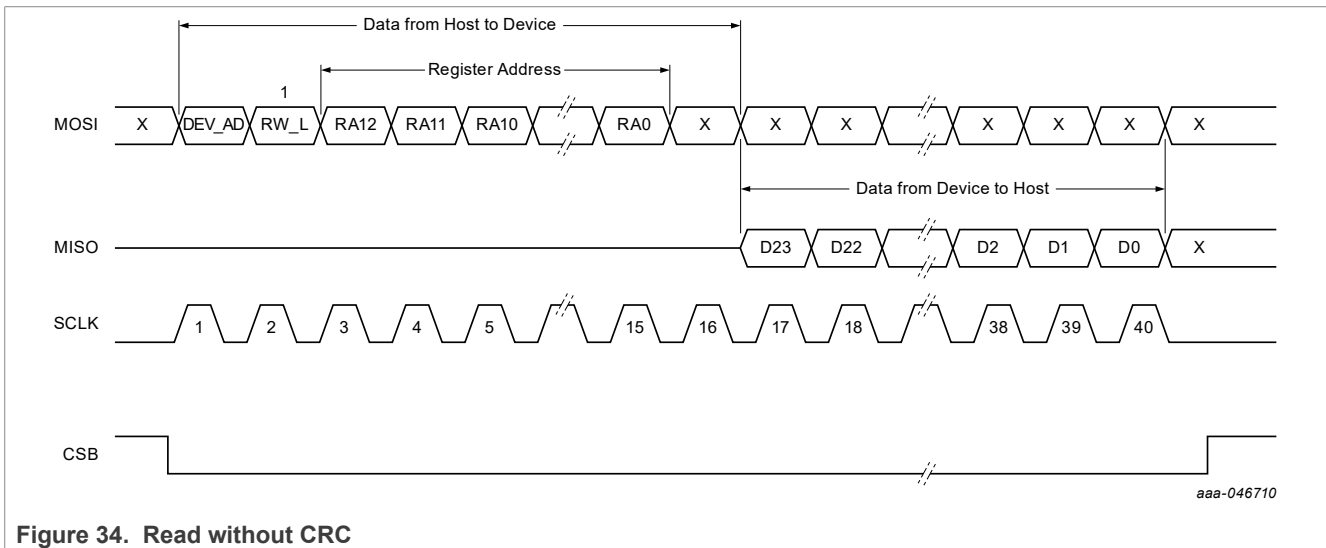
The second bit after the first SPI bit frame "RW\_L" is 0 indicates that it is a write transaction. SPI write command is used to configure the internal registers of the chip. The register values get updated every eighth clock cycle with a byte of data starting from the MSB. A minimum of eight SCLKs is needed to write the first byte of data in a multibyte register. For instance, if the user only needs to update the first MSB-byte (bit 23:16) of the register that has 24-bit data width and bits 15 to 0 retain the old value of the register, then eight SCLKs

are needed. Figure 33 shows the host partially write value 0xA5 to D23-D16 (bit location 23 to 16) of register 0x0020.



7.8.2.2 Read without CRC

The second bit after the first SPI bit frame "RW\_L" is 1 indicates it is a read transaction. SPI read command is used to read back the internal register contents of the chip and the ADC conversion results.



7.8.2.3 CRC-8 generator

The NAFE13388 provides assurance of the integrity of the data communication with optional 8-bit CRC data appended at the end of the data transfers. The CRC\_EN is bit 7 in the SYS\_CONFIG0 register, with CRC default off, CRC\_EN = 0. Setting CRC\_EN = 1 will enable CRC feature.

The following polynomial is always used in this chip:

$$y = x^8 + x^2 + x + 1 \text{ equivalent to binary number is } 100000111.$$

The cyclic redundancy byte is an error-detection byte that detects communication errors to and from the host and device. CRC byte is the division remainder of the payload data of CRC polynomial in which the polynomial function is  $x^8 + x^2 + x + 1$ . The 9-bit binary coefficients are: 100000111b. The payload data are either two or three bytes depending on the data transfer operation.

When CRC is enabled, the CRC byte is appended after the 16-bit command (two bytes) and after the ADC data.

7.8.2.4 16-bit command with CRC

The host computes the CRC over the 16-bit command and appends the 8-bit CRC to the command. The device performs the CRC calculation on 16-bit command and compares the result to the 8-bit CRC transmitted by the host. If the host and the device CRC values match, the command is executed. Otherwise, the command will be ignored and a CRC error is generated.

The CRC\_ERROR flag is routed out to GPIO2 if SYS\_CONFIG0.CRC\_ERROR\_ON\_GPIO2 is set to 1.

In addition, the CRC\_ERROR can be read on SYS\_STATUS0.CRC\_ERROR bit. The SYS\_STATUS0.CRC\_ERROR bit is cleared upon reading.

7.8.2.5 Write with CRC

Figure 35 and Figure 36 show the host writes NAFE 16-bit and 24-bit internal register respectively.

- **For 16-bit register write:** The host first calculates the 8-bit CRC\_A on 16-bit address and appends the 8-bit CRC\_A after the address. The host then calculates the 8-bit CRC\_D on 16-bit data and appends the 8-bit CRC\_D after 16-bit data.
- **For 24-bit register write:** The host first calculates the 8-bit CRC\_A on 16-bit address and appends the 8-bit CRC\_A after the address. The host then calculates the 8-bit CRC\_D on 24-bit data and appends the 8-bit CRC\_D after 24-bit data.

In both cases, the host should send an extra 8-bit clock to receive back the calculated CRC\_D from the device.

The 16-bit address register includes device ID bit, RW\_L bit, RA bits, and don't care bit (0).

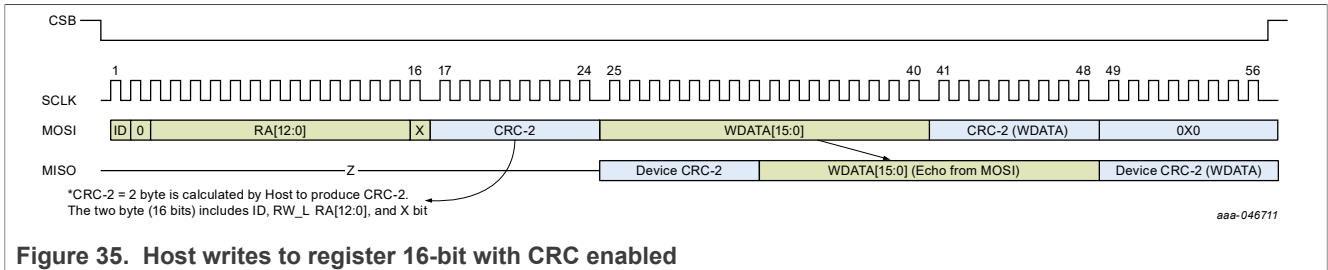


Figure 35. Host writes to register 16-bit with CRC enabled

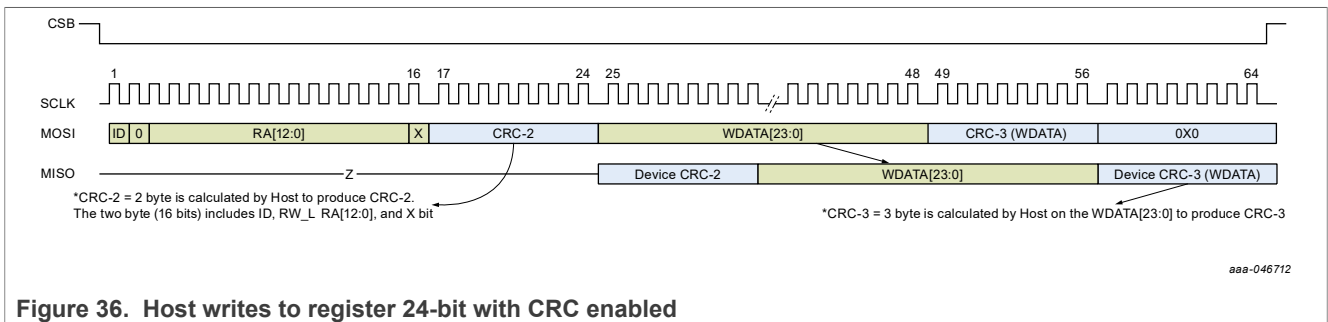


Figure 36. Host writes to register 24-bit with CRC enabled

7.8.2.6 Read with CRC

Figure 37 shows host read data from the 24-bit register. The host sends the first CRC byte, calculated based on the first 16-bit word, which includes device ID bit, RW\_L bit, RA bits, and don't care bit (0). The second CRC byte is from the device to the host. It is calculated based on RDATA from the device to the host. Figure 37 also shows host read data from the 16-bit register.

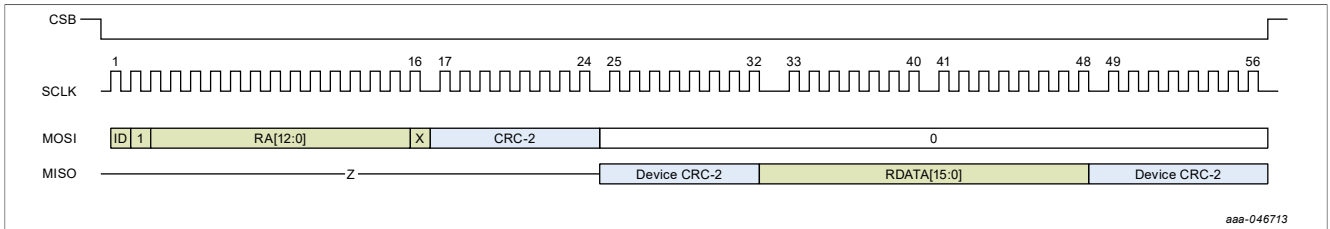


Figure 37. Host read data from the 24-bit register

7.8.2.7 System configuration with CRC

**Two-byte command:** Two-byte command format with no data return.

A non-return data command, including register write command, RW\_L bit is always set to 0. The figure below shows the timing of two-byte command with non-return ADC data.

- **Command examples:** CMD\_CH0, ... CMD\_CH15, CMD\_ABORT, CMD\_END, CMD\_CLEAR\_ALARM, CMD\_CLEAR\_DATA, CMD\_RESET, CMD\_REOAD

The host calculates the CRC of the two-input command bytes. Device CRC-2 byte is calculated by device, output based on the two received command bytes. If the two CRC values match, the command is executed at the beginning of the last falling edge of SCLK of the fourth byte in the sequence. Asserting CSB high before the command completes will result in command termination. When a new command starts, the device must see the CSB transition from high to low.

If both CRC\_EN, and STATUS byte output format are enabled, then the CRC calculation includes status byte plus the ADC conversion data, CRC4 for 24-bit ADC and CRC3 for 16-bit ADC.

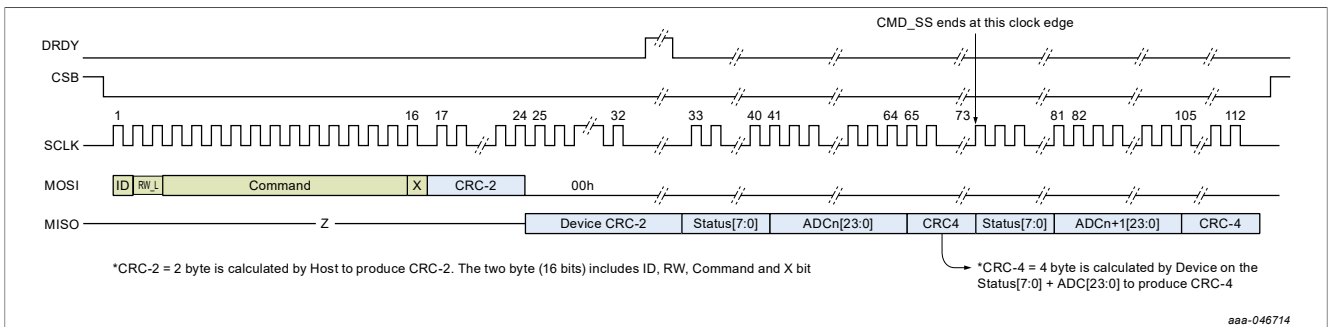
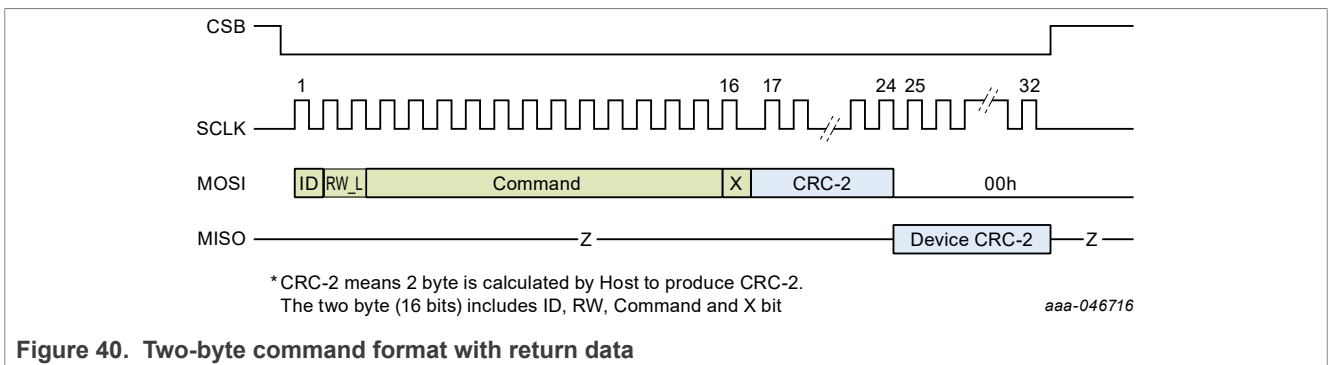
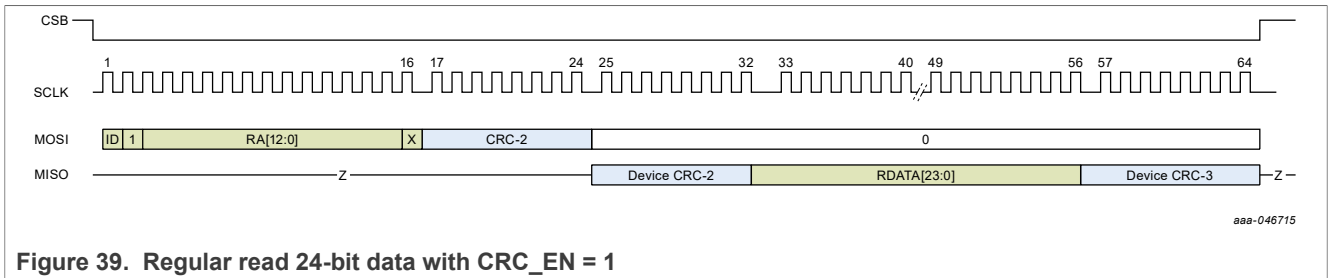


Figure 38. Conversion command data read operation 2/24-bit ADC, CRC\_Enable = 1, Status\_Enable = 0

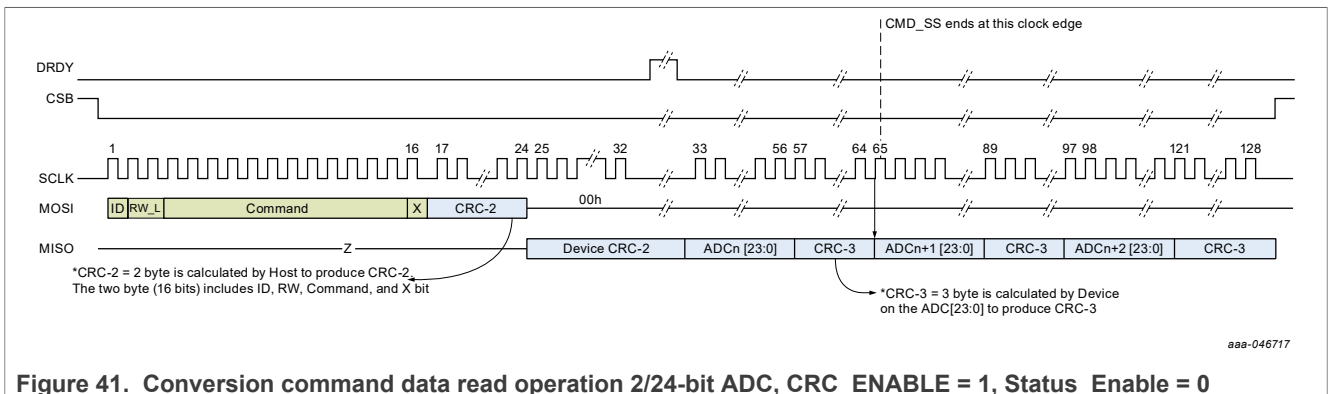


**Two-byte command:** Two-byte command format with data return.

A return data command, including register read command, RW\_L bit is always set to 1. [Figure 41](#) shows the timing of two-byte command with ADC data return.

- **Command examples:** CMD\_SS, CMD\_SC, CMD\_MM, CMD\_MC, and CMD\_BURST\_DATA

The host calculates CRC of the two-input bytes and sends the CRC-2 after the 16-bit command. Device CRC-2 byte is calculated by device, output based on the two received command bytes. If the two CRC values match, the command is executed. After the host sends CRC byte, it can continue to send eight more clocks to get the device calculated CRC before DRDY goes high. The host can keep the CSB low, while waiting for DRDY to assert HI, then provide the number of clocks required to retrieve the ADC conversion data along with its respective calculated CRC. If the device is 24-bit ADC, then CRC calculation will be based on three ADC bytes. If the device is 16-bit ADC, then CRC calculation will be based on two ADC bytes.



### 7.8.3 SPI programming and commands

The SPI instruction commands are dedicated SPI addresses with predefined functions for reducing SPI transactions on frequent data accesses and controls. This section is a summary of all the instruction commands.

**Note:** Instruction commands are encoded with 0's in bits RA5 to RA12. Registers are offset at address 0x20\h and RA5 bit is always set to 1 when accessing the registers.

**7.8.3.1 Commands definition**

16-bit SPI instructions and mnemonic.

**7.8.3.1.1 CMD channel selection**

CMD\_CHi should be used to select the logic channel CHx where x = 0...15

**Table 23. CMD channel selection**

RW_L	RA12	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	Mnemonic	HEX Code
0	0	0	0	0	0	0	0	0	0	0	0	0	0	CMD_CH0	0x0000
0	0	0	0	0	0	0	0	0	0	0	0	0	1	CMD_CH1	0x0001
0	0	0	0	0	0	0	0	0	0	0	0	1	0	CMD_CH2	0x0002
0	0	0	0	0	0	0	0	0	0	0	0	1	1	CMD_CH3	0x0003
0	0	0	0	0	0	0	0	0	0	0	1	0	0	CMD_CH4	0x0004
0	0	0	0	0	0	0	0	0	0	0	1	0	1	CMD_CH5	0x0005
0	0	0	0	0	0	0	0	0	0	0	1	1	0	CMD_CH6	0x0006
0	0	0	0	0	0	0	0	0	0	0	1	1	1	CMD_CH7	0x0007
0	0	0	0	0	0	0	0	0	0	1	0	0	0	CMD_CH8	0x0008
0	0	0	0	0	0	0	0	0	0	1	0	0	1	CMD_CH9	0x0009
0	0	0	0	0	0	0	0	0	0	1	0	1	0	CMD_CH10	0x000A
0	0	0	0	0	0	0	0	0	0	1	1	0	0	CMD_CH11	0x000B
0	0	0	0	0	0	0	0	0	0	1	1	0	1	CMD_CH12	0x000C
0	0	0	0	0	0	0	0	0	0	1	1	0	1	CMD_CH13	0x000D
0	0	0	0	0	0	0	0	0	0	1	1	1	0	CMD_CH14	0x000E
0	0	0	0	0	0	0	0	0	0	1	1	1	1	CMD_CH15	0x000F

**7.8.3.1.2 CMD initialize/clear**

The encoded 16-bit SPI instructions for clear and reset are:

CMD\_CLEAR\_ALARM, CMD\_CLEAR\_DATA, CMD\_CLEAR\_REG, CMD\_RELOAD, and CMD\_RESET.

Three types of resets are available:

- Chip power-on reset (POR)
- RSTB accessible by pulling the pin to ground
- CMD\_RESET

Hardware reset is achieved by pulling pin RSTB = 0 V or POR. When in reset, all HV input pins and GPIO pins are in high-Z input mode, internal voltage reference is used, ADC digital filters are cleared, all user registers are set to their default values and all NVM shadow register content will be reloaded. The input clock source will be defaulted back to internal RC oscillator and go through autoclock switching within 50 ms if the external clock is applied or crystal is installed.

CMD\_RESET is the same as the hardware reset by pulling RSTB pin down to GND.

Issuing the CMD\_CLEAR\_ALARM command clears GLOBAL ALARM INTERRUPT bits at register address: 0x33\h.

Issuing the CMD\_CLEAR\_DATA command will clear all channel data (CH\_DATA0 – CH\_DATA15) registers to 0x000000.

Issuing the CMD\_CLEAR\_REG command clears the user registers, except the clock source select, SYS\_CONFIG0.CK\_SRC\_SEL [1:0]. The clock source select bit does not get cleared even if they are part of the user's registers. The user can change this register after POR, while any conversion is in active. For instance, if CK\_SRC\_SEL held a value other than 0 before the command was issued, it would stay the same after this command was issued.

**Note:** CRC\_EN is also cleared.

Issuing the CMD\_RELOAD command reloads NVM contents to shadow registers. NVM contents consist of the NAFE trims parameters and offset and gain calibration coefficients. This command does not reset user registers.

Table 24. CMD initialize/clear

RW_L	RA12	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	Mnemonic	HEX Code
0	0	0	0	0	0	0	0	0	1	0	0	0	0	CMD_ABORT	0x0010
0	0	0	0	0	0	0	0	0	1	0	0	0	1	CMD_END	0x0011
0	0	0	0	0	0	0	0	0	1	0	0	1	0	CMD_CLEAR_ALARM	0x0012
0	0	0	0	0	0	0	0	0	1	0	0	1	1	CMD_CLEAR_DATA	0x0013
0	0	0	0	0	0	0	0	0	1	0	1	0	0	CMD_RESET	0x0014
0	0	0	0	0	0	0	0	0	1	0	1	0	1	CMD_CLEAR_REG	0x0015
0	0	0	0	0	0	0	0	0	1	0	1	1	0	CMD_RELOAD	0x0016
0	0	0	0	0	0	0	0	0	1	0	1	1	1	TBD	0x0017

7.8.3.1.3 CMD reading modes

Table 25. CMD reading modes

RW_L	RA12	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	Mnemonic	HEX Code
1	0	0	0	0	0	0	0	0	0	0	0	0	0	CMD_SS	0x2000
1	0	0	0	0	0	0	0	0	0	0	0	0	1	CMD_SC	0x2001
1	0	0	0	0	0	0	0	0	0	0	0	1	0	CMD_MM	0x2002
1	0	0	0	0	0	0	0	0	0	0	0	1	1	CMD_MC	0x2003
1	0	0	0	0	0	0	0	0	0	0	1	0	0	CMD_MS	0x2004

CMD\_SS: Set Single-Channel Single-Reading (conversion) mode. If bit ADC\_SYNC = 0, the conversion start is triggered by this SPI command at the last SPI clock falling edge. If bit ADC\_SYNC = 1, the conversion start is triggered by SYNC rising edge. In both cases, the conversion is executed on the selected channel. After the conversion completion, the device returns to waiting state. (SS: Single-channel Single-reading)

CMD\_SC: Set Single-Channel Continuous-Reading (conversion) mode. If bit ADC\_SYNC = 0, the conversion start is triggered by this SPI command at the last clock falling edge. If bit ADC\_SYNC = 1, the conversion start is triggered by SYNC rising edge. In both cases, the conversion is executed on the selected channel until it is interrupted or restarted. The conversion could be interrupted by CMD\_ABORT and CMD\_END, or could be aborted and restarted by SYNC pulse if ADC\_SYNC = 1 or any conversion command if ADC\_SYNC = 0. (SC: Single-channel Continuous reading)

CMD\_MC: Set Multichannel Continuous-readings (conversions) autonomous mode. The CMD\_MC is similar to CMD\_MM with infinite loop until it is interrupted or restarted. (MC: Multichannel Continuous reading)

CMD\_MS: Set Multichannel Single Reading (conversions) mode. If bit ADC\_SYNC = 0, the conversion start is triggered by this SPI command at the last clock falling edge. If bit ADC\_SYNC = 1, the conversion start is triggered by SYNC rising edge. Upon completion of each ADC conversion, the logic channel pointer is auto-incremented to the next enabled channel and awaits the arrival of a conversion start trigger. The ADC will loop back to first enabled channel when the last enabled channel was completed. This reading mode could be terminated by issuing the CMD\_END or CMD\_ABORT. If SYNC pulse or same conversion command is issued before completion of the conversion on the current channel, ADC aborts the conversion immediately and

restarts the conversion on the current channel. (This is different from MM and MC modes, which restart on the first enabled channel.) (MS: Multi-channel Single-reading)

7.8.3.1.4 CMD burst data

Table 26. CMD burst data

RW_L	RA12	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	Mnemonic	HEX Code
1	0	0	0	0	0	0	0	0	0	0	1	0	1	CMD_BURST_DATA	0x2005

CMD\_BURST\_DATA: Burst read the enabled data channels CH\_DATA from CH0 to CH15 sequentially (determined by MCH\_EN[15:0] bits).

**Note:** If MCH\_EN = 0x8000, data in CH\_DATA15 is read.

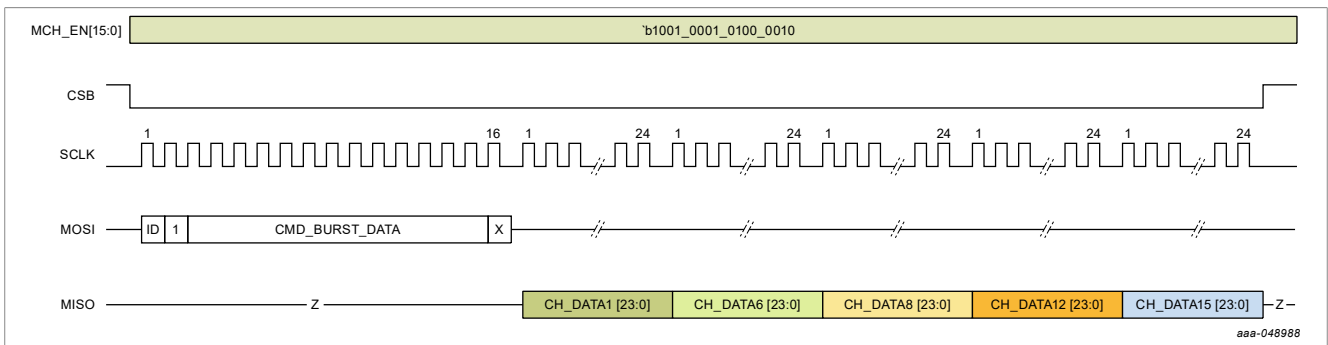


Figure 42. Burst data command

7.8.3.1.5 CMD CRC

Table 27. CMD CRC

RW_L	RA12	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	Mnemonic	HEX Code
1	0	0	0	0	0	0	0	0	0	0	1	1	0	CMD_CALC_CRC_CONFIG	0x2006
1	0	0	0	0	0	0	0	0	0	0	1	1	1	CMD_CALC_CRC_COEF	0x2007
1	0	0	0	0	0	0	0	0	0	1	0	0	0	CMD_CALC_CRC_FAC	0x2008

CMD\_CALC\_CRC\_CONFIG: Calculate CRC sum for all 16-bit user configuration registers and save result to 0x25\h(CRC\_CONFIG\_REGS).

CMD\_CALC\_CRC\_COEF: Calculate CRC sum for all 24-bit CAL coefficient and threshold registers and save result to 0x26\h(CRC\_COEF\_REGS).

CMD\_CALC\_CRC\_FAC: Calculate all factory OTP trim registers and save result to 0x27\h(CRC\_TRIM\_INT[15:0]).

After the command is issued by the host, the user must wait for DRDY assert high or wait for ~ 64 system clock period to read back the CRC calculation result at register address at 0x25, 0x26, or 0x27 if CMD\_CALC\_CRC\_CONFIG, CMD\_CALC\_CRC\_COEF, or CMD\_CALC\_CRC\_FAC is used respectively.



7.8.3.1.6 Read/Write

Table 28. Read/Write

RW_L	RA12	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	Mnemonic	HEX Code
1	RA12	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	eg: Read register CH_CONFIG0 : Reg_Rd(0x2020)	0x2000+RA(offset)
0	RA12	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	eg: Write register CH_CONFIG0 : Reg_Wr (0x0020, Data)	0x0000+RA(offset)

7.8.3.2 Channel data readback

ADC conversion results can be read by two methods:

1. Directly after conversion, read data is stored to the channel data register indicated by the rising edge of DRDY. The conversion result is automatically transferred to the SPI data buffer while the host provides the SPI clock. However, the CSB needs to stay low after the start conversion event has been issued.
2. Read data from the channel data register. This requires a new SPI transaction that addresses and fetches the channel data register.

By default, DRDY asserts high for two sys\_clk periods. This pulse width can be programmed to eight sys\_clk periods by setting SYSTEM\_CONFIG0.15 (DRDY\_PWDT) to 1.

7.9 Register map

There are three types of registers:

- 16-bit configuration and status registers
- 24-bit coefficient registers
- 24-bit or 16-bit data registers for 24-bit or 16-bit options

7.9.1 16-bit channel-based configuration

CH\_CONFIG0..2[15:0] are channel-based registers. Before reading or writing to CH\_CONFIG registers of a channel, select the channel by issuing CMD\_CHi to set the read/write pointer. The status register bits CONFIG\_CH\_PTR[3:0] show the channel pointer location. A total of 16 logical channels are available: CH0..CH15.

Table 29. 16-bit channel-based configuration

Register(16-bit)	Bit order	Bit name	RW	Reset	Short description
CH_CONFIG0 0x20\h	15:12	HV_AIP[3:0]	RW	0x0	HV Positive input pin select: 0\h = internal GND, 1\h = AI1P, 2\h = AI2P, 3\h = AI3P, 4\h = AI4P, 5\h = REFH, 6\h = REFL, 7\h = AICOM, 8\h = not used, 9\h to F\h = not used.
	11:8	HV_AIN[3:0]	RW	0x0	HV Negative input pin select: 0\h = internal GND, 1\h = AI1N, 2\h = AI2N, 3\h = AI3N, 4\h = AI4N, 5\h = REFH, 6\h = REFL, 7\h = AICOM, 8\h = not used, 9\h to F\h = not used.
	7:5	CH_GAIN[2:0]	RW	0x0	Select the channel gain (V/V): 0\h = 0.2x, 1\h = 0.4x, 2\h = 0.8x, 3\h-7\h = unused.
	4	HV_SEL	RW	0x0	Select HV or LV signals for ADC conversion: 0 = LVSIG_IN, 1\h = HV_AIP-HV_AIN signals.
	3:1	LVSIG_IN[2:0]	RW	0x0	LV signals (pos, neg) select: 0\h = (REF/2,REF/2), 1\h = (GPIO0,GPIO1), 2\h = (REF_Coarse,REF/2), 3\h = (VADD,REF/2), 4\h = (VHDD,REF/2), 5\h = (REF/2,VHSS),
CH_CONFIG1 0x21\h	0	TCC_OFF	RW	0x0	Proprietary Channel Temperature Coefficient Correction: 0\h = TCC ON, 1\h = TCC OFF
	15:12	CH_CAL_GAIN_OFFSET[3:0]	RW	0x0	The pointer to select 1 of 16 calibrated gain and offset coefficient pairs in the Calibrated Channel Coefficient Registers. See <a href="#">Table 14</a> .
	11:8	CH_THRS[3:0]	RW	0x0	Channel Over- and under-range threshold: See <a href="#">Table 30</a> .

Table 29. 16-bit channel-based configuration...continued

Register(16-bit)	Bit order	Bit name	RW	Reset	Short description
	7:3	ADC_DATA_RATE[4:0]	RW	0x00	ADC data rate: See <a href="#">Table 7</a>
	2:0	ADC_SINC[2:0]	RW	0x0	ADC sinc filter select 0h = bypass, 1h = SINC1, 2h = SINC2, 3h = SINC3, 4h = SINC4, 5h to 7h = bypass.
CH_CONFIG2 0x22h	15:10	CH_DELAY[5:0]	RW	0x0	Preset channel delay before ADC start conversion: (# of SYSCLK cycle) 0h = 0, 1h = 2, 2h = 4, 3h = 6, 4h = 8, 5h = 10, 6h = 12, 7h = 14, 8h = 16, 9h = 18, Ah = 20, Bh = 28, Ch = 38, Dh = 40, Eh = 42, Fh = 56, 10h = 64, 11h = 76, 12h = 90, 13h = 128, 14h = 154, 15h = 178, 16h = 204, 17h = 224, 18h = 256, 19h = 358, 1Ah = 512, 1Bh = 716, 1Ch = 1024, 1Dh = 1664, 1Eh = 3276, 1Fh = 7680, 20h = 19200, 21h-3Fh = 23040.
	9	ADC_NORMAL_SETTLING	RW	0x0	ADC single-cycle settling or Normal Settling: 0h = Single-cycle settling(SCS), 1h = Normal settling(NS)
	8	ADC_FILTER_RESET	RW	0x0	Reset ADC digital filters at the start of every ADC conversion when set. 0h = hold digital filter data from previous conversion, 1h = reset digital filters.
	7	CH_CHOP	RW	0x0	Enable input channel level chopping with 2 ADC conversions (Precision mode): 0h = Normal mode, 1h = Precision mode with 2 conversions chopping. (This supercedes the VIEX_CHOP)
CH_CONFIG3 0x23h	6:0	reserved			
	15	VIEX_VI	RW	0x0	Select Excitation source: 0 = Voltage, 1 = Current.
	14	VIEX_POL	RW	0x0	ExcitationV/I source polarity, 0 = positive polarity, 1 = negative polarity. See <a href="#">Table 16</a> .
	13:10	VIEX_MAG[3:0]	RW	0x0	ExcitationV/I source magnitude. See <a href="#">Table 16</a> .
	9	VEXC_EN	RW	0x0	Turn on excitation voltage source to enable internal direct routing from source to Input HVMUX. 0h = Disable VEXC voltage output 1h = Enable VEXC voltage output
	8	OPEN_DET_CURRENT (ODC)	RW	0x0	Excitation 65 nA sourcing current for open detection. (This bit supercedes VIEX_VI)
	7	reserved			
	6	VIEX_CHOP	RW	0x0	Enable excitation V/I source polarity chopping with two ADC conversions: (if VIEX_CHOP and CH_CHOP are both set, VIEX_CHOP bit is ignored) 0h = Normal, 1h = 2 conversions with polarity chopping.
CH_CONFIG4 0x24h	5:3	VIEX_AIP_EN[2:0]	RW	0x0	Excitation source output is applied to single pin AIxP: 0h = none, 1h = AI1P pin, 2h = AI2P pin, 3h = AI3P pin, 4h = AI4P pin, 5h to 7h = none.
	2:0	VIEX_AIN_EN[2:0]	RW	0x0	Excitation source output is applied to single pin AIxN: 0h = none, 1h = AI1N pin, 2h = AI2N pin, 3h = AI3N pin, 4h = AI4N pin, 5h to 7h = none.
CH_CONFIG4 0x24h	15:0	MCH_EN[15:0]	RW	0x0000	Enable logical configurable channel for ADC conversion in Sequencer mode: 0 = disable, 1 = enable. CH15 is bit15, CH0 is bit0.

7.9.2 24-bit channel-based coefficient and data registers

24-bit channel-based registers:

- Output data: DATA0..15
- Over-range alarm threshold: OVR\_THRS0..15
- Under-range alarm threshold: UDR\_THRS0..15
- Factory or user-calibration gain coefficients: GCC0..15
- Factory or user-calibration offset coefficients: OCC0..15

The non-channel based registers OPT0..15 are optional coefficients used for storing factory calibrated parameters.

Table 30. 24-bit channel-based coefficient and data registers

Register (24-bit)	Bit order	Bit name	RW	Reset	Short description
CH_DATA0..15 0x40h - 0x4Fh	23:0	DATA0[23:0] .. DATA15[23:0]	R	0x00_0000	Channel output data. Each channel has a corresponding data register. DATA0[23:0] is converted output of CH0.. DATA15[23:0] is converted output of CH15.
CH_CONFIG5 0x50h - 0x5Fh	23:0	OVR_THRS0[23:0] .. OVR_THRS15[23:0]	RW	0x00_0000	Over-range threshold setting for each logical data channel.

Table 30. 24-bit channel-based coefficient and data registers...continued

Register (24-bit)	Bit order	Bit name	RW	Reset	Short description
CH_CONFIG6 0x60h-0x6Fh	23:0	UDR_THRS0[23:0] .. UDR_THRS15[23:0]	RW	0x00_0000	Under-range threshold setting for each logical data channel.
GAIN_COEF0..15 0x80h-0x8Fh	23:0	GCC[23:0]	RW	0x	Calibrated gain coefficients. The user may alter or update the values to fit their application. For each of the logical channel setup, these GAIN_COEF registers are indexed addressable by pointer set by register bits CH_CAL_GAIN_OFFSET[4:0]. Initially after CHIP_READY, the content of these registers are populated with factory-calibrated coefficients, refer to TABLE_FAC_COEF if applicable. <b>Note:</b> Whenever the chip is in RESET, the factory-calibrated coefficient is reloaded from OTP into the registers. These same registers are used for displaying the factory calibrated coefficient upon RESET in certain order. However, the user has full read/write access and may reshuffle the order and coefficient values according to user-configured channels.
OFFSET_COEF0..15 0x90h-0x9Fh	23:0	OCC[23:0]	RW	0x	Calibrated offset coefficients. The user may alter or update the values to fit their application. For each of the logical channel setup, these OFFSET_COEFF registers are indexed addressable by pointer set by register bits CH_CAL_GAIN_OFFSET[4:0]. Initially after CHIP_READY, the content of these registers are populated with factory-calibrated coefficients, refer to TABLE_FAC_COEF if applicable. <b>Note:</b> Whenever the chip is in RESET, the factory-calibrated coefficient is reloaded into the registers from OTP. These same registers are used for displaying the factory-calibrated coefficient upon RESET in certain order. However, the user has full read/write access and may reshuffle the order and values, then update CH_CAL_GAIN_OFFSET accordingly.
OPT_COEF0..15 0xA0h-0xADh	23:0	OPT[23:0]	RW	0x00_0000	Extra register for temporary storing coefficients, eg it can be used as Self-calibrated ADC values with internal VREF and REFH, REFL at CH_GAIN or Calibrated values with Excitation sources. See <a href="#">Table 13</a> .

### 7.9.3 System-level configurations and status registers

Table 31. System-level configurations and status registers

Register (16-bit)	Bit order	Bit name	RW	Reset	Short description
CRC_CONF_REGS 0x25h	15:0	CRC_CONF_REGS[15:0]	R	0x0000	Integrated CRC result of all Configuration registers.
CRC_COEF_REGS 0x26h	15:0	CRC_COEF_REGS[15:0]	R	0x0000	Integrated CRC result of all user's coefficient registers.
CRC_TRIM_REGS 0x27h	15:0	CRC_TRIM_REGS[15:0]	R	0x0000	Integrated CRC result of all factory trim OTP registers.
Register (16-bit)	Bit order	Bit name	RW	Reset	Short description
CH_STATUS0 0x35h	15:0	CH_OVR[15:0]	R	0x0000	Channel over-range, logical CH15 is bit 15, CH0 is bit 0.
CH_STATUS1 0x36h	15:0	CH_UDR[15:0]	R	0x0000	Channel under-range, logical CH15 is bit 15, CH0 is bit 0.
Register (16-bit)	Bit order	Bit name	RW	Reset	Short description
GPI_DATA 0x29h	15:6	GPI_DATA[9:0]	R	0x0000	GPI data detected: 0 = Logic 0(DGND), 1 = Logic 1(DVDD). GPIO9 is bit15, GPIO0 is bit6.
	5:0	reserved			
GPIO_CONFIG0 0x2Ah	15:6	GPO_ENABLE[9:0]	RW	0x0000	GPO driving enable: 0 = disabled driving, 1 = enabled driving. GPIO9 is bit15, GPIO0 is bit6.
	5:0	reserved			
GPIO_CONFIG1 0x2Bh	15:6	GPIO_CON[9:0]	RW	0x0000	GPIO connect to pin: 0 = disconnect from pin, 1 = connect to pin. GPIO9 is bit15, GPIO0 is bit6.
	5:0	reserved			
GPIO_CONFIG2 0x2Ch	15:6	GPI_ENABLE[9:0]	RW	0x0000	GPI read enable: 0 = disabled read, 1 = enabled read. GPIO9 is bit15, GPIO0 is bit6.
	5:0	reserved			
GPI_EDGE_POS 0x2Dh	15:6	GPI_EDGE_POS[9:0]	R	0x0000	GPI positive edge(s) data: 0h = none, 1h = positive edge detected. Cleared after readback or CMD_CLEAR_ALARM.
	5:0	reserved			
GPI_EDGE_NEG 0x2Eh	15:6	GPI_EDGE_NEG[9:0]	R	0x0000	GPI negative edge(s) data: 0h = none, 1h = negative edge detected. Cleared after readback or CMD_CLEAR_ALARM.
	5:0	reserved			

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Table 31. System-level configurations and status registers...continued

GPO_DATA 0x2Fh	15:6	GPO_DATA[9:0]	RW	0x0000	Set GPO output data: 0h = output logic 0, 1h = output logic 1. GPIO9 is bit15, GPIO0 is bit6.
	5:0	reserved			
Register (16-bit)	Bit order	Bit name	RW	Reset	Short description
SYS_CONFIG0 0x30h	15	DRDY_PWDT	RW	0x0	DRDY pulse width duration (# of SYSCLK cycle): 0h = 2, 1h = 8
	14	ADC_DATA_OUT_16BIT	RW	0x0	ADC data register readout: 0h = 24 bit, 1h = 16 bit
	13	STATUS_STICKY			Prepended status bits behavior when bursting output data with STATUS_EN = 1. 0h = Sticky, 1h = Live (sampling at rising edge of DRDY).
	12	MCLK_OUT_ENABLE	RW	0x0	Enable the master clock(2*SYSCLK) output to GPIO9 pin. This bit supersedes and ignores the other GPIO9 setting.
	11:10	REF_SEL[1:0]	RW	0x0	<b>Select</b> to use Internal(REF_INT) or External(REF_EXT) 2.5 V voltage references for REF_BYP(of PGA) and REF_ADC(of ADC): <b>0h</b> = Both REF_BYP and REF_ADC use REF_INT. <b>1h</b> = REF_BYP uses REF_INT and REF_ADC uses REF_EXT. <b>2h</b> = REF_BYP uses REF_EXT and REF_ADC uses REF_INT. <b>3h</b> = REF_BYP uses REF_EXT and REF_ADC uses REF_EXT. <b>Note:</b> Internal reference is always powered on.
	9:8	CK_SRC_SEL[1:0]	RW	0x0	Select clock sources: 0h = internal clock, 1h = internal clock, and disable crystal oscillator circuit. 2h = applied external 18.432 MHz clock at XI pin, and disable crystal oscillator circuit. 3h = 18.432MHz Crystal is installed at XI, XO pins.
	7	CRC_EN	RW	0x0	Enable CRC: 0h = disable, 1h = enable.
	6	STATUS_EN	RW	0x0	To prepend 8-bit Live status bits to ADC data of enabled channels, MCH_EN[i] = 1. In Multichannel Read mode, the first 8 bits status bits is OR'd of the channels when in data output burst. SPI data: <status_8b><CH_DATAi>,<status_8b><CH_DATAj>... <b>Note:</b> Live status bits(MSB to LSB): overload, underload, over-range, under-range, overtemperature, global_alarm, overvoltage, CRC error.
	5	ADC_SYNC	RW	0x0	ADC Synchronization mode enabled for host-driven with SYNC pulse at pin. This works with all conversion modes. 0h = disabled SYNC pin, 1h = ADC is synchronized to SYNC pulse at rising edge and used as conversion start trigger
	4	DRDY_PIN_EDGE			To set the behavior of DRDY pin; especially in Multichannel modes. 0h = produce rising edge on every channel conversion done, 1h = produce rising edge only when the sequencer is done with the last enabled channel conversion.
3	GLOBAL_ALARM_STICKY	RW	0x0	Global alarm interrupt default behavior is: 0h = cleared when global alarm register is read, 1h = Write 0 to clear a specific bit.	
2	SPI_DOUT_DRIVE	RW	0x0	Increase DOUT output drive if high capacitance loading.	
1	INTB_DRIVER_TYPE	RW	0x0	INTB pin driver type: 0 = 100 Kohm pullup with open drain, 1 = CMOS push-pull.	
0	CRC_ERROR_ON_GPIO2	RW	0x0	To enable routing of CRC_ERROR interrupt to GPIO2 pin. 0h = normal GPIO function 1h = Output CRC_ERROR to GPIO2 pin, active high.	
SYS_STATUS0 0x31h	15	SINGLE_CH_ACTIVE	R	0x0	Single-channel conversion mode indicator, which includes CH_DELAY. 0h = idle, 1h = active.
	14	MULTI_CH_ACTIVE	R	0x0	Multichannel Conversion mode indicator, which includes CH_DELAY. 0h = idle, 1h = active.
	13	CHIP_READY	R	0x0	Chip status indicator. Upon power up, INTB pin will go LO (active low) to indicate the chip is ready. User is to read this register to clear INTB pin. This bit will stay HI when the chip is operational. 0h = Chip is not yet ready, 1h = Chip is ready.
	12	CRC_ERROR	R	0x0	CRC error encountered
	11:8	CONFIG_CH_PTR[3:0]	R	0x0	The selected logical channel for R/W access to CH_CONFIG0,1,2,3 registers. (Pointer is controlled by SPI CMD_CHx)
	7:4	ADC_CONV_CH[3:0]	R	0x0	The current active logical channel.
	3:0	reserved			
Register (16-bit)	Bit order	Bit name	RW	Reset	Short description
GLOBAL_ALARM_ENABLE 0x32h	15	OVER_TEMP_ALARM	RW	0x0	Overtemperature warning at 145 °C.
	14	HVDD_ALARM	RW	0x0	Enable alarm for HVDD supply detect below preset threshold.
	13	HVSS_ALARM	RW	0x0	Enable alarm for HVSS supply detect below preset threshold.
	12	ADVDD_ALARM	RW	0x0	Enable alarm for DVDD supply detect below preset threshold.
	11	reserved	RW	0x0	
	10	GPI_POS_ALARM	RW	0x0	Enable alarm for rising edge detected at any of GPI pins.
	9	GPI_NEG_ALARM	RW	0x0	Enable alarm for falling edge detected at any of GPI pins.
	8	CONFIG_ERROR_ALARM	RW	0x0	Enable alarm for register configuration error.
7	OVRRNG_ALARM	RW	0x0	Enable alarm for one or more data channel is over-range.	

Table 31. System-level configurations and status registers...continued

	6	UNDRNG_ALARM	RW	0x0	Enable alarm for one or more data channel is under-range.
	5	OVRLD_ALARM	RW	0x0	Enable alarm for one or more data channels is over-loaded or under-loaded.
	4	EXTCLK_FREQ_ALARM	RW	0x0	Enable alarm when XTAL or EXTCLK frequency varies with internal CLK by XX.
	3	reserved	RW	0x0	reserved
	2	ALRM	RW	0x0	Enable alarm for excitation voltage source is overloaded.
	1	ALRM	RW	0x0	Enable alarm for excitation current source is overloaded.
	0	TEMP_ALARM	RW	0x0	Enable programmable temperature alarm; the triggering threshold is set in THRS_TEMP register bits.
GLOBAL ALARM INT ERRUPT 0x33h	15	OVER_TEMP_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALARM_STICKY
	14	HVDD_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALARM_STICKY
	13	HVSS_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALARM_STICKY
	12	ADVDD_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALARM_STICKY
	11	reserved			
	10	GPI_POS_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALARM_STICKY
	9	GPI_NEG_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALARM_STICKY
	8	CONFIG_ERROR_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALARM_STICKY
	7	OVRRNG_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALARM_STICKY
	6	UNDRNG_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALARM_STICKY
	5	OVRLD_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALARM_STICKY
	4	EXTCLK_FREQ_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALARM_STICKY
	3	reserved			reserved
	2	VIEX_OV_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALARM_STICKY.
	1	VIEX_OI_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALARM_STICKY.
0	TEMP_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALARM_STICKY	
<b>Register (16-bit)</b>	<b>Bit order</b>	<b>Bit name</b>	<b>RW</b>	<b>Reset</b>	<b>Short description</b>
DIE_TEMP 0x34h	15:0	DIE_TEMP[15:0]	R	0x	16-bit die temperature readout in 2's complement. The temperature could be calculated with the following formula: Die_temp(°C) = code_decimal/64
THRS_TEMP 0x37h	15:0	THRS_TEMP[15:0]	RW	0x0000	Temperature threshold in 2's complement for setting custom temperature alarm.
<b>Register (16-bit)</b>	<b>Bit order</b>	<b>Bit name</b>	<b>RW</b>	<b>Reset</b>	<b>Short description</b>
PN2 0x7Ch	15:0	PN2[15:0]	R	0x	Part Number (MSB). Example, 1338 for NAFE13388B40BS part number
PN1 0x7Dh	15:0	PN1[15:0]	R	0x	Part Number (MidLSB). Example, 8B40 for NAFE13388B40BS
PN0 0x7Eh	15:8	PN0[15:8]	R	0x	reserved
	7:0	REVISION_ID[7:0]	R	0x	Revision
<b>Register (24-bit)</b>	<b>Bit order</b>	<b>Bit name</b>	<b>RW</b>	<b>Reset</b>	<b>Short description</b>
SERIAL1 0xAEh	23:0	SN1[23:0]	R	0x	Unique Serial Number (MSB)
SERIAL0 0xAFh	23:0	SN0[23:0]	R	0x	Unique Serial Number (LSB)
<b>Register (16-bit)</b>	<b>Bit order</b>	<b>Bit name</b>	<b>RW</b>	<b>Reset</b>	<b>Short description</b>
CRC_TRIM_INT 0x7Fh	15:0	CRC_TRIM_INT[15:0]	R	0x	CRC sum of internal trims, to be used for comparison against CRC_TRIM_REGS[15:0].

## 8 Limiting values

### 8.1 Maximum rating

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may lead to malfunction or permanent damage to the device.

Table 32. Absolute maximum rating <sup>[1]</sup>

Description	Min	Max	Units
HVDD to AGND <sup>[2]</sup>	-0.3	29	V
AGND to HVSS <sup>[2]</sup>	-0.3	29	V
HVDD to HVSS	-0.3	55	V
AVDD to AGND	-0.3	5.5	V
DVDD to DGND	-0.3	5.5	V
AGND to DGND	-0.3	0.3	V
AI1P, AI2P, AI3P, AI4P, AI1N, AI2N, AI3N, AI4N, AICOM to HVSS <sup>[3]</sup>	-0.3	46	V
HVSS to AI1P, AI2P, AI3P, AI4P, AI1N, AI2N, AI3N, AI4N or AICOM, with external 2.5 k $\Omega$ resistor in series for current limit with a duration of less than one hour. <sup>[3]</sup>	-60	36	V
HVDD to AI1P, AI2P, AI3P, AI4P, AI1N, AI2N, AI3N, AI4N, AICOM <sup>[3]</sup>	-0.3	46	V
HVDD to AI1P, AI2P, AI3P, AI4P, AI1N, AI2N, AI3N, AI4N or AICOM, with external 2.5 k $\Omega$ resistor in series for current limit with a duration of less than one hour. <sup>[3]</sup>	-36	60	V
REFH, REFL to AGND <sup>[4]</sup>	-0.3	VREF_BYP $\pm$ 0.1	V
REF_BYP, REFP_ADC, REFN_ADC to AGND <sup>[5]</sup>	-0.3	VAVDD	V
GPIO0.. GPIO9 to DGND <sup>[5][6]</sup>	-0.3	VDVDD + 0.3	V
CAPP, CAPN to AGND <sup>[7]</sup>	-	-	V
EXTCLK/XI, XO to DGND	-0.3	VDVDD + 0.3	V
SPI_ADDR, SCLK, MOSI, MISO, CSB, SYNC, RSTB to DGND <sup>[5]</sup>	-0.3	VDVDD + 0.3	V
LDO_DIG to DGND <sup>[3]</sup>	-0.3	2.1	V
REF_EXT, REF_NR, REF_INT to AGND <sup>[5]</sup>	-0.3	VAVDD + 0.3	V

[1] These are stress ratings at room temperature only. Functional operation of the product with conditions at or above its maximum ratings is not implied. Device reliability may be affected if stressed at or beyond limits for extended periods.

[2] Supply pins HVDD-AGND and AGND-HVSS are dc-clamped to 29 V.

[3] Pins AIxP, AIxN, AICOM are not to exceed HVDD or HVSS by 46 V. In limited testing at room temperature, these pins could sustain up to 60 V at  $\pm 24$  mA with 2.5 k $\Omega$  external series resistor for duration of up to one hour.

[4] Output pins REFH, REFL are diode-clamped to REF\_BYP and AGND internally.

[5] Low voltage input and output pins are diode-clamped to their respective power supplies and/or ground: The current is limited to  $\pm 10$  mA whenever the voltage at pin is 0.3 V (a) above AVDD/DVDD or (b) below AGND/DGND.

[6] Digital output pins, current limit is  $\pm 10$  mA.

[7] Analog buffered signal output pins CAPP, CAPN are with common-mode voltage of 1.4 V-1.6 V typical. Only a differential capacitor connection is recommended. Any other loading will affect the device functionality adversely.

### 8.2 ESD stress rating and latch-up

Table 33. ESD stress rating and latch-up

Description	Max	Units
Human body model (HBM) on all pins	$\pm 7500$	V
Charged device model (CDM) on all pins	$\pm 750$	V
Latch-up at 150 °C	$\pm 200$	mA

**Note:** These are stress ratings only. Functional operation of the product at conditions at or above its ratings is not implied.

## 9 Thermal characteristics

Table 34. Thermal characteristics

Description	Symbol	Min	Typ	Max	Units
Operating temperature					
Ambient	TA	-40		+125	°C
Junction	TJ	-40		+150	
Storage temperature	TSTO	-55		+150	°C
Peak package reflow temperature <sup>[1] [2]</sup>	TPPRT			+260	°C
Junction to case (bottom exposed pad soldered to board) <sup>[3]</sup>	R <sub>θJC</sub>		+2		°C/W
Junction to ambient <sup>[4]</sup>	R <sub>θJA</sub>		+24		°C/W
Junction to top of package	Ψ <sub>JT</sub>		+1		°C/W

[1] Pin soldering temperature limit is 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.

[2] NXP's package reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For peak package reflow temperature and moisture sensitivity levels (MSL), go to <https://www.nxp.com/>, search by part number (remove prefixes/suffixes) and enter the core ID to view all orderable parts and parametric.

[3] Junction-to-case thermal resistance was determined using an isothermal cold plate. Case temperature refers to the exposed pad surface temperature at the package bottom side dead center.

[4] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.

## 10 Electrical characteristics

All specifications are at VHVDD = -VHVSS = 15 V; VAVDD = VDVDD = 3.3 V; internal reference. Typical values are at TA = 40 °C, ADC at 3 kSPS in Normal Settling mode with 500 samples averaging; each HV analog input (AlxP, AlxN, AICOM) is connected to an external 2.5 kΩ resistor in series with 1 nF capacitor connected to GND. See [Figure 44](#). Offset, gain error, and INL parametric are input-referred to AlxP, AlxN pins w.r.t. AICOM pin, and characterized to the input full-scale (FS) in single-ended configuration at specified gain, unless otherwise stated. The minimum and maximum specifications cover TA = -40 °C to +125 °C.

$TUE [V/V] = (GE_v + OE + INL) / VFS$ , where VFS is 10 V, 5 V, 2.5 V, 2 V, 1 V, 0.5 V, 0.25 V, 0.125 V for channel gain of 0.2 V/V, 0.4 V/V, 0.8 V/V, 1 V/V, 2 V/V, 4 V/V, 8 V/V and 16 V/V, respectively. GE<sub>v</sub> is gain error expressed in [V] as GE\*VFS.

Table 35. HV input ranges

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>HV INPUT RANGES</b>						
VIN(SE)	Input voltage nominal range (single-ended)	PGA7: Channel gain = 16 V/V (±0.15625 V single-ended full-range setting)	-0.125		0.125	V
		PGA6: Channel gain = 8 V/V (±0.3125 V single-ended full-range setting)	-0.25		0.25	
		PGA5: Channel gain = 4 V/V (±0.625 single-ended full-range setting)	-0.5		0.5	
		PGA4: Channel gain = 2 V/V (±1.25 V single-ended full-range setting)	-1		1	
		PGA3: Channel gain = 1 V/V (±2.5 V single-ended full-range setting)	-2		2	
		PGA2: Channel gain = 0.8 V/V (±3.125V single-ended full-range setting)	-2.5		2.5	
		PGA1: Channel gain = 0.4 V/V (±6.25V single-ended full-range setting)	-5.0		5.0	
		PGA0: Channel gain = 0.2 V/V (±12.5V single-ended full-range setting)	-10.0		10.0	
VIN(DF)	Input voltage nominal range (differential)	PGA7: Channel gain = 16 V/V (±0.3125 V differential full-range setting)	-0.25		0.25	V
		PGA6: Channel gain = 8 V/V (±0.625 V differential full-range setting)	-0.5		0.5	
		PGA5: Channel gain = 4 V/V (±1.25 V differential full-range setting)	-1		1	
		PGA4: Channel gain = 2 V/V (±2.5 V differential full-range setting)	-2		2	
		PGA3: Channel gain = 1 V/V (±5 V differential full-range setting)	-4		4	
		PGA2: Channel gain = 0.8 V/V (±6.25 V differential full-range setting)	-5.0		5.0	
		PGA1: Channel gain = 0.4 V/V (±12.5 V differential full-range setting)	-10.0		10.0	
		PGA0: Channel gain = 0.2 V/V (±25 V differential full-range setting)	-20.0		20.0	



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Table 36. HV input accuracy before calibration

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TUE_Ai	Total unadjusted error at room	Initial accuracy without factory CAL coefficients. Single-ended inputs. Internal reference, TA = +40 °C		±0.5	±1.3	% FS
TUE_OTi	Total unadjusted error overtemperature	Initial accuracy without factory CAL coefficients. Single-ended inputs. Internal reference, TA = -25 °C to +105 °C		±0.6	±1.3	% FS
OEi	Offset error	Calibrated offset error without factory CAL coefficients. Single-ended inputs. Internal reference, TA = +40 °C				mV
		G = 16 V/V		±0.3	±0.6	
		G = 1 V/V		±5	±10	
		G = 0.8 V/V		±5	±10	
GEi	Gain error	Calibrated gain error without factory CAL coefficients. Single-ended inputs. Internal reference, TA = +40 °C				% FS
		G = 16 V/V		±0.2	±1.2	
		G = 1 V/V		±0.2	±1	
		G = 0.8 V/V		±0.2	±1	
INL	INL error	TA = +40 °C				µV
		G = 16 V/V		±1		
		G = 1 V/V		±10	±50	
		G = 0.8 V/V		±10	±50	
E_VHi	REFH error	Initial accuracy without factory CAL coefficients, REFH to AGND. Measured with internal ADC, internal reference, G = 0.8 V/V, single-ended mode. TA = +40 °C. CH_CHOP = 1, TCC_OFF = 1.		±1		%
		E_VLi	REFL error	Initial accuracy without factory CAL coefficients, REFL to AGND. Measured with internal ADC, internal reference, G = 16 V/V, single-ended mode. TA = +40 °C. CH_CHOP = 1, TCC_OFF = 1.		±1

Table 37. HV input initial accuracy after calibration

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TUE_AT	Total unadjusted error at room <sup>[1]</sup>	Initial accuracy after user calibration, TA = +40 °C TUE[V/V]=(OE+GEv+INL)/FS		±0.002	±0.005	% FS
		Initial accuracy with Factory calibration, TA = +40 °C TUE[V/V]=(OE+GEv+INL)/FS		±0.06	±0.15	
TUE_OT	Total unadjusted error over temperature <sup>[1]</sup>	Initial accuracy after user calibration at 40°C Internal voltage reference, TCC_OFF = 0, TA = -25°C to +105°C		±0.05	±0.1	% FS
		Initial accuracy with Factory calibration		±0.11	±0.22	% FS

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Table 37. HV input initial accuracy after calibration...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		Internal voltage reference, TCC_OFF = 0, TA = -25 °C to +105 °C				
OE	Calibrated offset error	Initial offset error with Factory calibration, single-ended inputs, Internal voltage reference, TA = +40 °C				µV
		G = 16 V/V		±5	±30	
		G = 1 V/V		±25	±75	
		G = 0.8 V/V		±25	±75	
		G = 0.2 V/V		±50	±300	
GE	Calibrated gain error <sup>[1]</sup>	Initial Gain Error after user calibration, TA = +40 °C		±0.0		% FS
		Initial Gain Error with Factory calibration, G = 16 V/V, TA = +40 °C		±0.05	±0.14	
		Initial Gain Error with Factory calibration, G = 1 V/V, TA = +40 °C		±0.05	±0.14	
		Initial Gain Error with Factory calibration, G = 0.8 V/V, TA = +40 °C		±0.05	±0.14	
		Initial Gain Error with Factory calibration, G = 0.2 V/V, TA = +40 °C		±0.05	±0.14	
INL	INL error	Internal voltage reference, TA = +40 °C				µV
		G = 16 V/V		±1		
		G = 1 V/V		±10	±50	
		G = 0.8 V/V		±10	±50	
		G = 0.2 V/V		±50	±200	
E_VH	Calibrated REFH (w.r.t. stored NVM value)	REFH to AGND, measured with Internal voltage reference and ADC with factory CAL coefficients, G = 0.8 V/V, single-ended mode, CH_CHOP = 1, TCC_OFF = 1, TA = +40 °C.		±0.01	±0.05	%
E_VL	Calibrated REFL (w.r.t. stored NVM value)	REFL to AGND, measured with Internal voltage reference and ADC with factory CAL coefficients, G = 16 V/V, single-ended mode, CH_CHOP = 1, TCC_OFF = 1, TA = +40 °C.		±0.01	±0.05	%

[1] An initial accuracy error could be affected by mechanical stress post assembly. To meet certain accuracy specifications, a 1-point gain or 2-point full calibration could be required. The user-calibrated accuracy is typically limited by NAFE integral non-linearity (INL) of the device at chosen ADC data rate, and additional errors could arise from other test setup and conditions.

Table 38. HV input temperature and aging drift characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TDE	TUE drift	Single-ended inputs. Internal reference, TA = -25 °C to +105°C. TCC_OFF = 0		±3	±10	ppm/°C
		Single-ended inputs. Internal reference, TA = -40 °C to +125°C. TCC_OFF = 0		±3	±10	ppm/°C
OD	Offset drift	All single-ended inputs and ranges. TA = -40 °C to 125°C				µV/°C
		G = 16 V/V		±0.02	±0.075	
		G = 1 V/V		±0.32	±1.25	
		G = 0.8 V/V		±0.4	±1.5	
		G = 0.2 V/V		±1.6	±6	
		G = 0.2 V/V, CH_CHOP=1, TCC_OFF=0		±0.02		
GD	Gain drift	External VREF and TCC_OFF = 1		±1	±2	ppm/°C
		Internal VREF and TCC_OFF = 0		±3	±8	ppm/°C
GD <sub>750hr</sub>	Gain drift over time <sup>[1]</sup>	External VREF and TCC_OFF = 1		±25		ppm over 750 h

Table 38. HV input temperature and aging drift characteristics...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		Internal VREF and TCC_OFF = 0		±490		ppm over 750 h
INLD	INL drift	Internal VREF -25 °C to +105 °C				µV/°C
		G = 16 V/V		±0.02	±0.05	
		G = 1 V/V		±0.1	±0.3	
		G = 0.8 V/V		±0.1	±0.3	
		G = 0.2 V/V		±0.3	±1.0	
VHD	Calibrated REFH drift	REFH to AGND, measured with ADC with factory CAL coefficients, internal reference and G = 0.8 V/V, CH_CHOP = 1, TCC_OFF = 1. TA = -25 °C to +105 °C.		±1		ppm/°C
VLD	Calibrated REFL drift	REFL to AGND, measured with ADC with factory CAL coefficients, internal reference and G = 16 V/V, CH_CHOP = 1, TCC_OFF = 1. TA = -25 °C to +105 °C.		±1		ppm/°C

[1] Data is based on standard high-temperature operating life (HTOL) method.

Table 39. HV input channel characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Input crosstalk DC	Tested input at 0 V with one aggressor channel at ± 10V, TA = +40 °C		±1		µV/V
	Input crosstalk dynamic	VAIxP = +10 V switch between VAlyN = -10 V, SCS, DRO = 12 ksps, CH_DELAY = 16.4µs. TA = +40 °C.		±1		µV/V
T <sub>switch</sub>	Channel switch time	V <sub>IN</sub> changes from one input to another input, G = 0.2 V/V ADC output code settles within 0.01 % of final value. ADC_NORMAL_SETTLING = 0, 24 ksps, SINC4 filter, single-ended input -10 V to +10 V and +10 V to -10 V.		16.4		µs
V <sub>noise</sub>	Input voltage noise	Inputs shorted to GND				µVrms
		ADC in Normal Settling mode versus data rate and channel gain		<a href="#">Table 8</a>		
		ADC in Normal Settling mode, 1.125KSPS, G = 16 V/V		0.61		
		ADC in Normal Settling mode, 1.125KSPS, G = 1 V/V		3.5		
		ADC in Normal Settling mode, 1.125 ksps, G = 0.8 V/V		4.1		
		ADC in Normal Settling mode, 1.125 ksps, G = 0.2 V/V		16.4		
Vhr	High-voltage headroom	VHVDD above positive input linear range of +10 V, G = 0.2 V/V	3.8			V

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Table 39. HV input channel characteristics...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		VHVSS below negative input linear range of -10 V, G = 0.2 V/V	3.8			
CMR <sub>DC</sub>	Common-mode rejection	Shorted differential inputs pair. VCM = AGND to REFH. ADC_DATA_RATE = 1.125 ksp/s, TA = +40 °C				dB
		G = 16 V/V		104		
		G = 1 V/V		86		
		G = 0.8 V/V		92		
		G = 0.2 V/V		80		
CMR <sub>50/60</sub>	Common-mode rejection	Shorted differential inputs pair. VCM = ±VFS, 50 Hz or 60 Hz., ADC_DATA_RATE = 10 sp/s, SINC4 filter, TA = +40 °C				dB
		G = 16 V/V		184		
		G = 1 V/V		160		
		G = 0.8 V/V		172		
		G = 0.2 V/V		160		
PSRR <sub>HV</sub>	HV Power-supply rejection ratio (RTI)	Shorted differential DC Inputs at 0V, V <sub>HVDD</sub> = +15 V to +24 V, VHVSS = -24 V to -15 V, TA = +40 °C				dB
		G = 16 V/V		145		
		G = 1 V/V		124		
		G = 0.8 V/V		124		
		G = 0.2 V/V		112		
		G = 0.2 V/V, CH_CHOP = 1		140		
PSRR <sub>LV</sub>	LV Power-supply rejection ratio (RTI)	Shorted differential DC Inputs at 0 V, VAVDD = VD VDD = 3 V to 3.6 V				dB
		G = 16 V/V		102		
		G = 1 V/V		80		
		G = 0.8 V/V		78		
		G = 0.2 V/V		66		
		G = 0.2 V/V, CH_CHOP = 1		110		
RIN	Input impedance	VAlxP, VAlxN pins, TA = +40 °C		1000		MΩ
IL	Input leakage current	Any single input switch in on-state, TA = -40 °C to +105 °C		1	5	nA
		Any single input switch in on-state, TA = -40 °C to +125 °C		5	15	

Table 40. HV output excitation voltage and current

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Maximum-compliance voltage headroom	Excitation voltage or current output at HV AI pins with ±2 mA max current, Max(HVDD- Vout , -HVSS- Vout ), TA = +40 °C.		3		V
	Maximum-output current	VIEX_VI = 1, VIEX_MAG[3:0] = 15\ld		±2		mA
	Maximum-output voltage	VIEX_VI = 0, VIEX_MAG[3:0] = 15\ld		±12		V
	Output-current drift	G = 8 V/V, TCC_OFF = 1, VIEX_CHOP = 0, VIEX_MAG[3:0] = 11\ld, 0.5 mA current into external 100Ω, TA = -40 °C to +125 °C			15	ppm/°C
	Output-voltage drift	G = 0.2 V/V, TCC_OFF = 1, VIEX_CHOP = 1, VIEX_MAG[3:0] = 11\ld, 3 V voltage output, TA = -40 °C to +125 °C			10	ppm/°C
ODC	Open-detection current source	OPEN_DET_CURRENT = 1		65		nA

Table 41. LV MUX inputs/GPIO0-GPIO1 as analog input

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>LV MUX INPUTS</b>						
	Power supplies accuracy	HVDD, HVSS and DVDD through ADC readback. HV_SEL = 0		±2		%
	REF_COARSE accuracy	REF2 through ADC readback. HV_SEL = 0		±2		%
	GND_LV	0 V through ADC readback. HV_SEL = 0		±100		µV
<b>GPIO0-GPIO1 as analog input</b>						
	Analog input signal range	Full Range 1.5V ± 1V	0.5		2.5	V
	Offset error	HV_SEL = 0. Linear range 1.5 V ± 0.8 V		±100		µV
	Gain error	HV_SEL = 0. Linear range 1.5 V ± 0.8 V		±0.7		%

Table 42. Temperature sensor

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Temperature sensor resolution	Die temperature		1/64		°C
	Temperature sensor accuracy	Die temperature		±3		°C

Table 43. Internal voltage reference (VREF)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VREF	Output voltage <sup>[1]</sup>	Internal reference, REFP_ADC pin.		2.496		V
	Initial accuracy	Internal reference voltage, TA = +40 °C	-0.5		0.5	%
TC <sub>VREF</sub>	Temperature coefficient	TA = -25 °C to +105 °C		±8		ppm/°C
		TA = -40 °C to +125 °C		±12		
LTS	Long-term stability <sup>[2]</sup>	Internal voltage reference, measured at REFP_ADC pin		±490		ppm over 750 h
	Load regulation	0.1 mA sourcing current load at REF_BYN pin.		±0.5		mV/mA
S <sub>VREF</sub>	Supply regulation	3V ≤ V <sub>AVDD</sub> ≤ 3.6 V. REFP_ADC pin.		±10		µV/V

[1] An initial accuracy error could be affected by mechanical stress post assembly.

[2] Data is based on standard high-temperature operating life (HTOL) method.

Table 44. Clock oscillators

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Clock frequency accuracy	Internal oscillator		±0.2	±1.1	%
	Input clock duty cycle	External clock applied to XIN pin. Frequency = 18.432 MHz	45	50	55	%
	Crystal oscillator startup time	18.432MHz crystal. capacitive load = 12 pF.		5		ms

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Table 45. Power supplies

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>HV</sub>	High-voltage supply	V <sub>HVDD</sub> - V <sub>HVSS</sub>	14		48	V
V <sub>HVDD</sub>	Positive high-voltage supply <sup>[1]</sup>	Referenced to AGND	7.0		28	V
V <sub>HVSS</sub>	Negative high-voltage supply <sup>[1]</sup>	Referenced to AGND	-28		-7.0	V
V <sub>VDD</sub>	Low-voltage supply	VDD = VAVDD = VDVDD, HVDD = -HVSS = 15 V, referenced to AGND	3.0	3.3	3.6	V
I <sub>VDD</sub>	Low-voltage supply quiescent current	I(AVDD)+I(DVDD), VDD=AVDD=DVDD = 3.3 V		12	17	mA
I <sub>HVDD</sub>	Positive high-voltage supply quiescent current	Default setting, All AIXP, AIXN inputs are at 0 V, HVDD = -HVSS = 15 V		4	4.9	mA
I <sub>HVSS</sub>	Negative high-voltage supply quiescent current	Default setting, All AIXP, AIXN inputs are at 0 V, HVDD = -HVSS = 15 V		3.9	4.8	mA
	Total quiescent power	Default setting, All AIXP, AIXN inputs are at 0 V, HVDD = -HVSS = 15 V		150	185	mW

[1] Not production tested and only limited samples were verified at ± 28 V supplies.

Table 46. GPIO and digital I/O pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>IH</sub>	Logic high-input voltage		0.7*VDVDD			V
V <sub>IL</sub>	Logic low-input voltage				0.3*VDVDD	V
	Input-voltage hysteresis			0.3		V
V <sub>OH</sub>	Logic high-output voltage	I <sub>OH</sub> = 1 mA	0.8*VDVDD			V
V <sub>OL</sub>	Logic low-output voltage	I <sub>OL</sub> = -1 mA			0.2*VDVDD	V

Table 47. SPI timing and characteristics

V<sub>HVDD</sub> = -V<sub>HVSS</sub> = 15 V, V<sub>AVDD</sub> = V<sub>DVDD</sub> = 3.3 V, typical values are at TA = 40 °C, unless otherwise specified. Capacitive loading should be < 20 pF on the digital output pin.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f <sub>SCLK</sub>	SCLK frequency				32	MHz
t <sub>SCLK_H</sub>	SCLK high pulse width		15.5			ns
t <sub>SCLK_L</sub>	SCLK low pulse width		14.5			ns
t <sub>CWH</sub>	CSB high pulse width	CSB high pulse width	32			ns
t <sub>IS</sub>	MOSI setup time	Time to SCLK falling edge	5			ns
t <sub>IH</sub>	MOSI hold time	Time after SCLK falling edge	5			ns
t <sub>OT</sub>	MISO transition time	Time after SCLK rising edge		10.5	14	ns
t <sub>CFS</sub>	CSB falling setup time	Time before SCLK first rising edge	5		25	ns
t <sub>CRE</sub>	CSB rising edge time	Time after the last SCLK falling edge	5		25	ns

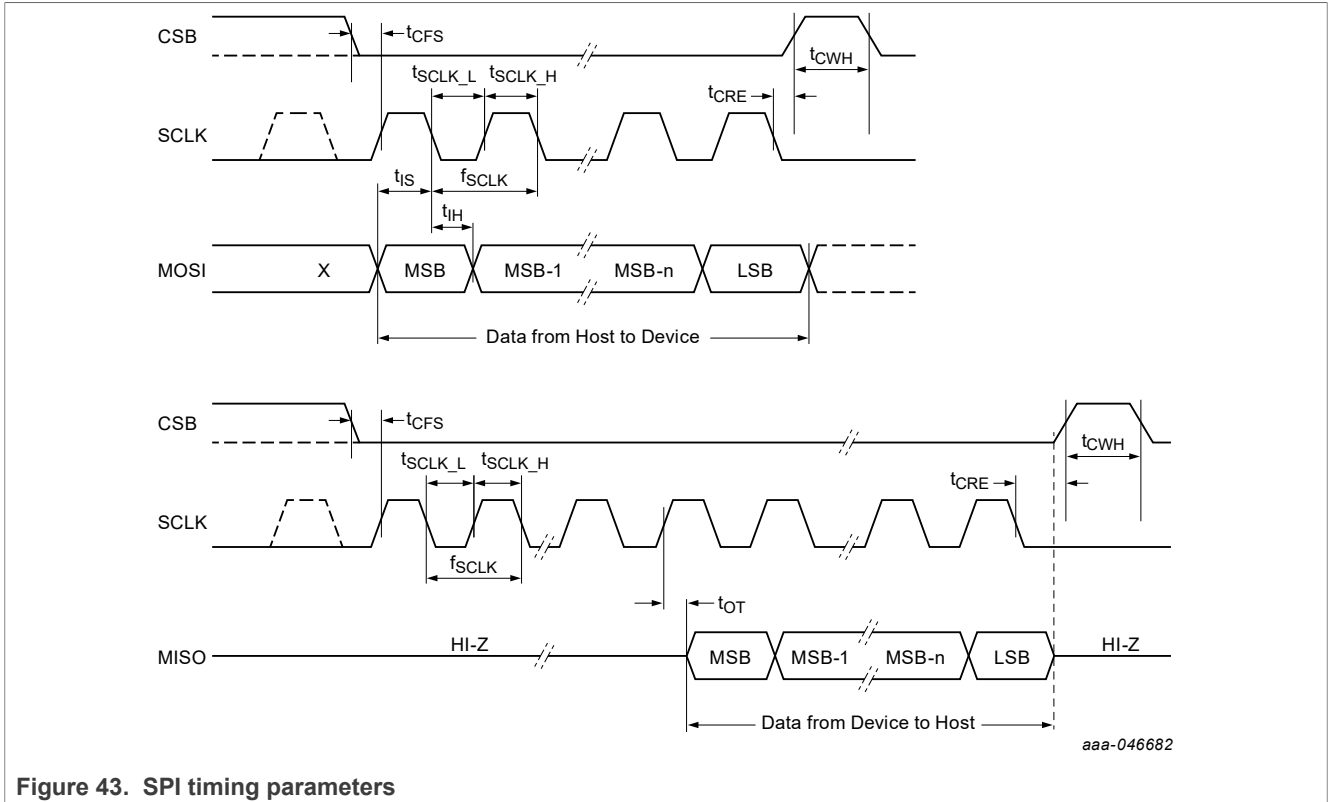


Figure 43. SPI timing parameters

# 11 Application information

## 11.1 Typical application block diagram

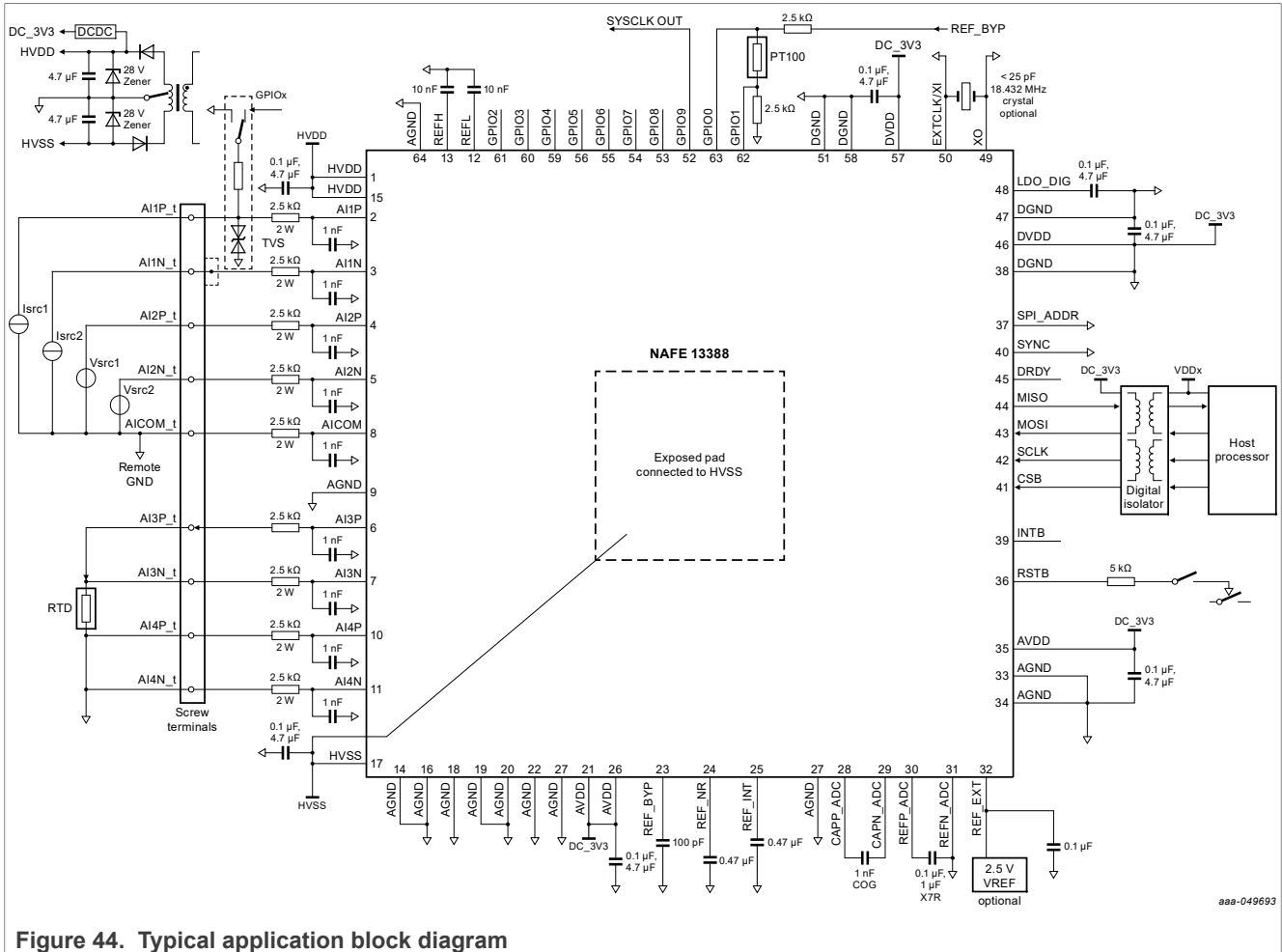


Figure 44. Typical application block diagram

**Note:** Dash box on AI1N input represents the dashed circuitry on AI1P.

Figure 44 depicts one of the typical use cases. Any of the eight HV inputs could be connected for measuring voltages and currents, either differentially or single-ended. For example, the AI2P and AI2N inputs are connected to measure voltages in the single-ended configuration. They may reference to AICOM or internal AGND, which is configured in channel CH\_CONFIG registers, or configured AI2P-AI2N differentially, as a different measurement channel. In Figure 44, the inputs AI1P and AI1N are connected to measure current with the shunt resistors controlled by GPO. The reference input could also be either AICOM, AGND, or any of the AI pins. For additional surge protection, TVS diodes could be added preceding the 2.5 kΩ series resistor.

The NAFE13388 is equipped with voltage and current excitation (VIE) sources, which could be routed out to any of the AI input pins through HVMUXOUTP,N for concurrent forcing and sensing when the channel enabled. Figure 44 shows four AFE channels, AI3P to AI4N, configured for force-and-sense ratio-metric RTD measurement. The internal VIE is used to source current to RTD from AI3P and the differential voltage across RTD is measured accurately by on-chip ADC by setting channel register bits HV\_AIP = 4 and HV\_AIN = 3.

The PT100 temperature sensor resistor network is biased with buffered REF\_BYP and connected to GPIO0-GPIO1 (pins 62 and 63) to monitor the local temperature. The differential voltage across PT100 is measured by configuring HV\_SEL = 0 and LVSIG\_IN = 1 for ADC conversion. An on-chip temperature readout is also



available at register DIE\_TEMP. Optional external VREF was connected to REF\_EXT pin and could be mixed and matched with internal VREF for various data acquisition and diagnostic applications. Note that calibration may be required as the factory coefficients are for use with internal VREF only.

In case of isolated applications, a transformer-based power supply design may be used and typically consists of a primary-side H-bridge driver, diodes, and passive filters (not shown) to generate HVDD/HVSS  $\pm 15$  V typical and DC-DC buck converter to provide a regulated 3.3 V supply. A digital isolator is used for SPI communication with the remote host to avoid the noise injection. For surge protection, 28 V Zener diodes should be installed on both HVDD and HVSS referenced to GND.

In this example, the NAFEx3388 is clocked at 18.432 MHz using a crystal with internal oscillator across XIN and XOUT pins. Alternatively, an 18.432 MHz on-chip oscillator or external clock could also be used for multi-device synchronization, where pin GPIO9 could be configured to output SYSCCLK.

## 11.2 Design for EMC

The NAFE13388 family of products is designed for industrial applications with enhanced electromagnetic compliance at device level. Although EMC is a system-level design consideration, use of robust device components may generally result in an overall lower-cost solution in a smaller board space. In limited laboratory testing scenarios, NAFE13388 parts were shown to be capable of sustaining IEC61000-4-5 surge up to  $\pm 2$  kV and IEC61000-4-4 electrical fast transient and burst immunity up to  $\pm 4$  kV on AI1P..AI4P, AI1N..AI4N, AICOM pins with 2.5 k $\Omega$  to 5.0 k $\Omega$  series MELF-type resistor without the need of external TVS on evaluation boards, while protection diodes are necessary at HVDD and HVSS pins.

Besides HV input and supply pins, the rest of the LV pins are also tested for ESD to the same maximum rating, as shown in [Table 32](#).

In applications where the surge protections are needed on LV pins, an external TVS suppressor will be needed.

## 11.3 Programmable logic controller I/O module

### 11.3.1 Design example: $\pm 10$ V input module

AI2P and AI2N in [Figure 44](#) illustrates an example of a  $\pm 10$  V analog input channels for programmable logic controller (PLC). These HV inputs can be protected by current limiting with the series resistor along with its internal clamping diodes to HVDD and HVSS supplies.

An internal current excitation source is used to pull the positive analog input to 15 V if the field-wiring connection is open or the transmitter has failed in Open-Circuit mode.

The signal from the transmitter is filtered by the external RC filter to remove EMI and RFI interference when operated in noisy environments. The negative input signal is connected to AICOM at 0 V. The ADC measures the differential voltage between inputs AI1P and AICOM. The input configuration is single-ended with the input voltage driven  $\pm 10$  V relative to AICOM at 0V.

The internal oscillator is selected and EXTCLK/XI pin is shorted to DGND. The serial interface and digital control lines of the ADC are connected to the host.

Two Zener diodes are installed to clamp the high-voltage supply (HVDD-AGND and AGND-HVSS) to provide overvoltage protection if an input signal is present with module power off.

### 11.3.2 Design requirements

The ADC programmability allows various tradeoffs of sample rate, conversion noise, and conversion latency.

11.3.2.1 Design goal values

- Accuracy:  $\pm 0.05$  %
- Temperature range (internal module):  $-25$  °C to  $+105$  °C
- Acquisition period:  $50$   $\mu$ s
- Effective resolution: 19 bits

11.3.2.2 Design parameter value

- Nominal signal range:  $\pm 10$  V
- Extended range:  $\pm 12$  V
- Input impedance:  $1000$  M $\Omega$
- Overvoltage rating:  $\pm 40$  V

11.3.2.3 Detailed design procedure

A key consideration in the design of an analog input module is the error over the ambient temperature range resulting from the drift of gain, offset, reference voltage, and linearity error. This includes the initial offset and gain (including reference voltage error) after factory calibration.

Figure 45 shows the maximum drift error of the NAFE over the  $-25$  °C to  $+105$  °C temperature range. The maximum error drift is  $< 0.02$  % in the temperature range of  $-10$  °C to  $90$  °C and  $0.04$  % in the temperature range  $-25$  °C to  $105$  °C.

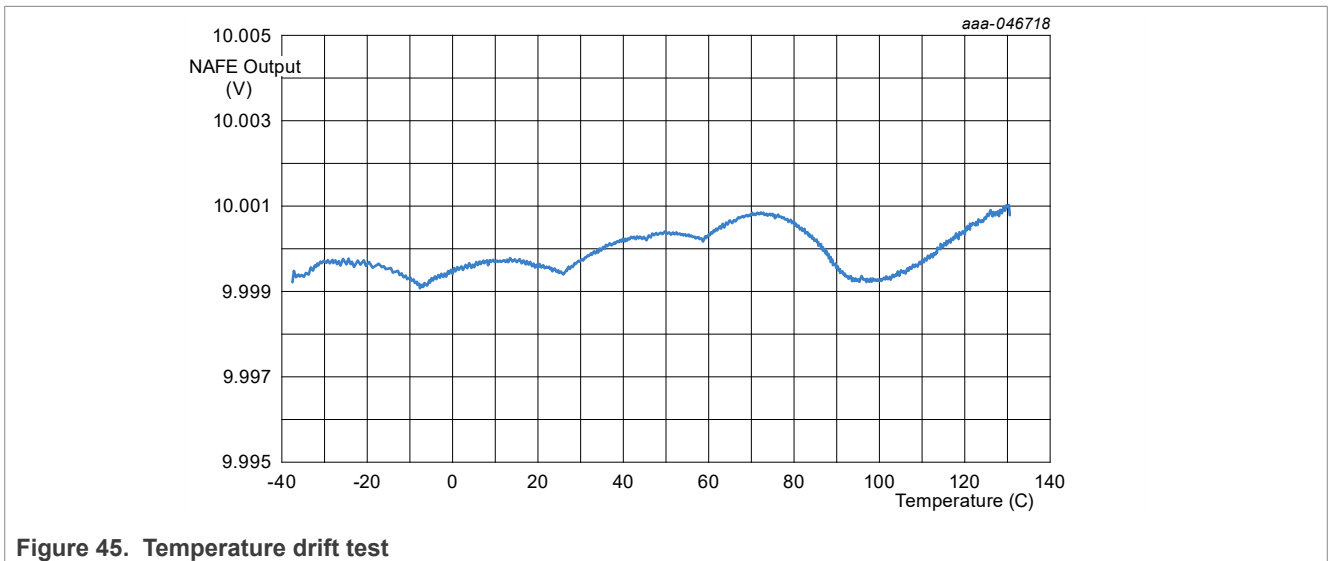


Figure 45. Temperature drift test

Figure 46 shows 100,000 consecutive conversions at 18000 sps. This example demonstrates the consistency of the ADC conversion results over time. The conversion noise in this example is  $6$   $\mu$ V<sub>RMS</sub>. The effective resolution calculates to 19.5 bits, which meets the design requirement.

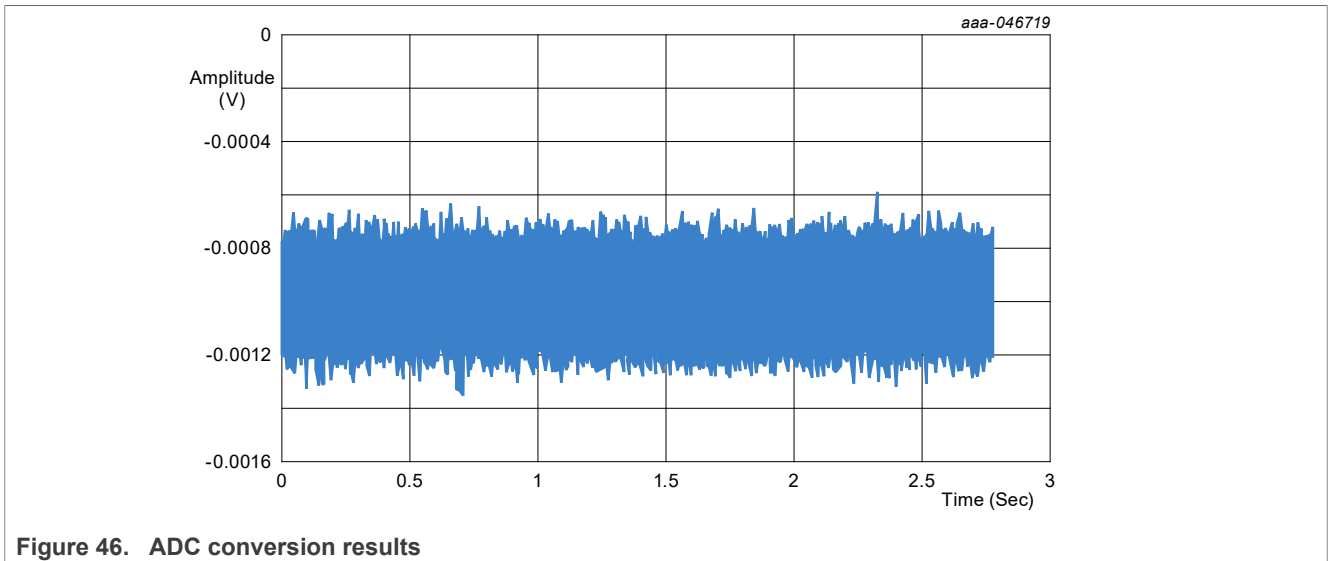


Figure 46. ADC conversion results

## 11.4 Power supplies and component selection

### 11.4.1 HV input pin protection and HV supply clamp

When any of the following pins HV AlxP, AlxN or AICOM is driven close to HVDD-0.5 V or HVSS+0.5 V, the internal protection diodes at the input pin may be forward-biased and start to conduct current flow from the input pin to the HVDD or HVSS pins. In general, the required external 2.5 kΩ series resistor is sufficient to limit the current. It is recommended to add supply clamping with Zener diodes at HVDD and HVSS to improve reliability. In case of surge events, TVS diodes could be added at the source side, before the resistor.

### 11.4.2 Power supply sequencing

As with many multiple-power supply systems, proper sequencing of the different supplies during power up and power down is a common practice to ensure robust device biasing without unnecessary electrical overstress. Though NAFE13388 devices were tested for robustness under various power supply ramping rates and order of sequences, testing is insufficient to cover all applications. Thus, for NAFE13388 devices, it is recommended to ramp up AVDD, DVDD before HVDD and/or HVSS. Ramping down HVDD and/or HVSS to ~3 V or less before starting to ramp down AVDD and DVDD, is also recommended. In most cases, any ramp rate slower than ±10 V/μs on HVDD, HVSS is acceptable.

### 11.4.3 HV input pin resistor

An external 2.5 kΩ series resistor is required at each of the AlxP, AlxN and AICOM pins. Higher resistance can lower the current limit in case of fault conditions with the expense of higher voltage error due to pin or board leakages and mismatches. Lower resistance is generally not advised in view of system reliability against surge and ESD events.

For precision HV applications, high-pulse load MELF resistors are typically used and often with TC > 100 ppm/°C. With low input leakage current and the differential input architecture in the NAFE13388, the requirement on the temperature coefficient of the resistor is largely relaxed. If 1 % resistance tolerance is used, it meets the accuracy requirement in most applications.

**Note:** For precise, high common-mode rejection single-ended measurement, AICOM pin in series with the same resistor type and value is to be used, instead of internal GND.

#### 11.4.4 Crystal

The NAFE13388 offers multiple 18.432 MHz clock-source options:

- Internal oscillator
- Crystal oscillator
- External clock source/module

For robustness, a crystal with higher drive level  $>100 \mu\text{W}$  is recommended.

#### 11.4.5 Capacitors

Use of high-grade capacitors is recommended for the following pins:

REFP\_ADC/REFN\_ADC (1  $\mu\text{F}$ , X7R) and CAPP/CAPN (1 nF, C0G).

#### 11.4.6 Grounds and plane

Good layout practices are crucial to realize the full performance of the ADC.

For best performance, dedicate an entire PCB layer to a ground plane. Do not route any other signal traces on this layer.

### 11.5 System-level calibration

#### 11.5.1 Procedures for gain and offset calibrations

This section describes the steps in performing digital calibration for offset and gain error correction.

##### 11.5.1.1 Transfer characteristics

The NAFE13388 integrates an offset and gain correction circuitry. The offset correction ( $O_c$ ) precedes the gain correction ( $G_c$ ) in digital domain.

The ideal transfer characteristic is

$$y = x$$

The actual transfer characteristic is

$$y = G_a \cdot x + O_a$$

Where  $G_a$  and  $O_a$  are the actual gain and actual offset respectively.

The calibrated transfer characteristic is

$$y = G_a \cdot G_c \cdot x + G_c \cdot (O_a - O_c)$$

Where  $G_c$  and  $O_c$  are the correction gain and offset coefficients, respectively.

$$\begin{cases} G_c = \frac{1}{G_a} \\ O_c = O_a \end{cases}$$

##### 11.5.1.2 Voltage and current input gain and offset calibration procedures

This section describes the steps for performing offset and gain digital calibration for voltage or current input.

**11.5.1.2.1 Steps for gain CAL**

1. Set  $O_c = 0$
2. Set  $G_c = 1$
3. Put a voltage source equals to  $x_1$ , about +100 % of full-scale.
4. Read  $y_1 = G_a \cdot 1 \cdot x_1 + 1 \cdot (O_a + 0)$
5. Put a voltage source equals to  $x_2$ , about -100 % of full-scale.
6. Read  $y_2 = G_a \cdot 1 \cdot x_2 + 1 \cdot (O_a + 0)$
7. Calculate  $G_a = \frac{y_2 - y_1}{(x_2 - x_1)}$
8. Set  $G_c = \frac{1}{G_a}$

**11.5.1.2.2 Steps for offset CAL**

1. Plug  $y_1 = G_a \cdot x_1 + O_a$
2. Calculate  $O_a = (y_1 - G_a \cdot x_1)$
3. Set  $O_c = O_a$

**11.5.1.3 Resistance and RTD input gain and offset calibration procedures**

This section describes the steps in performing offset and gain digital calibration for resistance and RTD input.

**11.5.1.3.1 Step for resistance gain CAL**

1. Set  $O_c = 0$
2. Set  $G_c = 1$
3. Put a resistance value equal to  $x_1$ , about +80 % of full-scale range.
4. Read  $y_1 = G_a \cdot 1 \cdot x_1 + 1 \cdot (O_a + 0)$
5. Put a resistance value equal to  $x_2$ , about 0 % of full-scale range (for example, short-circuit the input).
6. Read  $y_2 = G_a \cdot 1 \cdot x_2 + 1 \cdot (O_a + 0)$
7. Calculate  $G_a = \frac{y_2 - y_1}{(x_2 - x_1)}$
8. Set  $G_c = 1/G_a$

**11.5.1.3.2 Steps for resistance offset CAL**

1. Plug  $y_1 = G_a \cdot x_1 + O_a$
2. Calculate  $O_a = (y_1 - G_a \cdot x_1)$
3. Set  $O_c = O_a$

**11.5.2 Factory calibration and self-calibration**

The NAFE13388 offers different calibration features to improve system accuracy at lower cost.

The NXP factory-calibrated devices increase initial system accuracy while reducing the capital expenditure for expensive test instruments and reducing the production test time. The NAFE13388 stores factory-calibrated coefficients based on two points self-calibration to reduce the gain and offset error.

The NAFE13388 includes two voltage sources to perform built-in or dynamic end-to-end self-calibrations. The ratiometric REFH and REFL voltage sources derived from the REF\_BYN in combination with 0 V source (GND-GND) provide a precise and calibrated source for gain and offset calibration of all signal paths except reference voltage. The two points gain and offset calibration is performed measuring REFH-GND (or REFL-GND) and GND-GND and comparing against the internal stored value REFH-GND (or REFL-GND) and GND-GND = 0 V to calculate the gain and offset coefficients. Typically, REFH-GND with a typical value of 2.3 V, is suggested for low-channel gain, while REFL-GND, with a typical value of 0.2 V, is suggested for high-channel gain.

For systems that require low offset, an offset calibration could be performed measuring AICOM-AICOM to calculate and calibrate the offset error. Alternately, the NAFE13388 offers an automatic offset reduction circuit that is enabled by setting, CH\_CONFIG1.CH\_CHOP = 1, to activate the Precision mode. In this mode, the ADC runs two conversions and takes the average of the difference for offset removal.

**Note:** *The output data rate is halved.*

## 12 Typical operating characteristics

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, internal 2.5 V reference, TA = 40 °C, unless otherwise specified.

Table 48. Typical operating characteristics

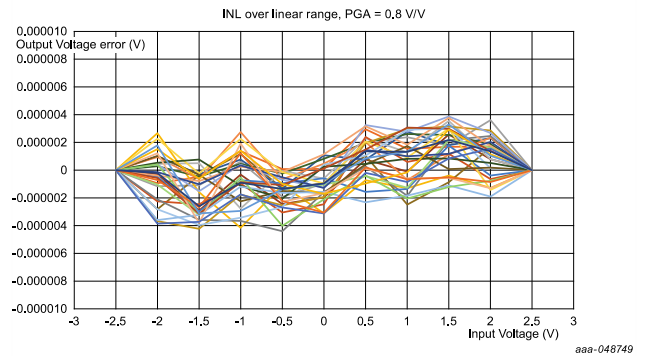
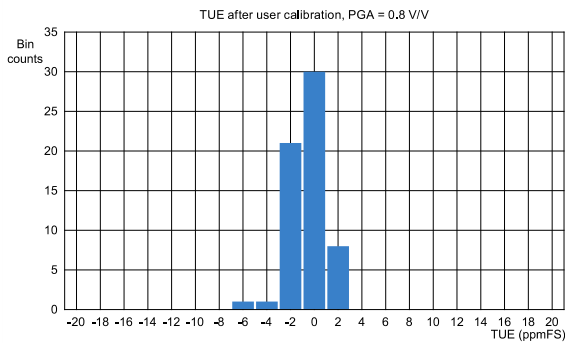
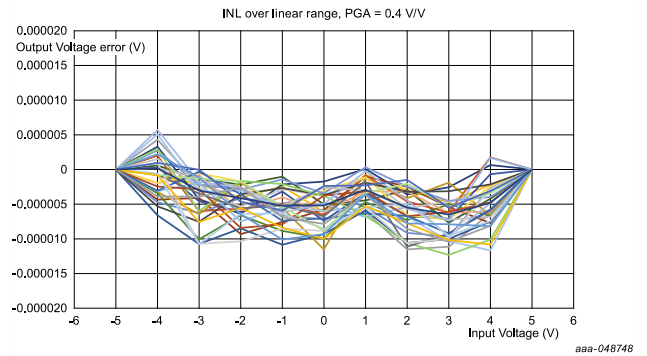
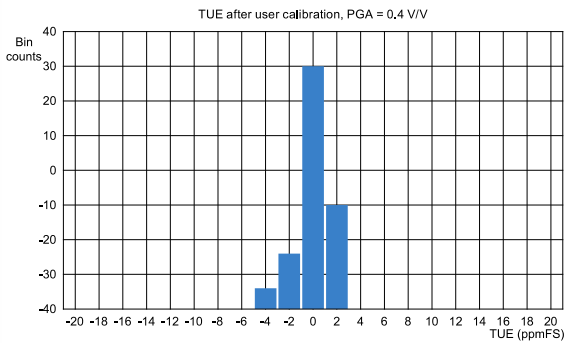
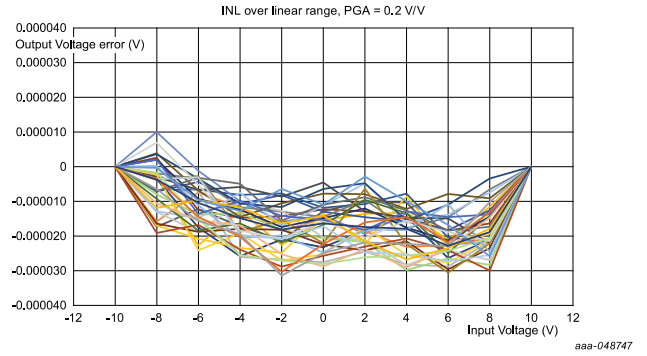
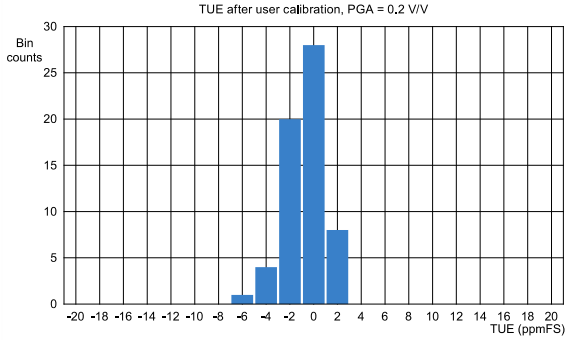


Table 48. Typical operating characteristics...continued

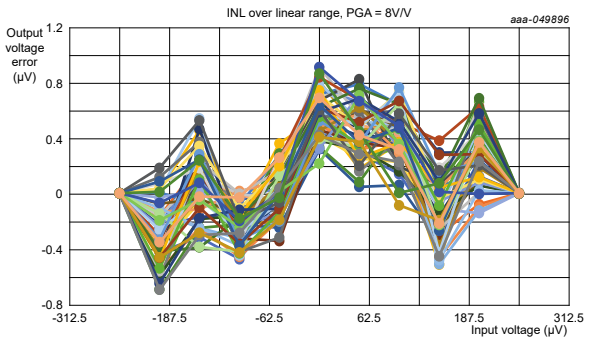
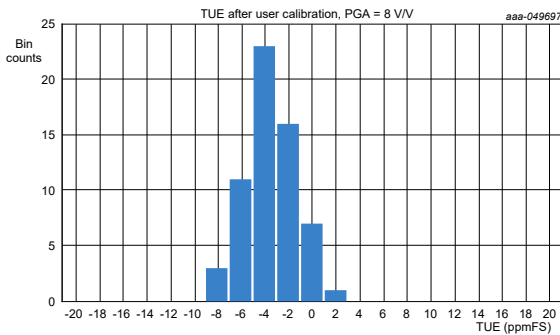
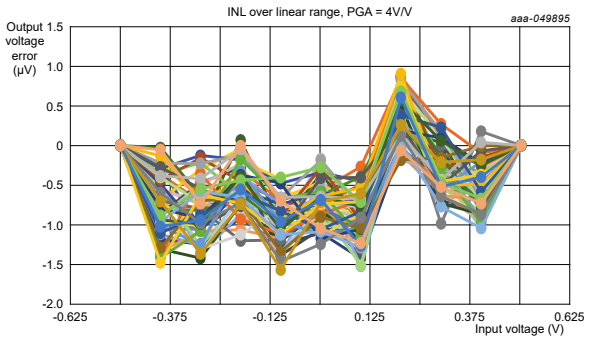
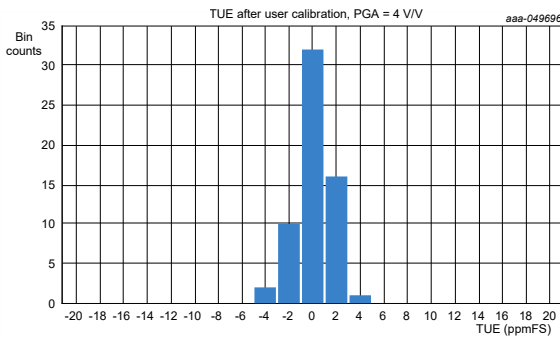
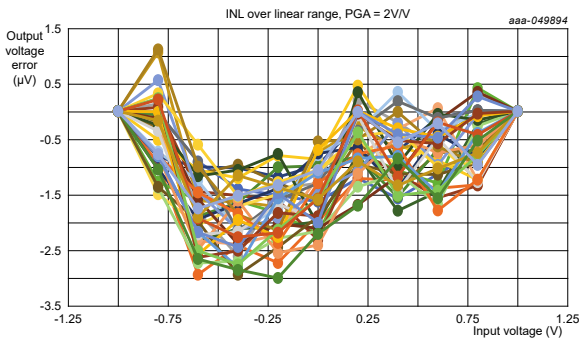
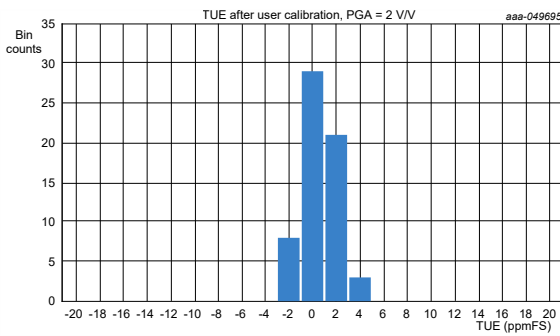
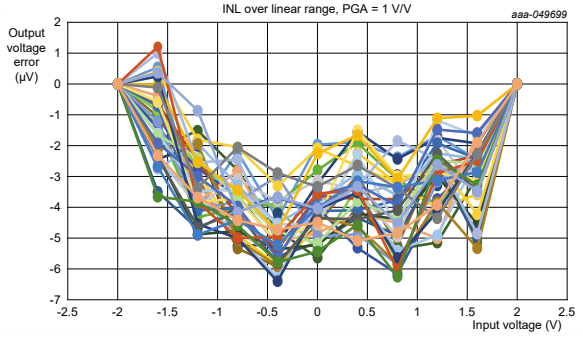
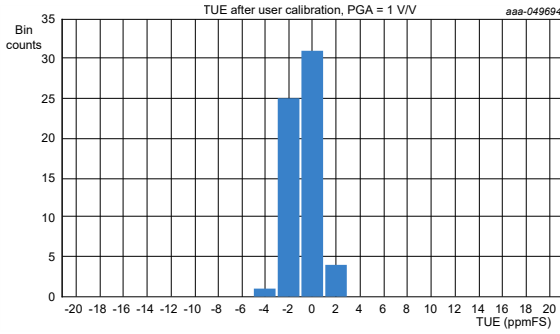




Table 48. Typical operating characteristics...continued

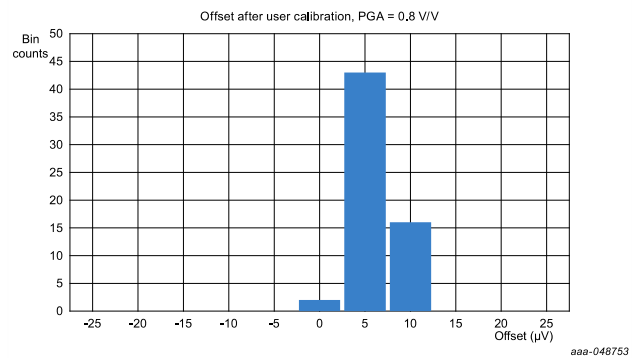
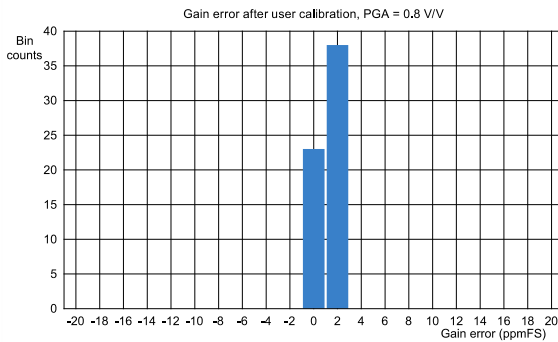
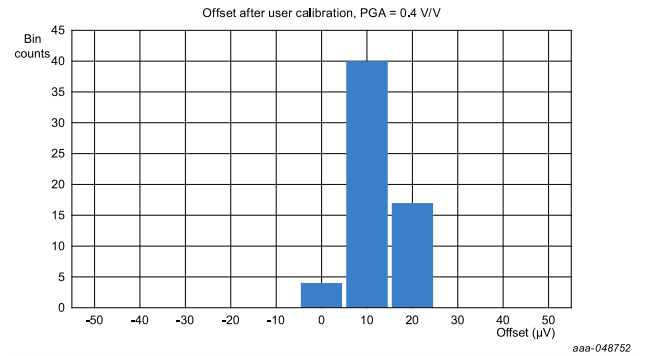
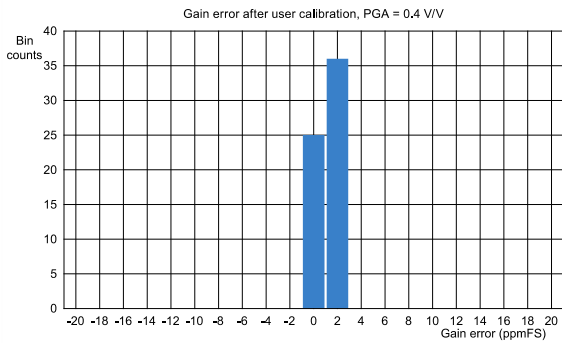
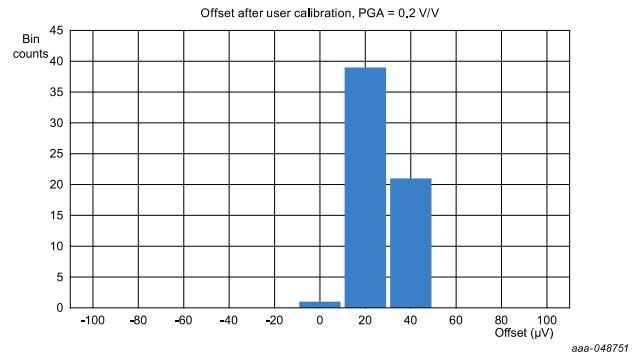
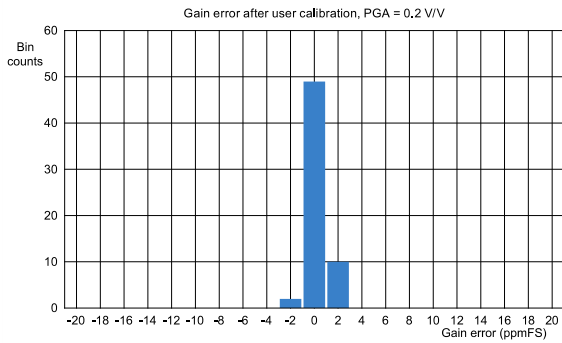
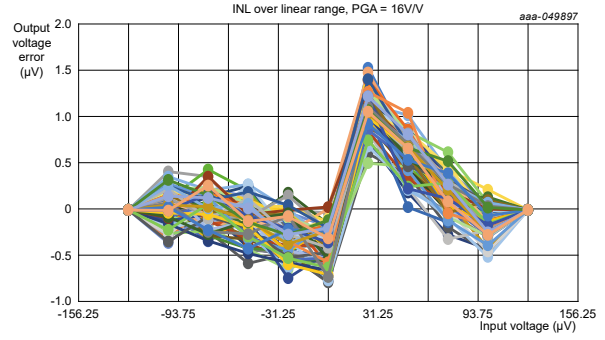
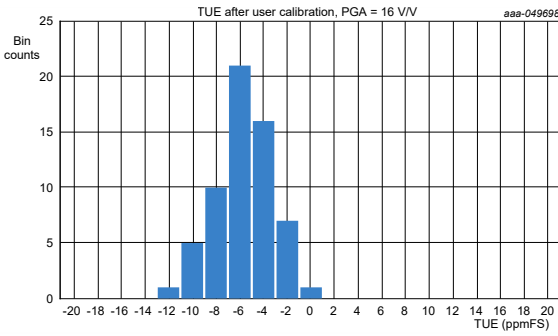


Table 48. Typical operating characteristics...continued

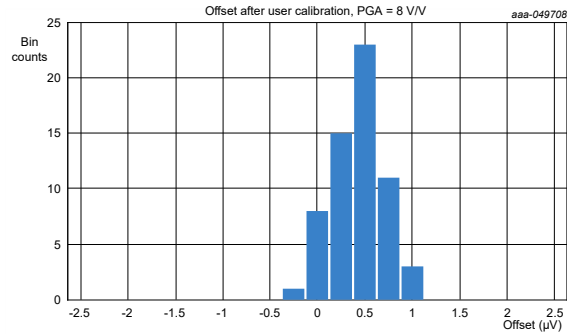
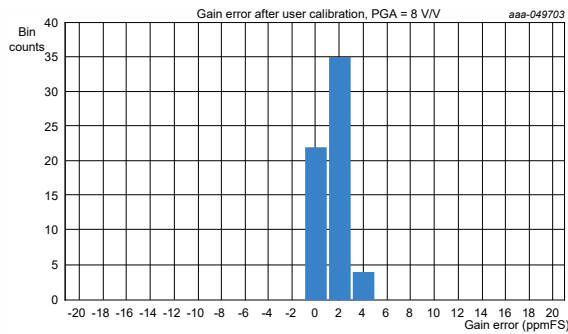
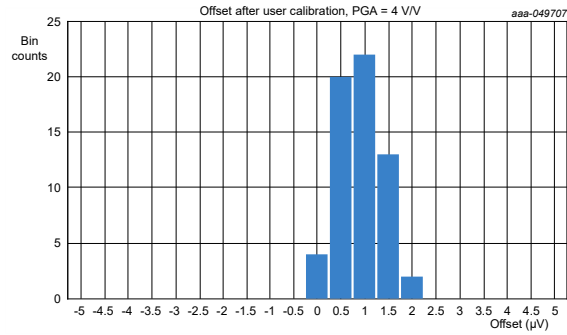
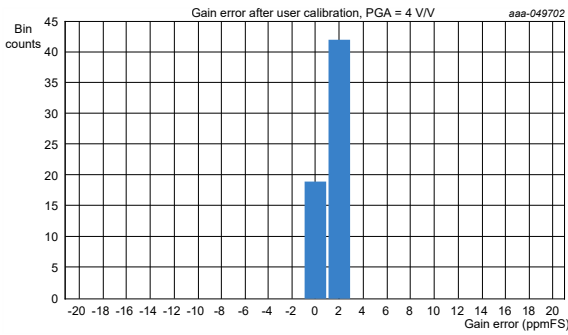
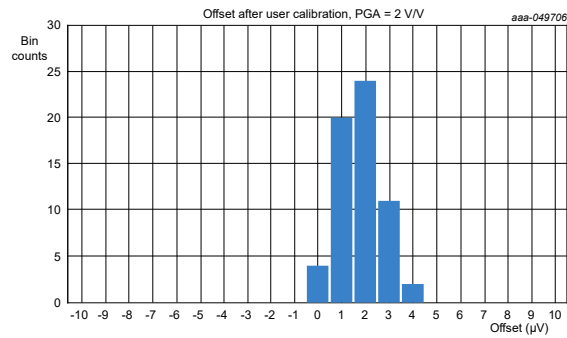
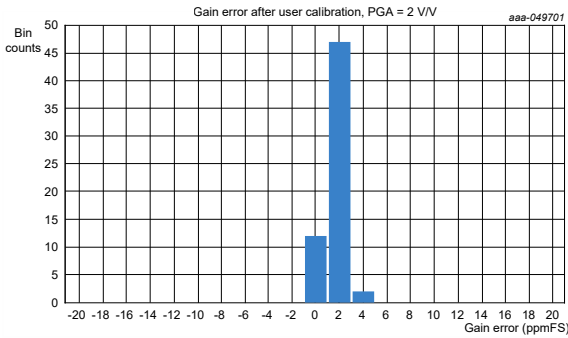
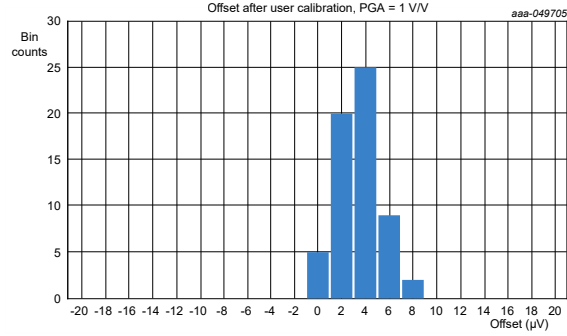
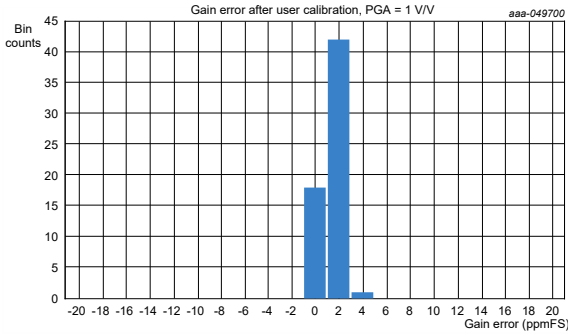


Table 48. Typical operating characteristics...continued

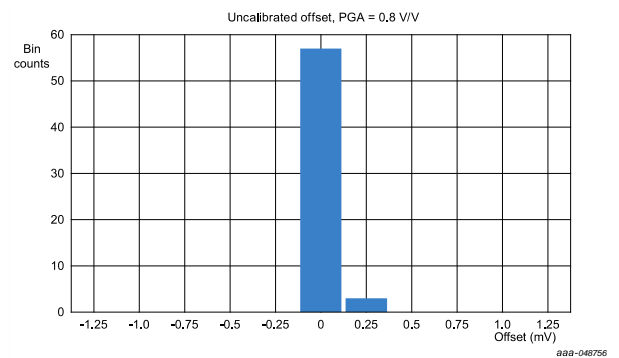
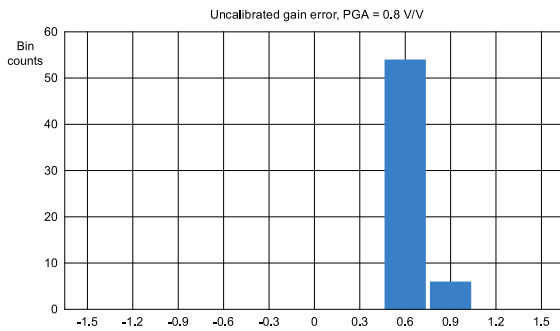
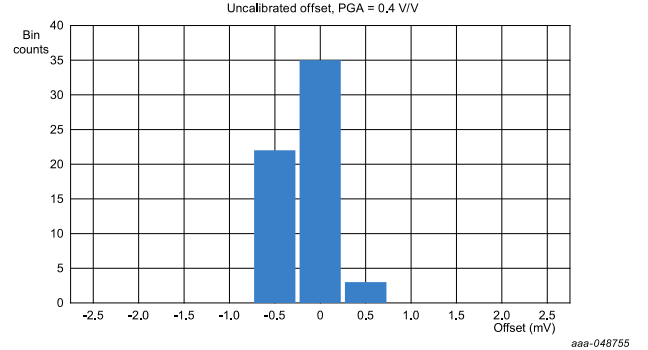
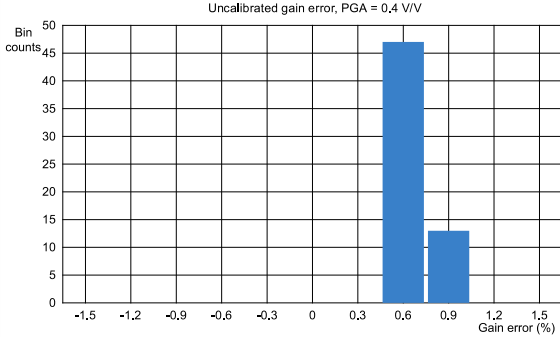
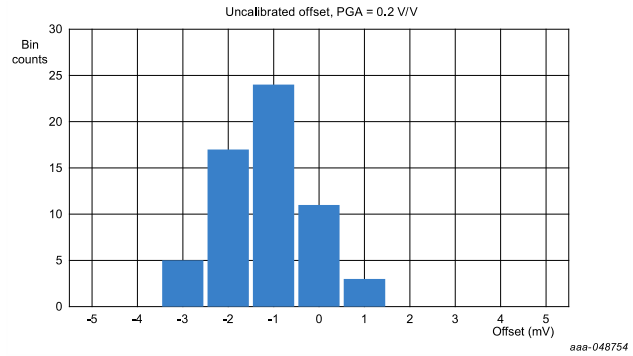
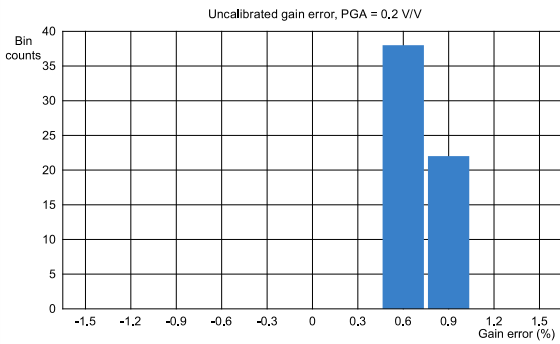
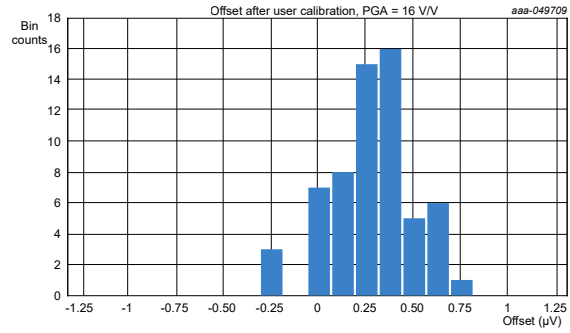
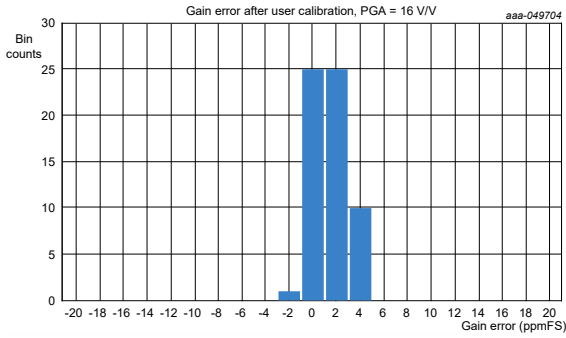


Table 48. Typical operating characteristics...continued

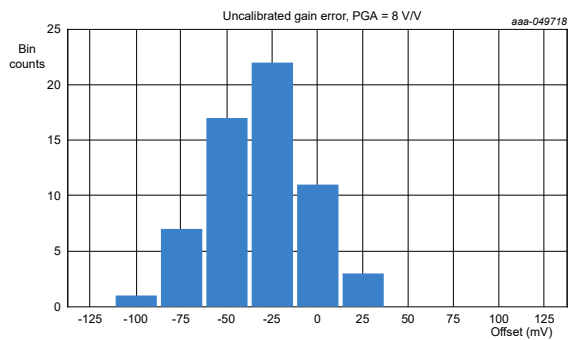
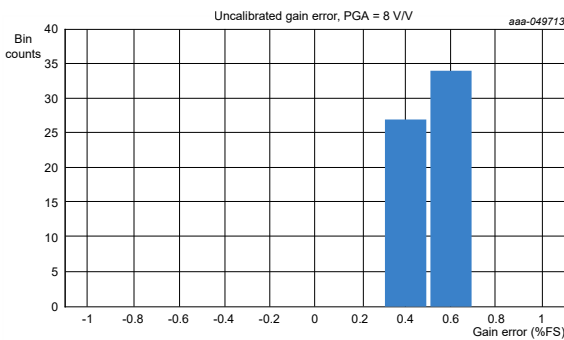
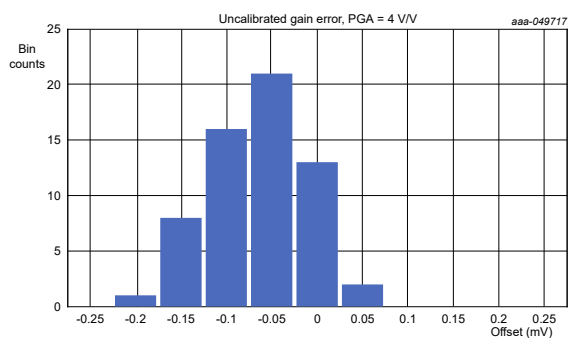
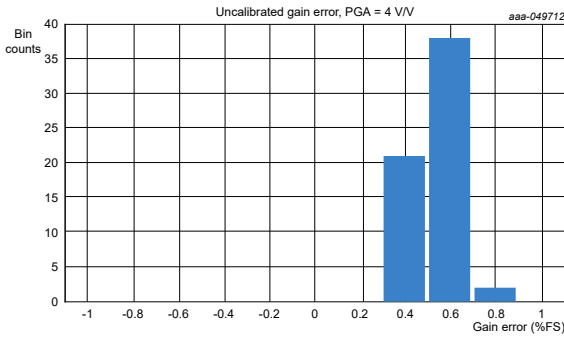
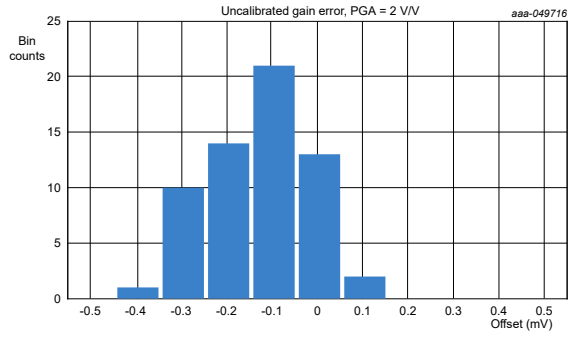
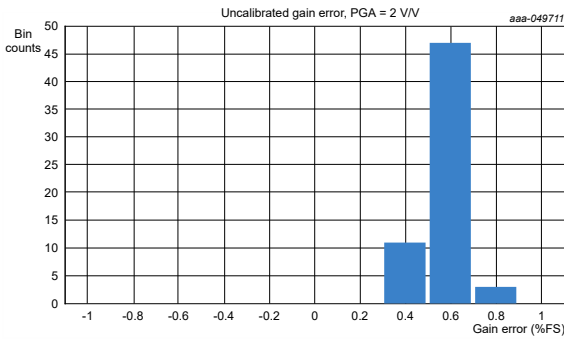
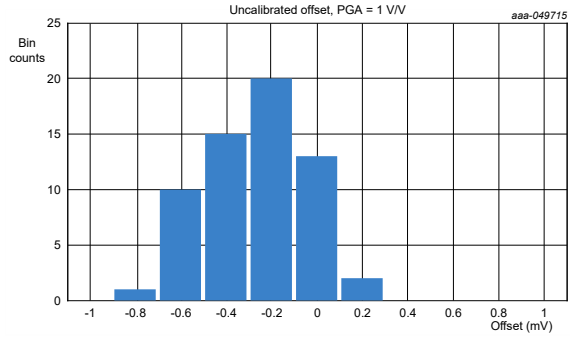
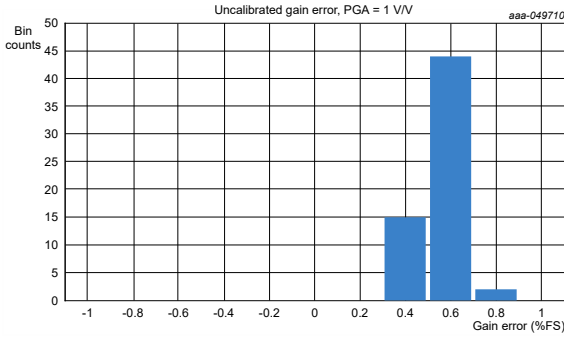


Table 48. Typical operating characteristics...continued

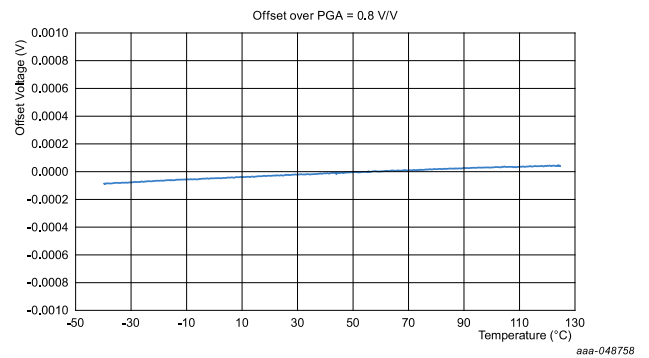
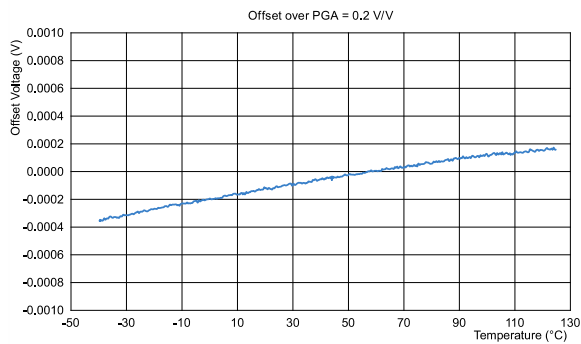
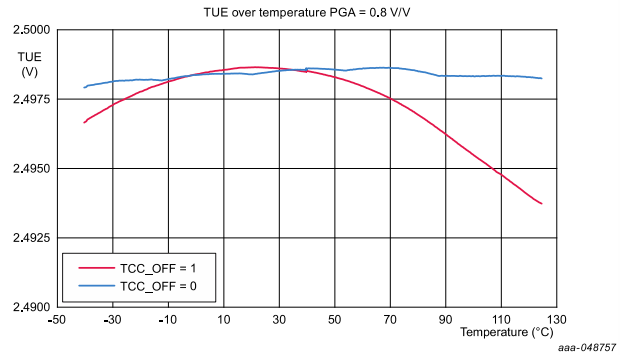
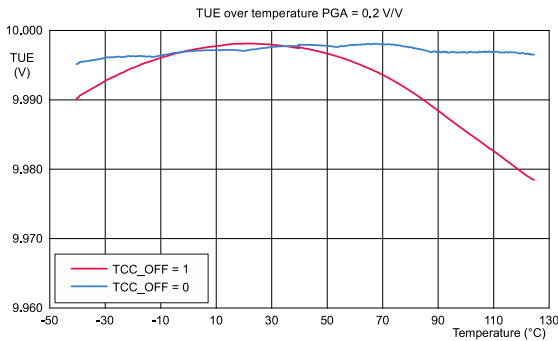
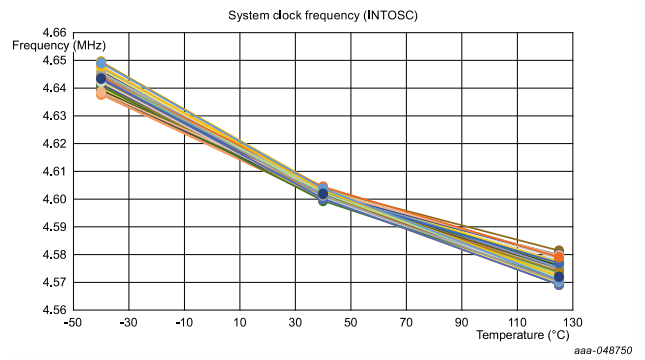
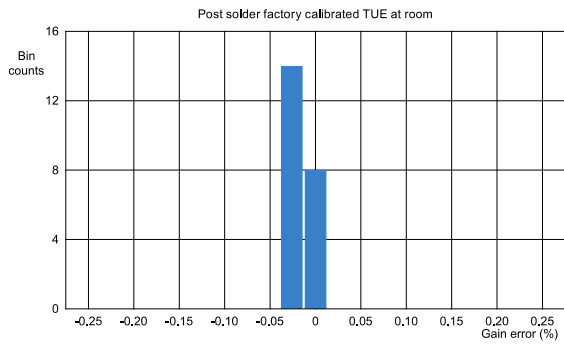
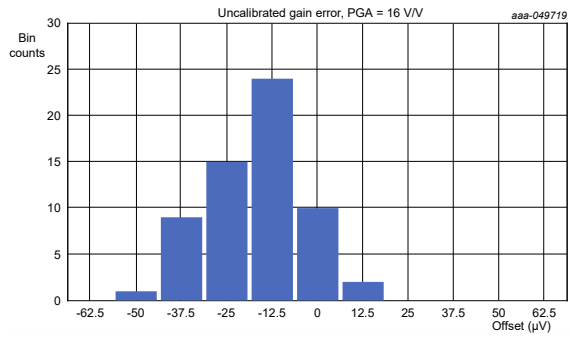
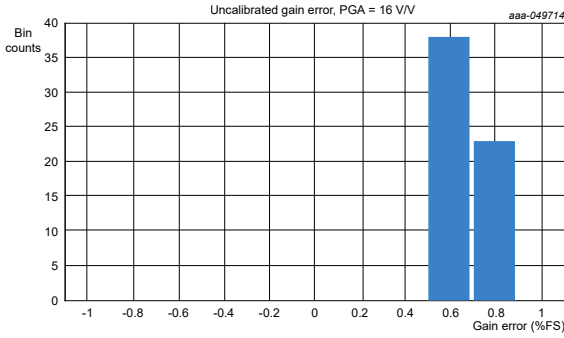


Table 48. Typical operating characteristics...continued

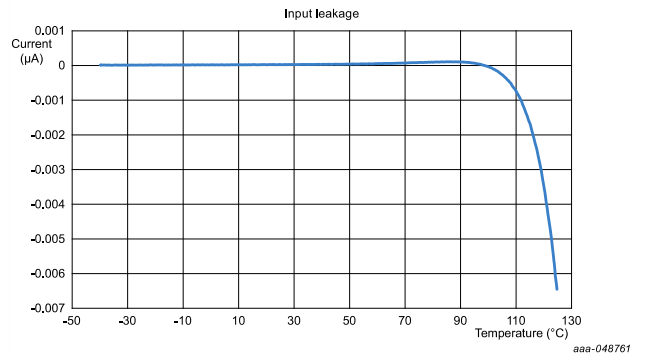
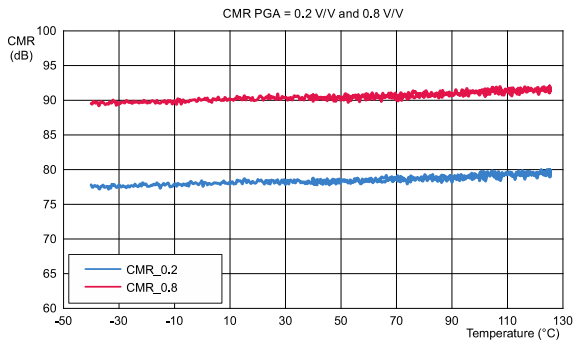
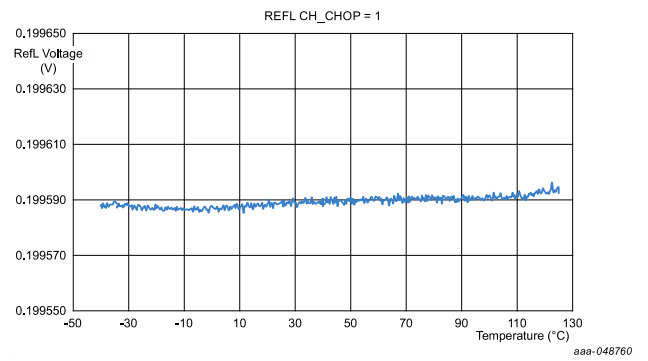
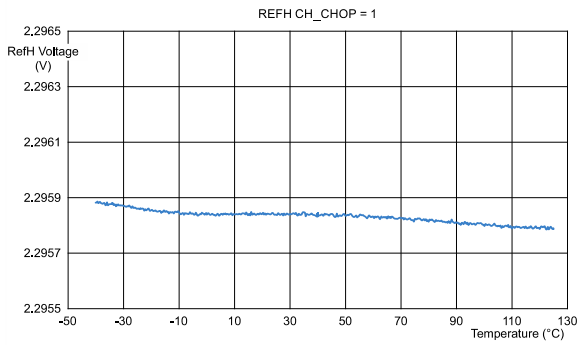
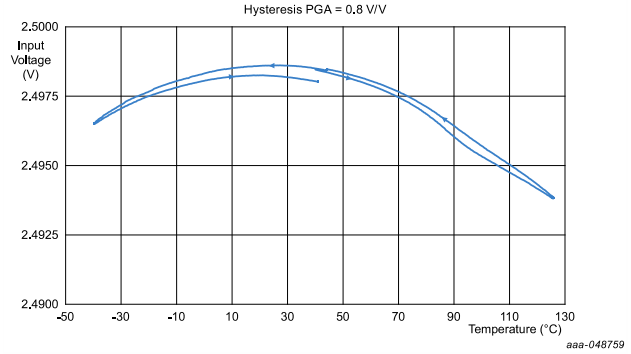
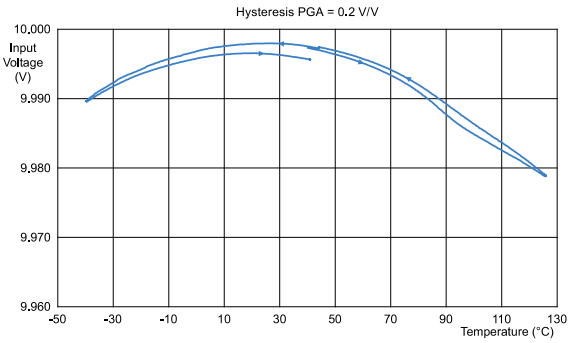


Table 48. Typical operating characteristics...continued

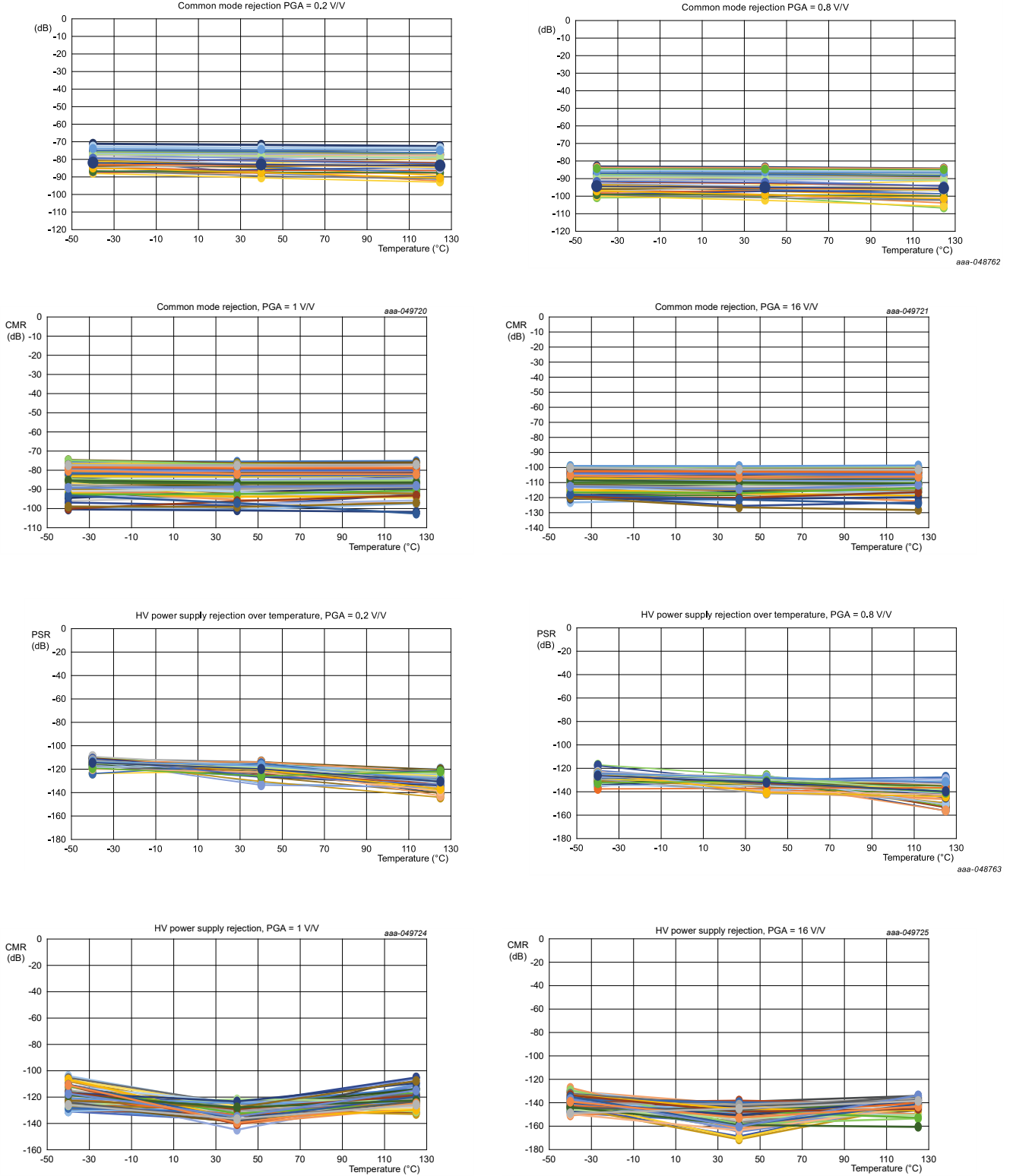


Table 48. Typical operating characteristics...continued

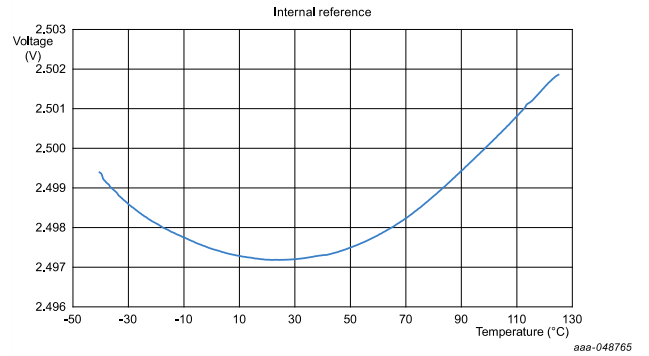
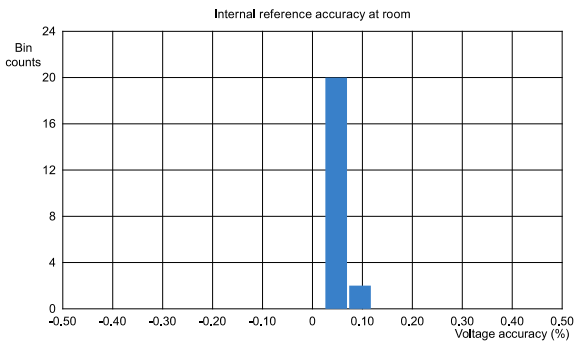
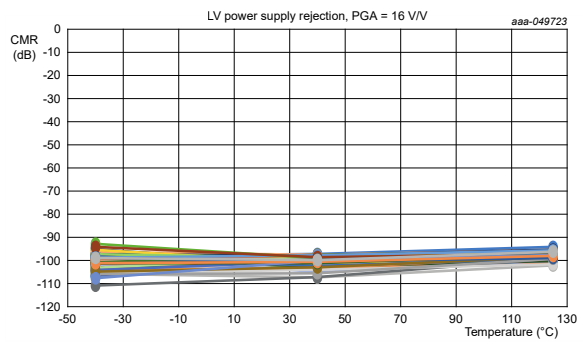
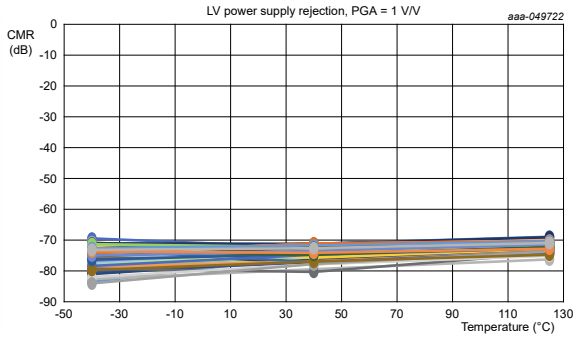
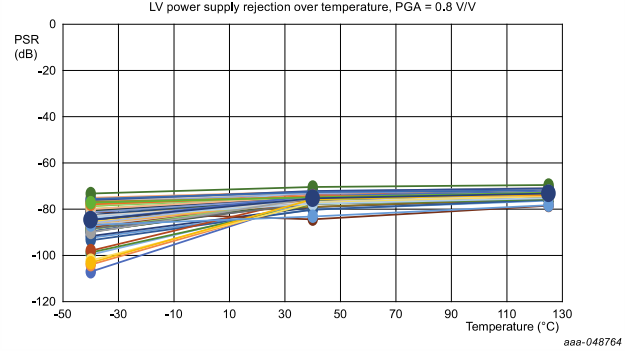
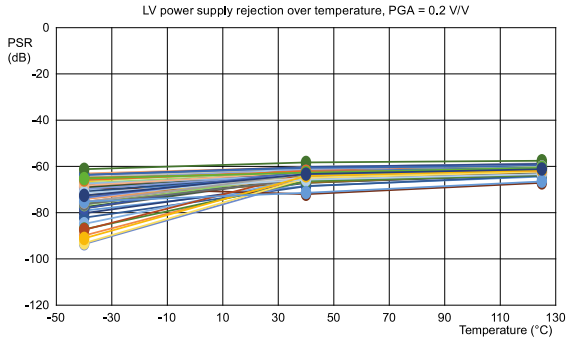
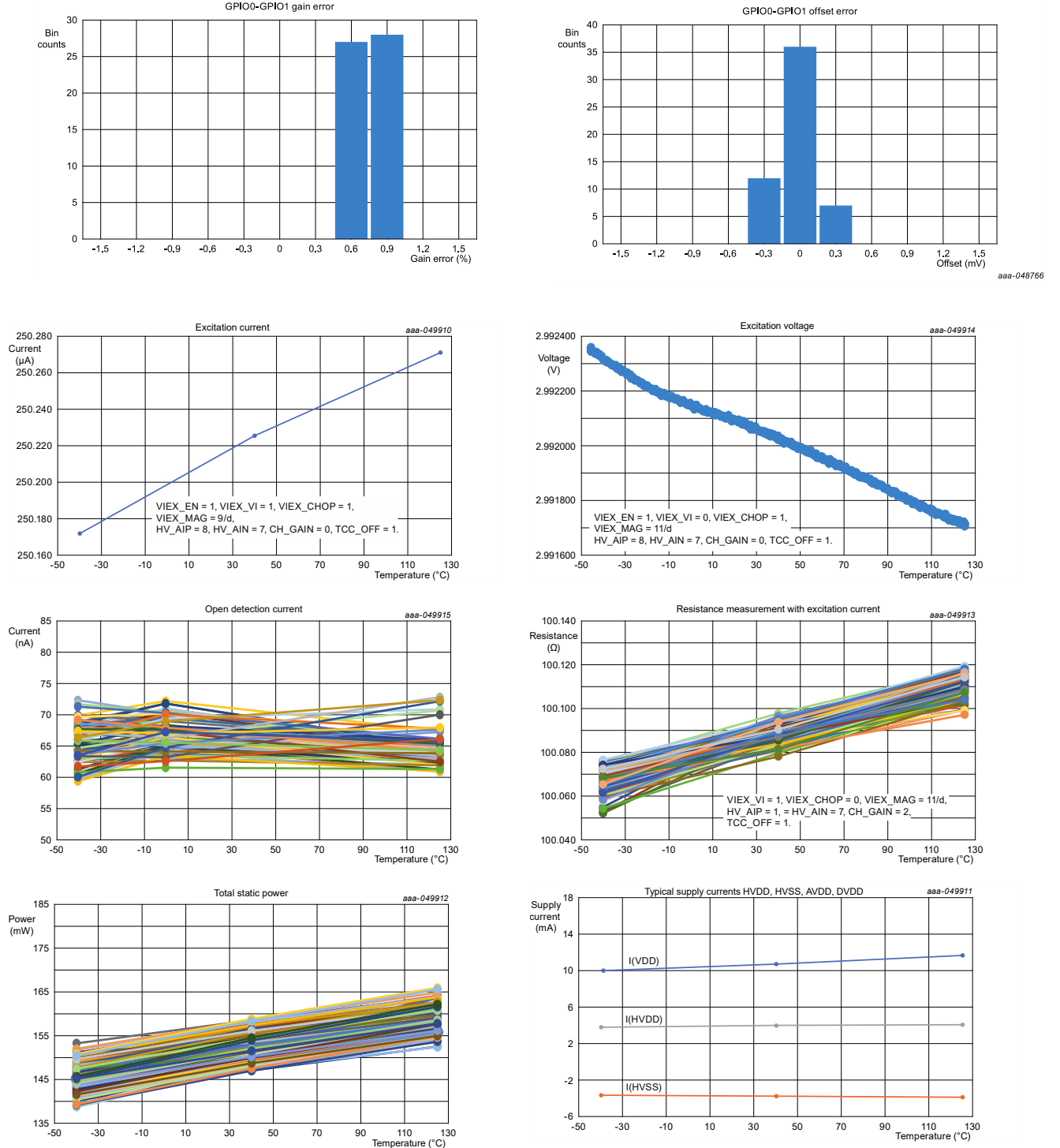
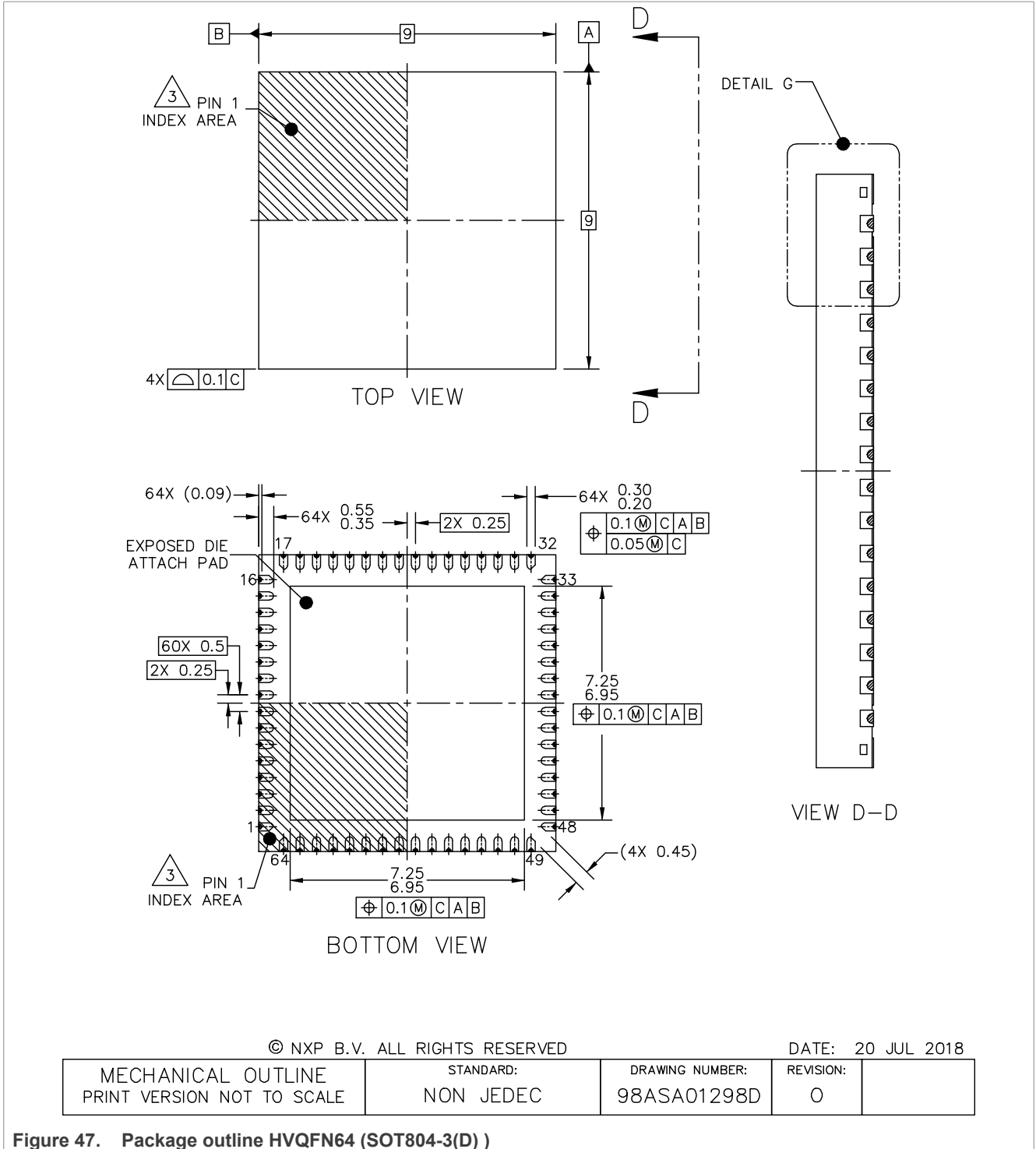


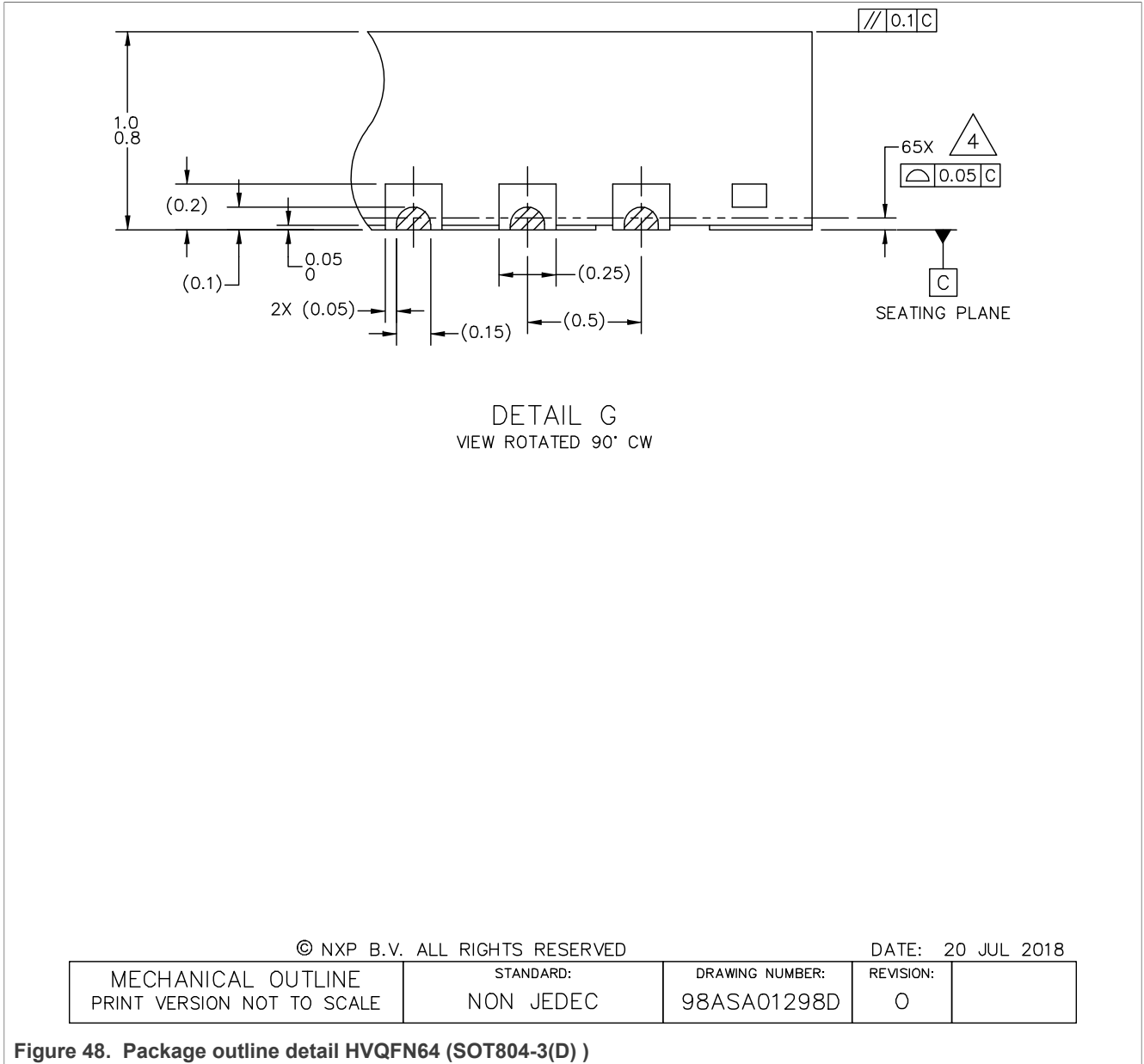


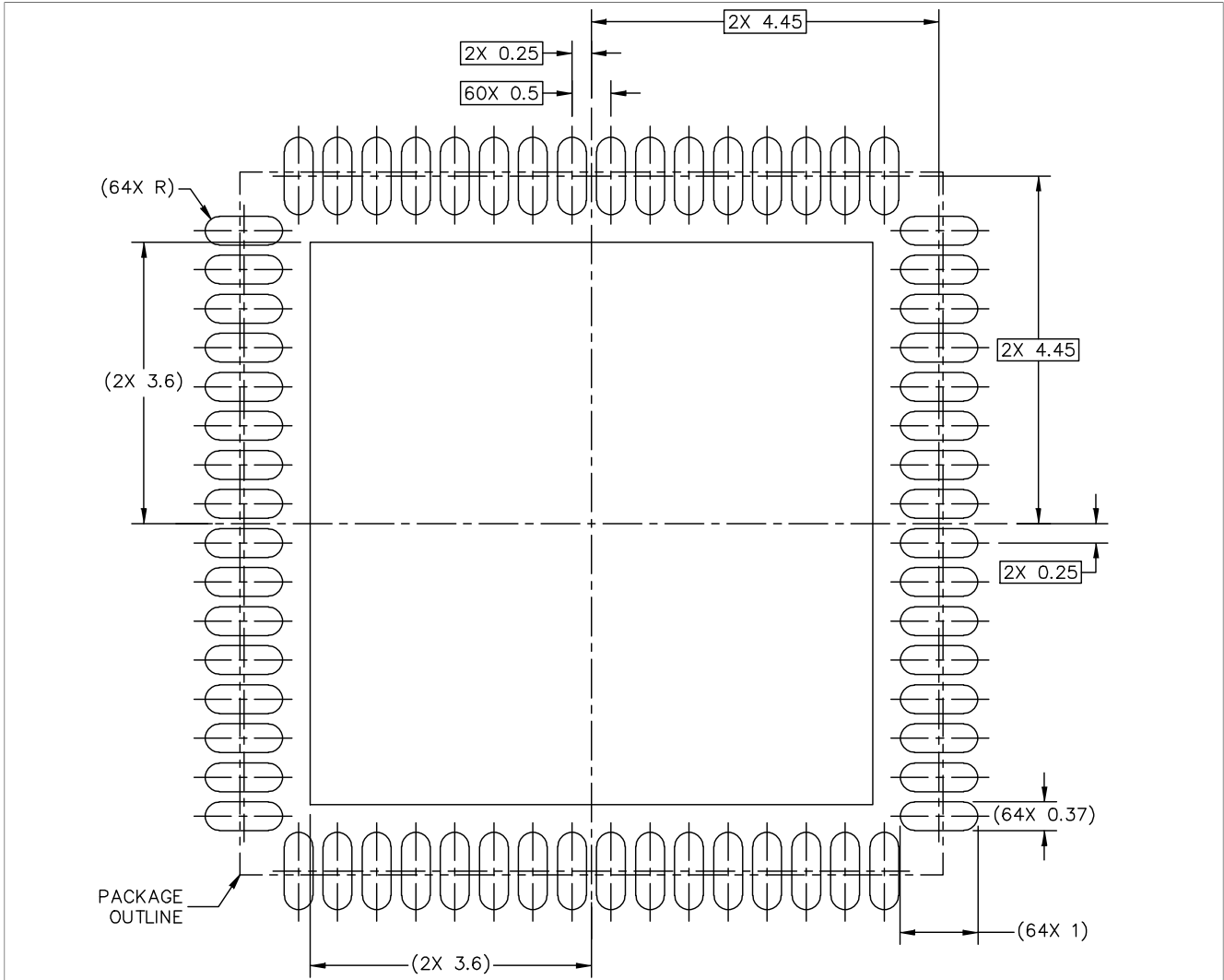
Table 48. Typical operating characteristics...continued



13 Package outline







PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

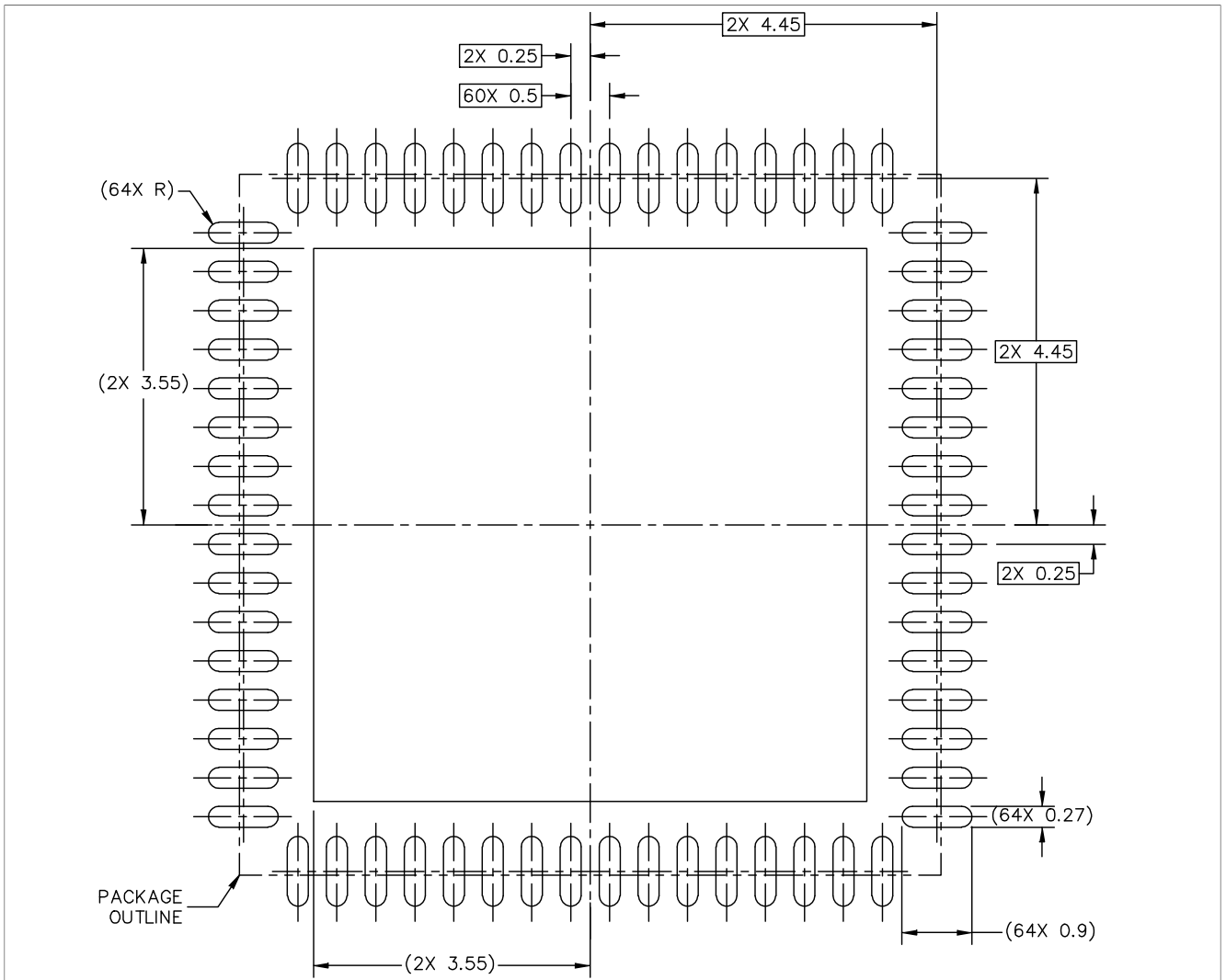
THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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DATE: 20 JUL 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01298D	REVISION: 0	
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Figure 49. Reflow soldering footprint part 1 for HVQFN64 (SOT804-3(D))



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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DATE: 20 JUL 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01298D	REVISION: 0	
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Figure 50. Reflow soldering footprint part 2 for HVQFN64 (SOT804-3(D))

Revision history

Rev	Date	Description
v.1	20230224	Initial version

## 14 Legal information

### 14.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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