NAFE71388

Universal ±25 V 8-Input High Speed AFE

Rev. 1 — 4 November 2022 **Product data sheet**

Document information

Information	Content
Keywords	NAFE71388, 8-channel, analog front-end (AFE), 24-bit ADC resolution
Abstract	Highly configurable multichannel precision AFE for industrial applications.

1 General description

The NAFE71388 is a highly configurable industrial-grade multichannel universal input analog front-end (AFE) that meets high-precision measurement requirements. The device integrates low-leakage, high-voltage (HV) fast multiplexers, low-offset and low-drift programmable gain amplifier (PGA) and buffers, high data-rate 24-bit Delta-Sigma analog-to-digital converter (ADC), and low-drift voltage reference. All of the HV analog pins are diode-protected internally for electromagnetic compatibility (EMC) and miswiring scenarios. The NAFE71388 is equipped with various diagnostic and supplies supervisory circuitry for condition monitoring and anomaly detection. Two precise calibration voltage sources are made available for ease of end-to-end system self-calibration and predictive maintenance.

The NAFE71388 family of products is designed for programmable logic controllers (PLCs), I/O modules, data loggers, instrumentation, and high-precision sensor and data acquisition systems.

2 Features and benefits

- Eight configurable HV inputs
  - Single-ended or differential, with ranges up to ±25 V
  - Independent configurations for voltage and current ranges
  - Overvoltage protected up to ±36 V for less than one hour
- Fast data rates
  - 15 SPS to 576 kSPS
  - Simultaneous 50 Hz/60 Hz line rejection
  - ENOB: 17-bit at 144 kSPS
- High accuracy
  - 0.005 %FS accuracy at room after user calibration
  - 0.1 %FS accuracy over -25 ℃ to 105 ℃
- System calibration
  - End-to-end calibration with integrated precise voltage sources
  - Accurate factory-calibrated products available
- ±3 ºC internal temperature sensor
- 0.2% internal oscillator accuracy at room temperature
- Diagnostic system for faults detection and prediction
- CRC error detection
- Ten GPIOs
- 32 MHz SPI interface
- Robust 8 kV HBM ESD and IEC61000-4-5 2 kV surge protection
- Power supply: HV: ±7 V to ±24 V, LV: 3.3 V
- 135 mW low power consumption
- Operating temperature range T_A: -40 ℃ to +125 ℃
- Package: 64 pin, 9 mm x 9 mm x 0.85 mm HVQFN

3 Applications

- Data acquisition system
- PLC, DCS I/O modules
- Industrial automation and process control

4 Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
NAFE71388 B40BS	NAFE71388 B40BS	HVQFN64	Plastic, thermal-enhanced very thin quad flatpack; no leads; 64 terminals; 0.5 mm pitch; 9 mm x 9 mm x 0.85 mm body	SOT804-3(D) https://www.nxp.com/packages/SOT804-3(D)

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
NAFE71388 B40BS	NAFE71388 B40BSMP	HVQFN64	Reel 13” Q2/T1 *Standard mark SMD dry pack	1000	TA = -40 °C to +125 °C
NAFE71388 B40BS	NAFE71388 B40BSE	HVQFN64	1 + 1 Tray *Standard mark SMD dry pack	260	TA = -40 °C to +125 °C
NAFE71388 B40BS	NAFE71388 B40BSK	HVQFN64	5+1 Tray *Standard mark SMD dry pack	1300	TA = -40 °C to +125 °C

4.2 Product family

The NAFE family is optimized for power and speed, with highly integrated functional features and modes for offloading the host processor to achieve higher performance and low power consumption of overall system.

In addition, the NXP analog input AFE family of products is pin-to-pin, software-compatible, and well-suited in scalable applications of analog I/O modules and data acquisition systems.

Table 1 shows the possible features to select for each family member. Contact the NXP factory or an NXP sales representative to get further information and availability of appropriate configurations.

Table 3. Part numbers

Part number	VI excitation source	Low-power high-speed	Resolution 16-bit/24-bit	#Input	Factory calibrated
NAFE11388B40BS	No	Low power	24	8	Yes
NAFE71388B40BS	No	High speed	24	8	Yes

5 Block diagram

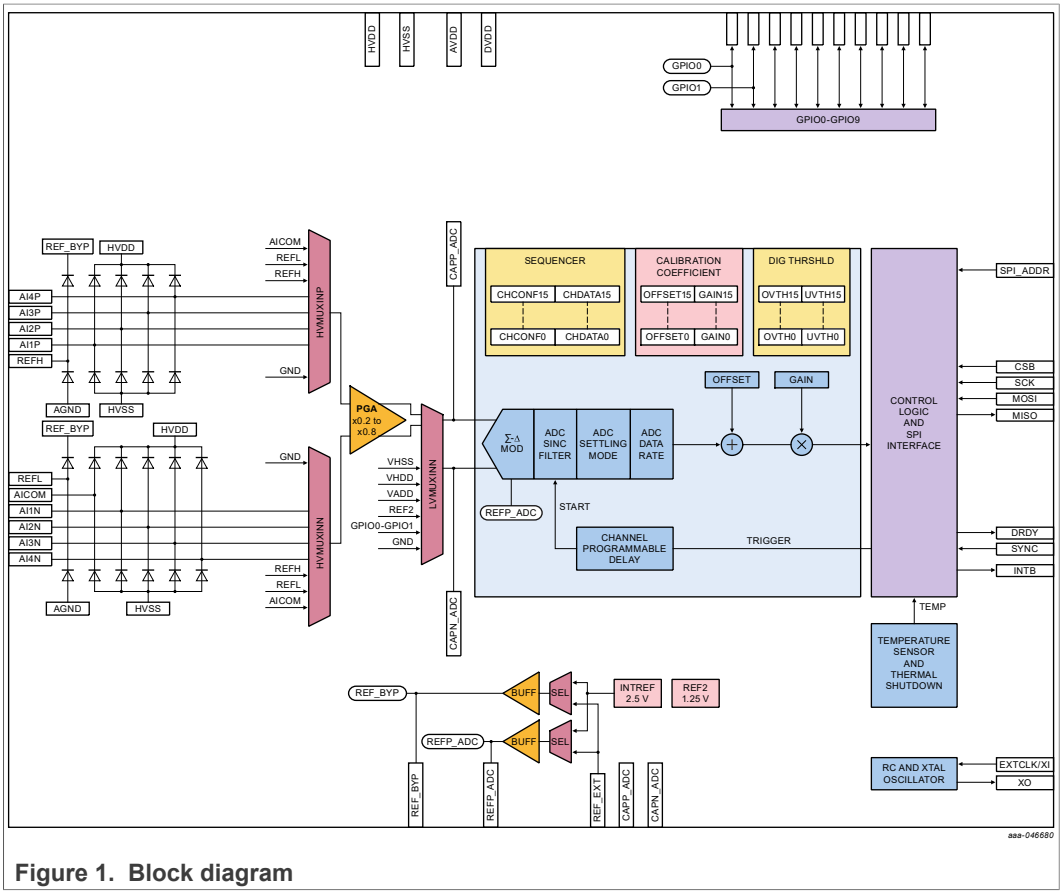


Figure 1. Block diagram

6 Pinning information

6.1 Pinning

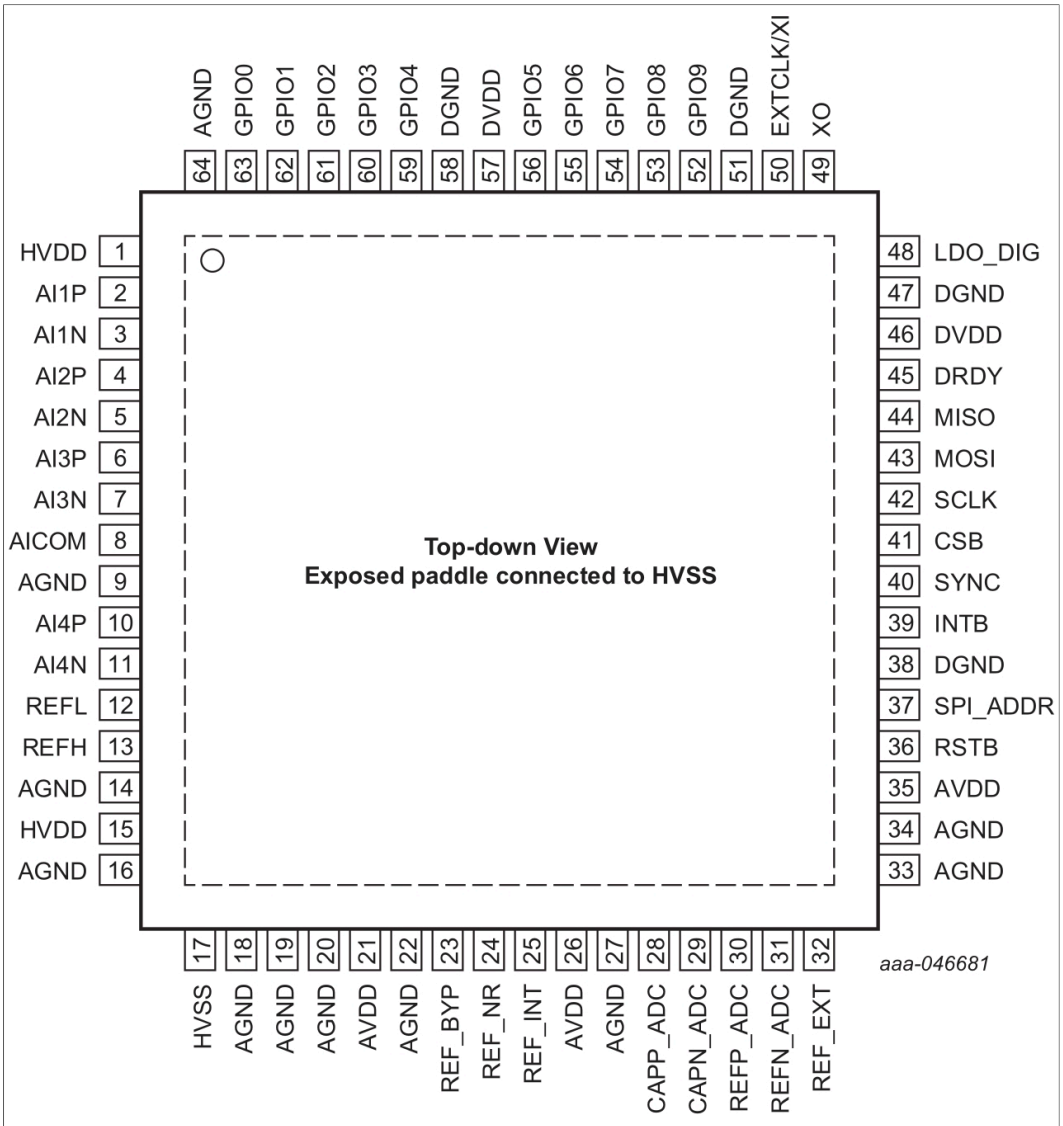


Figure 2. Pin configuration in 64-lead 9 mm x 9 mm x 0.85 mm VQFN package

6.2 Pin description

Table 4. Pin description

Pin	Name	I/O	Functional description
1	HVDD	Supply	High-voltage positive supply, 0.1 µF || 4.7 µF to AGND, optional: install 28 V Zener to AGND for protection
2	AI1P	AI	Analog Input in series with external 2.5 kΩ resistor with 1 nF or 10 nF cap to AGND
3	AI1N	AI	Analog Input in series with external 2.5 kΩ resistor with 1 nF or 10 nF cap to AGND

Table 4. Pin description*...continued*

Pin	Name	I/O	Functional description
4	AI2P	AI	Analog Input in series with external 2.5 kΩ resistor with 1 nF or 10 nF cap to AGND
5	AI2N	AI	Analog Input in series with external 2.5 kΩ resistor with 1 nF or 10 nF cap to AGND
6	AI3P	AI	Analog Input in series with external 2.5 kΩ resistor with 1 nF or 10 nF cap to AGND
7	AI3N	AI	Analog Input in series with external 2.5 kΩ resistor with 1 nF or 10 nF cap to AGND
8	AICOM	AI	Analog GND or common input in series with external 2.5 kΩ resistor with 1 nF or 10 nf cap to AGND
9	AGND	Ground	Analog ground
10	AI4P	AI	Analog Input in series with external 2.5 kΩ resistor with 1 nF or 10 nF cap to AGND
11	AI4N	AI	Analog Input in series with external 2.5 kΩ resistor with 1 nF or 10 nF cap to AGND
12	REFL	AO	0.2 V unbuffered internal voltage source, 10 nF cap to AGND
13	REFH	AO	2.3 V unbuffered internal voltage source, 10 nF cap to AGND
14	AGND	Ground	Analog ground
15	HVDD	Supply	High-voltage positive supply, 0.1 µF || 4.7 µF cap to AGND
16	AGND	Ground	Analog ground
17	HVSS	Supply	High-voltage negative supply, 0.1 µF || 4.7 µF cap to AGND. (internally shorted to exposed pad) Zener to AGND for protection.
18	AGND	Ground	Analog ground
19	AGND	Ground	Analog ground
20	AGND	Ground	Analog ground
21	AVDD	Supply	3.3 V analog power supply, 0.1 µF || 4.7 µF cap to AGND.
22	AGND	Ground	Analog ground
23	REF_BYP	AO	Buffered voltage reference bypass, 100 pF (max loading) cap to AGND
24	REF_NR	AI	Voltage reference noise reduction, 0.47 µF cap to AGND
25	REF_INT	AO	Internal voltage reference output bypass, 0.47 µF
26	AVDD	Supply	3.3 V analog power supply, 0.1 µF || 4.7 µF cap to AGND
27	AGND	Ground	Analog ground
28	CAPP_ ADC	AO	ADC buffer positive output, 1 nF C0G cap to CAPN
29	CAPN_ ADC	AO	ADC buffer negative output, 1 nF C0G cap to CAPP
30	REFP_ ADC	AO	ADC positive reference bypass, 0.1 µF || 1 µF X7R cap to REFN_ADC

Table 4. Pin description*...continued*

Pin	Name	I/O	Functional description
31	REFN_ ADC	AI	ADC ground reference, 0.1 µF || 1 µF X7R cap to REFP_ADC
32	REF_EXT	AI	External 2.5 V reference voltage Input. 0.1 µF cap to AGND
33	AGND	Ground	Analog ground
34	AGND	Ground	Analog ground
35	AVDD	Supply	Connect 0.1 µF || 4.7 µF cap to AGND (pin-34) close to the AVDD pin
36	RSTB	DI	Chip reset, active-low (CMOS push-pull or open drain with internal 100 kΩ pullup).
37	SPI_ ADDR	DI	SPI address 0 (with internal 100 kΩ pulldown).
38	DGND	Ground	Digital ground
39	INTB	DO	Active low interrupt output (CMOS push-pull or open drain internally pulled up)
40	SYNC	DI	ADC sync pulse input
41	CSB	DI	Chip select input, active-low (with internal 100 kΩ pullup)
42	SCLK	DI	SPI clock input
43	MOSI	DI	SPI data input
44	MISO	DO	SPI data output
45	DRDY	DO	ADC data ready output, active-high
46	DVDD	Supply	3.3 V digital power supply, 0.1 µF || 4.7 µF cap to DGND.
47	DGND	Ground	Digital ground
48	LDO_DIG	AO	Internal 1.8 V LDO bypass, 0.1 µF || 4.7 µF uF cap to DGND.
49	XO	DI	18.432 MHz crystal XOUT with loading cap (< 20 pF). No-connect or float if crystal is not used
50	EXTCLK/ XI	DI	External clock input or 18.432 MHz crystal XIN with loading cap(< 20 pF)
51	DGND	Ground	Digital ground
52	GPIO9	DI, DO	General-purpose digital input/output or system clock output
53	GPIO8	DI, DO	General-purpose digital input/output
54	GPIO7	DI, DO	General-purpose digital input/output
55	GPIO6	DI, DO	General-purpose digital input/output
56	GPIO5	DI, DO	General-purpose digital input/output
57	DVDD	Supply	3.3 V digital power supply, 0.1 µF || 4.7 µF cap to DGND.
58	DGND	Ground	Digital ground
59	GPIO4	DI, DO	General-purpose digital input/output
60	GPIO3	DI, DO	General-purpose digital input/output
61	GPIO2	DI, DO	General-purpose digital input/output

Table 4. Pin description*...continued*

Pin	Name	I/O	Functional description
62	GPIO1	DI, DO, AI	General-purpose digital I/O or ADC differential analog input: GPIO0-GPIO1
63	GPIO0	DI, DO, AI	General-purpose digital I/O or ADC differential analog input: GPIO0-GPIO1
64	AGND	Ground	Analog ground
	EP		Exposed pad is connected to HVSS internally. Exposed pad should be tied to HVSS on PCB.

7 Functional description

7.1 Overview

The NAFE71388 is a highly configurable, universal eight-input AFE with various integrated diagnostic features. At HV analog inputs, the low-leakage pins could be configured anywhere from eight single-ended to four differential signals, with external common input AICOM or internal AGND reference. Three selectable PGA gain settings of 0.2 V/V, 0.4 V/V, and 0.8 V/V are available to provide differential full ranges of ±25 V to ±6.25 V. In general, all of the HV input characteristics are specified to the linear (nominal) input ranges for all of the channel gain settings, which is 80 % of the full input range. In addition to the differential signals at PGA output, one auxiliary differential input GPIO0-GPIO1, four low-voltage diagnostic signals are also multiplexed to ADC: power supplies AVDD, HVDD, HVSS, and an independent coarse voltage reference (REF_coarse).

The voltage reference (VREF) derived voltage sources REFH and REFL are available through pins for external measurement. These two voltage sources are also connected as inputs to high-voltage multiplexer (HVMUX). They could be used for on-chip self-calibration or self-diagnostic purposes, regardless of the voltage reference sources, which can be either external, internal, or mixed. When supplied with the factory-calibrated coefficients, REFH and REFL facilitate routine calibrations without the need for additional accurate components.

An independent on-chip temperature sensor is included for continuous die temperature monitoring with a 16-bit readout. This temperature reading is also used to trigger an overtemperature warning at 145 ºC, auto-shutdown at 165 ºC, or the user-programmable temperature alarm.

The NAFE71388 comes with ten GPIOs that satisfy most of the needs for monitoring and control in typical applications. The selectable clock sources could be either the internal oscillator or a crystal oscillator, or external clock. In addition, a data and conversion synchronization is available via SYNC and DRDY pins, and the last falling edge of the SPI clock.

Succeeding to 24-bit ΔΣ modulator, a multistage digital filter was designed to offer a wide range of data rates with a selectable cascade of SINC filters and the option of Single-Cycle Settling mode versus Normal Settling mode. In multichannel, fast-switching applications, the user may trade off speed/accuracy and fine-tune the effective data rate. Simultaneous 50 Hz and 60 Hz line rejection is available in lower data rates.

The software-configurable sequencer enables high data-rate input channel scanning at system level.

Five efficient reading modes are available for ADC data conversion: single-channel single-reading (SCSR), single-channel continuous-reading (SCCR), multichannel single-reading (MCSR), multichannel multireading (MCMR), and multi-channel continuous-reading (MCCR). The user may issue command CMD_BURST_DATA to read back multiple channels data in a single SPI transaction. See Table 17 for conversion start commands.

7.2 Precise and fast data acquisition

The NAFE71388 is suitable for data acquisition of high-precision and high-speed analog inputs.

The NAFE71388 integrates an input multiplexer (MUX), high gain bandwidth (GBW) programmable gain amplifier (PGA), and a high-resolution 24-bit sigma-delta ADC. The optimized architecture of the MUX, PGA, and ADC provides fast input-scanning with flexible output data rates, which are comparable with SAR ADC architecture used in fast response-time system.

Programmable ADC output data rate range:

- 576 ksps to 15 sps in Normal Settling mode
- 144 ksps to 3 sps in Single-Sycle Settling mode

Figure 3 shows the scanning time required when HV MUX switches from one input to another (effectively presenting a step function), and PGA follows to settle with limited bandwidth and the required ADC conversion time at a specified data rate.

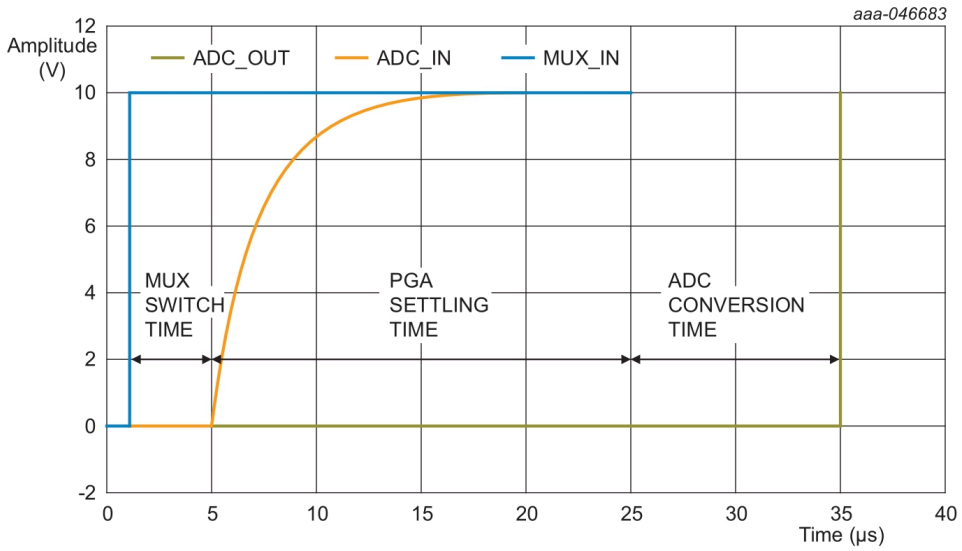


Figure 3. Scanning time per input

7.3 Detailed description

This section describes the building blocks integrated in the NAFE71388.

7.3.1 Architecture block diagram

The NAFE71388 can be grouped in seven sections: high-voltage multiplexer, PGA, low-voltage multiplexer, ADC, digital calibration, voltage reference, and clock sources as shown in Figure 1.

7.3.2 High-voltage multiplexer — HVMUX

The high-voltage analog input section serves as an externally accessible input and internal input.

The external inputs are: AI1P, AI2P, AI3P, AI4P, AI1N, AI2N, AI3N, AI4N, AICOM

- AI1P, AI2P, AI3P, AI4P are connected to the positive high-voltage multiplexer HVMUXINP input.
- AI1N, AI2N, AI3N, AI4N are connected to the negative high-voltage multiplexers HVMUXINN input.

AICOM, REFH, REFL, and AGND (internal ground) are connected to both positive and negative high-voltage input multiplexers HVMUXINP and HMMUXINN, respectively.

7.3.2.1 Analog input protection diodes and clamping

As shown in Figure 4, the external analog input pins of the NAFE are followed by clamping circuits for electrostatic discharge (ESD) and surge protection.

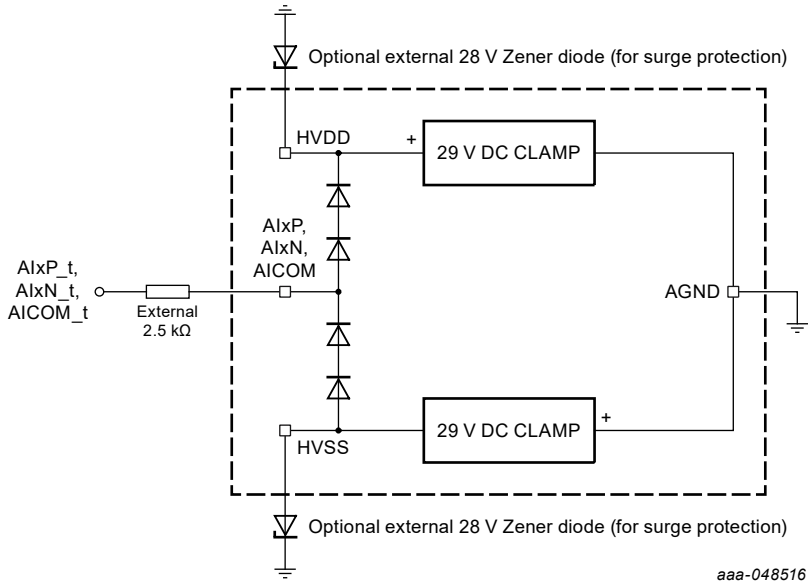


Figure 4. Input pins protection

Each HV input pin is equipped with input protection diodes connected to HVDD, HVSS.

It is recommended that an external series 2.5 kOhm resistor with 1 nF or 10 nF capacitor to AGND is installed for each HV input pin for reliability. See Section 11.1.

The integrated clamping circuits, shown in Figure 4, protect the NAFE inputs from possible surge voltage and from ESD events occurring during the manufacturing process and during printed-circuit board (PCB) assembly.

If an analog input is driven below HVSS, or above HVDD, the internal protection diodes may conduct current. A 2.5 kΩ or greater external series resistor is required to limit the input current to the specified value.

7.3.2.2 HV input multiplexer - HVMUXIN

The NAFE uses two independent HV input multiplexers to measure the differential, pseudo-differential, and single-ended signal. When the input is used in differential or pseudo-differential mode, the NAFE provides high common-mode rejection.

The differential configuration is obtained by connecting the positive wire of signal to any of the AIxP inputs and the negative wire of signal to any of the AIxN inputs and via software configuration selecting the respective inputs of HVMUX.

The pseudo-differential configuration is obtained by connecting the positive wire of signal to any of the AIxP or AIxN inputs and the negative wire of signal to AICOM input and via software configuration selecting the respective inputs of HVMUX.

The single-ended configuration is achieved by connecting the positive signal to any of the AIxP or AIxN inputs and the negative wire of signal to AICOM.

The selected input to positive and negative HVMUX should be configured appropriately to match the physical connections. When CH_CHOP = 1 is set, two ADC conversions will be performed. Therefore the final ADC output is the average of the difference of these two ADC intermediate outputs. As such, the channel offset is canceled and the effective output data rate is half of the programmed value.

Note: *The ADC output polarity sign is inverted internally and automatically whenever AIxP input is connected to AICOM or GND while AIxN input is AI1N..AI4N, REFH, REFL.*

7.3.2.2.1 Analog common input (AICOM)

To ensure precise single-ended measurements, AICOM pin should be connected in series with a 2.5 kΩ resistor and connected to an external GND reference physically close to the measured positive signal on the printed-circuit board (PCB).

7.3.2.2.2 REFH and REFL

REFH and REFL provide stable and accurate voltage sources derived from VREF_BYP. REFH and REFL are 92 % and 8 %, of VREF_BYP, with a nominal value of 2.3 V and 0.2 V, respectively.

REFH and REFL are connected to inputs of both HVMUXINP and HVMUXINN multiplexer.

REFH and REFL could be used for system-level self-calibration on the field, failure prediction, and predictive maintenance. Factory OPT_COEF1 and OPT_COEF2 is available for REFH and REFL on optional part numbers.

7.3.2.2.3 Low-leakage circuit

The NAFE71388 provides a high-input impedance of 1 GΩ and low-input leakage current less than 5 nA at 105 °C. In combination with its low-noise and low-offset drift PGA, the device is well-suited for precision temperature measurement with RTD and TC.

7.3.3 Programmable gain amplifier

The programmable gain amplifier (PGA) is a low-noise, programmable gain, differential input, differential output amplifier. The PGA operates in Gain or Attenuation mode, depending on the gain selected. Typically, the PGA is programmed to utilize the input range of the ADC to the full-scale input signal. Available PGA gains are 0.2, 0.4, 0.8 V/V.

7.3.3.1 PGA input operating ranges

Table 5 shows the HV input nominal ranges, the max and min values, full-scale range, and resolution for the different types of input signals and PGA gain setting.

Table 5. HV input ranges and resolutions

Nominal values (V)			
Type	PGA gain setting		
	0.2	0.4	0.8
Bipolar DIFF	±20	±10	±5
Bipolar SE	±10	±5	±2.5
Unipolar DIFF	±10	±5	±2.5
Unipolar SE	0-10	0-5	0-2.5
Min and max values (V)			
Type	PGA gain setting		
	0.2	0.4	0.8
Bipolar DIFF	±25	±12.5	±6.25
Bipolar SE	±12.5	±6.25	±3.125
Unipolar DIFF	±12.5	±6.25	±3.125
Unipolar SE	0-12.5	0-6.25	0-3.125
Full Scale range (V)			
Type	PGA gain setting		
	0.2	0.4	0.8
Bipolar DIFF	50	25	12.5
Bipolar SE	25	12.5	6.25
Unipolar DIFF	25	12.5	6.25
Unipolar SE	12.5	6.25	3.125
Resolution (V)			
Type	PGA gain setting		
	0.2	0.4	0.8
Bipolar DIFF	3.0E-6	1.5E-6	750E-9
Bipolar SE	3.0E-6	1.5E-6	750E-9
Unipolar DIFF	3.0E-6	1.5E-6	750E-9
Unipolar SE	3.0E-6	1.5E-6	750E-9

7.3.3.2 PGA input common mode ranges

PGA input common mode voltage range depends on PGA gain.

For cases with fully differential input voltages, the maximum allowable input common mode voltage can be calculated as:

If $V_{in+} = VCM + \frac{V_{DIFF}}{2}$ and $V_{in-} = VCM - \frac{V_{DIFF}}{2}$

Then, $VCM_{max} = A \cdot \left(V_{REF} - CH_{GAIN} \cdot \frac{V_{DIFF}}{2}\right)$

$A = 5$ for $CH_{GAIN} = 0.2,\ \ 0.4,\ \ 0.8.$

And $V_{REF} = 2.5\ V$

7.3.4 Low-voltage multiplexer - LVMUX

The internal node voltages (scaled HVDD and HVSS, AVDD, VREF_Coarse, GPIO0-GPIO1) and PGA outputs are routed to the ADC input using the low-voltage multiplexer.

7.3.5 Analog-to-digital converter

7.3.5.1 ADC buffer

The ADC buffer is used to drive the sampling circuit of the ADC, where its differential output pins, CAPP and CAPN, are to be loaded with external C0G type capacitor.

7.3.5.2 Sigma delta ADC

The ADC is based on sigma delta architecture that provides low-noise and high-speed acquisition in Single-Channel and Multichannel mode. The sigma delta architecture includes a sigma delta modulator followed by a configurable digital filter.

The ADC modulator is a third-order ΣΔ modulator. The modulator samples the analog input voltage at a high-sample rate (fMOD = fsys_clk / 2) and converts the analog input to a bit stream that is processed by the following digital filter.

The digital filter processes the modulator output data to produce the high-resolution conversion result. The digital filter filters and decimates the data. Software selection of a certain digital filter depends on the trade-off between resolution, data rate, and line-cycle rejection acceptable in a system.

The ADC digital filter consists of two SINC filter stages. The first stage is a variable decimation SINC4 filter followed by the second stage variable-decimation, variable-order SINC filters. The optimized high-speed SINC4 filter averages and down-samples the modulator data to produce high-speed data rates from 576 ksps to 12 ksps.

The low-speed digital filter performs additional filtering and decimation to produce data rates of 9 ksps to 15 sps. The low-speed stage is a programmable-order SINC filter as SINC1, SINC2, SINC3, SINC4.

The data rate is programmed by the CH_CONFIG1.ADC_DATA_RATE bits.

The digital filters are controlled by CH_CONFIG1.ADC_SINC bits.

Note: *SINCx filter has settling time of x clock cycles, where x is the order. To manage the SINC filter settling, the NAFE71388 offers two different Conversion modes.*

The Single-Cycle Settling mode is suggested for a multichannel system to avoid the settling error. The Normal Settling mode is suggested for single channel to get a faster data rate or lower noise.

7.3.5.3 Frequency response

The low-pass filtering effect of the SINC filters sets the overall frequency response of the ADC.

In Normal Settling mode, the frequency response of data rates, 12000 sps to 576000 sps, is determined by the transfer function of the first stage SINC4 filter. The frequency response of data rates, 15 sps to 9000 sps, is the product of the transfer function of the first digital filter stage (SINC4) and the selected digital filter of the second stage (SINC1, SINC2, SINC3, SINC4).

Figure 5 shows an example of filter response for data rate 12000 sps with first stage SINC4 filter; and for data rate 6000 sps with second stage SINC4 filter.

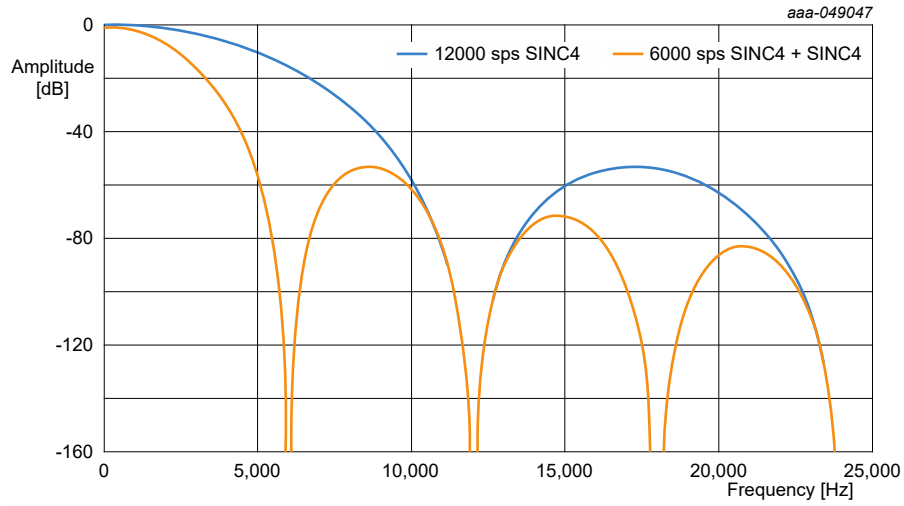


Figure 5. SINC filter transfer function

Figure 6 shows the frequency responses of the second stage SINC1, SINC2, SINC3, and SINC4 filter.

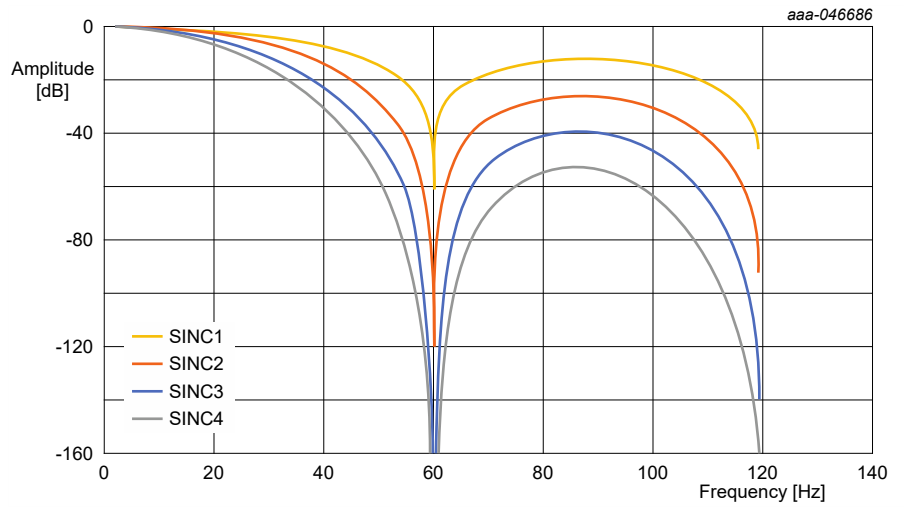


Figure 6. Second stage SINC filter transfer function

7.3.5.4 50 Hz/60 Hz Normal mode noise rejection

The NAFE71388 features a digital filter that provides a 50 Hz and 60 Hz Normal mode rejection (NMR).

Figure 7 shows the SINC4 filter NMR at the date rate of 15 sps, 50 sps, and 60 sps.

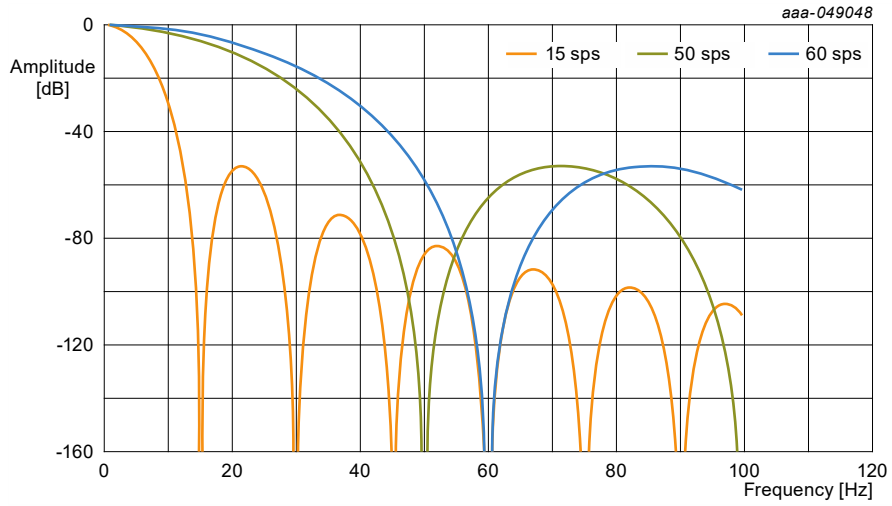


Figure 7. SINC Normal mode rejection vs frequency vs data rata

7.3.5.5 Step response

The NAFE71388 could be configured for the following settling mode:

- **Normal settling:** Fits better for single-channel reading, providing lower noise measurements.
- **Single-cycle settling:** Fits better for multichannel reading, providing settled output.

Figure 8 shows the relative settling time of the digital filter for the normal settling for different orders of SINC filter.

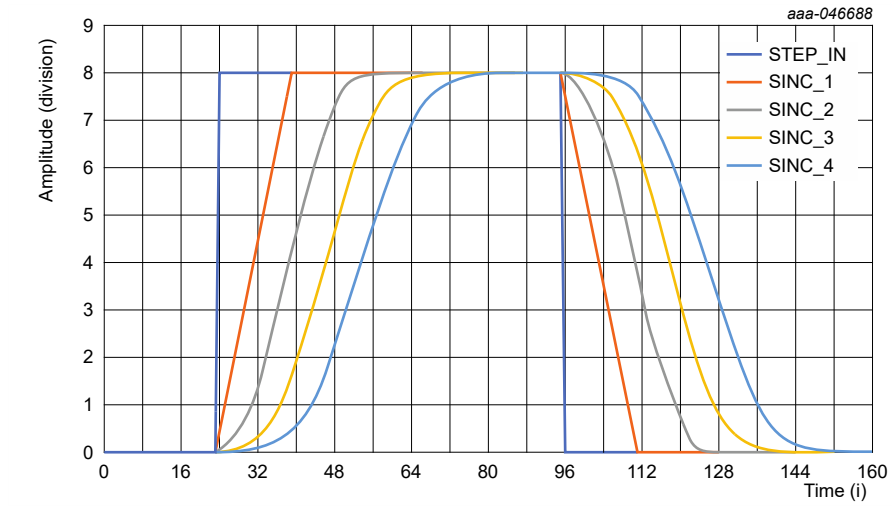


Figure 8. SINC filter step response

7.3.5.5.1 Normal settling vs. single-cycle settling

Figure 9 shows a 100 Hz digitized square wave sampled at 36 ksps. The digital filter is SINC4 and the Settling mode is set to normal. During the square wave transition from low to high, the output takes four samples to settle.

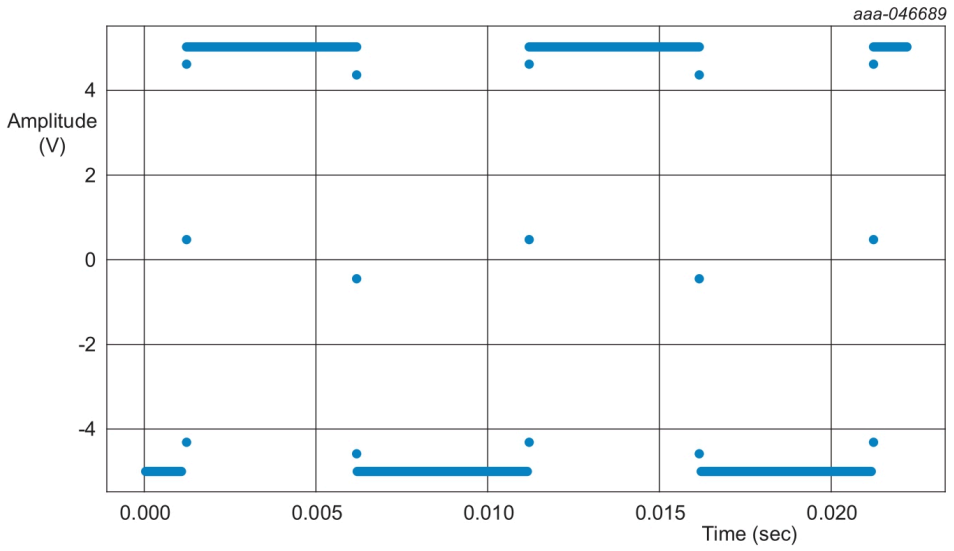


Figure 9. Normal Settling mode and SINC4

Instead, Figure 10 shows a 100 Hz digitized square wave with Settling mode set to single-cycle. The waveform is sampled at 9 ksps and the digital filter is SINC4. In Single-Cycle Settling mode, during the square wave transition from low to high, the output takes one sample to settle.

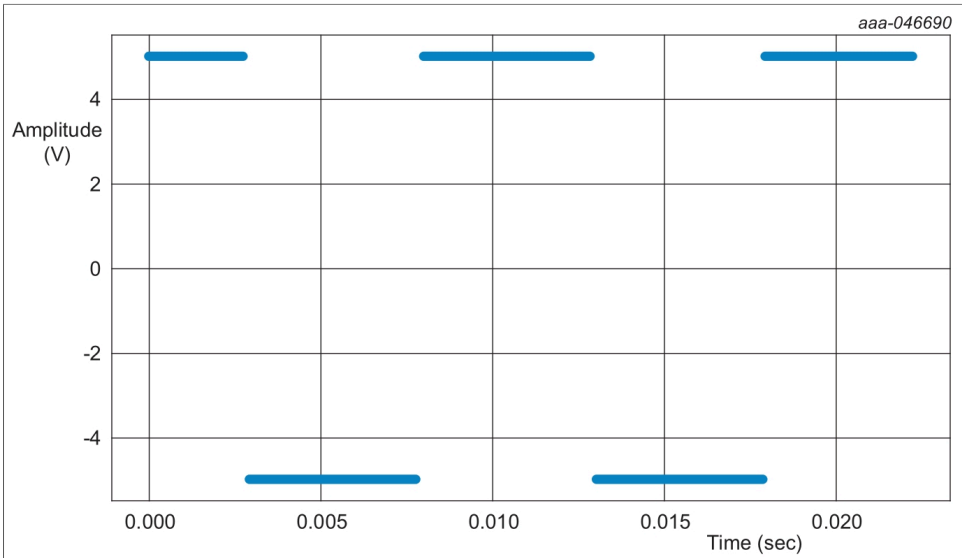


Figure 10. Single-Cycle Settling mode and SINC4

7.3.5.6 ADC data rate

Table 6 shows the programmable data rates for different SINC digital filters and Settling modes.

A total of 29 programmable data rates is available. The rates are set by channel-based CH_CONFIG1 register bits *ADC_DATA_RATE[4:0]*. The highest data rate codes (DRO = 0..11) are with second-stage SINC filter bypassed, *ADC_SINC[2:0]=0*. Moreover, data rates with Single-Cycle Settling modes are four times slower with respect to

Normal Settling mode, CH_CONFIG2 register bit ADC_NORMAL_SETTLING = 1. The final effective data rate, in Single-Cycle Settling mode, could be further reduced by CH_DELAY[5:0]. The details are described in Section 7.5.3.3.

Although all conversions are from the 24-bit ADC, the data may be read out in 24-bit or 16-bit format by setting ADC_DATA_OUT_16BIT bit in SYS_CONFIG0 register.

Table 6. Data rate (system clock: 9.216 MHz)

		Normal settling					Single-cycle settling				
DRO code	OSR	SINC4	SINC4+ SINC1	SINC4+ SINC2	SINC4+ SINC3	SINC4+ SINC4	SINC4	SINC4+ SINC1	SINC4+ SINC2	SINC4+ SINC3	SINC4+ SINC4
0	8	576000					144000				
1	12	384000					96000				
2	16	288000					72000				
3	24	192000					48000				
4	32	144000					36000				
5	48	96000					24000				
6	64	72000					18000				
7	96	48000					12000				
8	128	36000					9000				
9	192	24000					6000				
10	256	18000					4500				
11	384	12000					3000				
12	512		9000.00	9000.00	9000.00	9000.00		4500.00	3000.00	2250.00	1800.00
13	768		6000.00	6000.00	6000.00	6000.00		3000.00	2000.00	1500.00	1200.00
14	1,024		4500.00	4500.00	4500.00	4500.00		2250.00	1500.00	1125.00	900.00
15	2,048		2250.00	2250.00	2250.00	2250.00		1125.00	750.00	562.50	450.00
16	4,096		1125.00	1125.00	1125.00	1125.00		562.50	375.00	281.25	225.00
17	5,760		800.00	800.00	800.00	800.00		400.00	266.67	200.00	160.00
18	7,680		600.00	600.00	600.00	600.00		300.00	200.00	150.00	120.00
19	11,520		400.00	400.00	400.00	400.00		200.00	133.33	100.00	80.00
20	23,040		200.00	200.00	200.00	200.00		100.00	66.67	50.00	40.00
21	38,400		120.00	120.00	120.00	120.00		60.00	40.00	30.00	24.00
22	46,080		100.00	100.00	100.00	100.00		50.00	33.33	25.00	20.00
23	76,800		60.00	60.00	60.00	60.00		30.00	20.00	15.00	12.00
24	92,160		50.00	50.00	50.00	50.00		25.00	16.67	12.50	10.00
25	115,200		40.00	40.00	40.00	40.00		20.00	13.33	10.00	8.00
26	153,600		30.00	30.00	30.00	30.00		15.00	10.00	7.50	6.00
27	230,400		20.00	20.00	20.00	20.00		10.00	6.67	5.00	4.00
28	307,200		15.00	15.00	15.00	15.00		7.50	5.00	3.75	3.00

Table 6 shows the output data rate of high-speed parts. The highest data rate is achieved with the lowest OSR, SINC4 only in Normal Settling mode.

7.3.5.7 Noise performance vs data rate

The NAFE71388 noise performance depends on the device configuration: data rate, PGA gain, digital filter order, and Settling mode configuration. Two settings that affect noise performance are data rate and PGA gain. Decreasing the data rate results in a proportional decrease of total noise because the equivalent noise bandwidth of the

digital filter is reduced proportionally with the data rate. Increasing the gain reduces input referred noise of the NAFE71388 because the noise of the PGA is lower than the noise of the ADC. Noise performance also depends on the shape of the digital filter because the order of the digital filter decreases the equivalent noise bandwidth, which results in lower noise.

The table below lists the typical noise performance of gain equal to 0.2 to 0.8 V/V (corresponding input full-scale ranges of ±25 V to ±6.25 V) as input-referred values.

The noise performance data are in units of µVRMS (RMS = root mean square) under the conditions listed.

The data shown in the noise performance tables represent typical performance in normal settling at TA = 25 °C and internal 2.5 V reference voltage. The noise data are acquired with inputs shorted and is based on continuous ADC readings for a period of ten seconds or 1024 samples, whichever occurs first. Repeated noise measurements may yield higher or lower noise performance results because of the statistical nature of the noise.

The following tables in this section report the noise performance versus data rate and PGA gain setting.

Effective number of bits (ENOB) is calculated from the RMS noise applying the following formula:

ENOB = MIN(LOG(Full_Scale_Range / Noise_RMS, 2), 24)

$$Full\ \ Scale\ \ Range = \frac{10}{PGAGAIN}$$

7.3.5.7.1 Noise 24-bit option

Table 7. Noise 24-bit option

		4,608,000 Hz	Estimate noise (uVrms) vs PGA gain setting		
Code	Data rate	OSR	0.2	0.4	0.8
0	576000	8	27947.2	13973.6	6986.8
1	384000	12	7546.8	3773.4	1886.7
2	288000	16	2985.9	1493.0	746.5
3	192000	24	822.2	411.1	205.7
4	144000	32	350.8	175.5	87.9
5	96000	48	149.0	74.6	37.6
6	72000	64	110.9	55.6	28.1
7	48000	96	86.7	43.5	22.0
8	36000	128	74.7	37.5	18.9
9	24000	192	61.0	30.6	15.5
10	18000	256	52.8	26.5	13.4
11	12000	384	43.1	21.6	10.9
12	9000	512	37.3	18.7	9.5
13	6000	768	30.5	15.3	7.7
14	4500	1024	26.4	13.2	6.7
15	2250	2048	18.7	9.4	4.7

Table 7. Noise 24-bit option*...continued*

Code	Data rate	4,608,000 Hz	Estimate noise (uVrms) vs PGA gain setting		
		OSR	0.2	0.4	0.8
16	1125	4096	13.2	6.6	3.4
17	800	5760	11.2	5.6	2.8
18	600	7680	9.7	4.9	2.5
19	400	11520	7.9	4.0	2.0
20	200	23040	5.7	2.8	1.4
21	200	23040	5.7	2.8	1.4
22	100	46080	4.1	2.0	1.0
23	60	76800	3.2	1.6	0.8
24	50	92160	3.0	1.5	0.8
25	40	115200	2.7	1.4	0.7
26	30	153600	2.4	1.2	0.6
27	20	230400	2.1	1.0	0.5
28	15	307200	1.9	0.9	0.5

7.3.5.7.2 ENOB 24-bit option

Table 8. ENOB 24-bit option

Code	Data rate	4,608,000	Estimate ENOB vs PGA gain setting		
		OSR	0.2	0.4	0.8
0	576000	8	10.8	10.8	10.8
1	384000	12	12.7	12.7	12.7
2	288000	16	14.0	14.0	14.0
3	192000	24	15.9	15.9	15.9
4	144000	32	17.1	17.1	17.1
5	96000	48	18.4	18.4	18.3
6	72000	64	18.8	18.8	18.8
7	48000	96	19.1	19.1	19.1
8	36000	128	19.4	19.3	19.3
9	24000	192	19.6	19.6	19.6
10	18000	256	19.9	19.8	19.8
11	12000	384	20.1	20.1	20.1
12	9000	512	20.4	20.3	20.3
13	6000	768	20.6	20.6	20.6
14	4500	1024	20.9	20.8	20.8
15	2250	2048	21.4	21.3	21.3
16	1125	4096	21.8	21.8	21.8
17	800	5760	22.1	22.1	22.1

Table 8. ENOB 24-bit option*...continued*

Code	Data rate	4,608,000 OSR	Estimate ENOB vs PGA gain setting 0.2	0.4	0.8
18	600	7680	22.3	22.3	22.3
19	400	11520	22.6	22.6	22.6
20	200	23040	23.1	23.1	23.1
21	200	23040	23.1	23.1	23.1
22	100	46080	23.5	23.5	23.5
23	60	76800	23.9	23.9	23.9
24	50	92160	24.0	24.0	24.0
25	40	115200	24.0	24.0	24.0
26	30	153600	24.0	24.0	24.0
27	20	230400	24.0	24.0	24.0
28	15	307200	24.0	24.0	24.0

7.3.5.7.3 Noise 16-bit option

Table 9. Noise 16-bit option

Code	Data rate	4,608,000 OSR	Estimate noise (uVrms) vs PGA gain setting 0.2	0.4	0.8
0	576000	8	27948.6	13974.3	6987.2
1	384000	12	7551.9	3775.9	1888.0
2	288000	16	2998.6	1499.3	749.7
3	192000	24	867.1	433.6	216.9
4	144000	32	445.9	223.0	111.7
5	96000	48	313.0	156.6	78.4
6	72000	64	296.8	148.4	74.3
7	48000	96	288.6	144.3	72.2
8	36000	128	285.3	142.7	71.4
9	24000	192	282.0	141.0	70.5
10	18000	256	280.3	140.2	70.1
11	12000	384	278.7	139.3	69.7
12	9000	512	277.8	138.9	69.5
13	4500	1024	276.6	138.3	69.1
14	2250	2048	275.9	138.0	69.0
15	1125	4096	275.6	137.8	68.9
16	600	7680	275.5	137.7	68.9
17	450	10240	275.4	137.7	68.9
18	300	15360	275.4	137.7	68.8
19	200	23040	275.4	137.7	68.8

Table 9. Noise 16-bit option*...continued*

Code	Data rate	4,608,000 OSR	Estimate noise (uVrms) vs PGA gain setting 0.2	0.4	0.8
20	100	46080	275.3	137.7	68.8
21	60	76800	275.3	137.7	68.8
22	50	92160	275.3	137.7	68.8
23	30	153600	275.3	137.7	68.8
24	25	184320	275.3	137.7	68.8
25	20	230400	275.3	137.7	68.8
26	10	460800	275.3	137.7	68.8
27	5	921600	275.3	137.7	68.8
28	2.5	1843200	275.3	137.7	68.8

7.3.5.7.4 ENOB 16-bit option

Table 10. ENOB 16-bit option

Code	Data rate	4,608,000 OSR	Estimate ENOB vs PGA gain setting 0.2	0.4	0.8
0	576000	8	10.8	10.8	10.8
1	384000	12	12.7	12.7	12.7
2	288000	16	14.0	14.0	14.0
3	192000	24	15.8	15.8	15.8
4	144000	32	16.0	16.0	16.0
5	96000	48	16.0	16.0	16.0
6	72000	64	16.0	16.0	16.0
7	48000	96	16.0	16.0	16.0
8	36000	128	16.0	16.0	16.0
9	24000	192	16.0	16.0	16.0
10	18000	256	16.0	16.0	16.0
11	12000	384	16.0	16.0	16.0
12	9000	512	16.0	16.0	16.0
13	4500	1024	16.0	16.0	16.0
14	2250	2048	16.0	16.0	16.0
15	1125	4096	16.0	16.0	16.0
16	600	7680	16.0	16.0	16.0
17	450	10240	16.0	16.0	16.0
18	300	15360	16.0	16.0	16.0
19	200	23040	16.0	16.0	16.0
20	100	46080	16.0	16.0	16.0
21	60	76800	16.0	16.0	16.0

Table 10. ENOB 16-bit option*...continued*

Code	Data rate	4,608,000	Estimate ENOB vs PGA gain setting		
		OSR	0.2	0.4	0.8
22	50	92160	16.0	16.0	16.0
23	30	153600	16.0	16.0	16.0
24	25	184320	16.0	16.0	16.0
25	20	230400	16.0	16.0	16.0
26	10	460800	16.0	16.0	16.0
27	5	921600	16.0	16.0	16.0
28	2.5	1843200	16.0	16.0	16.0

7.3.6 Gain and offset calibration

All NAFE family products include 46 user-accessible calibration coefficient registers divided into three groups:

- **Gain:** GAIN_COEF0[23:0] to GAIN_COEF15[23:0]
- **Offset:** OFFSET_COEF0[23:0] to OFFSET_COEF15[23:0]
- **Optional:** OPTC_COEF0[23:0] to OPTC_COEF13[23:0]

To reduce the calibration error, the bit-width of gain, offset, and self-calibration coefficient registers are 24-bit wide, the same as main ADC.

The above user-calibration coefficients can be read and written by the user. During device power up or reset, the factory calibrated coefficients stored in NVM are loaded into the preset registers, if available. The user may overwrite with different calibration coefficients as needed.

In general, there are three categories of calibration coefficients:

- System offset and gain calibration coefficients for voltage or current input
- System offset and gain calibration coefficients for resistance and RTD input
- Self-calibration values
  - 2.5 V VREF
  - 2.3 V REFH and 0.2 V REFL

These features enable accurate dynamic self-calibration without external voltage sources and advanced predictive maintenance.

Table 11 describes the calibration gain/offset coefficient pair, addressable by coefficient pointer CH_CONFIG1.CH_CAL_GAIN_OFFSET.

Note: *The gain and offset coefficients are channel-gain setting dependent.*

Table 11. System gain and offset calibration registers

Pointer	Gain register	ADDR \h	Offset register	ADDR \h	NVM stored coefficient and setting
0	GAIN_COEF0[23:0]	80	OFFSET_COEF0[23:0]	90	Gain = 0.2 V/V, single-ended AIxx-AICOM
1	GAIN_COEF1[23:0]	81	OFFSET_COEF1[23:0]	91	Gain = 0.4 V/V, single-ended AIxx-AICOM
2	GAIN_COEF2[23:0]	82	OFFSET_COEF2[23:0]	92	Gain = 0.8 V/V, single-ended AIxx-AICOM
3	GAIN_COEF3[23:0]	83	OFFSET_COEF3[23:0]	93	-
4	GAIN_COEF4[23:0]	84	OFFSET_COEF4[23:0]	94	-
5	GAIN_COEF5[23:0]	85	OFFSET_COEF5[23:0]	95	-

Table 11. System gain and offset calibration registers...*continued*

Pointer	Gain register	ADDR \h	Offset register	ADDR \h	NVM stored coefficient and setting
6	GAIN_COEF6[23:0]	86	OFFSET_COEF6[23:0]	96	-
7	GAIN_COEF7[23:0]	87	OFFSET_COEF7[23:0]	97	-
8	GAIN_COEF8[23:0]	88	OFFSET_COEF8[23:0]	98	-
9	GAIN_COEF9[23:0]	89	OFFSET_COEF9[23:0]	99	-
10	GAIN_COEF10[23:0]	8A	OFFSET_COEF10[23:0]	9A	-
11	GAIN_COEF11[23:0]	8B	OFFSET_COEF11[23:0]	9B	-
12	GAIN_COEF12[23:0]	8C	OFFSET_COEF12[23:0]	9C	-
13	GAIN_COEF13[23:0]	8D	OFFSET_COEF13[23:0]	9D	-
14	GAIN_COEF14[23:0]	8E	OFFSET_COEF14[23:0]	9E	-
15	GAIN_COEF15[23:0]	8F	OFFSET_COEF15[23:0]	9F	-

Table 12. Optional calibration registers

CAL REGISTER	NVM stored parameter	Nominal value	Stored format	Setting description
OPT_COEF0[23:0]	VREFP_ADC	2.496 V	(VREF/5)*2^24	REFP_ADC -REFN_ADC pin voltage
OPT_COEF1[23:0]	REFH - GND	2.29632 V	(REFH/5)*2^24	gain = 0.2 V/V, TCC_OFF = 1, CH_CHOP = 1, Factory CAL.
OPT_COEF2[23:0]	REFL - GND	0.19968 V	(REFL/5)*2^24	gain = 0.8 V/V, TCC_OFF = 1, CH_CHOP = 1, Factory CAL.
OPT_COEF3[23:0]	-			
OPT_COEF4[23:0]	-			
OPT_COEF5[23:0]	-			
OPT_COEF6[23:0]	-			
OPT_COEF7[23:0]	-			
OPT_COEF8[23:0]	-			
OPT_COEF9[23:0]	-			
OPT_COEF10[23:0]	-			
OPT_COEF11[23:0]	-			
OPT_COEF12[23:0]	-			
OPT_COEF13[23:0]	-			

Note: *Units used in nominal value: voltage (V), gain (V/V), offset (V)*

7.3.6.1 Gain and offset calibration coefficients

NAFE71388 product family includes 16 pairs of offset and gain calibration registers and internal adder and multiplier for offset and gain compensation.

Offset calibration registers are 24-bit wide. Their values are in two's complement format with a minimum negative value equal to 80_0000\h and a maximum positive value equal to 7F_FFFF\h. A register value of 00_0000\h has no offset correction.

$$Offset = \left(\frac{10}{2^{24}}\right) \cdot \frac{1}{GAIN} \cdot \left(mod\left(hex2dec\left(COEF\right) + 2^{23},\ 2^{24}\right) - 2^{23}\right)$$

Gain calibration registers are 24-bit wide. Their values are straight binary format. The registers map a gain range from 0 to 3.99999976158142. The unity gain value is 40_0000\h. Table 13 shows the full range of gain factor correction.

$$Gain = \frac{COEF}{2^{22}}$$

The NAFE output equation with internal digital calibration is as follows:

$$AFE_{OUT} = (ADCOUT + CAL\_OFFSET) \cdot CAL\_GAIN$$

Table 13. Gain calibration coefficient and factor

Gain calibration coefficient (Hexadecimal)	Gain calibration coefficient (Decimal)	Gain calibration factor = Gain_coeff./(2^22)
FFFFFF	16777215	3.9999998
800000	8388608	2.0000000
400001	4194305	1.0000002
400000	4194304	1.0000000
3FFFFF	4194303	0.9999998
200000	2097152	0.5000000
000000	0	0.0000000

Table 14. Offset calibration coefficient and factor

Offset calibration coefficient (Hexadecimal)	Offset calibration coefficient (Decimal)	Offset calibration PGA = 0.2 (V)
7FFFFF	8388607	24.9999970
400000	4194304	12.5000000
000001	1	0.0000030
000000	0	0.0000000
FFFFFF	-1	-0.0000030
C00000	-4194304	-12.5000000
800000	-8388608	-25.0000000

7.3.6.2 Factory calibrated coefficients

Some NAFE71388 products come with a factory calibration option that is supplemented with factory digitally calibrated coefficients (CAL) stored in the internal NVM register. The calibrated gain/offset coefficient pairs are accessible through the calibration registers, GAIN_COEF0[23:0].. GAIN_COEF 15[23:0] and OFFSET_COEF0[23:0]..OFFSET_COEF15[23:0]. At the power up, the calibrated coefficients are uploaded from the NVM to the user-calibration coefficients registers.

Note: *The coefficients stored in NVM are loaded into their respective registers every time upon power up, reset or CMD_RELOAD.*

As the registers for gain (GAIN_COEFi[23:0]) and offset (OFFSET_COEFi[23:0]) coefficient pairs are read/write accessible, the user may shuffle the location of the calibrated coefficient pairs as necessary.

Note: *There is only one register, CH_CONFIG1.CH_CAL_GAIN_OFFSET[3:0], to address the calibrated coefficient pair to be used for each channel setup.*

The gain and offset coefficient pair is programmed to use one of the 16 gain/offset registers with the same index or the address with matching 4-bit in the lowest nibble. That is, GAIN_COEF0(at 0x80) is to be paired with OFFSET_COEF0(at 0x90). Similarly

GAIN_COEF1(at 0x81) is paired with OFFSET_COEF1(at 0x91), and GAIN_COEF15(at 0x8F) is paired with OFFSET_COEF15(at 0x9F).

7.3.6.3 Loading and use

Upon chip power up, the factory calibration coefficients are uploaded from NVM to user-calibration coefficient registers GAIN_COEF*i*[23:0], OFFSET_COEF*i*[23:0], OPTC_COEF*i*[23:0]. When CHIP_READY bit in SYS_STATUS0 register is asserted to 1, that indicates the chip is ready to perform conversion.

For ADC conversion on the logical channel (default is channel 0, CH0), a pair of offset and gain coefficients is mated with each logical channel by register CH_CONFIG1.CH_CAL_GAIN_OFFSET[3:0]. Before the conversion takes place, the value in the designated pair of offset and gain coefficient will be latched into the internal registers to be used for compensating internal gain and offset errors. The user may shuffle GAIN_COEF and OFFSET_COEF when setting up the logical channel after initialization or power up. For example, setting channel CH0 to gain = 0.8 V/V, the user will need to set GAIN_COEF0[23:0] and OFFSET_COEF0[23:0] with the calibrated coefficient to gain = 0.8 V/V and so forth. See Table 11 for the stored location of each gain-dependent coefficients.

The selected channel for read/write register configuration is indicated by using the pointer position. The position is displayed in bit CONFIG_CH_PTR[3:0]. Similarly, the active ADC conversion on channel-pointer position is shown in bit ADC_CONV_CH[3:0]

SPI command CMD_RELOAD will reload the factory calibrated coefficients from internal non-volatile memory into registers GAIN_COEF, OFFSET_COEF and SELF_CAL_COEF. This will overwrite previously modified values. When CMD_RELOAD is issued, the status bit SYS_STATUS0.CHIP_READY will be deasserted. It will then be asserted when NVM data reloading is complete.

7.3.7 Temperature coefficient correction

TCC_OFF = 0 enables a temperature coefficient correction that reduces the temperature drift error. Set this bit to 1 to disable the TCC feature for any of the following three situations:

- REF_EXT is used
- The ratiometric measurement is used with internal reference (SYS_CONFIG0.REF_SEL[1:0] = 00h)
- The following input signals are used: REFH (= VREF*0.92), REFL (= VREF*0.08)

7.3.8 Voltage reference

7.3.8.1 Low-drift voltage reference 1

The NAFE71388 integrates a voltage reference with calibrated TCC coefficients to reduce the drift error over temperature. Set register bits TCC_OFF = 0 to apply TCC coefficients for non-ratiometric measurement. If external voltage reference is used as ADC reference, set TCC_OFF = 1.

7.3.8.2 Coarse voltage reference 2

The NAFE71388 includes a second and independent internal coarse voltage reference for diagnostic purpose.

7.3.8.3 Voltage reference selector

The voltage reference selector enables the selection of either internal or external reference, or a combination of internal and external reference by setting register bits REF_SEL[1:0]. External 2.5 V voltage reference is applied at REF_EXT pin when required. See Table 29.

7.3.9 Temperature sensor

The NAFE71388 includes a temperature sensor to monitor the IC junction temperature and provides temperature alarm with user-programmable threshold. Overtemperature warning and shutdown factory defaults are 145 ℃ and 165 ℃, respectively.

7.3.10 General-purpose input/output

The NAFE71388 includes ten GPIOs. The operating input and output voltage ranges are 0 V to VDD when pins GPIO0..9 are configured as GPIO.

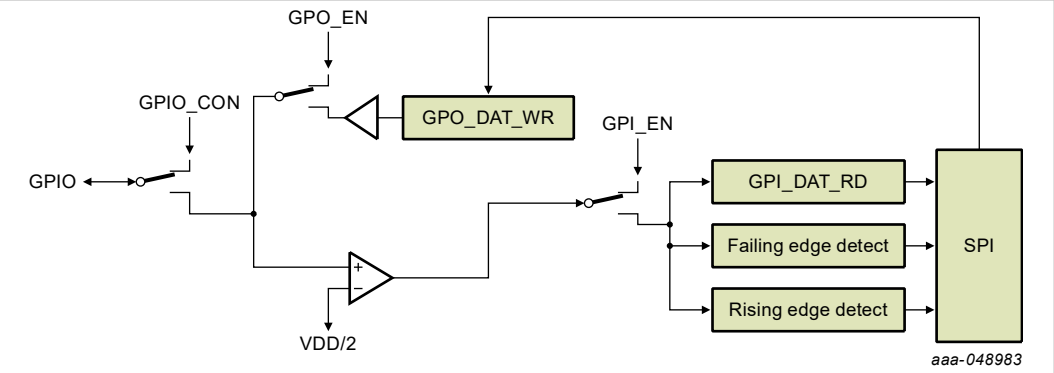


Figure 11. General-purpose input/output

The GPIO control and data registers are organized in the following registers, right-aligned in 16-bit space:

GPI_DATA (0x29\h): Read (R) only register. It detects input logic level signal at the corresponding pin.

GPIO_CONFIG0 (0x2A\h): Read/Write (R/W) GPO_EN register. It enables an output path.

GPIO_ CONFIG1(0x2B\h): R/W GPIO_CON register. It connects the internal circuitry to GPIO pins for either out or input function as programmed by user.

GPIO_CONFIG2 (0x2C\h): R/W GPI_ENABLE. It enables the input path to allow reading data from PAD, looping back from GPO_DATA register and/or GPIO edges detection.

GPIO double edge detection (low-to-high and high-to-low) results in 2x10-bit register GPI_EDGE_POS(0x2D) for positive and GPI_EDGE_NEG(0x2E) for negative, respectively, are implemented as follows.

While GPIO_CONFIG2.GPI_ENABLE[i] and GPIO_CONFIG1.GPIO_CON[i] = 1, any transition from 0 -> 1 (positive edge) or 1 -> 0 (negative edge) the edge detection register is set to 1. These edge detection registers, GPI_POS_EDGE and GPI_NEG_EDGE, are defined as a sticky by nature and requires the host to clear it by writing 1 to the bit that is set to 1 (W1C) by the previous event.

Some GPIOs, such as GPIO0, GPIO1, GPIO2, and GPIO9 serve dual functions.

The GPIO0 and GPIO1, in addition to general-purpose digital input and output function, serve as differential analog input GPIO0-GPIO1 by selecting the appropriate input in LVMUXIN multiplexer. The input common voltage range is from 0.5 V to 2.5 V.

The GPIO9 can output the system clock for synchronization by writing '1' to SYS_CONFIG0.MCLK_OUT_ENABLE.

GPIO2 can provide CRC_ERROR status flag by writing '1' to SYS_CONFIG0.CRC_EN.

7.3.11 Clock sources

The NAFE71388 provides flexible and configurable clocking modes. It can function with three different clock sources: internal RC oscillator, oscillator with external crystal, external oscillator.

Figure 12 shows the clock architecture.

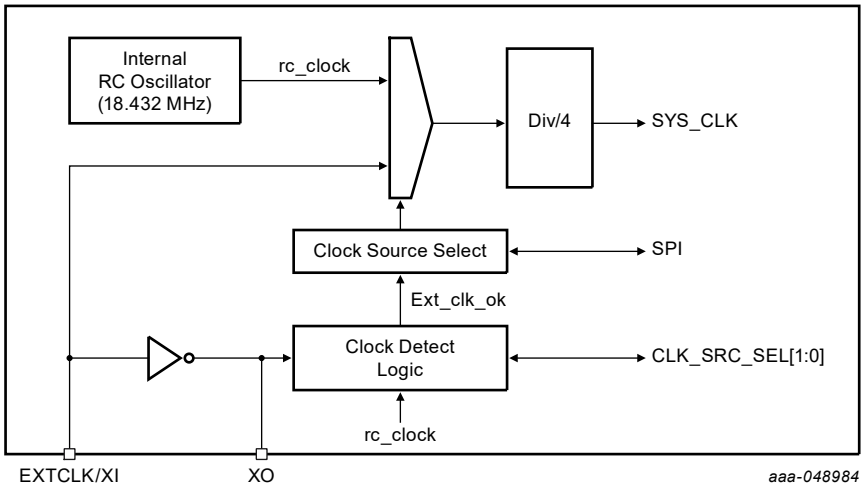


Figure 12. Clock architecture

7.3.11.1 Internal RC oscillator

The NAFE71388 integrates an internal oscillator to allow autonomous and cost-effective operation without support of any external clock source.

The internal oscillator nominal frequency is 18.432 MHz.

7.3.11.2 Oscillator with external crystal

The oscillator with external crystal enables all the applications that require more accurate and stable clock frequency.

The 18.432 MHz external crystal is installed between pins EXTCLK/XI and XO with the appropriate loading caps.

7.3.11.3 External oscillator

The NAFE71388 can operate with an external oscillator. Operating in this manner enables applications that require synchronization between the NAFE71388 and the host, as well as coherent sampling of the input signal.

The external oscillator should be applied to pin EXTCLK/XI.

7.3.11.4 Clock selection

The NAFE71388 provides two mechanisms for system clock source selection:

- Auto-selection upon power on
- User selection via system register configuration

7.3.11.5 Auto-selection of clock source

The automatic clock selection detects the presence of either the crystal oscillator or an external clock pulse upon power up and switches over to the available clock source.

The first phase detects if the clock is present at XI pin, by expecting at least 256 clock pulses within a 0.5 ms window. If the first detection phase is true, then the second detection is skipped and the logic sets the SRC_SEL[1:0] to 2’b10. Detection is complete at this point with the external clock used as the system clock.

When the first phase detection is not true, the second phase is set to detect if the crystal is installed. The logic looks for at least 256 clock pulses within a 15.5 ms window. If the second phase detection is true, the logic sets the SRC_SEL[1:0] to 2'b11. Detection is complete at this point with the external crystal set as the system clock.

If both phases of detection are not true, the SRC_SEL [1:0] is not updated. It remains at the default 2’b00, which implies the internal clock is used. Then, CLK_DET_DONE is asserted 1 when both phases are complete. After CLK_DET_DONE = 1, the internal digital CHIP_RDY is asserted to 1.

7.3.11.6 User selection of clock sources

The user selection option allows the user to select the desired clock after power on. The clock source can be selected by writing to the clock source system configuration register.

Check the presence of the external clock while making external clock selection in system configuration register to ensure proper functioning of the NAFE71388. If the external clock is detected and the NAFE71388 switches to the external clock, the system status register is updated accordingly. If the external clock is not detected, the NAFE71388 maintains the previous clock configuration.

7.3.11.7 Clock period drift detection

Whenever SRC_SEL[1:0] is set to 2’b11 or 2’b10 by the user or by the auto-detect logic, one-time switch over at power-on reset (POR), the clock period monitoring circuit is activated to continuously measure the clock period difference between the external clock and internal RC Oscillator.

The typical value of clock period difference is set to 20 % at POR. The clock comparison logic issues an alarm when the running average clock count difference is greater than 20 %. The internal oscillator clock is the main reference. The alarm status bit for clock variation is user accessible via SPI register. The average time window is ~64 ms. If external clock is selected to be used as the system clock source and while EXTCLK_FREQ_ALRM bit is enabled, the external clock alarm interrupt triggers (EXTCLK_FREQ_INT = 1) whenever the EXTCLK is over the 20 % period difference.

7.4 Channel configuration and multichannel sequencer

7.4.1 Channel configuration

The NAFE71388 has eight HV configurable analog inputs, LV diagnostic signals, and on-chip scaled reference voltages for built-in self-test (BIST), self-calibration. Coupling the various inputs with channel-based ADC configurations allows a highly flexible analog input configurations. With the channel-based configurations, the user may switch among the configured channels seamlessly, and without the need to perform multiple SPI transactions to set up various configurations before each ADC conversion. The 16 configurable logical channels are all independent and the associated registers. Figure 13 shows structure of one logic channel:

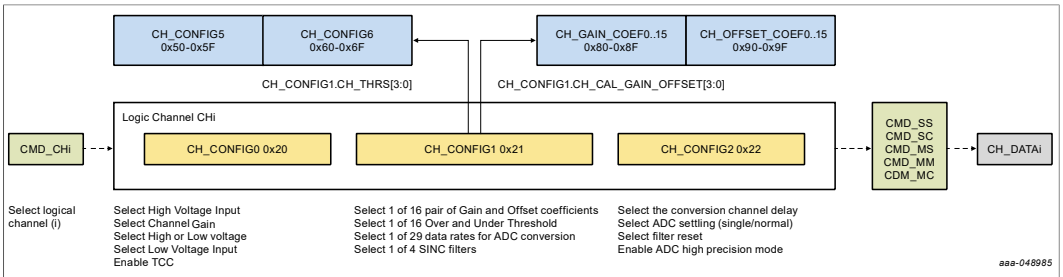


Figure 13. Logical channel structure

- Channel configuration registers: CH_CONFIG0, CH_CONFIG1, and CH_CONFIG2.
  - CH_CONFIG0 (0x20\h)
    - Select input channel, either high voltage (HV_AIP/HV_AIN, HV_SEL=1) or low voltage (LVSIG_IN[2:0], HV_SEL = 0).
    - Select one of the eight channel gains if high-voltage input is selected.
    - Disable/enabled the channel temperature coefficients correction (TCC_OFF = 1).
  - CH_CONFIG1 (0x21\h)
    - Set the pointer (CH_CAL_GAIN_OFFSET[3:0]) to select one of the 16 calibrated gain and offset coefficient pairs in the calibrated channel coefficient registers: GAIN_COEF0…15 and OFFSET_COEF0…15.
    - Set the pointer (CH_THRS[3:0]) to select one of the 16 channel over- and under-range threshold pairs: CH_CONFIG5.OVR_THRS0…15 and CH_CONFIG6.UDR_THRS0…15.
    - Select one of 29 possible data rates: ADC_DATA_RATE[4:0].
    - Select one of the five possible filter options for second-stage SINC filter: ADC_SINC[2:0].
  - CH_CONFIG2 (0x22\h)
    - Select one of the 64 possible preset channel delays before ADC start conversion: CH_DELAY[5:0].
    - Select ADC Settling mode, single-cycle, or normal: ADC_NORMAL_ SETTLING.
    - Select to reset ADC digital filters at the start of every ADC conversion: ADC_FILTER_RESET.

  - Select to enable input channel level chopping with two ADC conversions (Precision mode): CH_CHOP = 1.
- Channel gain coefficients: GAIN_COEF0..15 [23:0] (0x80 – 0x8F)
  - These 16 24-bit calibrated gain coefficients are used to correct the gain error for the selected logic channel. The uncalibrated default is equivalent to 1 V/V.
- Channel offset coefficients: OFFSET_COEF0..15[23:0] (0x90 – 0x9F)
  - These 16 24-bit calibrated offset coefficients are used to correct the offset error for the selected logic channel. The uncalibrated default offset value is 0 V.
- Channel input range detect threshold
  - CH_CONFIG5 (0x50..0x5F): Over-range 24-bit threshold setting
    These 16 24-bit registers are used to set the over-range threshold values.
  - CH_CONFIG6 (0x60..0x6F): Under-range 24-bit threshold setting
    These 16 24-bit registers are used to set the under-range threshold values.
- Channel output data
  - CH_DATA*i*[23:0]: Holds ADC converted output data as selected by CMD_CHi. CH0 data is address 0x40 and CH15 data address is 0x4F.
- Channel status
  - CH_STATUS0[*i*]: Over-range status bit. CH0 status is in bit[0] and CH15 is in bit[15].
  - CH_STATUS1[*i*] - Under-range status bit. CH0 status is in bit[0] and CH15 is in bit[15].

Upon startup, chip reset, and register clear, each of the logical channels is to be reconfigured once. Channel gain/offset coefficients are preloaded from the on-chip NVM after POR. The user could overwrite these coefficients after the POR.

Channel select, CMD_CHi :

- SPI command CMD_CHi is used to select the logic channel CHi, and the CH_DATAi, where i = 0..15 is the channel index.
- Channel configuration is activated after the conversion command is issued.
- The activated logical channel is indicated by reading CONFIG_CH_PTR[3:0] in SYS_STATUS0 register.

For single-channel conversion, the host will issue (CMD_SS, CMD_SC), then wait for DRDY signal asserted high where ADC data is ready for the host to read. Figure 14 shows a typical sequence before CMD_SS or CMD_SC is issued.

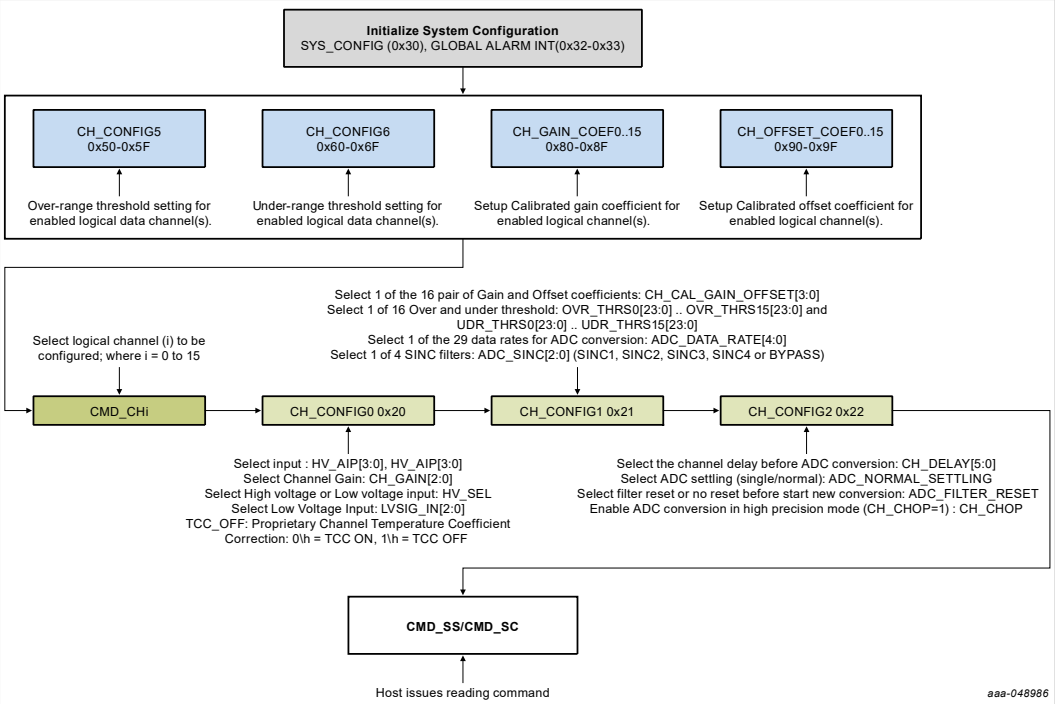


Figure 14. Steps to setup for single-channel conversion reading

Example code sequence

```
For example, setup a single conversion using CMD_SS command with the
 following setup and the conversion result will be stored at CH_DATA5.
Example how to select, config, enable, run, read data.
hv_aip = 1; // 4-bit
hv_ain = 1; // 4-bit
hvlv_sel = 1;
CH_GAIN = 0; // 0.2; // 3-bit
AI1P = 10.35 V;
AI1N = -10.72 V;
ADC_SINGLE_NORMAL = 0; // Single cycle settling
ADC_DATA_RATE = 2;
CH_CAL_GAIN_OFFSET = 0; // 4-bit pointer points to GAIN_COEF0 &
 OFFSET_COEF0
CH_THRS = 0; // 4-bit pointer points to OVR_THRS0 & UDR_THRS0
ADC_SINC = 0; // 3-bit, SINC4 bypass stage 2
ADC_FILTER_RESET = 1; // filter reset at start of ADC conversion
CH_CHOP = 0; // disable precision mode
CONV_DELAY = 1;
write_cmd_ch(5) ; // CMD_WR_POINTER5 - set conversion pointer to 5
write_reg16("CH_CONFIG0", { hv_aip, hv_ain, CH_GAIN,
 hvlv_sel,4'b0000}); // TCC is enabled
write_reg16("CH_CONFIG1", {CH_CAL_GAIN_OFFSET, CH_THRS, ADC_DATA_RATE,
 ADC_SINC} );
write_reg16("CH_CONFIG2", {CONV_DELAY, ADC_SINGLE_NORMAL,
 ADC_FILTER_RESET ,CH_CHOP,7'b000_0000});
write_cmd_ss()  ; // CMD_SS - issue single ADC conversion command
wait_rise_edge (DRDY);
CH_DATA5 = read_reg24("CH_DATA5"); // read the conversion data at
 logical channel 5
```

7.4.2 Working with multichannel sequencer

The sequencer will step through CH0 to CH15 (or current channel to CH15) to execute the enabled channels (CH_CONFIG4.MCH_EN[15:0]) and store ADC output in the corresponding ADC_DATA output register (CH_DATA0..CH_DATA15).

ADC conversion can be set either to Single-Cycle Settling mode or Normal Settling mode with CH_CONFIG4.ADC_SINGLE_NORMAL = 0 or 1, respectively. However, single-cycle settling is typically preferable in many applications.

When CMD_MM or CMD_MC command is issued, the sequencer will begin ADC conversions on the enabled channels and stop upon completing the conversion of the last enabled channel. At the end of the Sequencer mode, SYS_STATUS0.ADC_CONV_CH[3:0] is set to CH0. The DRDY pin will transition from 0 to 1 when ADC_DATA is ready for the host to read. The register SYS_STATUS0.ADC_CONV_CH[3:0] can be used for tracking the current ADC channel. ADC busy status is indicated in either status bit SYS_STATUS0.SINGLE_CH_ACTIVE or SYS_STATUS0.MULTI_CH_ACTIVE.

See Section 7.5.9, Section 7.5.10, Section 7.5.11 in modes (MM, MC, MS) for the expected behavior of the sequencer with the use of SYNC pulse and reading command as triggers.

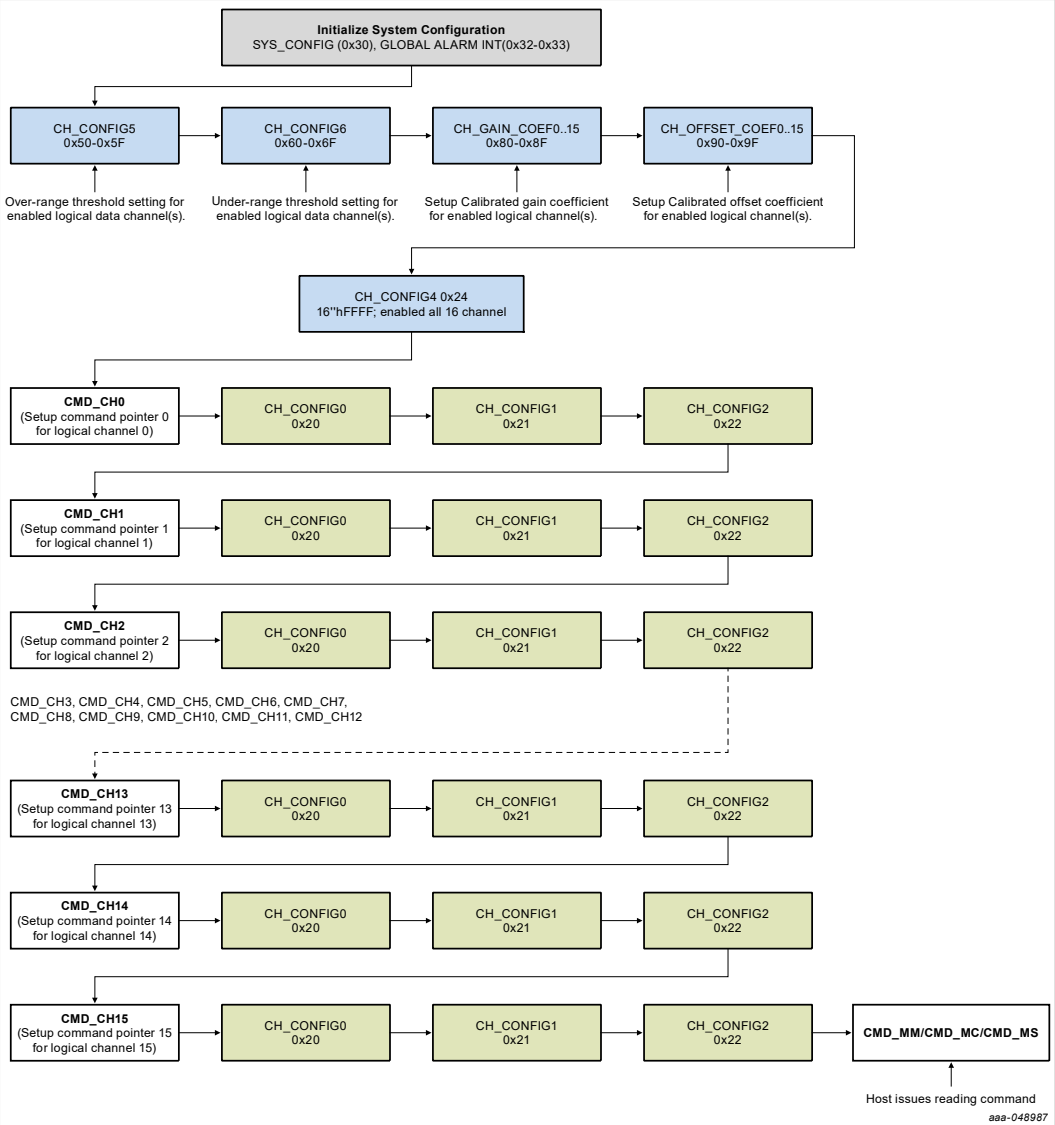


Figure 15. Steps to setup for multichannel conversion reading

7.4.2.1 Channel enable

CH_CONFIG4[15:0] = MCH_EN[15:0] is an index-based channel enable bit for ADC conversion for multichannel reading. If MCH_EN = 0xFFFF, all 16 channels are enabled in multichannel sequencer conversions.

When single-conversion, single-reading (CMD_SS) or single-conversion continuous-reading (CMD_SC) is used, channel enable CH_CONFIG4[15:0] is ignored. This register is only used in multichannel reading, sequencer conversions. MCH_EN = 0xFFFF, all 16 channels are enabled in multichannel sequencer conversions.

7.4.2.2 On-the-fly channel configuration

Any of the 16 logical channels are configurable on-the-fly and could be modified while the sequencer is **running**.

Note: *Any register setting changes on ADC active channel (SINGLE_CH_ACTIVE or MULTI_CH_ACTIVE) will not be taken into effect until next ADC conversion command CMD_ is issued.*

7.5 ADC Conversion and Reading modes

The NAFE71388 reading process starts when a start event is received, and finishes with an event that signals the completion of reading. The reading process includes four main steps:

1. Reading start event received.
2. Wait a period equal to the configured programmable delay.
3. Execute one or more analog-to-digital conversions.
4. Send the DRDY signal when the reading process is complete.

7.5.1 Reading start event

The NAFE71388 provides two types of reading start event to fit simplicity and performance.

One reading event is command based. It is intrinsic in the SPI command transaction. The other is triggered through SYNC pin.

The SPI reading process starts on the last falling edge of the SPI command clock. The SYNC reading process begins on the rising edge of the SYNC pulse at the SYNC pin.

7.5.2 Reading process stop event

The reading process can be stopped by the host issuing either SPI commands or a SYNC pulse. This command is useful if the host wants to stop an infinite reading process executed autonomously by the NAFE71388.

The SPI commands to stop reading in progress are CMD_ABORT or CMD_END.

7.5.2.1 CMD_ABORT

While the NAFE reading period is active and the ADC is converting, if a CMD_ABORT command is received, the ongoing conversion is aborted, and the device returns to its initial waiting state. The corresponding CH_DATA register will not be updated.

7.5.2.2 CMD_END

While the NAFE reading period is active and the ADC is converting, if CMD_END is received, ADC conversion is allowed to complete (contrary to CMD_ABORT) and CH_DATA register is updated with new results before device returns to its initial waiting state.

7.5.3 Reading period

The reading period is defined as the time interval between the reading start event and the reading end event.

If SYS_CONFIG0.ADC_SYNC = 0, the conversion start event is the last falling edge of the SPI command clock. If SYS_CONFIG0.ADC_SYNC = 1, the conversion start event is the rising edge of the SYNC pulse. The reading completion event is the rising edge of the DRDY signal.

The reading period is a function of system clock, reading mode, fixed delay, data rate and programmable delay. Also, the fixed delay is different for the first reading and the readings after first reading.

Reading modes:

- Single-channel single-reading (SCSR)
- Single-channel continuous-reading (SCCR)
- Multichannel single-reading (MCSR)
- Multichannel multireading (MCMR)
- Multichannel continuous reading (MCCR)

The system clock frequency is 9.216 MHz. The period of system (T_sys_clk) is 1/(9.216 MHz) = 108.5 ns with the master clock at 18.432 MHz.

Table 15. Channel programmable delay

	Master clock	**18,432,000**
	System clock	**9,216,000**
Prog delay code	Prog delay (# sysclk)	Programmable delay
0	0	000.000E+0
1	2	217.014E-9
2	4	434.028E-9
3	6	651.042E-9
4	8	868.056E-9
5	10	1.085E-6
6	12	1.302E-6
7	14	1.519E-6
8	16	1.736E-6
9	18	1.953E-6
10	20	2.170E-6
11	28	3.038E-6
12	38	4.123E-6
13	40	4.340E-6
14	42	4.557E-6
15	56	6.076E-6
16	64	6.944E-6
17	**76**	**8.247E-6**
18	90	9.766E-6
19	128	13.889E-6
20	154	16.710E-6
21	178	19.314E-6
22	204	22.135E-6
23	224	24.306E-6

Table 15. Channel programmable delay*...continued*

		Master clock	18,432,000
		System clock	9,216,000
24	256		27.778E-6
25	358		38.845E-6
26	512		55.556E-6
27	716		77.691E-6
28	1024		111.111E-6
29	1664		180.556E-6
30	3276		355.469E-6
31	7680		833.333E-6
32	19200		2.083E-3
33	23040		2.500E-3

7.5.3.1 Calculate the effective reading period

The general reading period formula is:

T_reading = T_fixed + T_prog_delay + T_conv

For all Reading modes, due to internal setup requirements, the fixed delay is always built into the first sample reading time. The subsequent readings are free of this setup time overhead. Because the Single-Reading modes produce only one sample, the effective data rate is 1/(T_conv + T_fixed), if T_prog_delay = 0. Some reading period examples are provided in the Reading mode sections.

7.5.3.2 Fastest reading period in SCCR mode

The fastest reading period is achievable in Single-Channel Continuous-Reading mode with the ADC digital filter set in Normal Settling mode. In particular, after the first reading, it is possible to achieve a data rate up to 576 ksps.

7.5.3.3 Effective output data rate with CH_DELAY

In addition to the programmable date rate provided by the ADC, the NAFE offers further data rate output availability with the combination of ADC conversion period and programmable delay, CH_CONFIG2.CH_DELAY[5:0].

Table 16 shows examples of the most common reading periods.

Table 16. Popular reading periods

System Clock = 9,216,000						
ADC data rate (sps)	ADC conversion period (s)	Fixed delay (# sysclk)	Prog delay (# sysclk)	Prog delay	Actual reading periods (s)	Target reading Time (s)
576000.00	1.736E-6	0	0	000.0E+0	1.7E-6	2.0E-6
576000.00	1.736E-6	0	2	217.0E-9	2.0E-6	2.0E-6
384000.00	2.604E-6	0	4	434.0E-9	3.0E-6	3.0E-6
384000.00	2.604E-6	0	6	651.0E-9	3.3E-6	3.3E-6
288000.00	3.472E-6	0	4	434.0E-9	3.9E-6	4.0E-6

Table 16. Popular reading periods*...continued*

System Clock = 9,216,000						
288000.00	3.472E-6	0	14	1.5E-6	5.0E-6	5.0E-6
192000.00	5.208E-6	0	8	868.1E-9	6.1E-6	6.0E-6
192000.00	5.208E-6	0	12	1.3E-6	6.5E-6	6.7E-6
192000.00	5.208E-6	0	16	1.7E-6	6.9E-6	7.0E-6
144000.00	6.944E-6	0	10	1.1E-6	8.0E-6	8.0E-6
144000.00	6.944E-6	0	18	2.0E-6	8.9E-6	9.0E-6
144000.00	6.944E-6	0	28	3.0E-6	10.0E-6	10.0E-6
96000.00	10.417E-6	0	20	2.2E-6	12.6E-6	12.5E-6
96000.00	10.417E-6	0	42	4.6E-6	15.0E-6	15.0E-6
72000.00	13.889E-6	0	56	6.1E-6	20.0E-6	20.0E-6
48000.00	20.833E-6	0	38	4.1E-6	25.0E-6	25.0E-6
36000.00	27.778E-6	0	20	2.2E-6	29.9E-6	30.0E-6
36000.00	27.778E-6	0	90	9.8E-6	37.5E-6	37.5E-6
36000.00	27.778E-6	0	204	22.1E-6	49.9E-6	50.0E-6
24000.00	41.667E-6	0	76	8.2E-6	49.9E-6	50.0E-6
18000.00	55.556E-6	0	40	4.3E-6	59.9E-6	60.0E-6
18000.00	55.556E-6	0	64	6.9E-6	62.5E-6	62.5E-6
18000.00	55.556E-6	0	178	19.3E-6	74.9E-6	75.0E-6
18000.00	55.556E-6	0	224	24.3E-6	79.9E-6	80.0E-6
12000.00	83.333E-6	0	154	16.7E-6	100.0E-6	100.0E-6
9000.00	111.111E-6	0	128	13.9E-6	125.0E-6	125.0E-6
9000.00	111.111E-6	0	358	38.8E-6	150.0E-6	150.0E-6
4500.00	222.222E-6	0	256	27.8E-6	250.0E-6	250.0E-6
4500.00	222.222E-6	0	716	77.7E-6	299.9E-6	300.0E-6
2250.00	444.444E-6	0	512	55.6E-6	500.0E-6	500.0E-6
2250.00	444.444E-6	0	1,664	180.6E-6	625.0E-6	625.0E-6
2250.00	444.444E-6	0	3,276	355.5E-6	799.9E-6	800.0E-6
1125.00	888.889E-6	0	1,024	111.1E-6	1.0E-3	1.0E-3
800.00	1.250E-3	0	0	000.0E+0	1.3E-3	1.3E-3
400.00	2.500E-3	0	0	000.0E+0	2.5E-3	2.5E-3
200.00	5.000E-3	0	0	000.0E+0	5.0E-3	5.0E-3
120.00	8.333E-3	0	0	000.0E+0	8.3E-3	8.3E-3
100.00	10.000E-3	0	0	000.0E+0	10.0E-3	10.0E-3
60.00	16.667E-3	0	0	000.0E+0	16.7E-3	16.7E-3
60.00	16.667E-3	0	19,200	2.1E-3	18.8E-3	18.8E-3
50.00	20.000E-3	0	0	000.0E+0	20.0E-3	20.0E-3

Table 16. Popular reading periods*...continued*

System Clock = 9,216,000						
50.00	20.000E-3	0	23,040	2.5E-3	22.5E-3	22.5E-3
40.00	25.000E-3	0	0	000.0E+0	25.0E-3	25.0E-3
30.00	33.333E-3	0	0	000.0E+0	33.3E-3	33.3E-3
20.00	50.000E-3	0	0	000.0E+0	50.0E-3	50.0E-3
15.00	66.667E-3	0	0	000.0E+0	66.7E-3	66.7E-3
15.00	66.667E-3	0	7,680	833.3E-6	67.5E-3	67.5E-3
15.00	66.667E-3	0	0	000.0E+0	66.7E-3	180.0E-3

7.5.4 ADC synchronization

Generally, the NAFE71388 supports four different types of synchronization:

- Synchronize multi NAFE with SYNC pulse at SYNC pin
- Synchronize the NAFE to host for conversion start by SYNC pulse
- Synchronize the host to the NAFE through DRDY signal
- Synchronize the NAFE and the host clock to the same clock, by one of the following methods:
  - Configure the NAFE to use external clock and apply 18.432 MHz clock pulses at EXTCLK/XI pin
  - Configure the NAFE to output its system clock to GPIO9

7.5.4.1 ADC_SYNC bit

When bit SYS_CONFIG0.ADC_SYNC = 1, a detection of the rising edge at the SYNC pin starts a new conversion. If there is an ongoing conversion and the rising edge of the SYNC is received, the ongoing conversion is aborted. Then, a new conversion is restarted. In this case, CMD_xy is used to select the Conversion mode. The conversion start is only triggered by a rising edge at the SYNC pin.

SYNC pulse width should be greater or equal to two system clock periods, 2 x T_sys_clk and SYS_CONFIG0.ADC_SYNC is set to 1.

If bit SYS_CONFIG0.ADC_SYNC = 0, the SYNC pulse is ignored. The conversion start is triggered by the last SPI clock falling edge of SPI conversion commands. In this case, the CMD_xy has two functions:

- Select the Reading mode
- Trigger the conversion start

The conversion start with SYNC pulse is supported in all Reading modes. Table 17 summarizes the Reading mode and start commands.

Table 17. Reading mode and start commands

		Conversion start trigger	
		ADC_SYNC = 0	ADC_SYNC =1
Reading modes	SCSR	CMD_SS	SYNC pin
	SCCR	CMD_SC	SYNC pin
	MCSR	CMD_MS	SYNC pin
	MCMR	CMD_MM	SYNC pin

Table 17. Reading mode and start commands...*continued*

	MCCR	CMD_MC	SYNC pin
Trigger event on CMD_xy is the last SPI command falling edge check			
Trigger event on SYNC pin is the pulse rising edge			

7.5.4.2 Synchronize multi-NAFE with SYNC pulse at SYNC pin

The SYNC pin function enables the synchronization of multiple NAFE71388s connected to the same SYNC signal generated by the host. When the host issues the SYNC pulse, all the connected devices start the conversion on the rising edge of the SYNC pulse.

7.5.4.3 Synchronize the NAFE to the host with SYNC pin

The SYNC input enables the host to control the start conversion of the NAFE. Consequently, this provides a synchronization mechanism driven by the host.

7.5.4.4 Synchronize the host to the NAFE through DRDY signal

DRDY rising edge can be used to synchronize the host with the NAFE71388 data rate output (DRO). This enables the host to estimate the effective DRO and to be synchronized with the device on fetching the data at the correct time. This function is critical for synchronizing the reading time for an infinite reading loop.

7.5.4.5 Synchronize the NAFE and the host to the same clock

The NAFE71388 offers two options to synchronize the NAFE and the host to the same clock:

- Apply an external 18.432 MHz master clock to XI/EXTCLK pin and set SYS_CONFIG0.CK_SRC_SEL[1:0] = 1. This enables coherent measurements and the possibility to synchronize the SPI data fetching using this clock as a timer.
- Use internal 9.216 MHz system clock at GPIO9 pin configuring SYS_CONFIG0.MCLK_OUT_ENABLE = 1 in SYS_CONFIG0 register. This implementation enables synchronization to the NAFE so the host can synchronize the SPI data fetching using this clock as a timer.

7.5.4.6 Reading conversion start - SYNC pulse

If SYS_CONFIG0.ADC_SYNC = 1, a new ADC conversion will start at each rising edge of the SYNC pulse at the pin.

SYNC pulse width should be a minimum of two system clock cycles.

Figure 16 shows an ADC conversion triggered by a pulse at the SYNC pin in Single-Channel Continuous-Reading mode (CMD_SC). The Continuous Reading mode, in combination with SYNC, allows the fastest reading mode, while requiring only one SYNC pulse to collect many or infinite reading samples. In addition, it mitigates the timing requirements for fetching channel data on the SPI bus. The fetching period is close to the reading period for the second reading and beyond.

SYNC pulse triggers the conversion start for all the reading modes.

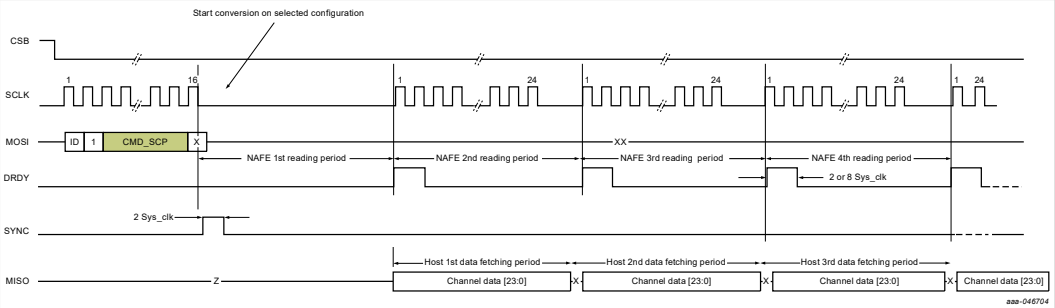


Figure 16. Conversion start

7.5.5 Reading modes

The NAFE71388 provides five reading (conversion) modes:

1. Single-channel single-reading (SCSR) set by the CMD_SS command
2. Single-channel continuous-reading (SCCR) set by the CMD_SC command
3. Multichannel single-reading (MCSR) set by the CMD_MS command
4. Multichannel multireading (MCMR) set by the CMD_MM command
5. Multichannel continuous-reading (MCCR) set by the CMD_MC command

The following sections describe the reading modes in details.

7.5.6 Reading sequence

In general, the ADC follows a five-step sequence to complete a reading (conversion) process. The reading (conversion) process is initiated by either SPI start command or SYNC pulse.

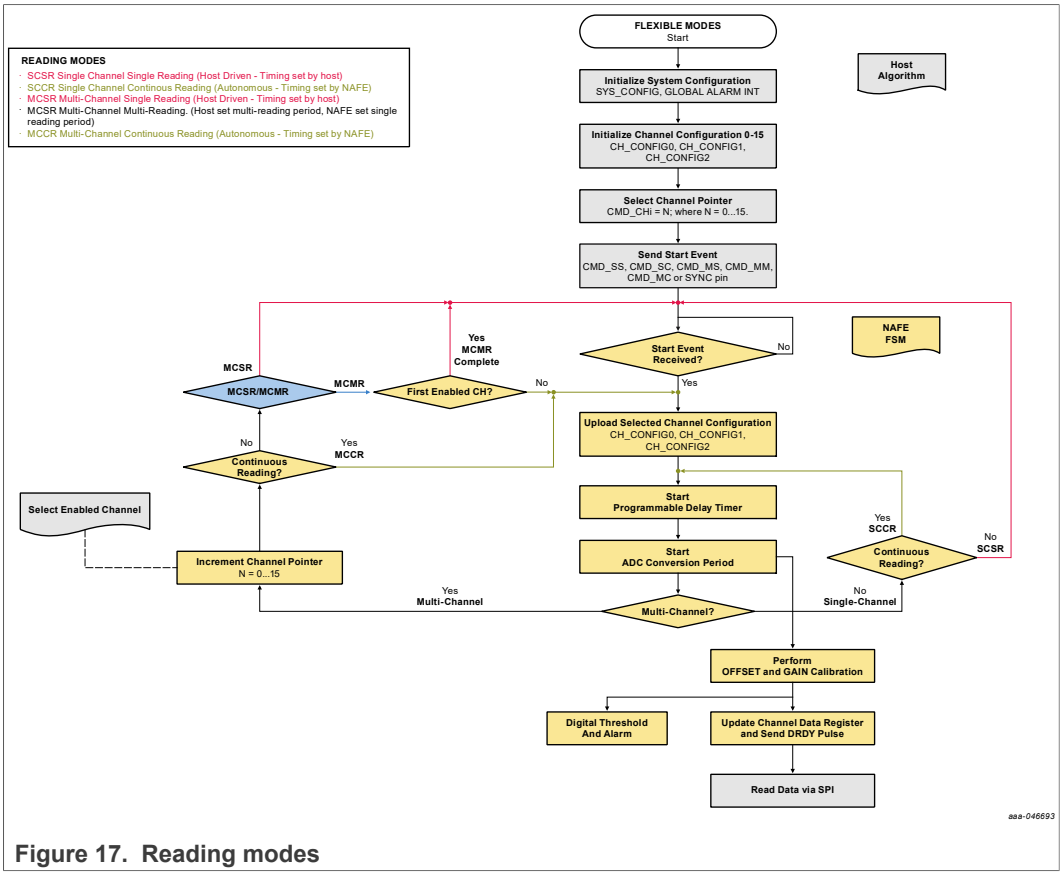


Figure 17. Reading modes

Reading sequence:

1. Idle state. Wait for a start event: SPI start command or SYNC pulse
2. Update the active channel configuration and pointer location (as needed)
3. Wait for the timer of programmable delay to expire
4. Start and complete ADC conversion on the selected channel, check active converting channel pointer with register bits ADC_CONV_CH[3:0]
   a. In Multichannel Reading mode MCSR, MCMR, and MCCR, the active converting channel pointer is automatically incremented to the next enabled channel after the conversion is complete.
5. Loop increment for Continuous-Reading and Multireading modes:
   a. In Single-Reading modes: SCSR and MCSR - ADC returns to Step 1, idle state
   b. In Continuous-Reading modes: SCCR, MCCR – ADC jumps to Step 2 and repeats the sequence until interrupted
   c. In Multireading mode: MCMR – ADC jumps to Step 2 until the reading completion of the last enabled channel defined in CH_CONFIG4.MCH_EN[15:0]. The loop is then broken and ADC returns to Step 1.

In Single-Reading mode SS mode, the host issues the conversion start by sending CMD_SS if SYS_CONFIG0.ADC_SYNC = 0, or the SYNC pulse if SYS_CONFIG0.ADC_SYNC = 1. After the NAFE completes the reading conversion process, it returns to idle and waits for the next instruction command or next SYNC pulse.

In Continuous-Reading SCCR and MCCR modes, the host issues the conversion start by sending CMD_SC, CMD_MC, or the SYNC pulse (when SYS_CONFIG0.ADC_SYNC = 1

is set). After the NAFE completes first reading conversion process, it jumps to Step 2 and continues the reading process forever or until is interrupted.

There are three ways to interrupt an ADC conversion:

1. CMD_END: Stop ADC conversion reading process after the current conversion is completed.
2. CMD_ABORT: Abort the ADC conversion reading process immediately.
3. Conversion start event:
   a. If SYS_CONFIG0.ADC_SYNC = 0, the last falling edge of SPI command restarts a new conversion. A pulse at the SYNC pin is ignored.
   b. If SYS_CONFIG0.ADC_SYNC = 1, a rising edge signal at SYNC pin will trigger ADC a new conversion start.

7.5.7 CMD_SS (single-channel single-reading)

Start Single-Channel Single-Reading (conversion) mode.

If SYS_CONFIG0.ADC_SYNC = 0, the conversion start is triggered by this SPI command at the last SPI clock falling edge. If SYS_CONFIG0.ADC_SYNC = 1, the conversion start is triggered by SYNC rising edge. In both cases, the conversion is executed on the selected channel. After the conversion is complete, the device returns to its waiting state.

Data can be read serially via the MISO pin after the DRDY pin asserts high, or after the reading process is complete.

7.5.7.1 Flow chart - SCSR

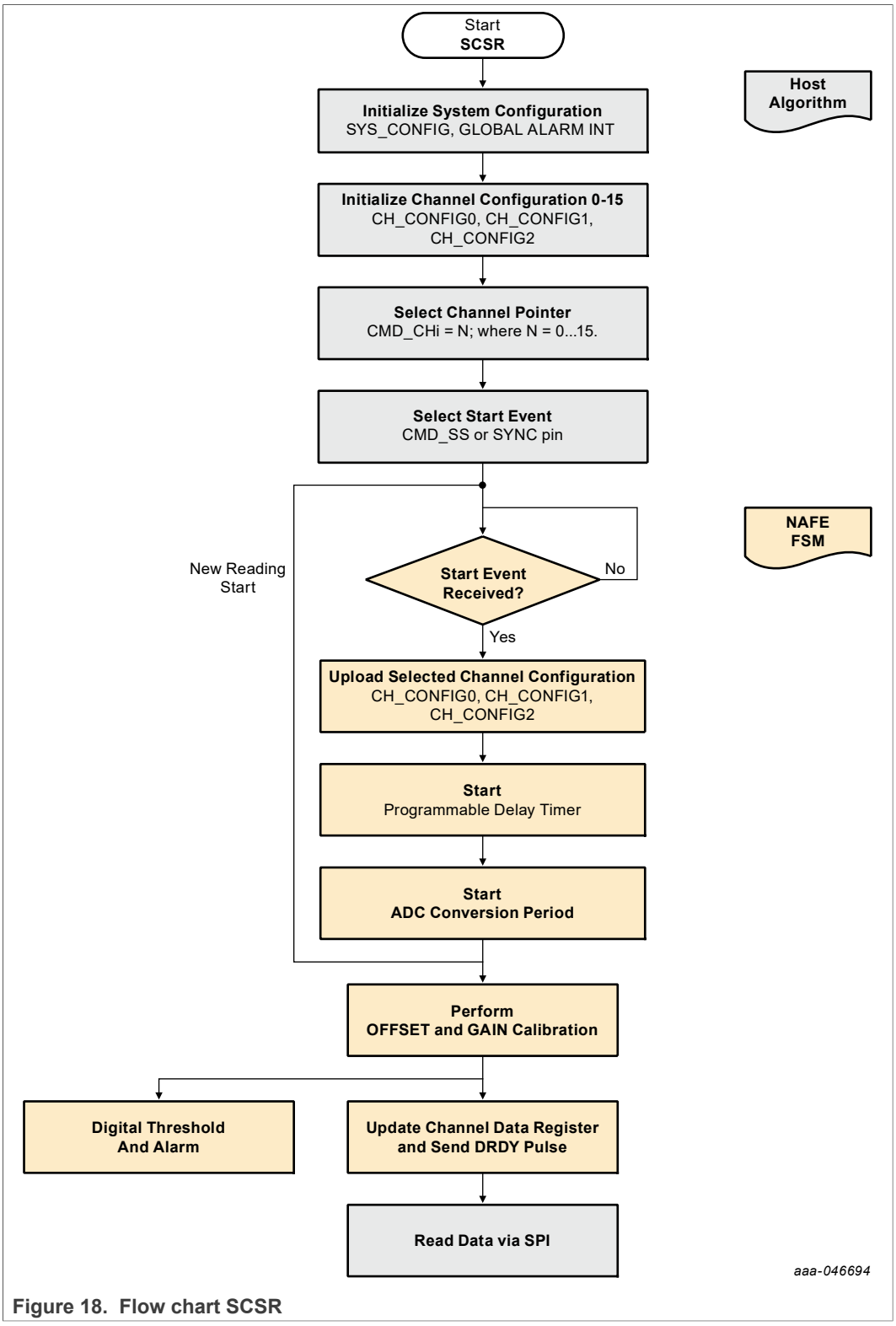


Figure 18. Flow chart SCSR

7.5.7.2 Timing diagram - SCSR

The host can fetch single-channel data after the NAFE reading period by two methods:

- Keep the CSB low after the command was issued. Then wait for DRDY assert high. Data is available at the MISO pin at every rising of SCLK. MSB outputs first.
- Deassert the CSB high, then wait until the DRDY goes high and read the channel data.

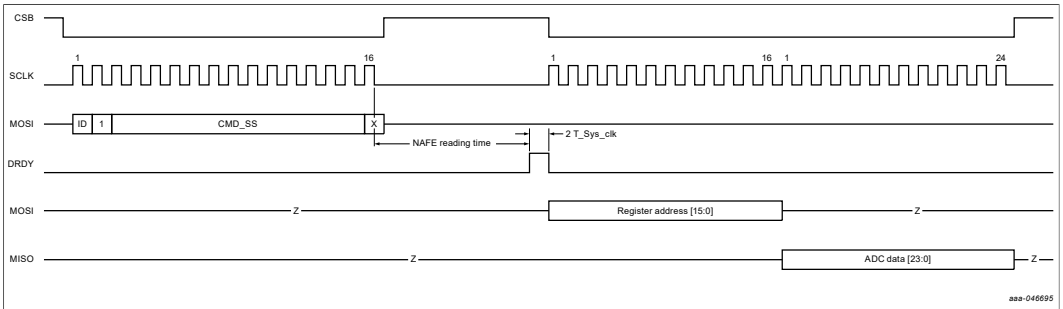


Figure 19. CMD_SS timing diagram with CSB high

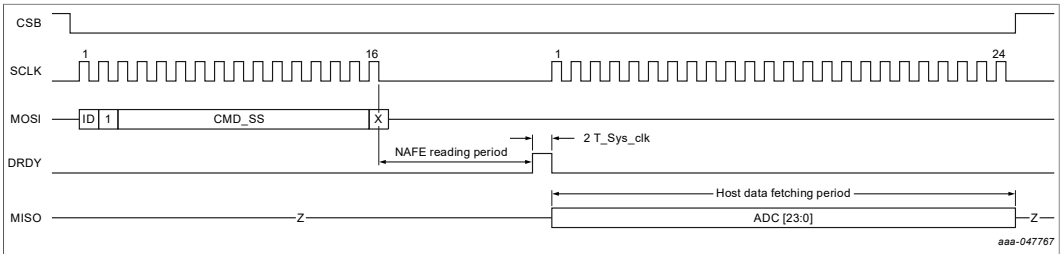


Figure 20. CMD_SS timing diagram with CSB low

7.5.7.3 Code example - SCSR

```
Reg_Read ('SYS_STATUS0) ; to clear INTB
Reg_write ('SYS_CONFIG, sys_config_data); //
Reg_write ('CH_CONFIGi, ch_config_datai); // i = 0…15
Send CMD_CHi;
Send CMD_SS;
Send SYNC Pulse (if SYNC_BIT = 1);
```

7.5.7.4 Reading period for SCSR

SS Reading period: T_reading = T_fixed + T_prog_delay + T_conv

On single reading, T_fixed = (2 × T_sys_clk) ± 1 × T_sys_clk

For example,

Set CH_DELAY[5:0]=17\d; #delay 76 sys_clk

Set ADC_DATA_RATE[4:0] = 5\d; #DRO is 24000 sps

Set ADC_NORMAL_SETTLING = 0\d; #Single-ycle mode

T_sys_clk =1/sys_clk = 1/9216000 = 0.1085 us

T_prog_delay = 76 * T_sys_clk #Table Channel Programmable Delay

T_conv = 1/24000 = 41.67 us #Table Data Rate

Hence,

On single reading, T_reading = 0.1085 us * (2 ± 1 + 76) + 41.67 us = 50.13 ± 0.1085 us.

7.5.8 CMD_SC (single-channel continuous-reading)

Start Single-Channel Continuous-Reading (conversion) mode.

If bit SYS_CONFIG0.ADC_SYNC = 0, the conversion start is triggered by this SPI command at the last clock falling edge.

If bit SYS_CONFIG0.ADC_SYNC = 1, the conversion start is triggered by SYNC rising edge.

In both cases, the conversion is executed on the selected channel until it is interrupted or restarted. The conversion could be interrupted by CMD_ABORT or CMD_END, or could be aborted and restarted by a SYNC pulse if SYS_CONFIG0.ADC_SYNC = 1 or any conversion command if SYS_CONFIG0.ADC_SYNC = 0.

Data can be read serially via the MISO pin after the DRDY pin asserts high or after the reading is completed.

7.5.8.1 Flow chart - SCCR

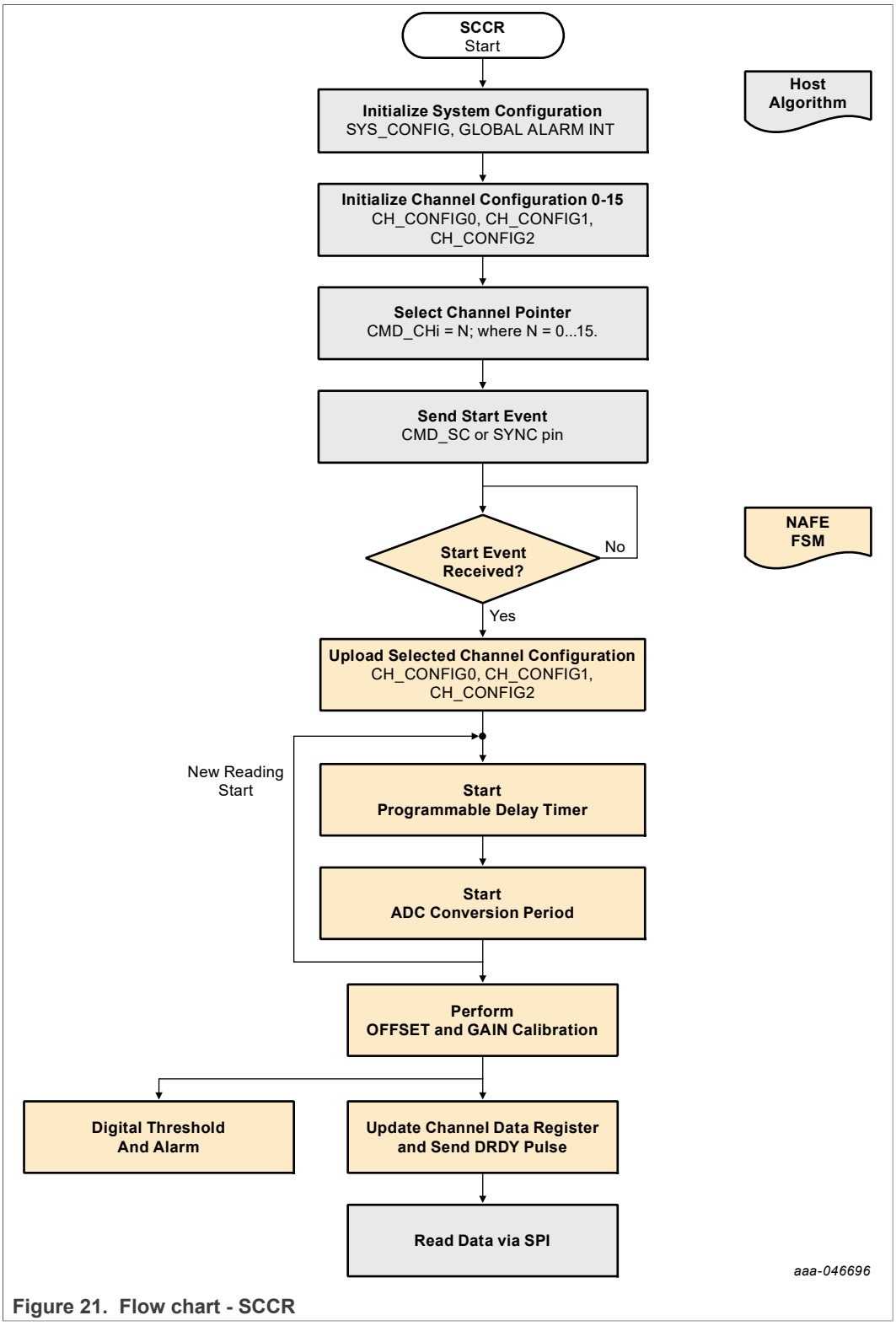


Figure 21. Flow chart - SCCR

7.5.8.2 Timing diagram - SCCR

The host can fetch single-channel data after the NAFE reading period by the two methods:

• Keep the CSB low after the command was issued. Then wait for DRDY pin assert high and read the channel data. Data is available at MISO pin at every rising of SCLK. MSB outputs first.

• De-assert the CSB high, then wait until the DRDY goes high and read the channel data.

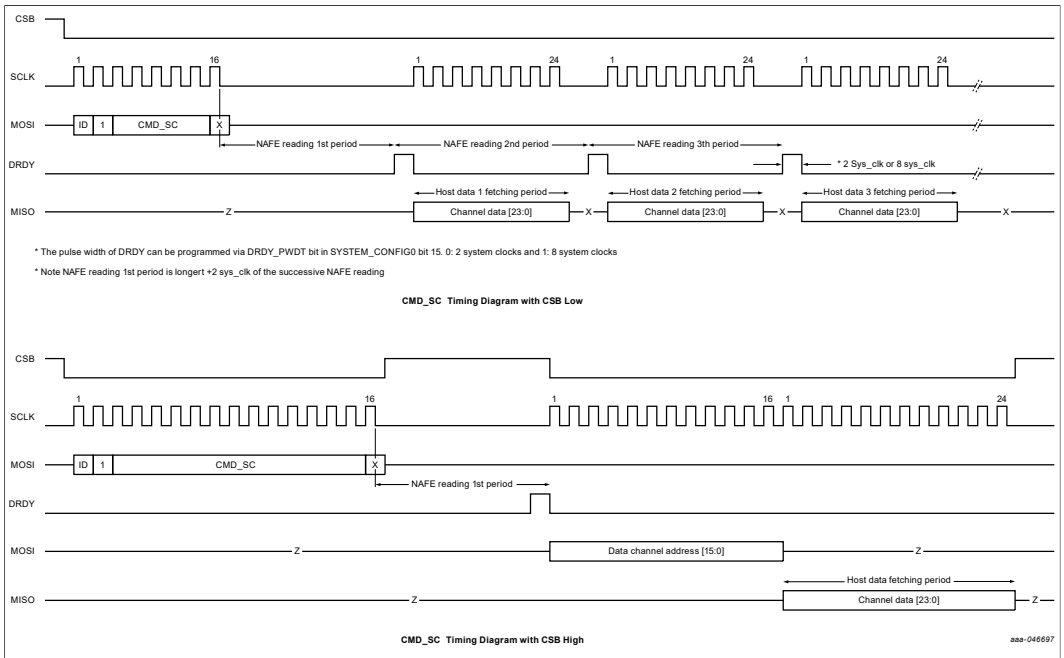


Figure 22. CMD_SC timing diagram CSB low/high

7.5.8.3 Code example - SCCR

```
Reg_Read ('SYS_STATUS0) ; to clear INTB
Reg_write ('SYS_CONFIG, sys_config_data); //
Reg_write ('CH_CONFIGi, ch_config_datai); // i = 0…15
Send CMD_CHi;
Send CMD_SC;
Send SYNC Pulse (if SYNC_BIT = 1);
```

7.5.8.4 Reading period for SCCR

SC Reading period: T_reading = T_fixed + T_prog_delay + T_conv

On first reading, T_fixed = (2 × T_sys_clk) ± 1 × T_sys_clk

On subsequent readings, T_fixed = 0.

For example,

Set CH_DELAY[5:0] = 17\d; #delay 76 sys_clk

Set ADC_DATA_RATE[4:0] = 5\d; #DRO is 24000 sps

Set ADC_NORMAL_SETTLING = 0\d; #Single-cycle mode

T_sys_clk =1/sys_clk = 1/9216000 = 0.1085 us

T_prog_delay = 76 * T_sys_clk #Table Channel Programmable Delay

T_conv = 1/24000 = 41.67 us #Table Data Rate

Hence,

On first reading, T_reading = 0.1085 us * (2 ± 1 + 76) + 41.67 us = 50.13 ± 0.1085 us

On subsequent readings, T_reading = 0.1085 us * (0 + 76) + 41.67 us = 49.92 us.

7.5.9 CMD_MM (multichannel multireading)

Start Multichannel Multireading (conversion) mode.

If SYS_CONFIG0.ADC_SYNC = 0, the conversion start is triggered by this SPI command at the last clock falling edge.

If SYS_CONFIG0.ADC_SYNC = 1, the conversion start is triggered by SYNC rising edge.

After first conversion, the sequencer will start conversion by sequencing on the enabled channel set via CH_CONFIG4.MCH_EN[15:0] register, from CH0 to CH15. Upon the completion of the last enabled channel, the device returns to waiting state.

The conversion could be interrupted by CMD_ABORT or CMD_END, or could be aborted and restarted by SYNC pulse if SYS_CONFIG0.ADC_SYNC = 1 or any conversion command if ADC_SYNC = 0.

If an SPI conversion command or a SYNC pulse is issued before completion of the current conversion, ADC aborts the conversion immediately and restarts the conversion starting from first enabled channel.

Data can be read serially via the MISO pin after the DRDY pin asserts high or after the reading is completed.

7.5.9.1 Flow chart - MCMR

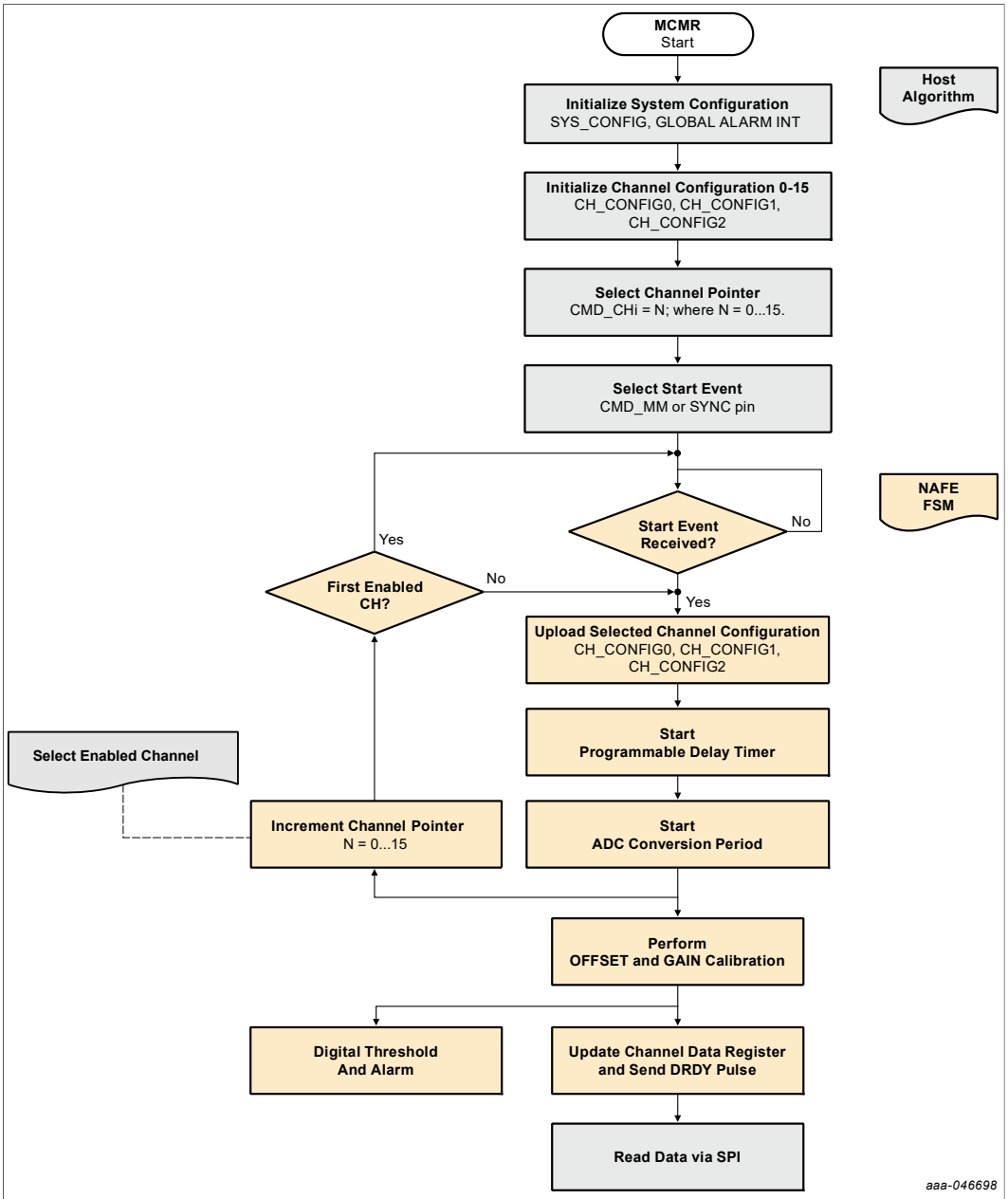


Figure 23. Flow chart MCMR

7.5.9.2 Timing diagram - MCMR

In this example, channels 0, 4, 8, and 12 are enabled in multichannel conversion as shown in Figure 24, CH_CONFIG4.MCH_EN[15:0] = 0001_0001_0001_0001. The sequencer generates four conversions results based on the four configurations stored at these respective locations 0, 4, 8, and 12 in the sequencer table.

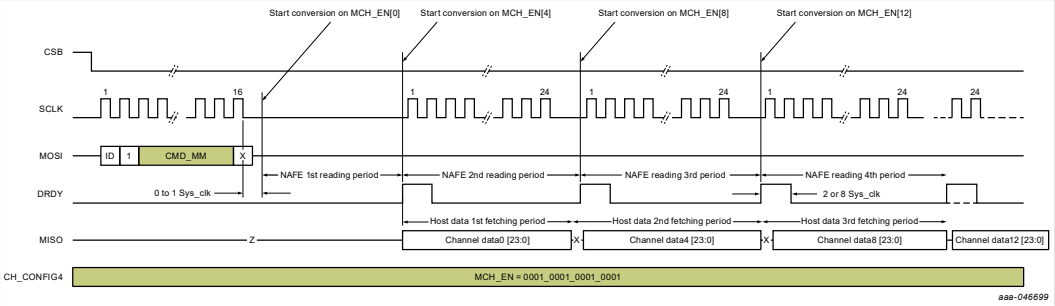


Figure 24. Timing diagram - MCMR

7.5.9.3 Code example - MCMR

```
Reg_Read ('SYS_STATUS0) ; to clear INTB
Reg_write ('SYS_CONFIG, config_data); //
Reg_write ('CH_CONFIGi, config_data); // i = 0…15
Send CMD_CHi;
Send CMD_MM;
Send SYNC Pulse (if SYNC_BIT = 1);
```

7.5.9.4 Reading period for MCMR

MM Reading period: T_reading = T_fixed + T_prog_delay + T_conv

On first reading, T_fixed = (2 × T_sys_clk) ± 1 × T_sys_clk

On subsequent reading, T_fixed = 0

For example,

Set CH_DELAY[5:0]=17\d; #delay 76 sys_clk

Set ADC_DATA_RATE[4:0]=5\d; #DRO is 24000 sps

Set ADC_NORMAL_SETTLING=0\d; #Single-cycle mode

T_sys_clk =1/sys_clk = 1/9216000 = 0.1085 us

T_prog_delay = 76 * T_sys_clk #Table Channel Programmable Delay

T_conv = 1/24000 = 41.67 us #Table Data Rate

Hence,

On first reading, T_reading = 0.1085 us * (2 ± 1 + 76) + 41.67 us = 50.13 ± 0.1085 us

On subsequent readings, T_reading = 0.1085 us * (0 + 76) + 41.67 us = 49.92 us.

7.5.10 CMD_MC (multichannel continuous-reading)

Start Multichannel Continuous-Reading (conversion) autonomous mode.

The CMD_MC is similar to CMD_MM with infinite loop until it is interrupted or restarted.

CMD_MC sets multichannel continuous-reading (conversion) mode.

If SYS_CONFIG0.ADC_SYNC = 0, the conversion start is triggered by this SPI command at the last clock falling edge.

If SYS_CONFIG0.ADC_SYNC = 1, the conversion start is triggered by SYNC rising edge.

After first conversion, the sequencer will start conversion by sequencing on the enabled channel set via CH_CONFIG4.MCH_EN[15:0] register, from CH0 to CH15. After the conversion completion of the last enabled channel, the device restarts a new cycle in an infinite loop.

The conversion could be interrupted by CMD_ABORT or CMD_END; or could be aborted and restarted by SYNC pulse if SYS_CONFIG0.ADC_SYNC = 1 or any conversion command if SYS_CONFIG0.ADC_SYNC = 0.

If an SPI conversion command or a SYNC pulse is issued before completion of the current conversion, ADC aborts the conversion immediately and restarts the conversion, starting from first enabled channel.

Data can be read serially via the MISO pin after the DRDY pin asserts high or after the reading is completed.

7.5.10.1 Flow chart - MCCR

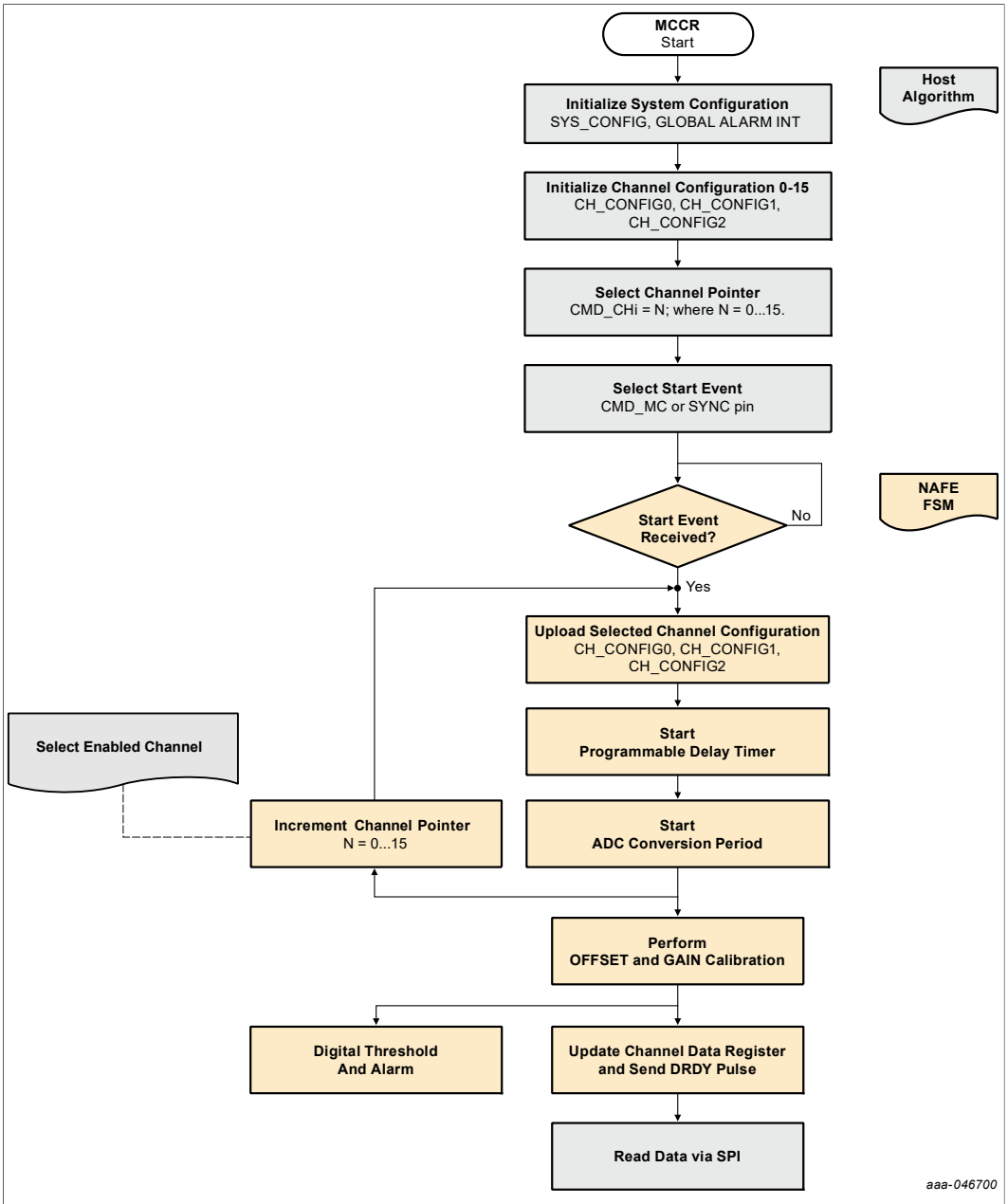


Figure 25. Flow chart - MCCR

7.5.10.2 Timing diagram - MCCR

The timing diagram for a multichannel continuous reading is shown in Figure 26, where Channels 0 and 12 are enabled by setting CH_CONFIG4.MCH_EN = 0001_0000_0000_0001. For CMD_MC command, the sequencer generates looping through two conversions based on the two configurations stored at these respective locations, 0 and 12, in the sequencer table. The conversions keep running through the loop until CMD_ABORT or CMD_END is issued.

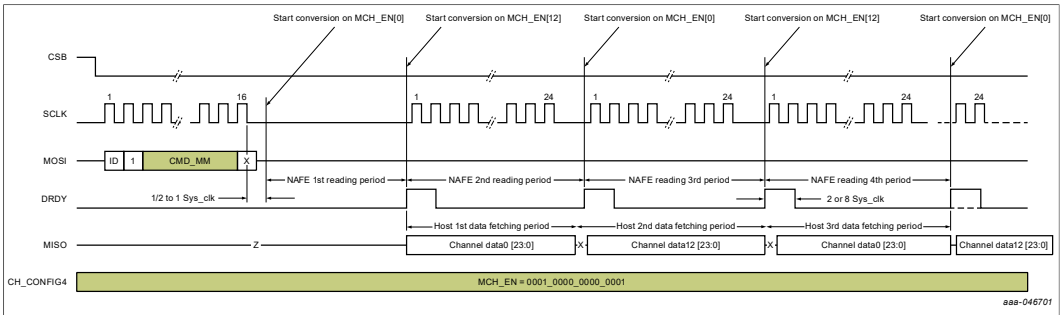


Figure 26. Timing diagram - MCCR

7.5.10.3 Code example - MCCR

```
Reg_Read ('SYS_STATUS0) ; to clear INTB
Reg_write ('SYS_CONFIG, sys_config_data); //
Reg_write ('CH_CONFIGi, ch_config_datai); // i = 0…15
Send CMD_CHi;
Send CMD_MC;
Send SYNC Pulse (if SYNC_BIT = 1);
```

7.5.10.4 Reading period for MCCR

MC Reading period: T_reading = T_fixed + T_prog_delay + T_conv

On first reading, T_fixed = (2 × T_sys_clk) ± 1 × T_sys_clk

On subsequent readings, T_fixed = 0.

For example,

Set CH_DELAY[5:0] = 17\d; #delay 76 sys_clk

Set ADC_DATA_RATE[4:0] = 5\d; #DRO is 24000 sps

Set ADC_NORMAL_SETTLING = 0\d; #Single-cycle mode

T_sys_clk =1/sys_clk = 1/9216000 = 0.1085 us

T_prog_delay = 76 * T_sys_clk #Table Channel Programmable Delay

T_conv = 1/24000 = 41.67 us #Table Data Rate

Hence,

On first reading, T_reading = 0.1085 us * (2 ± 1 + 76) + 41.67 us = 50.13 ± 0.1085 us

On subsequent readings, T_reading = 0.1085 us * (0 + 76) + 41.67 us = 49.92 us.

7.5.11 CMD_MS (multichannel single-reading)

Start Multichannel Single-Reading (conversion) mode.

If SYS_CONFIG0.ADC_SYNC = 0, the conversion start is triggered by this SPI command at the last clock falling edge.

If SYS_CONFIG0.ADC_SYNC = 1, the conversion start is triggered by SYNC rising edge.

Upon completion of each ADC conversion, the logic channel pointer is auto-incremented to the next enabled channel and awaits the arrival of a conversion start trigger. The ADC loops back to the first enabled channel when the last enabled channel is complete.

This reading mode could be terminated by issuing the CMD_END or CMD_ABORT.

If SYNC pulse or same conversion command is issued before completion of the conversion on the current channel, ADC aborts the conversion immediately and restarts the conversion on the current channel. (This is different from MM and MC modes, which restart on the first enabled channel)

Data can be read serially via the MISO pin after the DRDY pin asserts high or after the reading is completed.

7.5.11.1 Flow chart - MCSR

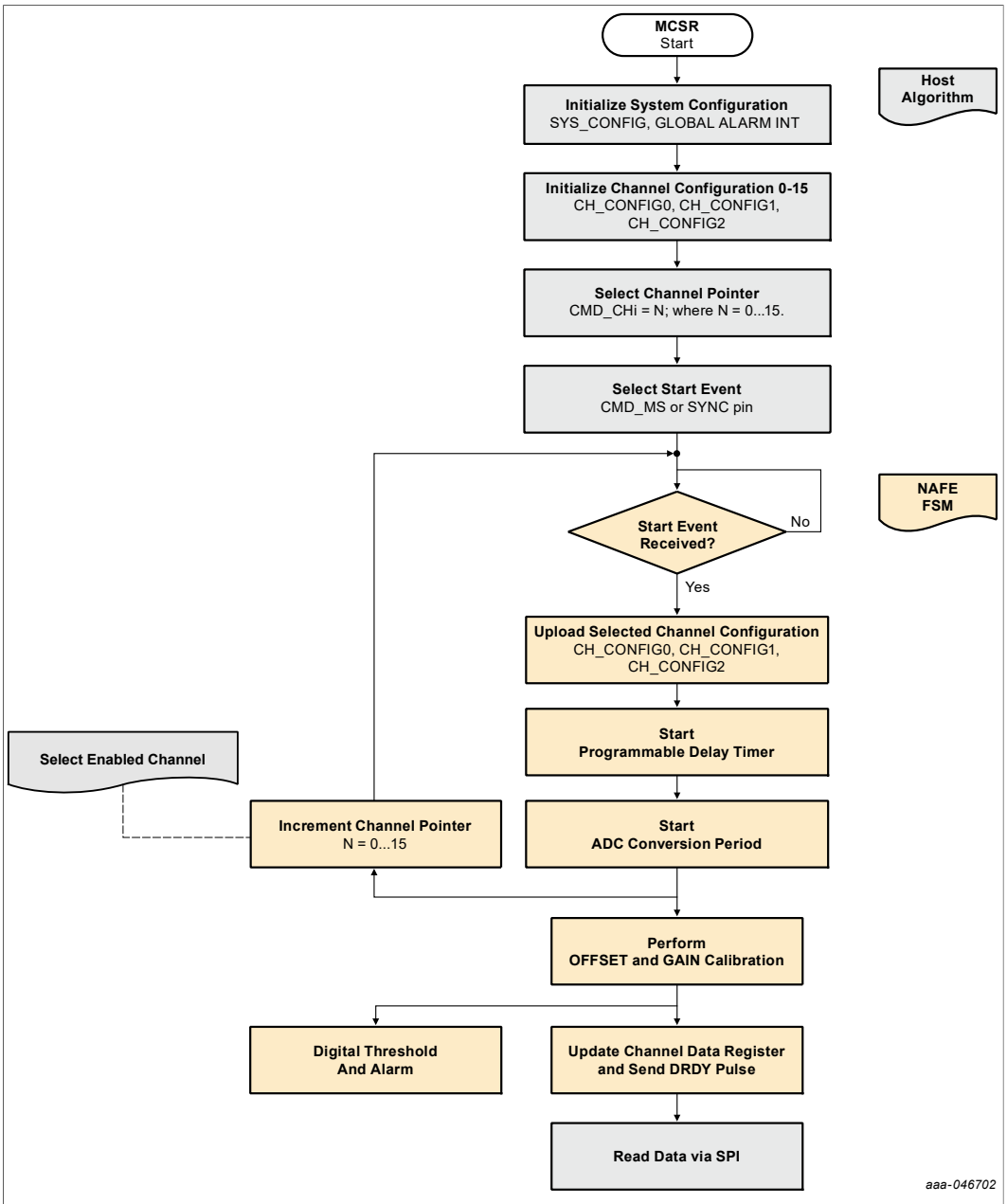


Figure 27. Flow chart - MCSR

7.5.11.2 Timing diagram - Flow chart - MCSR

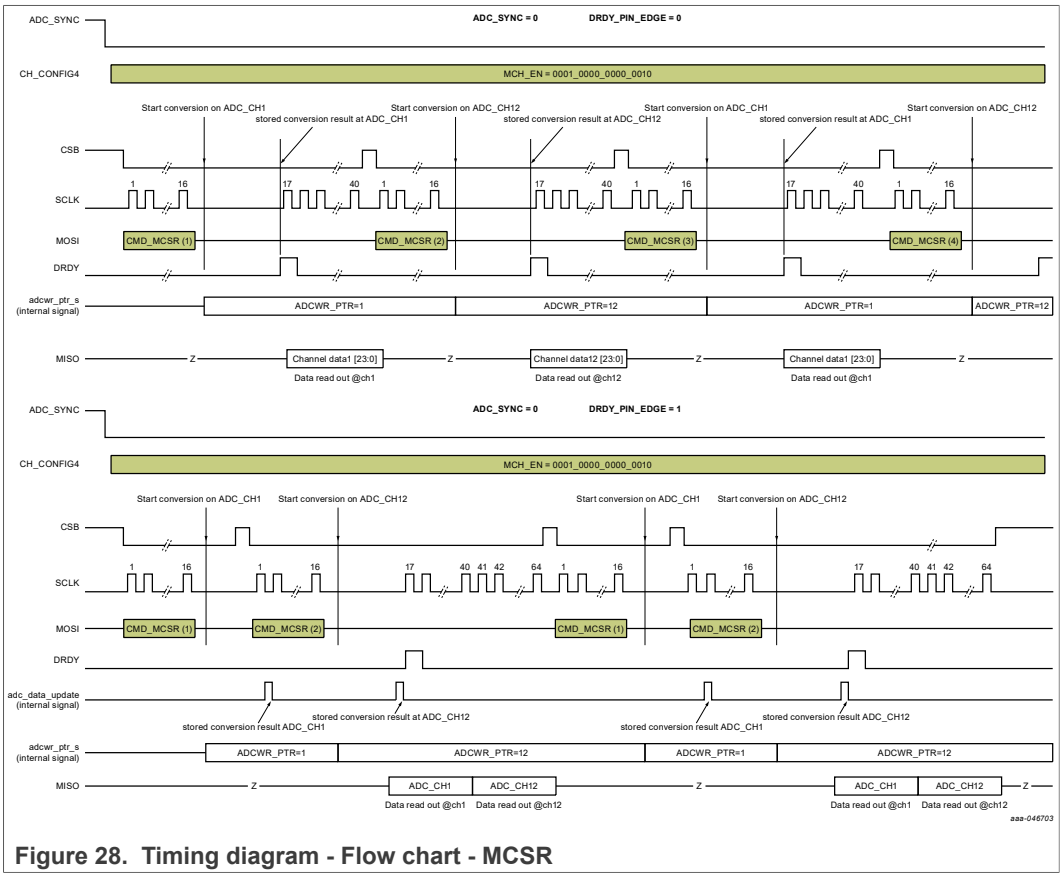


Figure 28. Timing diagram - Flow chart - MCSR

7.5.11.3 Code example - Flow chart - MCSR

```
Reg_Read ('SYS_STATUS0) ; to clear INTB
Reg_write ('SYS_CONFIG, sys_config_data); //
Reg_write ('CH_CONFIGi, ch_config_datai); // i = 0…15
Send CMD_CHi;
Send CMD_MS;
Send SYNC Pulse (if SYNC_BIT = 1);
```

7.5.11.4 Reading period for MCSR

MS Reading period: T_reading = T_fixed + T_prog_delay + T_conv

On single reading, T_fixed = (2 × T_sys_clk) ± 1 × T_sys_clk

For example,

Set CH_DELAY[5:0] = 17\d; #delay 76 sys_clk

Set ADC_DATA_RATE[4:0] = 5\d; #DRO is 24000 sps

Set ADC_NORMAL_SETTLING = 0\d; #Single-cycle mode

T_sys_clk =1/sys_clk = 1/9216000 = 0.1085 us

T_prog_delay = 76 * T_sys_clk #Table Channel Programmable Delay

T_conv = 1/24000 = 41.67 us #Table Data Rate

Hence,

On single reading, T_reading = 0.1085 us * (2 ± 1 + 76) + 41.67 us = 50.13 ± 0.1085 us.

7.6 ADC code to voltage translation

ADC code output can be translated to voltage with the simple formula provided in Table 18.

Note: *For HVMUX inputs, the readout voltage is scaled by PGA gain setting and the LVMUX diagnostic voltage readout is scaled with a fixed gain of 2.5.*

24-bit ADC hexadecimal code maximum (most positive) is 7F_FFFF\h and minimum (most negative) is 80_0000\h. The equivalent max- and min-signed decimal are 8,388,607\d and -8,388,608\d respectively.

The temperature sensor 16-bit code continuous readout is independent of main the ADC. The code to temperature translation is provided in Table 18.

Table 18. ADC code conversion formulas

Description	Gain	Formula
24-bit Hex to signed Decimal, $sINT_{24}$	-	$sINT_{24} = [(hex2dec(Hex) + 2^{23}) \% 2^{24}] - 2^{23}$
16-bit Hex to signed Decimal, $sINT_{16}$	-	$sINT_{16} = [(hex2dec(Hex) + 2^{15}) \% 2^{16}] - 2^{15}$
24-bit ADC scaled voltage	Gain	$VG = 10 / 2^{24} * (sINT_{24} / GAIN)$
16-bit ADC scaled voltage	Gain	$VG = 10 / 2^{16} * (sINT_{16} / GAIN)$
HV inputs	0.2, 0.4, 0.8	$V_{HV} = VG$
LV: GPIO0-GPIO1	2.5	$V_{GPIO} = 1 * (VG + 0)$
LV: REF2	2.5	$V_{REF2} = 2 * (VG + 1.5)$
LV: AVDD	2.5	$V_{AVDD} = 2 * (VG + 1.5)$
LV: HVDD	2.5	$V_{HVDD} = 32 * (VG + 0.25)$
LV: HVSS	2.5	$V_{HVSS} = -32 * (VG - 0.25)$
Temperature, DIE_TEMP[15:0]	-	$T (ºC) = sINT_{16} / 64$

7.7 Diagnostic features

The NAFE71388 is equipped with temperature and voltage condition monitoring and anomaly detection circuitries for system and self diagnostics. These flexible and configurable global alarms to allow the user to configure for various applications and needs. Useful, programmable-input signal monitoring and interrupt is also made available, as described in the following sections.

Table 19. Alarm and interrupt

Register	Bit order	Bit name	RW	Reset	Description
GLOBAL ALARM ENABLE 0x32\h	15	OVER_TEMP_ALRM	RW	0x0	Overtemperature warning at 145 °C
	14	HVDD_ALRM	RW	0x0	Enable alarm for HVDD supply detect below preset threshold.
	13	HVSS_ALRM	RW	0x0	Enable alarm for HVSS supply detect above preset threshold
	12	ADVDD_ALRM	RW	0x0	Enable alarm for DVDD supply detect below preset threshold.
	11	reserved	RW	0x0	reserved

Table 19. Alarm and interrupt*...continued*

Register	Bit order	Bit name	RW	Reset	Description
	10	GPI_POS_ALRM	RW	0x0	Enable alarm for rising edge detected at any GPI pins.
	9	GPI_NEG_ALRM	RW	0x0	Enable alarm for falling edge detected at any GPI pins.
	8	CONFIG_ERROR_ALRM	RW	0x0	Enable alarm for register configuration error.
	7	OVRRNG_ALRM	RW	0x0	Enable alarm when one or more data channels is over-range
	6	UNDRNG_ALRM	RW	0x0	Enable alarm when one or more data channels is under-range.
	5	OVRLOAD_ALRM	RW	0x0	Enable alarm when one or more data channels is overloaded or underloaded.
	4	EXTCLK_FREQ_ALRM	RW	0x0	Enable alarm when EXTCLK or XTAL clock period deviates > 20 % from 18.432 MHz INTOSC.
	3	reserved	RW	0x0	reserved
	2	reserved	RW	0x0	reserved
	1	reserved	RW	0x0	reserved
	0	TEMP_ALRM	RW	0x0	Enable programmable temperature alarm. The triggering threshold is set in THRS_TEMP register bit.
GLOBAL ALARM INTERRUPT 0x33\h	15	OVER_TEMP_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY
	14	HVDD_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	13	HVSS_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	12	ADVDD_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	11	reserved	R	0x0	reserved
	10	GPI_POS_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	9	GPI_NEG_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	8	CONFIG_ERROR_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	7	OVRRNG_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	6	UNDRNG_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	5	OVRLOAD_ALRM	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	4	EXTCLK_FREQ_ALRM	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	3	reserved	R	0x0	reserved
	2	reserved	R	0x0	reserved
	1	reserved	R	0x0	reserved
	0	TEMP_ALRM	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.

The alarm clearing behavior is determined by GLOBAL_ALRM_STICKY.

See Section 7.9.2 for address, bit order, and description of various global alarm configurations available.

7.7.1 Input under-range and over-range

Each of the 16 configured channels is paired with its own channel-based programmable thresholds for under- or over-range detection based on its ADC output.

These channel-based over-range (OVRRNG_ALRM) and under-range (UNDRNG_ALRM) conditions could also be set as INTB pin interrupt with register bit OVRRNG_INT = 1 and UNDRNG_INT = 1, respectively.

If the ADC detects a max or min value generates an over-load (OVRLOAD_ALRM) which could be set as INTB pin interrupt with register bit OVRLOAD_ALRM_INT = 1

7.7.2 REFH and REFL for diagnostic

REFL and REFH are two unbuffered, precise voltage sources connected to the analog input of HVMUXP and HVMUXN. With appropriate channel gain setting, it could be used as a reference channel or channel self-test in the field.

7.7.3 Voltage supply rail monitoring

The NAFE71388 can measure and monitor its own power supplies: HVDD, HVSS, and VDD.

When these values are read, a global alarm is issued if the read value is out of the user-programmed threshold. HVDD, HVSS, VDD (AVDD = DVDD) also have dedicated circuits with the undervoltage lockout (UVLO) to allow the device to operate above POR level at preset threshold.

7.7.4 Thermal monitoring and thermal shutdown

The NAFE71388 integrates a temperature sensor that allows continuous monitoring of die temperature by reading the DIE_TEMP(0x34) register. In addition, a user-programmable alarm threshold THRS_TEMP(0x37) can provide early over-temperature warning interrupt, TEMP_INT.

The NAFE includes a thermal shutdown circuit to protect the device from overheating. The thermal monitoring circuit asserts an alarm if the temperature is in the range 145 ºC. The circuit resets the chip when the junction temperature reaches 165 ºC.

7.7.5 Alarm

EXTCLK_FREQ_ALRM is triggered when the period deviation of external clock to internal oscillator clock is more than 20 %.

INTB alarms for detected input rising or falling edge at GPIO pins (GPI_POS_INT and GPI_NEG_INT) could also be used with configured setting on GPIO_CON, GPI_ENABLE, GPI_EDGE_POS, GPI_EDGE_NEG.

7.7.6 Interrupts

The INTB pin of the chip is a NOR function of the internal 12-bit of global alarm interrupt (GAI) registers. Each of these GAI registers' bits can be written 1 or 0 to enable or disable independently by SPI's register write command to global alarm enable register (address = 0x32\h).

Note: *When all the CH_DATA readback is enabled, the readback data could be prepended with channel-specific status byte, by enabling SYS_CONFIG0.STATUS_EN. Each of the status bit is OR's of all 16 channels.*

The logic equivalence is shown in Figure 29.

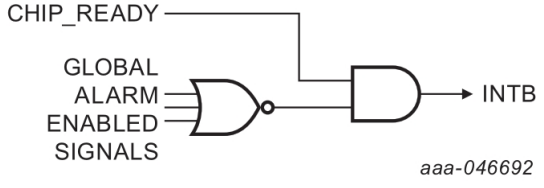


Figure 29. Interrupt

Note: *The status byte is only prepended when reading out the ADC data with SYS_CONFIG0.STATUS_EN=1.*

Each individual status bit is concatenated in single byte listed in Table 20.

Table 20. Status byte description

Status bit function	Representation Base		Bit index
	channel	global	
ADC underloaded or overloaded	√		7
ADC over user set threshold	√		6
ADC under user set threshold	√		5
Reserved	–		4
Reserved	–		3
Current die temperature over user-set threshold		√	2
Clock alarm error		√	1
Result of 3-bit logical OR of HVDD_ALRM, HVSS_ALRM, and AVDD_ALRM signals		√	0

These status bits behave independently of the SYS_CONFIG.GLOBAL_ALRM_STICKY state. They behave depending on what CMD_xy was issued:

Command CMD_SS: Status become sticky until host initiates another conversion then the status updates accordingly. Host can clear this channel-based status by issuing CMD_CLEAR_DATA or CMD_CLEAR_REG.

Commands CMD_MM, CMD_MC, CMD_MS, and CMD_SC: During multichannel or continuous conversions these status bits are updated live for each channel. For commands CMD_MM and CMD_MS, the last conversion channel status bits will not be cleared until the host issues CMD_CLEAR_DATA or CMD_CLEAR_REG.

This behavior applies for channel-based status during active conversion. The 3-MSB status bits are ADC underload/overload, ADC over-range and ADC under-range.

Global alarm interrupt (GAI) register (address 0x33\h) can be configured non-sticky or sticky behavior by programing. SYS_CONFIG0.GLOBAL_ALRM_STICKY = 0 or GLOBAL_ALRM_STICKY = 1, respectively. When the sticky option is selected, each GAI register bit is set by hardware if an interrupt event occurs with respect to each functional bit described in the GAI register. The host needs to clear whatever bit is already set in the GAI register by writing 1 to the respective bit locations to see the next interrupt event.

Note: *Writing 1 to the bit that is 0 in GAI register, will not alter it to 1.*

7.7.7 Behavior of sticky v. non-sticky alarms

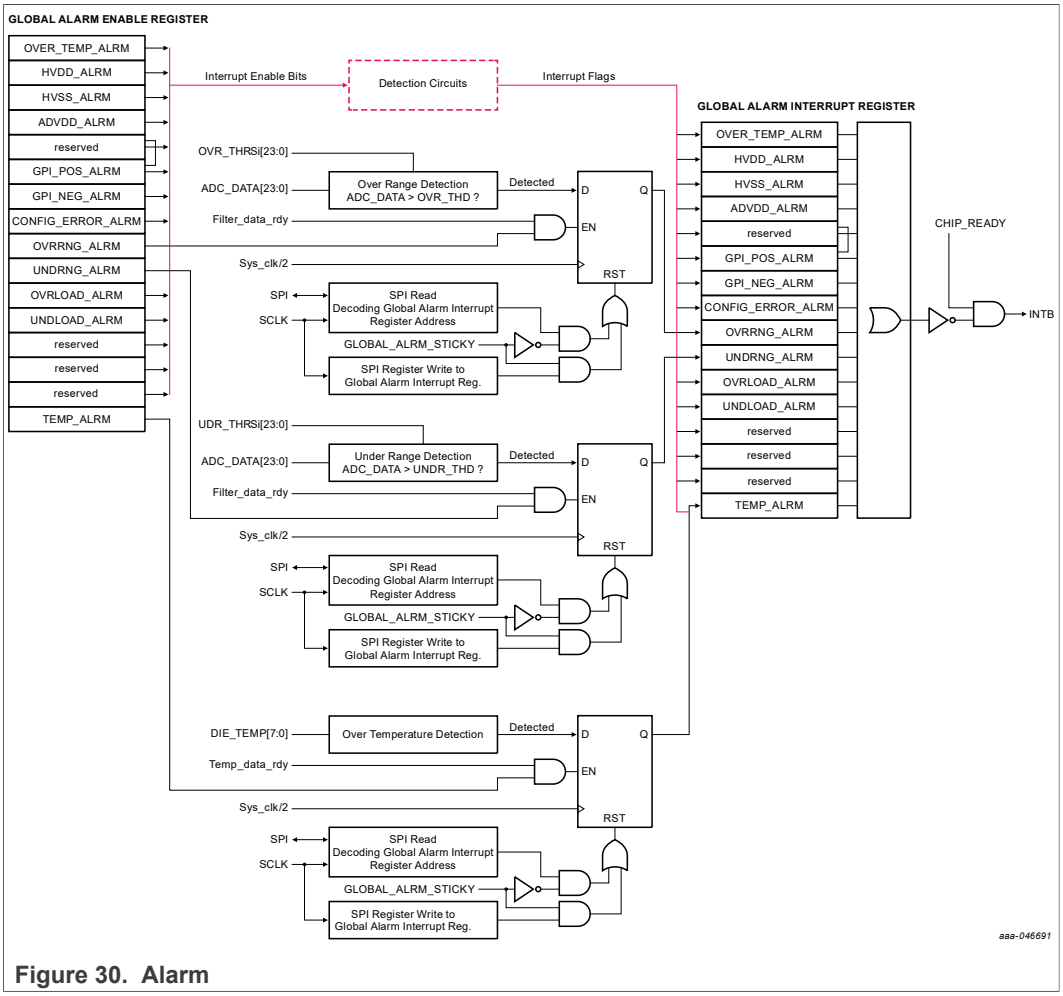


Figure 30. Alarm

When the non-sticky option is selected, the content of the GAI register reflects the current chip or channel conversion status at the time the host reads this register. The functionality of the INTB pin depends on how the host program SYS_CONFIG0.GLOBAL_ALRM_STICKY bit. For example, SYS_CONFIG0.GLOBAL_ALRM_STICKY = 1, sticky, INTB is de-asserted low until all interrupts are clear, whereas SYS_CONFIG0.GLOBAL_ALRM_STICKY = 0, non-sticky, INTB is low whenever there is an interrupt occurring and high whenever there is no interrupt. INTB might be toggling, meaning interrupt comes and goes regardless of GAI register read or not.

7.7.8 Configuration or loading error

When a user configuration error or chip error is detected, GLOBALALARMINTERRUPT.CONFIG_ERROR_INT will be asserted 1. A chip configuration error could be triggered by command CMD_RELOAD, at POR or pulling low on RSTB pin. If any of these events take place, on-chip NVM module loads the information to the shadow's trim registers and the data integrity is checked at this time. If the data was found to be corrupted or inconsistent, the configuration error would be set to 1.

7.8 SPI interface and controls

7.8.1 SPI signal pins

The SPI-compatible serial interface is used to read the conversion data, internal register content and to configure the device and control the ADC. The serial interface consists of four signals: CSB, SCLK, MOSI, and MISO. One external pin, SPI_ADDR, is used as SPI address such that the host can address two devices without using a separate CSB pin. In addition, DRDY and SYNC signals allow the handshaking and data synchronization between the host and the device. The conversion data are provided with an optional CRC code for improved data integrity. 24-bit ADC word can be read with and without 8-bit CRC appended at the end of data.

The SPI pin functions are described in the following sub-sections.

7.8.1.1 CSB (active low)

CSB is an input pin that enables the communication between the host and the chip. CSB must remain low for the entire data transaction. When CSB is set to high, the serial interface is reset, SCLK input and command inputs are ignored.

7.8.1.2 SCLK

SCLK is the serial interface clock that operates up to 32 MHz. It is a noise-filtered, Schmitt-triggered input used to clock data in and out of the chip. Serial input data is latched in the falling edge of SCLK and serial data outputs from the chip are updated on the rising edge of SCLK.

7.8.1.3 MOSI

MOSI is the serial data input to the chip. MOSI is used to input commands and register data to the chip.

7.8.1.4 MISO

MISO is the serial data output from the chip. MISO data contains: internal registers data, ADC results, status byte, and/or 8-bit CRC if CRC_EN and/or STATUS_EN are set to 1, respectively. When CSB is high, MISO is in high-impedance. When CSB is low, MISO is updated on the rising edge of the SCLK.

7.8.1.5 SPI_ADDR

SPI_ADDR is an additional input pin used to address a second device with a single CSB to reduce the number of chip select signals required.

7.8.1.6 DRDY

DRDY (rising edge) is an output pin that indicates the conversion status. DRDY is driven to high when the new conversion result is stored in the SPI buffer and ready for reading.

DRDY pulse stays high for 2 x T_sys_clk if SYS_CONFIG0.DRDY_PWDT bit = 0. Otherwise, the pulse stays high for 8 x T_sys_clk if DRDY_PWDT bit = 1.

7.8.1.7 SYNC

SYNC is an external pin used to synchronize the data conversion to external events. The user can start any conversion mode either by using SPI command or asserting low to high transition on the SYNC pin given that the SYS_CONFIG0.ADC_SYNC bit = 1.

The minimum width of SYNC pulse should be 2 x T_sys_clk.

7.8.1.8 INTB (active low)

INTB (active low) is an output pin that notifies when a global alarm interrupt has occurred. The driver can be programmed as open-drain with internal pullup or CMOS output.

7.8.2 SPI communication protocols

This section describes the user SPI communication protocols. The SPI host must always start with DEV_AD bit either 0 or 1 to match the device ADDR0's pin to initiate the communication with that device. The following bits are: RW_L bit (read or write transaction), 13 RA bits (addressable up to 8192 locations), and D is data from the host to the device or the device to the host depending on write or read operation, respectively. RW_L should be set to 0 for write, whereas it should be 1 for read.

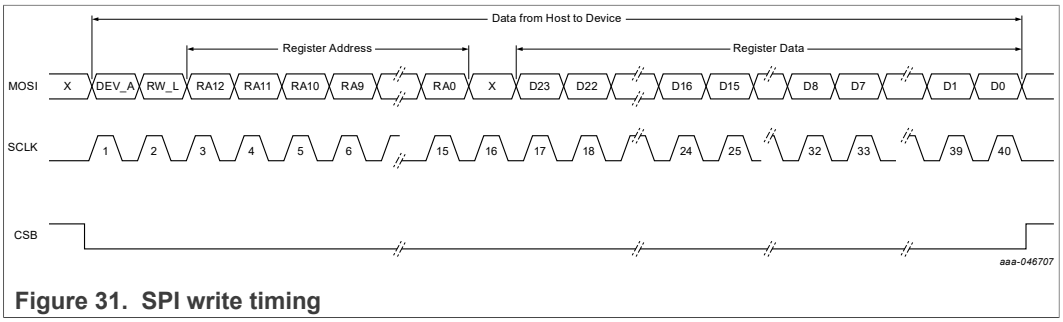


Figure 31. SPI write timing

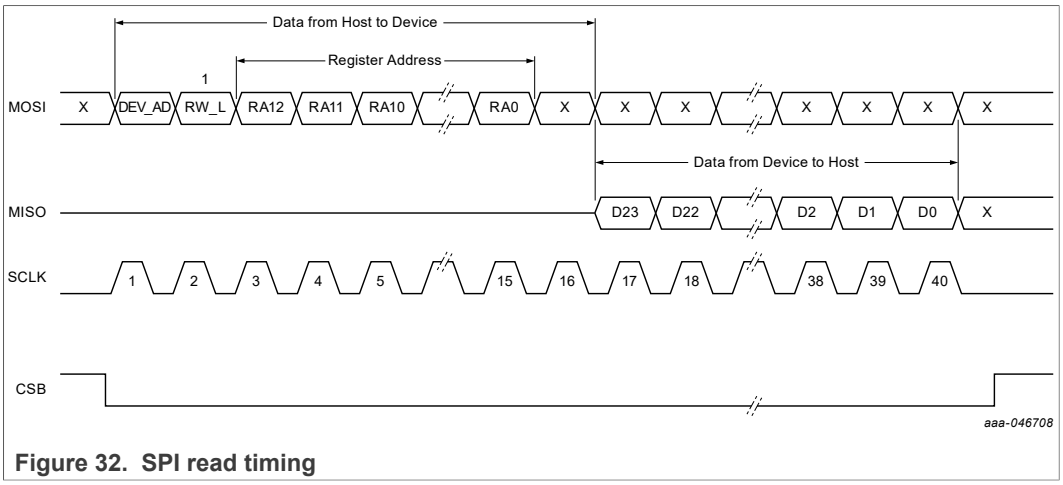


Figure 32. SPI read timing

7.8.2.1 Write without CRC

The second bit after the first SPI bit frame "RW_L" is 0 indicates that it is a write transaction. SPI write command is used to configure the internal registers of the chip. The register values get updated every eighth clock cycle with a byte of data starting

from the MSB. A minimum of eight SCLKs is needed to write the first byte of data in a multibyte register. For instance, if the user only needs to update the first MSB-byte (bit 23:16) of the register that has 24-bit data width and bits 15 to 0 retain the old value of the register, then eight SCLKs are needed. Figure 33 shows the host partially write value 0xA5 to D23-D16 (bit location 23 to 16) of register 0x0020.

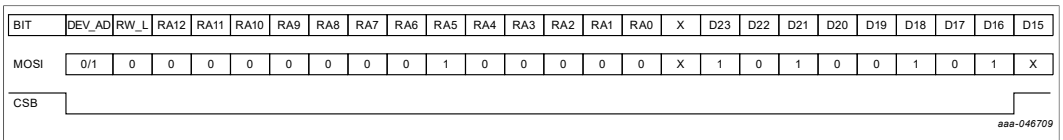


Figure 33. Write without CRC

7.8.2.2 Read without CRC

The second bit after the first SPI bit frame "RW_L" is 1 indicates it is a read transaction. SPI read command is used to read back the internal register contents of the chip and the ADC conversion results.

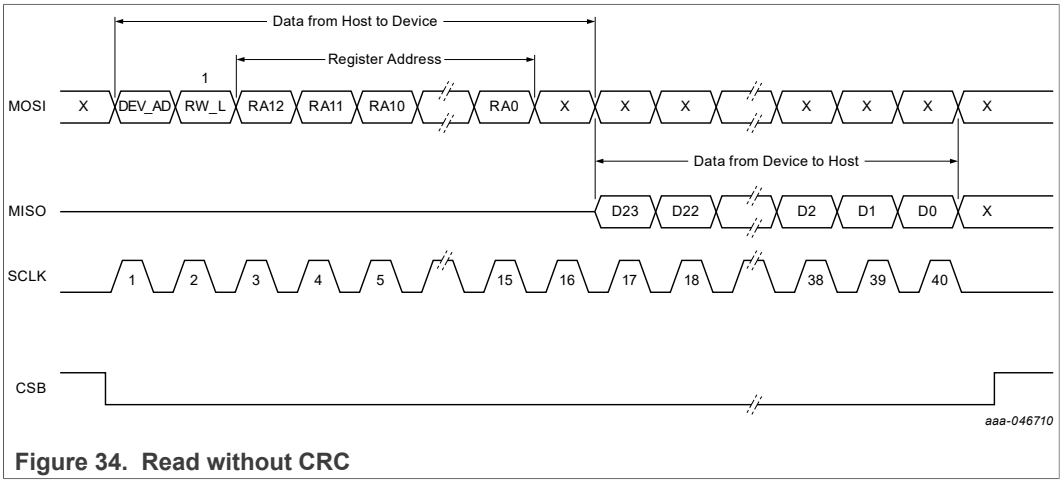


Figure 34. Read without CRC

7.8.2.3 CRC-8 generator

The NAFE71388 provides assurance of the integrity of the data communication with optional 8-bit CRC data appended at the end of the data transfers. The CRC_EN is bit 7 in the SYS_CONFIG0 register, with CRC default off, CRC_EN = 0. Setting CRC_EN = 1 will enable CRC feature.

The following polynomial is always used in this chip:

$y = x^8 + x^2 + x + 1$ equivalent to binary number is 100000111.

The cyclic redundancy byte is an error-detection byte that detects communication errors to and from the host and device. CRC byte is the division remainder of the payload data of CRC polynomial in which the polynomial function is $x^8 + x^2 + x + 1$. The 9-bit binary coefficients are: 100000111b. The payload data are either two or three bytes depending on the data transfer operation.

When CRC is enabled, the CRC byte is appended after the 16-bit command (two bytes) and after the ADC data.

7.8.2.4 16-bit command with CRC

The host computes the CRC over the 16-bit command and appends the 8-bit CRC to the command. The device performs the CRC calculation on 16-bit command and compares the result to the 8-bit CRC transmitted by the host. If the host and the device CRC values match, the command is executed. Otherwise, the command will be ignored and a CRC error is generated.

The CRC_ERROR flag is routed out to GPIO2 if SYS_CONFIG0.CRC_ERROR_ON_GPIO2 is set to 1.

In addition, the CRC_ERROR can be read on SYS_STATUS0.CRC_ERROR bit. The SYS_STATUS0.CRC_ERROR bit is cleared upon reading.

7.8.2.5 Write with CRC

Figure 35 and Figure 36 show the host writes NAFE 16-bit and 24-bit internal register respectively.

- **For 16-bit register write:** The host first calculates the 8-bit CRC_A on 16-bit address and appends the 8-bit CRC_A after the address. The host then calculates the 8-bit CRC_D on 16-bit data and appends the 8-bit CRC_D after 16-bit data.
- **For 24-bit register write:** The host first calculates the 8-bit CRC_A on 16-bit address and appends the 8-bit CRC_A after the address The host then calculates the 8-bit CRC_D on 24-bit data and appends the 8-bit CRC_D after 24-bit data.

In both cases, the host should send an extra 8-bit clock to receive back the calculated CRC_D from the device.

The 16-bit address register includes device ID bit, RW_L bit, RA bits, and don't care bit (0).

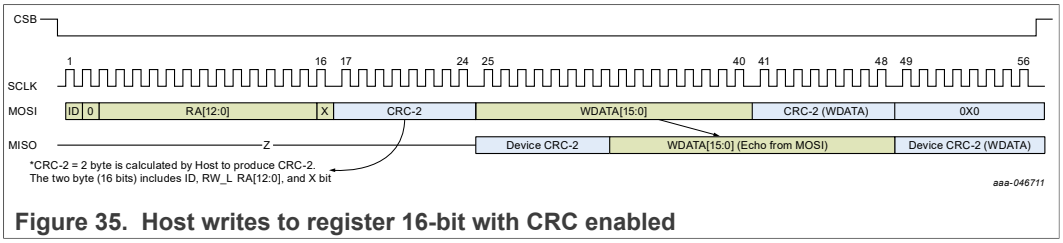


Figure 35. Host writes to register 16-bit with CRC enabled

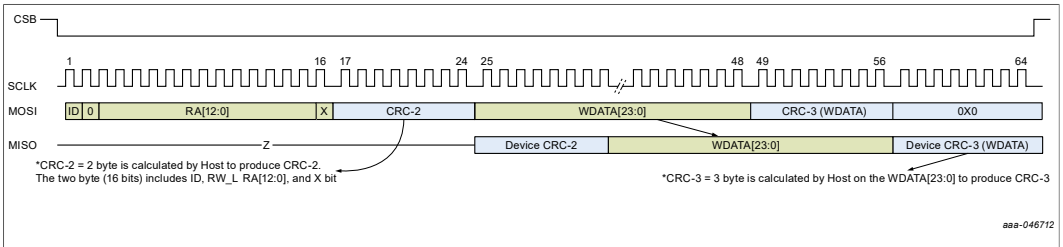


Figure 36. Host writes to register 24-bit with CRC enabled

7.8.2.6 Read with CRC

Figure 37 shows host read data from the 24-bit register. The host sends the first CRC byte, calculated based on the first 16-bit word, which includes device ID bit, RWL bit, RA bits, and don't care bit (0). The second CRC byte is from the device to the host. It is

calculated based on RDATA from the device to the host. Figure 37 also shows host read data from the 16-bit register.

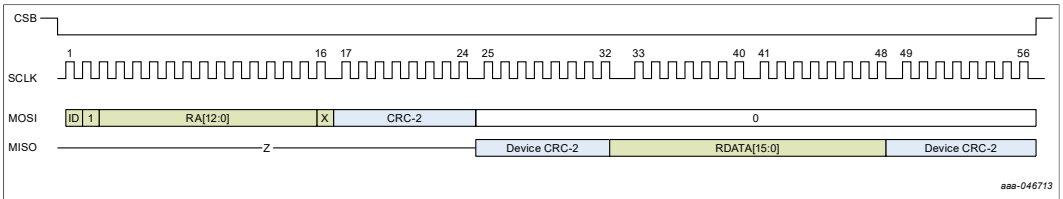


Figure 37. Host read data from the 24-bit register

7.8.2.7 System configuration with CRC

Two-byte command: Two-byte command format with no data return.

A non-return data command, including register write command, RW_L bit is always set to 0. The figure below shows the timing of two-byte command with non-return ADC data.

- **Command examples:** CMD_CH0, … CMD_CH15, CMD_ABORT, CMD_END, CMD_CLEAR_ALARM, CMD_CLEAR_DATA, CMD_RESET, CMD_REOAD

The host calculates the CRC of the two-input command bytes. Device CRC-2 byte is calculated by device, output based on the two received command bytes. If the two CRC values match, the command is executed at the beginning of the last falling edge of SCLK of the fourth byte in the sequence. Asserting CSB high before the command completes will result in command termination. When a new command starts, the device must see the CSB transition from high to low.

If both CRC_EN, and STATUS byte output format are enabled, then the CRC calculation includes status byte plus the ADC conversion data, CRC4 for 24-bit ADC and CRC3 for 16-bit ADC.

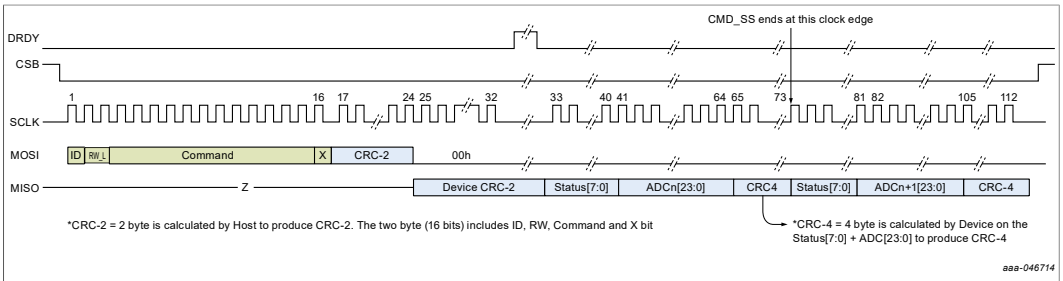


Figure 38. Conversion command data read operation 2/24-bit ADC, CRC_Enable = 1, Status_Enable = 0

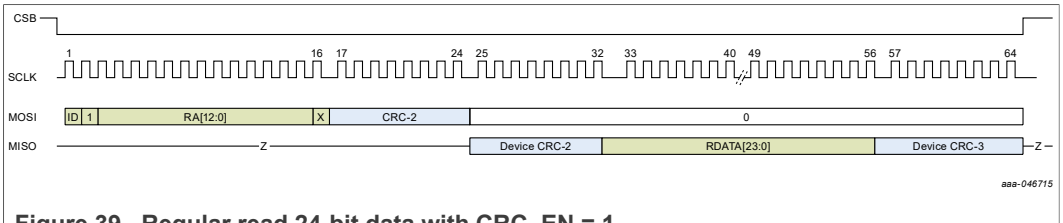


Figure 39. Regular read 24-bit data with CRC_EN = 1

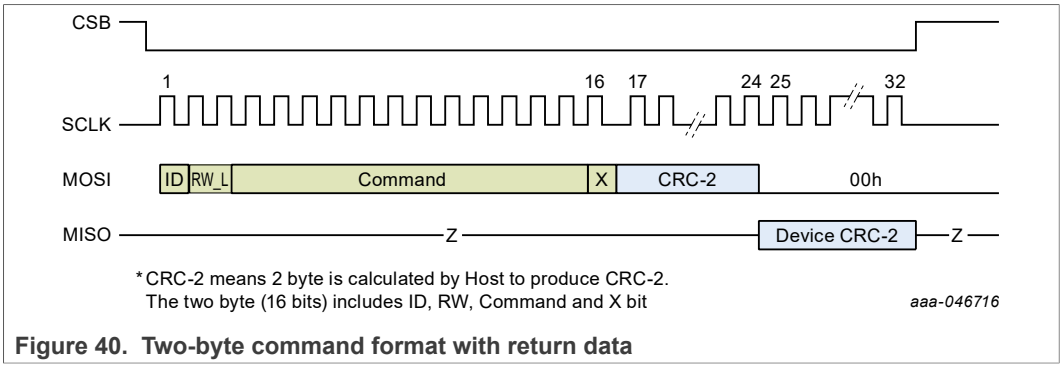


Figure 40. Two-byte command format with return data

Two-byte command: Two-byte command format with data return.

A return data command, including register read command, RW_L bit is always set to 1. Figure 41 shows the timing of two-byte command with ADC data return.

- **Command examples:** CMD_SS, CMD_SC, CMD_MM, CMD_MC, and CMD_BURST_DATA

The host calculates CRC of the two-input bytes and sends the CRC-2 after the 16-bit command. Device CRC-2 byte is calculated by device, output based on the two received command bytes. If the two CRC values match, the command is executed. After the host sends CRC byte, it can continue to send eight more clocks to get the device calculated CRC before DRDY goes high. The host can keep the CSB low, while waiting for DRDY to assert HI, then provide the number of clocks required to retrieve the ADC conversion data along with its respective calculated CRC. If the device is 24-bit ADC, then CRC calculation will be based on three ADC bytes. If the device is 16-bit ADC, then CRC calculation will be based on two ADC bytes.

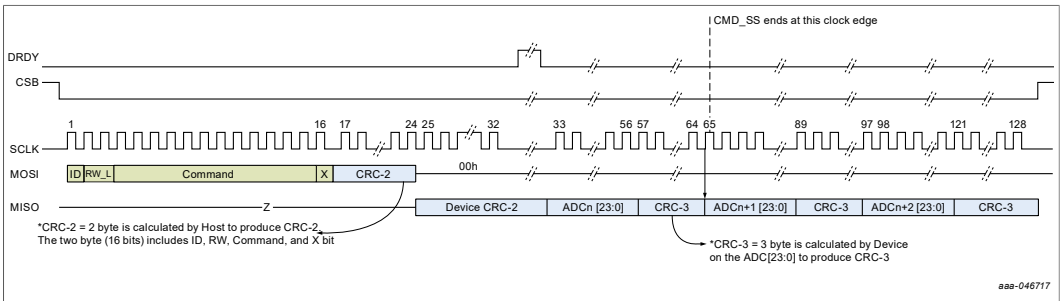


Figure 41. Conversion command data read operation 2/24-bit ADC, CRC_ENABLE = 1, Status_Enable = 0

7.8.3 SPI programming and commands

The SPI instruction commands are dedicated SPI addresses with predefined functions for reducing SPI transactions on frequent data accesses and controls. This section is a summary of all the instruction commands.

Note: *Instruction commands are encoded with 0's in bits RA5 to RA12. Registers are offset at address 0x20\h and RA5 bit is always set to 1 when accessing the registers.*

7.8.3.1 Commands definition

16-bit SPI instructions and mnemonic.

7.8.3.1.1 CMD channel selection

CMD_CHi should be used to select the logic channel CHx where x = 0...15

Table 21. CMD channel selection

RW_L	RA12	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	Mnemonic	HEX Code
0	0	0	0	0	0	0	0	0	0	0	0	0	0	CMD_CH0	0x0000
0	0	0	0	0	0	0	0	0	0	0	0	0	1	CMD_CH1	0x0001
0	0	0	0	0	0	0	0	0	0	0	0	1	0	CMD_CH2	0x0002
0	0	0	0	0	0	0	0	0	0	0	0	1	1	CMD_CH3	0x0003
0	0	0	0	0	0	0	0	0	0	0	1	0	0	CMD_CH4	0x0004
0	0	0	0	0	0	0	0	0	0	0	1	0	1	CMD_CH5	0x0005
0	0	0	0	0	0	0	0	0	0	0	1	1	0	CMD_CH6	0x0006
0	0	0	0	0	0	0	0	0	0	0	1	1	1	CMD_CH7	0x0007
0	0	0	0	0	0	0	0	0	0	1	0	0	0	CMD_CH8	0x0008
0	0	0	0	0	0	0	0	0	0	1	0	0	1	CMD_CH9	0x0009
0	0	0	0	0	0	0	0	0	0	1	0	1	0	CMD_CH10	0x000A
0	0	0	0	0	0	0	0	0	0	1	0	1	1	CMD_CH11	0x000B
0	0	0	0	0	0	0	0	0	0	1	1	0	0	CMD_CH12	0x000C
0	0	0	0	0	0	0	0	0	0	1	1	0	1	CMD_CH13	0x000D
0	0	0	0	0	0	0	0	0	0	1	1	1	0	CMD_CH14	0x000E
0	0	0	0	0	0	0	0	0	0	1	1	1	1	CMD_CH15	0x000F

7.8.3.1.2 CMD initialize/clear

The encoded 16-bit SPI instructions for clear and reset are:

CMD_CLEAR_ALARM, CMD_CLEAR_DATA, CMD_CLEAR_REG, CMD_RELOAD, and CMD_RESET.

Three types of resets are available:

- Chip power-on reset (POR)
- RSTB accessible by pulling the pin to ground
- CMD_RESET

Hardware reset is achieved by pulling pin RSTB = 0 V or POR. When in reset, all HV input pins and GPIO pins are in high-Z input mode, internal voltage reference is used, ADC digital filters are cleared, all user registers are set to their default values and all NVM shadow register content will be reloaded. The input clock source will be defaulted back to internal RC oscillator and go through autoclock switching within 50 ms if the external clock is applied or crystal is installed.

CMD_RESET is the same as the hardware reset by pulling RSTB pin down to GND.

Issuing the CMD_CLEAR_ALARM command clears GLOBAL ALARM INTERRUPT bits at register address: 0x33\h.

Issuing the CMD_CLEAR_DATA command will clear all channel data (CH_DATA0 – CH_DATA15) registers to 0x000000.

Issuing the CMD_CLEAR_REG command clears the user registers, except the clock source select, SYS_CONFIG0.CK_SRC_SEL [1:0]. The clock source select bit does not get cleared even if they are part of the user's registers. The user can change this register after POR, while any conversion is in active. For instance, if CK_SRC_SEL held a value other than 0 before the command was issued, it would stay the same after this command was issued.

Note: *CRC_EN is also cleared.*

Issuing the CMD_RELOAD command reloads NVM contents to shadow registers. NVM contents consist of the NAFE trims parameters and offset and gain calibration coefficients. This command does not reset user registers.

Table 22. CMD initialize/clear

RW_L	RA12	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	Mnemonic	HEX Code
0	0	0	0	0	0	0	0	0	1	0	0	0	0	CMD_ABORT	0x0010
0	0	0	0	0	0	0	0	0	1	0	0	0	1	CMD_END	0x0011
0	0	0	0	0	0	0	0	0	1	0	0	1	0	CMD_CLEAR_ALARM	0x0012
0	0	0	0	0	0	0	0	0	1	0	0	1	1	CMD_CLEAR_DATA	0x0013
0	0	0	0	0	0	0	0	0	1	0	1	0	0	CMD_RESET	0x0014
0	0	0	0	0	0	0	0	0	1	0	1	0	1	CMD_CLEAR_REG	0x0015
0	0	0	0	0	0	0	0	0	1	0	1	1	0	CMD_RELOAD	0x0016
0	0	0	0	0	0	0	0	0	1	0	1	1	1	TBD	0x0017

7.8.3.1.3 CMD reading modes

Table 23. CMD reading modes

RW_L	RA12	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	Mnemonic	HEX Code
1	0	0	0	0	0	0	0	0	0	0	0	0	0	CMD_SS	0x2000
1	0	0	0	0	0	0	0	0	0	0	0	0	1	CMD_SC	0x2001
1	0	0	0	0	0	0	0	0	0	0	0	1	0	CMD_MM	0x2002
1	0	0	0	0	0	0	0	0	0	0	0	1	1	CMD_MC	0x2003
1	0	0	0	0	0	0	0	0	0	0	1	0	0	CMD_MS	0x2004

CMD_SS: Set Single-Channel Single-Reading (conversion) mode. If bit ADC_SYNC = 0, the conversion start is triggered by this SPI command at the last SPI clock falling edge. If bit ADC_SYNC = 1, the conversion start is triggered by SYNC rising edge. In both cases, the conversion is executed on the selected channel. After the conversion completion, the device returns to waiting state. (SS: Single-channel Single-reading)

CMD_SC: Set Single-Channel Continuous-Reading (conversion) mode. If bit ADC_SYNC = 0, the conversion start is triggered by this SPI command at the last clock falling edge. If bit ADC_SYNC = 1, the conversion start is triggered by SYNC rising edge. In both cases, the conversion is executed on the selected channel until it is interrupted or restarted. The conversion could be interrupted by CMD_ABORT and CMD_END, or could be aborted and restarted by SYNC pulse if ADC_SYNC = 1 or any conversion command if ADC_SYNC = 0. (SC: Single-channel Continuous reading)

CMD_MC: Set Multichannel Continuous-readings (conversions) autonomous mode. The CMD_MC is similar to CMD_MM with infinite loop until it is interrupted or restarted. (MC: Multichannel Continuous reading)

CMD_MS: Set Multichannel Single Reading (conversions) mode. If bit ADC_SYNC = 0, the conversion start is triggered by this SPI command at the last clock falling edge. If bit ADC_SYNC = 1, the conversion start is triggered by SYNC rising edge. Upon completion of each ADC conversion, the logic channel pointer is auto-incremented to the next enabled channel and awaits the arrival of a conversion start trigger. The ADC will loop back to first enabled channel when the last enabled channel was completed. This reading mode could be terminated by issuing the CMD_END or CMD_ABORT. If SYNC pulse or same conversion command is issued before completion of the conversion on the current channel, ADC aborts the conversion immediately and restarts the conversion on the current channel. (This is different from MM and MC modes, which restart on the first enabled channel.) (MS: Multi-channel Single-reading)

7.8.3.1.4 CMD burst data

Table 24. CMD burst data

RW_L	RA12	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	Mnemonic	HEX Code
1	0	0	0	0	0	0	0	0	0	0	1	0	1	CMD_ BURST_ DATA	0x2005

CMD_BURST_DATA: Burst read the enabled data channels CH_DATA from CH0 to CH15 sequentially (determined by MCH_EN[15:0] bits).

Note: *If MCH_EN = 0x8000, data in CH_DATA15 is read.*

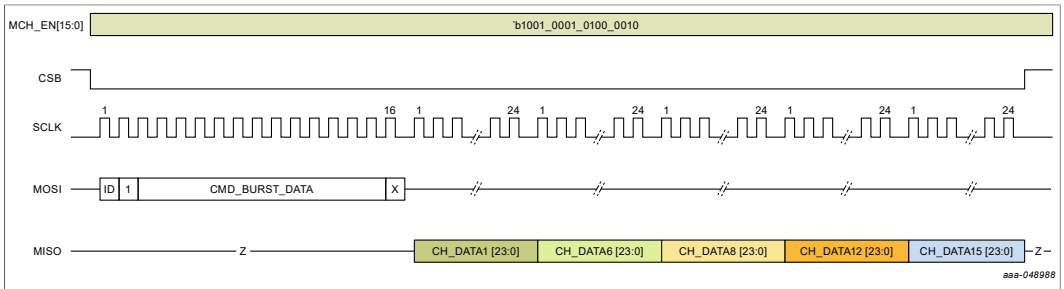


Figure 42. Burst data command

7.8.3.1.5 CMD CRC

Table 25. CMD CRC

RW_L	RA12	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	Mnemonic	HEX Code
1	0	0	0	0	0	0	0	0	0	0	1	1	0	CMD_CALC_CRC_CONFG	0x2006
1	0	0	0	0	0	0	0	0	0	0	1	1	1	CMD_CALC_CRC_COEF	0x2007
1	0	0	0	0	0	0	0	0	0	1	0	0	0	CMD_CALC_CRC_FAC	0x2008

CMD_CALC_CRC_CONFG: Calculate CRC sum for all 16-bit user configuration registers and save result to 0x25\h(CRC_CONFIG_REGS).

CMD_CALC_CRC_COEF: Calculate CRC sum for all 24-bit CAL coefficient and threshold registers and save result to 0x26\h(CRC_COEF_REGS).

CMD_CALC_CRC_FAC: Calculate all factory OTP trim registers and save result to 0x27\h(CRC_TRIM_INT[15:0]).

After the command is issued by the host, the user must wait for DRDY assert high or wait for ~ 64 system clock period to read back the CRC calculation result at register address at 0x25, 0x26, or 0x27 if CMD_CALC_CRC_CONFG, CMD_CALC_CRC_COEF, or CMD_CALC_CRC_FAC is used respectively.

7.8.3.1.6 Read/Write

Table 26. Read/Write

RW_L	RA12	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	Mnemonic	HEX Code
1	RA12	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	eg: Read register CH_CONFIG0 : Reg_Rd(0x2020)	0x2000+RA(offset)
0	RA12	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	eg: Write register CH_CONFIG0 : Reg_Wr (0x0020, Data)	0x0000+RA(offset)

7.8.3.2 Channel data readback

ADC conversion results can be read by two methods:

1. Directly after conversion, read data is stored to the channel data register indicated by the rising edge of DRDY. The conversion result is automatically transferred to the SPI data buffer while the host provides the SPI clock. However, the CSB needs to stay low after the start conversion event has been issued.
2. Read data from the channel data register. This requires a new SPI transaction that addresses and fetches the channel data register.

By default, DRDY asserts high for two sys_clk periods. This pulse width can be programmed to eight sys_clk periods by setting SYSTEM_CONFIG0.15 (DRDY_PWDT) to 1.

7.9 Register map

There are three types of registers:

- 16-bit configuration and status registers

- 24-bit coefficient registers
- 24-bit or 16-bit data registers for 24-bit or 16-bit options

7.9.1 16-bit channel-based configuration

CH_CONFIG0..2[15:0] are channel-based registers. Before reading or writing to CH_CONFIG registers of a channel, select the channel by issuing CMD_CHi to set the read/write pointer. The status register bits CONFIG_CH_PTR[3:0] show the channel pointer location. A total of 16 logical channels are available: CH0..CH15.

Table 27. 16-bit channel-based configuration

Register(16-bit)	Bit order	Bit name	RW	Reset	Short description
CH_CONFIG0 0x20\h	15:12	HV_AIP[3:0]	RW	0x0	HV Positive input pin select: 0\h = internal GND, 1\h = AI1P, 2\h = AI2P, 3\h = AI3P, 4\h = AI4P, 5\h = REFH, 6\h = REFL, 7\h = AICOM, 8\h = not used, 9\h to F\h = not used.
	11:8	HV_AIN[3:0]	RW	0x0	HV Negative input pin select: 0\h = internal GND, 1\h = AI1N, 2\h = AI2N, 3\h = AI3N, 4\h = AI4N, 5\h = REFH, 6\h = REFL, 7\h = AICOM, 8\h = not used, 9\h to F\h = not used.
	7:5	CH_GAIN[2:0]	RW	0x0	Select the channel gain (V/V): 0\h = 0.2x, 1\h = 0.4x, 2\h = 0.8x, 3\h-7\h = unused.
	4	HV_SEL	RW	0x0	Select HV or LV signals for ADC conversion: 0 = LVSIG_IN, 1\h = HV_AIP-HV_AIN signals.
	3:1	LVSIG_IN[2:0]	RW	0x0	LV signals (pos, neg) select: 0\h = (REF/2,REF/2), 1\h = (GPIO0,GPIO1), 2\h = (REF_Coarse,REF/2), 3\h = (VADD,REF/2), 4\h = (VHDD,REF/2), 5\h = (REF/2,VHSS),
	0	TCC_OFF	RW	0x0	Proprietary Channel Temperature Coefficient Correction: 0\h = TCC ON, 1\h = TCC OFF
CH_CONFIG1 0x21\h	15:12	CH_CAL_GAIN_OFFSET[3:0]	RW	0x0	The pointer to select 1 of 16 calibrated gain and offset coefficient pairs in the Calibrated Channel Coefficient Registers. SeeTable 13 .
	11:8	CH_THRS[3:0]	RW	0x0	Channel Over- and under-range threshold: See Table 28.
	7:3	ADC_DATA_RATE[4:0]	RW	0x00	ADC data rate: See Table 6
	2:0	ADC_SINC[2:0]	RW	0x0	ADC sinc filter select 0\h = bypass, 1\h = SINC1, 2\h = SINC2, 3\h = SINC3, 4\h = SINC4, 5\h to 7\h = bypass.
CH_CONFIG2 0x22\h	15:10	CH_DELAY[5:0]	RW	0x0	Preset channel delay before ADC start conversion: (# of SYSCLK cycle) 0\h = 0, 1\h = 2, 2\h = 4, 3\h = 6, 4\h = 8, 5\h = 10, 6\h = 12, 7\h = 14, 8\h = 16, 9\h = 18, A\h = 20, B\h = 28, C\h = 38, D\h = 40, E\h = 42, F\h = 56, 10\h = 64, 11\h = 76, 12\h = 90, 13\h = 128, 14\h = 154, 15\h = 178, 16\h = 204, 17\h = 224, 18\h = 256, 19\h = 358, 1A\h = 512, 1B\h = 716, 1C\h = 1024, 1D\h = 1664, 1E\h = 3276, 1F\h = 7680, 20\h = 19200, 21\h-3F\h = 23040.
	9	ADC_NORMAL_SETTLING	RW	0x0	ADC single-cycle settling or Normal Settling: 0\h = Single-cycle settling(SCS), 1\h = Normal settling(NS)
	8	ADC_FILTER_RESET	RW	0x0	Reset ADC digital filters at the start of every ADC conversion when set. 0\h = hold digital filter data from previous conversion, 1\h = reset digital filters.
	7	CH_CHOP	RW	0x0	Enable input channel level chopping with 2 ADC conversions (Precision mode): 0\h = Normal mode, 1\h = Precision mode with 2 conversions chopping
	6:0	reserved			
CH_CONFIG3 0x23\h	15:0	reserved	RW	0x0	
CH_CONFIG4 0x24\h	15:0	MCH_EN[15:0]	RW	0x0000	Enable logical configurable channel for ADC conversion in Sequencer mode: 0 = disable, 1 = enable. CH15 is bit15, CH0 is bit0.

7.9.2 24-bit channel-based coefficient and data registers

24-bit channel-based registers:

- Output data: DATA0..15
- Over-range alarm threshold: OVR_THRS0..15
- Under-range alarm threshold: UDR_THRS0..15
- Factory or user-calibration gain coefficients: GCC0..15
- Factory or user-calibration offset coefficients: OCC0..15

The non-channel based registers OPTC0..15 are optional coefficients used for storing factory calibrated parameters.

Table 28. 24-bit channel-based coefficient and data registers

Register (24-bit)	Bit order	Bit name	RW	Reset	Short description
CH_DATA0..15 0x40\h - 0x4F\h	23:0	DATA0[23:0] .. DATA15[23:0]	R	0x00_0000	Channel output data. Each channel has a corresponding data register. DATA0[23:0] is converted output of CH0.. DATA15[23:0] is converted output of CH15.
CH_CONFIG5 0x50\h - 0x5F\h	23:0	OVR_THRS0[23:0] .. OVR_THRS15[23:0]	RW	0x00_0000	Over-range threshold setting for each logical data channel.
CH_CONFIG6 0x60\h 0x6F\h	23:0	UDR_THRS0[23:0] .. UDR_THRS15[23:0]	RW	0x00_0000	Under-range threshold setting for each logical data channel.
GAIN_COEF0..15 0x80\h-0x8F\h	23:0	GCC[23:0]	RW	0x	Calibrated gain coefficients. The user may alter or update the values to fit their application. For each of the logical channel setup, these GAIN_COEF registers are indexed addressable by pointer set by register bits CH_CAL_GAIN_OFFSET[4:0]. Initially after CHIP_READY, the content of these registers are populated with factory-calibrated coefficients, refer to TABLE_FAC_COEF if applicable. ***Note:*** *Whenever the chip is in RESET, the factory-calibrated coefficient is reloaded from OTP into the registers. These same registers are used for displaying the factory calibrated coefficient upon RESET in certain order. However, the user has full read/write access and may reshuffle the order and coefficient values according to user-configured channels.*
OFFSET_COEF0..15 0x90\h-0x9F\h	23:0	OCC[23:0]	RW	0x	Calibrated offset coefficients. The user may alter or update the values to fit their application. For each of the logical channel setup, these OFFSET_COEFF registers are indexed addressable by pointer set by register bits CH_CAL_GAIN_OFFSET[4:0]. Initially after CHIP_READY, the content of these registers are populated with factory-calibrated coefficients, refer to TABLE_FAC_COEF if applicable. ***Note:*** *Whenever the chip is in RESETx, the factory-calibrated coefficient is reloaded into the registers from OTP. These same registers are used for displaying the factory-calibrated coefficient upon RESETx in certain order. However, the user has full read/write access and may reshuffle the order and values, then update CH_CAL_GAIN_OFFSET accordingly.*
OPT_COEF0..13 0xA0\h-0xAD\h	23:0	OPTC[23:0]	RW	0x00_0000	Extra register for temporary storing coefficients, eg it can be used as Self-calibrated ADC values with internal VREF and REFH, REFL at CH_GAIN or Calibrated values with Excitation sources. See Table 12.

7.9.3 System-level configurations and status registers

Table 29. System-level configurations and status registers

Register (16-bit)	Bit order	Bit name	RW	Reset	Short description
CRC_CONF_REGS 0x25\h	15:0	CRC_CONF_REGS[15:0]	R	0x0000	Integrated CRC result of all Configuration registers.

Table 29. System-level configurations and status registers*...continued*

CRC_COEF_REGS 0x26\h	15:0	CRC_COEF_REGS[15:0]	R	0x0000	Integrated CRC result of all user's coefficient registers.
CRC_TRIM_REGS 0x27\h	15:0	CRC_TRIM_REGS[15:0]	R	0x0000	Integrated CRC result of all factory trim OTP registers.
Register (16-bit)	**Bit order**	**Bit name**	**RW**	**Reset**	**Short description**
CH_STATUS0 0x35\h	15:0	CH_OVR[15:0]	R	0x0000	Channel over-range, logical CH15 is bit 15, CH0 is bit 0.
CH_STATUS1 0x36\h	15:0	CH_UDR[15:0]	R	0x0000	Channel under-range, logical CH15 is bit 15, CH0 is bit 0.
Register (16-bit)	**Bit order**	**Bit name**	**RW**	**Reset**	**Short description**
GPI_DATA 0x29\h	15:6	GPI_DATA[9:0]	R	0x0000	GPI data detected: 0 = Logic 0(DGND), 1 = Logic 1(DVDD). GPIO9 is bit15, GPIO0 is bit6.
	5:0	reserved			
GPIO_CONFIG0 0x2A\h	15:6	GPO_ENABLE[9:0]	RW	0x0000	GPO driving enable: 0 = disabled driving, 1 = enabled driving. GPIO9 is bit15, GPIO0 is bit6.
	5:0	reserved			
GPIO_CONFIG1 0x2B\h	15:6	GPIO_CON[9:0]	RW	0x0000	GPIO connect to pin: 0 = disconnect from pin, 1 = connect to pin. GPIO9 is bit15 GPIO0 is bit6.
	5:0	reserved			
GPIO_CONFIG2 0x2C\h	15:6	GPI_ENABLE[9:0]	RW	0x0000	GPI read enable: 0 = disabled read, 1 = enabled read. GPIO9 is bit15, GPIO0 is bit6.
	5:0	reserved			
GPI_EDGE_POS 0x2D\h	15:6	GPI_EDGE_POS[9:0]	R	0x0000	GPI positive edge(s) data: 0\h = none, 1\h = positive edge detected. Cleared after readback or CMD_CLEAR_ALRM.
	5:0	reserved			
GPI_EDGE_NEG 0x2E\h	15:6	GPI_EDGE_NEG[9:0]	R	0x0000	GPI negative edge(s) data: 0\h = none, 1\h = negative edge detected. Cleared after readback or CMD_CLEAR_ALRM.
	5:0	reserved			
GPO_DATA 0x2F\h	15:6	GPO_DATA[9:0]	RW	0x0000	Set GPO output data: 0\h = output logic 0, 1\h = output logic 1. GPIO9 is bit15, GPIO0 is bit6.
	5:0	reserved			
Register (16-bit)	**Bit order**	**Bit name**	**RW**	**Reset**	**Short description**
SYS_CONFIG0 0x30\h	15	DRDY_PWDT	RW	0x0	DRDY pulse width duration (# of SYSCLK cycle): 0\h = 2, 1\h = 8
	14	ADC_DATA_OUT_16BIT	RW	0x0	ADC data register readout: 0\h = 24 bit, 1\h = 16 bit
	13	STATUS_STICKY			Prepended status bits behavior when bursting output data with STATUS_EN = 1. 0\h = Sticky, 1\h = Live (sampling at rising edge of DRDY).
	12	MCLK_OUT_ENABLE	RW	0x0	Enable the master clock(2*SYSCLK) output to GPIO9 pin. This bit supersedes and ignores the other GPIO9 setting.
	11:10	REF_SEL[1:0]	RW	0x0	**Select** to use Internal(REF_INT) or External(REF_EXT) 2.5 V voltage references for REF_BYP(of PGA) and REF_ADC(of ADC): **0\h** = Both REF_BYP and REF_ADC use REF_INT. **1\h** = REF_BYP uses REF_INT and REF_ADC uses REF_EXT. **2\h** = REF_BYP uses REF_EXT and REF_ADC uses REF_INT. **3\h** = REF_BYP uses REF_EXT and REF_ADC uses REF_EXT. ***Note:*** *Internal reference is always powered on.*
	9:8	CK_SRC_SEL[1:0]	RW	0x0	Select clock sources: 0\h = internal clock, 1\h = internal clock, and disable crystal oscillator circuit. 2\h = applied external 18.432 MHz clock at XI pin, and disable crystal oscillator circuit. 3\h = 18.432MHz Crystal is installed at XI, XO pins.
	7	CRC_EN	RW	0x0	Enable CRC: 0\h = disable, 1\h = enable.

Table 29. System-level configurations and status registers*...continued*

	6	STATUS_EN	RW	0x0	To prepend 8-bit Live status bits to ADC data of enabled channels, MCH_EN[i] = 1. In Multichannel Read mode, the first 8 bits status bits is OR'd of the channels when in data output burst. SPI data: <status_8b><CH_DATAi>,<status_8b><CH_DATAj>... ***Note:*** *Live status bits(MSB to LSB): overload, underload, over-range, under-range, overtemperature, global_alarm, overvoltage, CRC error.*
	5	ADC_SYNC	RW	0x0	ADC Synchronization mode enabled for host-driven with SYNC pulse at pin. This works with all conversion modes. 0\h = disabled SYNC pin, 1\h = ADC is synchronized to SYNC pulse at rising edge and used as conversion start trigger
	4	DRDY_PIN_EDGE			To set the behavior of DRDY pin; especially in Multichannel modes, 0\h = produce rising edge on every channel conversion done, 1\h = produce rising edge only when the sequencer is done with the last enabled channel conversion.
	3	GLOBAL_ALRM_STICKY	RW	0x0	Global alarm interrupt default behavior is: 0\h = cleared when global alarm register is read, 1\h = Write 0 to clear a specific bit.
	2	SPI_DOUT_DRIVE	RW	0x0	Increase DOUT output drive if high capacitance loading.
	1	INTB_DRIVER_TYPE	RW	0x0	INTB pin driver type: 0 = 100 Kohm pullup with open drain, 1 = CMOS push-pull.
	0	CRC_ERROR_ON_GPIO2	RW	0x0	To enable routing of CRC_ERROR interrupt to GPIO2 pin. 0\h = normal GPIO function 1\h = Output CRC_ERROR to GPIO2 pin, active high.
SYS_STATUS0 0x31\h	15	SINGLE_CH_ACTIVE	R	0x0	Single-channel conversion mode indicator, which includes CH_DELAY. 0\h = idle, 1\h = active.
	14	MULTI_CH_ACTIVE	R	0x0	Multichannel Conversion mode indicator, which includes CH_DELAY. 0\h = idle, 1\h = active.
	13	CHIP_READY	R	0x0	Chip status indicator. Upon power up, INTB pin will go LO (active low) to indicate the chip is ready. User is to read this register to clear INTB pin. This bit will stay HI when the chip is operational. 0\h = Chip is not yet ready, 1\h = Chip is ready.
	12	CRC_ERROR	R	0x0	CRC error encountered
	11:8	CONFIG_CH_PTR[3:0]	R	0x0	The selected logical channel for R/W access to CH_CONFIG0,1,2,3 registers. (Pointer is controlled by SPI CMD_CHx)
	7:4	ADC_CONV_CH[3:0]	R	0x0	The current active logical channel.
	3:0	reserved			
Register (16-bit)	**Bit order**	**Bit name**	**RW**	**Reset**	**Short description**
GLOBAL ALARM ENABLE 0x32\h	15	OVER_TEMP_ALRM	RW	0x0	Overtemperature warning at 145 ℃.
	14	HVDD_ALRM	RW	0x0	Enable alarm for HVDD supply detect below preset threshold.
	13	HVSS_ALRM	RW	0x0	Enable alarm for HVSS supply detect below preset threshold.
	12	ADVDD_ALRM	RW	0x0	Enable alarm for DVDD supply detect below preset threshold.
	11	reserved	RW	0x0	
	10	GPI_POS_ALRM	RW	0x0	Enable alarm for rising edge detected at any of GPI pins.
	9	GPI_NEG_ALRM	RW	0x0	Enable alarm for falling edge detected at any of GPI pins.
	8	CONFIG_ERROR_ALRM	RW	0x0	Enable alarm for register configuration error.
	7	OVRRNG_ALRM	RW	0x0	Enable alarm for one or more data channel is over-range.
	6	UNDRNG_ALRM	RW	0x0	Enable alarm for one or more data channel is under-range.
	5	OVRLOAD_ALRM	RW	0x0	Enable alarm for one or more data channels is over-loaded or under-loaded.
	4	EXTCLK_FREQ_ALRM	RW	0x0	Enable alarm when XTAL or EXTCLK frequency varies with internal CLK by XX.
	3	reserved			
	2	reserved			

Table 29. System-level configurations and status registers*...continued*

	1	reserved			
	0	TEMP_ALRM	RW	0x0	Enable programmable temperature alarm; the triggering threshold is set in THRS_TEMP register bits.
GLOBAL ALARM INTERRUPT 0x33\h	15	OVER_TEMP_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY
	14	HVDD_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY
	13	HVSS_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY
	12	ADVDD_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY
	11	reserved			
	10	GPI_POS_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY
	9	GPI_NEG_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY
	8	CONFIG_ERROR_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY
	7	OVRRNG_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY
	6	UNDRNG_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY
	5	OVRLOAD_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY
	4	EXTCLK_FREQ_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY
	3	reserved			Bit clear behavior controlled by GLOBAL_ALRM_STICKY
	2	reserved			
	1	reserved			
	0	TEMP_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY
Register (16-bit)	**Bit order**	**Bit name**	**RW**	**Reset**	**Short description**
DIE_TEMP 0x34\h	15:0	DIE_TEMP[15:0]	R	0x	16-bit die temperature readout in 2's complement. The temperature could be calculated with the following formula: Die_temp(ºC) = code_decimal/64
THRS_TEMP 0x37\h	15:0	THRS_TEMP[15:0]	RW	0x0000	Temperature threshold in 2's complement for setting custom temperature alarm.
Register (16-bit)	**Bit order**	**Bit name**	**RW**	**Reset**	**Short description**
PN2 0x7C\h	15:0	PN2[15:0]	R	0x	Part Number (MSB). Example, 7138 for NAFE71388B40BS part number
PN1 0x7D\h	15:0	PN1[15:0]	R	0x	Part Number (MidLSB). Example, 8B40 for for NAFE71388B40BS
PN0 0x7E\h	15:8	PN0[15:8]	R	0x	reserved
	7:0	REVISION_ID[7:0]	R	0x	Revision
Register (24-bit)	**Bit order**	**Bit name**	**RW**	**Reset**	**Short description**
SERIAL1 0xAE\h	23:0	SN1[23:0]	R	0x	Unique Serial Number (MSB)
SERIAL0 0xAF\h	23:0	SN0[23:0]	R	0x	Unique Serial Number (LSB)
Register (16-bit)	**Bit order**	**Bit name**	**RW**	**Reset**	**Short description**
CRC_TRIM_INT 0x7F\h	15:0	CRC_TRIM_INT[15:0]	R	0x	CRC sum of internal trims, to be used for comparison against CRC_TRIM_REGS[15:0].

8 Limiting values

8.1 Maximum rating

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may lead to malfunction or permanent damage to the device.

Table 30. Absolute maximum rating [1]

Description	Min	Max	Units
HVDD to AGND[2]	-0.3	29	V
AGND to HVSS[2]	-0.3	29	V
HVDD to HVSS	-0.3	55	V
AVDD to AGND	-0.3	5.5	V
DVDD to DGND	-0.3	5.5	V
AGND to DGND	-0.3	0.3	V
AI1P, AI2P, AI3P, AI4P, AI1N, AI2N, AI3N, AI4N, AICOM to HVSS[3]	-0.3	46	V
HVSS to AI1P, AI2P, AI3P, AI4P, AI1N, AI2N, AI3N, AI4N or AICOM, with external 2.5 kΩ resistor in series for current limit with a duration of less than one hour.[3]	-60	36	V
HVDD to AI1P, AI2P, AI3P, AI4P, AI1N, AI2N, AI3N, AI4N, AICOM[3]	-0.3	46	V
HVDD to AI1P, AI2P, AI3P, AI4P, AI1N, AI2N, AI3N, AI4N or AICOM, with external 2.5 kΩ resistor in series for current limit with a duration of less than one hour.[3]	-36	60	V
REFH, REFL to AGND[4]	-0.3	VREF_BYP ± 0.1	V
REF_BYP, REFP_ADC, REFN_ADC to AGND[5]	-0.3	VAVDD	V
GPIO0.. GPIO9 to DGND[5][6]	-0.3	VDVDD + 0.3	V
CAPP, CAPN to AGND[7]	–	–	V
EXTCLK/XI, XO to DGND	-0.3	VDVDD + 0.3	V
SPI_ADDR, SCLK, MOSI, MISO, CSB, SYNC, RSTB to DGND[5]	-0.3	VDVDD + 0.3	V
LDO_DIG to DGND[3]	-0.3	2.1	V
REF_EXT, REF_NR, REF_INT to AGND[5]	-0.3	VAVDD + 0.3	V

[1] These are stress ratings at room temperature only. Functional operation of the product with conditions at or above its maximum ratings is not implied. Device reliability may be affected if stressed at or beyond limits for extended periods.
[2] Supply pins HVDD-AGND and AGND-HVSS are dc-clamped to 29 V.
[3] Pins AIxP, AIxN, AICOM are not to exceed HVDD or HVSS by 46 V. In limited testing at room temperature, these pins could sustain up to 60 V at ±24 mA with 2.5 kΩ external series resistor for duration of up to one hour.
[4] Output pins REFH, REFL are diode-clamped to REF_BYP and AGND internally.
[5] Low voltage input and output pins are diode-clamped to their respective power supplies and/or ground: The current is limited to ±10 mA whenever the voltage at pin is 0.3 V (a) above AVDD/DVDD or (b) below AGND/DGND.
[6] Digital output pins, current limit is ±10 mA.
[7] Analog buffered signal output pins CAPP, CAPN are with common-mode voltage of 1.4 V-1.6 V typical. Only a differential capacitor connection is recommended. Any other loading will affect the device functionality adversely.

8.2 ESD stress rating and latch-up

Table 31. ESD stress rating and latch-up

Description	Max	Units
Human body model (HBM) on all pins	±8000	V
Charged device model (CDM) on all pins	±1000	V
Latch-up at 125 ºC	±250	mA

Note: *These are stress ratings only. Functional operation of the product at conditions at or above its ratings is not implied.*

9 Thermal characteristics

Table 32. Thermal characteristics

Description	Symbol	Min	Typ	Max	Units
Operating temperature Ambient Junction	 TA TJ	 -40 -40		 +125 +150	 °C
Storage temperature	TSTO	-55		+150	°C
Peak package reflow temperature[1] [2]	TPPRT			+260	°C
Junction to case (bottom exposed pad soldered to board)[3]	$R_{\theta JC}$		+2		°C/W
Junction to ambient[4]	$R_{\theta JA}$		+24		°C/W
Junction to top of package	Ψ_{JT}		+1		°C/W

[1] Pin soldering temperature limit is 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.

[2] NXP's package reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For peak package reflow temperature and moisture sensitivity levels (MSL), go to https://www.nxp.com/, search by part number (remove prefixes/ suffixes) and enter the core ID to view all orderable parts and parametric.

[3] Junction-to-case thermal resistance was determined using an isothermal cold plate. Case temperature refers to the exposed pad surface temperature at the package bottom side dead center.

[4] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.

10 Electrical characteristics

All specifications are at VHVDD = -VHVSS = 15 V; VAVDD = VDVDD = 3.3 V; internal reference. Typical values are at TA = 40 ºC, ADC at 6 kSPS in Normal Settling mode with 500 samples averaging; each HV analog input (AIxP, AIxN, AICOM) is connected to an external 2.5 kΩ resistor in series with 1 nF capacitor connected to GND. See Figure 44. Offset, gain error, and INL parametric are input-referred to AIxP, AIxN pins w.r.t. AICOM pin, and characterized to the input full-scale (FS) in single-ended configuration at specified gain, unless otherwise stated. The minimum and maximum specifications cover TA = -40 ºC to +125 ºC.

TUE [V/V] = (GEv + OE + INL) / FS, where FS is 10 V, 5 V, 2.5 V for channel gain of 0.2 V/V, 0.4 V/V, and 0.8 V/V, respectively. GEv is gain error expressed in [V] as GE*FS.

Table 33. HV input ranges

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIN(SE)	Input voltage nominal range (single-ended)	PGA2: Channel gain = 0.8 V/V (±3.125 V single-ended full-range setting)	-2.5		2.5	V
		PGA1: Channel gain = 0.4 V/V (±6.25 V single-ended full-range setting)	-5.0		5.0	
		PGA0: Channel gain = 0.2 V/V (±12.5 V single-ended full-range setting)	-10.0		10.0	
VIN(DF)	Input voltage nominal range (Differential)	PGA2: Channel gain = 0.8 V/V (±6.25 V differential full-range setting)	-5.0		5.0	V
		PGA1: Channel gain = 0.4 V/V (±12.5 V differential full-range setting)	-10.0		10.0	
		PGA0: Channel gain = 0.2 V/V (±25 V differential full-range setting)	-20.0		20.0	

Table 34. HV input accuracy before calibration

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TUE_Ai	Total unadjusted error at room	Initial accuracy without factory CAL coefficients. Single-ended inputs. Internal reference, TA = +40 °C		±0.5	±1.2	% FS
TUE_OTi	Total unadjusted error overtemperature	Initial accuracy without factory CAL coefficients. Single-ended inputs. Internal reference, TA = -25 °C to +105 °C		±0.6	±1.3	% FS
OEi	Offset error	Calibrated offset error without factory CAL coefficients. Single-ended inputs. Internal reference, TA = +40 °C				mV
		G = 0.8 V/V		±5	±10	
		G = 0.2 V/V		±20	±40	
GEi	Gain error	Calibrated gain error without factory CAL coefficients. Single-ended inputs. Internal reference, TA = +40 °C				% FS
		G = 0.8 V/V		±0.2	±1	
		G = 0.2 V/V		±0.2	±1	
INL	INL error	TA = +40 °C				µV
		G = 0.8 V/V		±10	±50	
		G = 0.2 V/V		±50	±200	
E_VHi	REFH Error	Initial accuracy without factory CAL coefficients, REFH to AGND. Measured with internal ADC, internal reference, G = 0.2 V/V, single-ended mode. TA = +40 °C. CH_CHOP = 1, TCC_OFF = 1.		±1		%
E_VLi	REFL Error	Initial accuracy without factory CAL coefficients, REFL to AGND. Measured with internal ADC, internal reference, G = 0.8 V/V, single-ended mode. TA = +40 °C. CH_CHOP = 1, TCC_OFF = 1.		±1		%

Table 35. HV input accuracy after calibration

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TUE_AT	Total unadjusted error at room[1]	Total accuracy after user calibration TUE[V/V]=(OE+GEv+INL)/FS		±0.002	±0.005	% FS
		Total accuracy with Factory calibration TUE[V/V]=(OE+GEv+INL)/FS		±0.06	±0.15	
TUE_OT	Total unadjusted error over temperature[1]	Total accuracy after user calibration at 40°C, Internal voltage reference, TCC_OFF = 0, TA = -25°C to +105°C		±0.05	±0.1	% FS
		Total accuracy with Factory calibration, Internal voltage reference, TCC_OFF = 0, TA = -25 °C to +105 °C		±0.11	±0.22	% FS
OE	Calibrated offset error	Calibrated offset error with Factory calibration, single-ended inputs, Internal voltage reference, TA = +40°C				µV
		G = 0.8 V/V		±25	±75	
		G = 0.2 V/V		±50	±300	
GE	Calibrated gain error[1]	Gain Error after user calibration, TA = +40 °C		±0.0		% FS
		Gain Error with Factory calibration, G = 0.8 V/V, TA = +40 °C		±0.05	±0.14	
		Gain Error with Factory calibration, G =0.2 V/V, TA = +40 °C		±0.05	±0.14	
INL	INL error	Internal voltage reference, TA = +40 °C				µV
		G = 0.8 V/V		±10	±50	
		G = 0.2 V/V		±50	±200	
E_VH	Calibrated REFH (w.r.t. stored NVM value)	REFH to AGND, measured with Internal voltage reference and ADC with factory CAL coefficients, G = 0.2 V/V, single-ended mode, CH_CHOP = 1, TCC_OFF = 1, TA = +40 °C.		±0.01	±0.03	%
E_VL	Calibrated REFL (w.r.t. stored NVM value)	REFL to AGND, measured with Internal voltage reference and ADC with factory CAL coefficients, G = 0.8 V/V, single-ended mode, CH_CHOP = 1, TCC_OFF = 1, TA = +40 °C.		±0.01	±0.03	%

[1] An initial accuracy error could be affected by mechanical stress post assembly. To meet certain accuracy specifications, a 1-point gain or 2-point full calibration could be required. The user-calibrated accuracy is typically limited by NAFE integral non-linearity (INL) of the device at chosen ADC data rate, and additional errors could arise from other test setup and conditions.

Table 36. HV input temperature and aging drift characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TDE	TUE drift	Single-ended inputs. Internal reference, TA = -25 °C to +105°C. TCC_OFF = 0		±3	±10	ppm/°C
		Single-ended inputs. Internal reference, TA = -40 °C to +125°C. TCC_OFF = 0		±3	±10	ppm/°C
OD	Offset drift	All single-ended inputs and ranges. TA = -40 °C to 125°C				µV/°C
		G = 0.8 V/V		±0.4	±1.5	
		G = 0.2 V/V		±1.6	±6	
		G = 0.2 V/V, CH_CHOP=1, TCC_OFF=0		±0.02		
GD	Gain drift	External VREF and TCC_OFF = 1		±1	±2	ppm/°C
		Internal VREF and TCC_OFF = 0		±3	±8	ppm/°C
GD_{750hr}	Gain drift over time[1]	External VREF and TCC_OFF = 1		±25		ppm over 750 h
		Internal VREF and TCC_OFF = 0		±490		ppm over 750 h
INLD	INL drift	Internal VREF -25 °C to +105 °C				µV/°C
		G = 0.8 V/V		±0.1	±0.3	
		G = 0.2 V/V		±0.3	±1.0	
VHD	Calibrated REFH drift	REFH to AGND, measured with ADC with factory CAL coefficients, internal reference and G = 0.2 V/V, CH_CHOP = 1, TCC_OFF = 1. TA = -25 °C to +105 °C.		±1		ppm/℃
VLD	Calibrated REFL drift	REFL to AGND, measured with ADC with factory CAL coefficients,, internal reference and G = 0.8 V/V, CH_CHOP = 1, TCC_OFF = 1. TA = -25 °C to +105 °C.		±1		ppm/℃

[1] Data is based on standard high-temperature operating life (HTOL) method.

Table 37. HV input channel characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Input crosstalk DC	Tested input at 0 V with one aggressor channel at ± 10V, TA = +40 °C		±1		µV/V
	Input crosstalk dynamic	VAIxP = +10 V switch to VAIyN = -10 V, SCS, DRO = 24 ksps, CH_DELAY = 8.2 us. TA = +40 °C.		±1		µV/V
T_{switch}	Channel switch time	V_{IN} changes from one input to another input, G = 0.2 V/V ADC output code settles within 0.01 % of final value. ADC_NORMAL_SETTLING = 0, 24 ksps, SINC4 filter, single-ended input -10 V to +10 V and +10 V to -10 V.		8.5		µs
V_{noise}	Input voltage noise	Inputs shorted to GND				µVrms
		ADC in Normal Settling mode versus data rate and channel gain		See Section 7.3.5.7		
		ADC in Normal Settling mode, 1.125 ksps, G = 0.8 V/V		3.4		
		ADC in Normal Settling mode, 1.125 ksps, G = 0.2 V/V		13.2		
Vhr	High-voltage headroom	VHVDD above positive input linear range of +10 V, G = 0.2 V/V	3.8			V
		VHVSS below negative input linear range of -10 V, G = 0.2 V/V	3.8			
CMR_{DC}	Common-mode rejection	Shorted differential inputs pair. V_{CM} = -1 V to +1 V DC. DRO = 1.125 ksps				dB
		G = 0.8 V/V		92		
		G = 0.2 V/V		80		
$CMR_{50/60}$	Common-mode rejection	Shorted differential inputs pair. V_{CM} = -1 V to +1 V 50Hz/60Hz. DRO = 10 sps, SINC4 filter				dB
		G = 0.8 V/V		172		
		G = 0.2 V/V		160		
$PSRR_{HV}$	Power-supply rejection ratio (RTI)	Shorted differential DC Inputs at 0V, V_{HVDD} = +15 V to +24 V, VHVSS = -24 V to -15 V				dB
		G = 0.8 V/V		124		
		G = 0.2 V/V		112		
		G = 0.2 V/V, CH_CHOP = 1		160		
$PSRR_{LV}$	Power-supply rejection ratio (RTI)	Shorted differential DC Inputs at 0 V, VAVDD = VDVDD = 3 V to 3.6 V				dB
		G = 0.8 V/V		78		
		G = 0.2 V/V		66		
		G = 0.2 V/V, CH_CHOP = 1		120		
RIN	Input impedance	VAIxP, VAIxN pins, TA = +40 °C		1000		MΩ
IL	Input leakage current	Any single input switch in on-state, TA = -40 °C to +105 °C		1	5	nA
		Any single input switch in on-state, TA = -40 °C to +125 °C		5	15	

Table 38. LV MUX inputs/GPIO0-GPIO1 as analog input

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LV MUX INPUTS						
	Power supplies accuracy	HVDD, HVSS and DVDD through ADC readback. HV_SEL = 0		±2		%
	REF_COARSE accuracy	REF2 through ADC readback. HV_SEL = 0		±2		%
	GND_LV	0 V through ADC readback. HV_SEL = 0		±100		µV
GPIO0-GPIO1 as analog input						
	Analog input signal range	Full Range 1.5V ± 1V	0.5		2.5	V
	Offset error	HV_SEL = 0. Linear range 1.5 V ± 0.8 V		±100		µV
	Gain error	HV_SEL = 0. Linear range 1.5 V ± 0.8 V		±0.7		%

Table 39. Temperature sensor

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Temperature sensor resolution	Die temperature		1/64		°C
	Temperature sensor accuracy	Die temperature		±3		°C

Table 40. Internal voltage reference (VREF)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VREF	Output voltage[1]	Internal reference, REFP_ADC pin.		2.496		V
	Initial accuracy	Internal reference voltage, TA = +40 °C	-0.5		0.5	%
TC_{VREF}	Temperature coefficient	TA = -25 °C to +105 °C		±8		ppm/°C
		TA = -40 °C to +125 °C		±12		
LTS	Long-term stability[2]			±490		ppm over 750 h
	Load regulation	0.1 mA sourcing current load at REF_BYP pin.		±0.5		mV/mA
S_{VREF}	Supply regulation	3V ≤ V_{AVDD} ≤ 3.6 V. REFP_ADC pin.		±10		µV/V

[1] An initial accuracy error could be affected by mechanical stress post assembly.
[2] Data is based on standard high-temperature operating life (HTOL) method.

Table 41. Clock oscillators

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Clock frequency accuracy	Internal oscillator		±0.2	±1.1	%
	Input clock duty cycle	External clock applied to XIN pin. Frequency = 18.432 MHz	45	50	55	%
	Crystal oscillator startup time	18.432MHz crystal. capacitive load = 12 pF.		5		ms

Table 42. Power supplies

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{HV}	High-voltage supply	V_{HVDD} - V_{HVSS}	14		48	V
V_{HVDD}	Positive high-voltage supply[1]	Referenced to AGND	7.0		28	V
V_{HVSS}	Negative high-voltage supply[1]	Referenced to AGND	-28		-7.0	V
V_{VDD}	Low-supply voltage	VDD = VAVDD = VDVDD, HVDD = -HVSS = 15 V. referenced to AGND	2.97	3.3	3.63	V
I_{VDD}	Low-voltage supply quiescent current	I(AVDD) + I(DVDD)		13	16	mA
I_{HVDD}	Positive high-voltage supply quiescent current	Default setting, All AIxP, AIxN inputs are at 0 V, HVDD = -HVSS = 15 V		3.3	3.65	mA
I_{HVSS}	Negative high-voltage supply quiescent current	Default setting, All AIxP, AIxN inputs are at 0 V, HVDD = -HVSS = 15 V		3.0	3.65	mA
	Total quiescent power	Default setting, All AIxP, AIxN inputs are at 0 V. HVDD = -HVSS = 15 V		135	160	mW

[1] Not production tested and only limited samples were verified at ± 28 V supplies.

Table 43. GPIO and digital I/O pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIH	Logic high-input voltage		0.7*VDVDD			V
VIL	Logic low-input voltage				0.3*VDVDD	V
	Input-voltage hysteresis			0.3		V
VOH	Logic high-output voltage	IOH = 1 mA	0.8*VDVDD			V
VOL	Logic low-output voltage	IOL = -1 mA			0.2*VDVDD	V

Table 44. SPI timing and characteristics

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, typical values are at TA = 25 ºC, unless otherwise specified. Capacitive loading should be < 20 pF on the digital output pin.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{SCLK}	SCLK frequency				32	MHz
t_{SCLK_H}	SCLK high pulse width		15.5			ns
t_{SCLK_L}	SCLK low pulse width		14.5			ns
t_{CWH}	CSB high pulse width	CSB high pulse width	32			ns
t_{IS}	MOSI setup time	Time to SCLK falling edge	5			ns
t_{IH}	MOSI hold time	Time after SCLK falling edge	5			ns
t_{OT}	MISO transition time	Time after SCLK rising edge		10.5	14	ns
t_{CFS}	CSB falling setup time	Time before SCLK first rising edge	5		25	ns
t_{CRE}	CSB rising edge time	Time after the last SCLK falling edge	5		25	ns

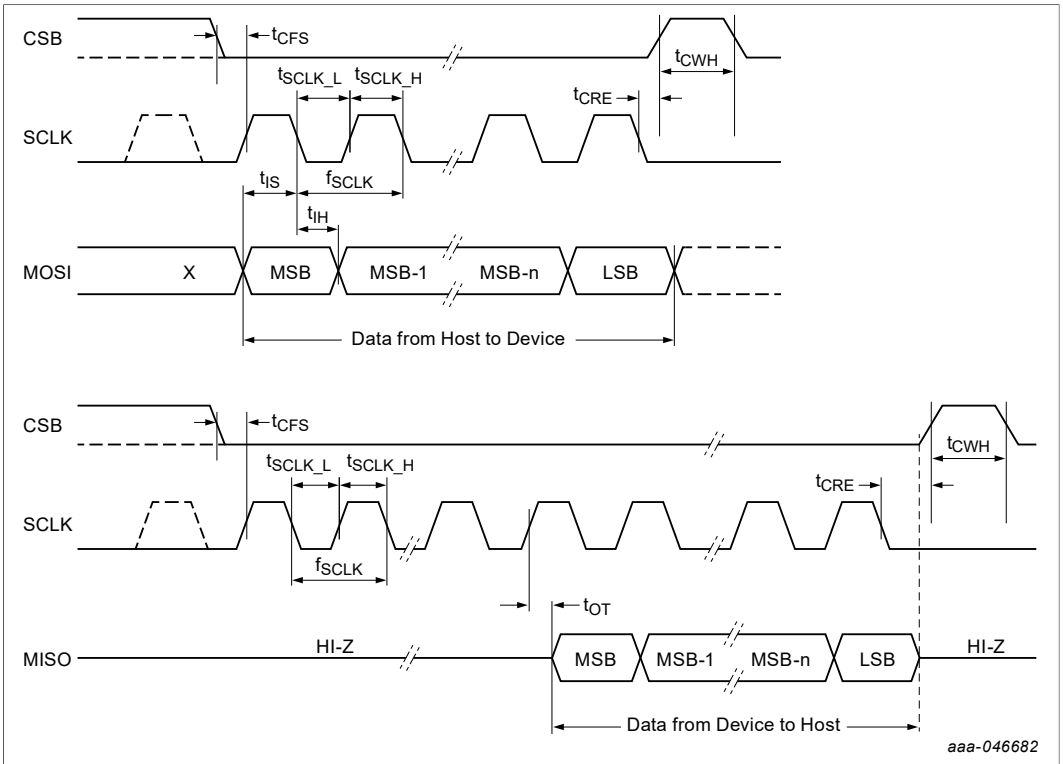


Figure 43. SPI timing parameters

11 Application information

11.1 Typical application block diagram

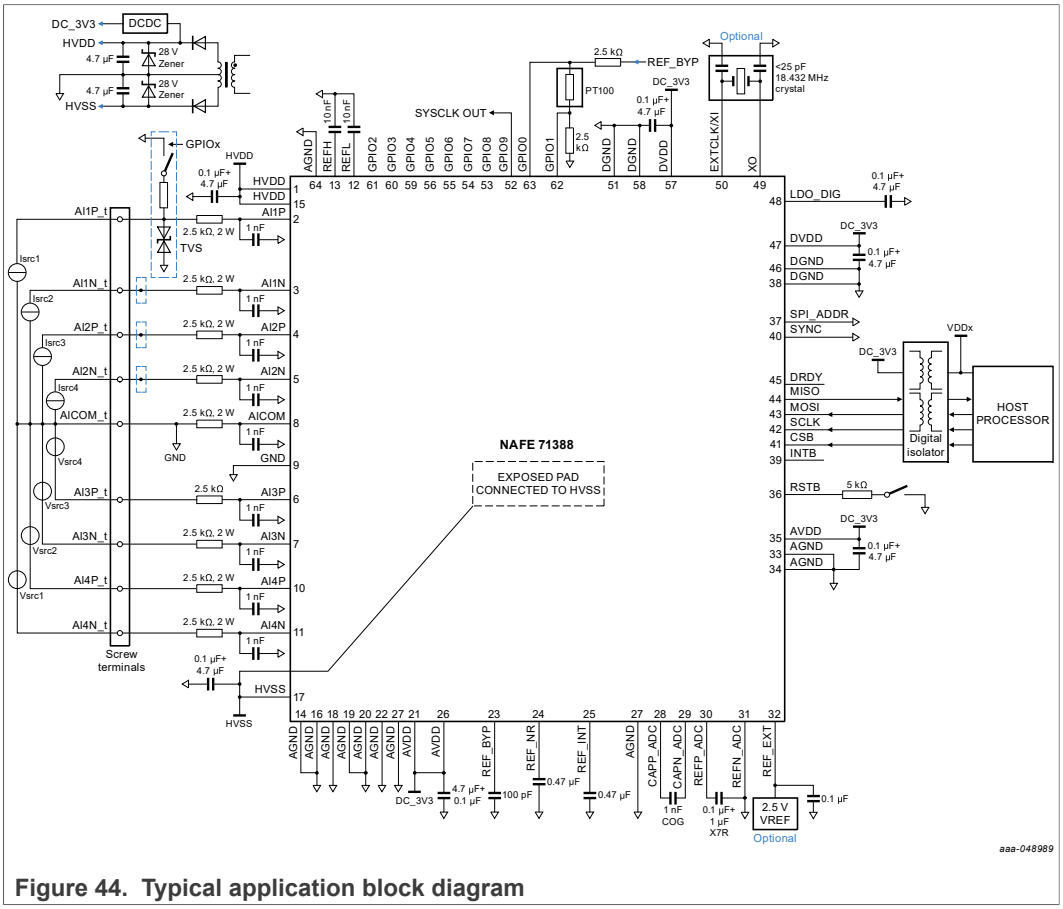


Figure 44. Typical application block diagram

Note: *Dash boxes on AI1N, AI2P, AI2N inputs represent the dashed circuitry on AI1P.*

11.2 Design for EMC

The NAFE71388 family of products is designed for industrial applications with enhanced electromagnetic compliance at device level. Although EMC is a system-level design consideration, use of robust device components may generally result in an overall lower-cost solution in a smaller board space. In limited laboratory testing scenarios, NAFE71388 parts were shown to be capable of sustaining IEC61000-4-5 surge up to ±2 kV and IEC61000-4-4 electrical fast transient and burst immunity up to ±4 kV on AI1P..AI4P, AI1N..AI4N, AICOM pins with 2.5 kΩ series MELF-type resistor without the need of external TVS on evaluation boards, while protection diodes are only necessary at HVDD and HVSS pins.

Besides HV input and supply pins, the rest of the LV pins are also tested for ESD to the same maximum rating, as shown in Table 30.

In applications where the surge protections are needed on LV pins, an external TVS suppressor will be needed.

11.3 Programmable logic controller I/O module

11.3.1 Design example: ±10 V input module

AI3P, AI3N, AI4P and AI4N in Figure 44 illustrates an example of a ±10 V analog input channels for programmable logic controller (PLC). These HV inputs can be protected by current limiting with the series resistor along with its internal clamping diodes to HVDD and HVSS supplies.

The signal from the transmitter is filtered by the external RC filter to remove EMI and RFI interference when operated in noisy environments. The negative input signal is connected to AICOM at 0 V. The ADC measures the differential voltage between inputs AI1P and AICOM. The input configuration is single-ended with the input voltage driven ±10 V relative to AICOM at 0V.

The internal oscillator is selected and EXTCLK/XI pin is shorted to DGND. The serial interface and digital control lines of the ADC are connected to the host.

Two Zener diodes are installed to clamp the high-voltage supply (HVDD-AGND and AGND-HVSS) to provide overvoltage protection if an input signal is present with module power off.

11.3.2 Design requirements

The ADC programmability allows various tradeoffs of sample rate, conversion noise, and conversion latency.

11.3.2.1 Design goal values

- **Accuracy:** ±0.05 %
- **Temperature range (internal module):** -25 °C to +105 °C
- **Acquisition period:** 50 µs
- **Effective resolution:** 19 bits

11.3.2.2 Design parameter value

- **Nominal signal range:** ±10 V
- **Extended range:** ±12 V
- **Input impedance:** 1000 MΩ
- **Overvoltage rating:** ±40 V

11.3.2.3 Detailed design procedure

A key consideration in the design of an analog input module is the error over the ambient temperature range resulting from the drift of gain, offset, reference voltage, and linearity error. This includes the initial offset and gain (including reference voltage error) after factory calibration.

Figure 45 shows the maximum drift error of the NAFE over the -25 °C to +105 °C temperature range. The maximum error drift is < 0.02 % in the temperature range of -10 °C to 90 °C and 0.04 % in the temperature range -25 °C to 105 °C.

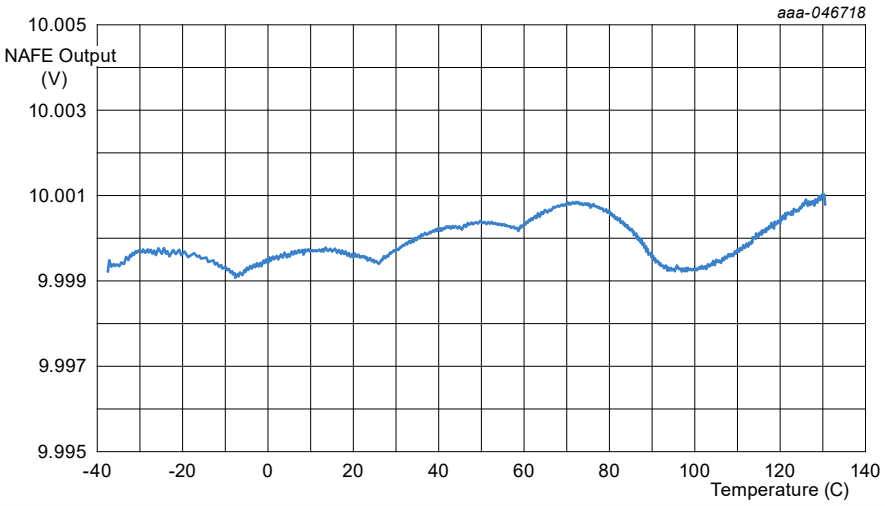


Figure 45. Temperature drift test

Figure 46 shows 100,000 consecutive conversions at 36000 sps. This example demonstrates the consistency of the ADC conversion results over time. The conversion noise in this example is 75 µVRMS. The effective resolution calculates to 19.4 bits, which meets the design requirement.

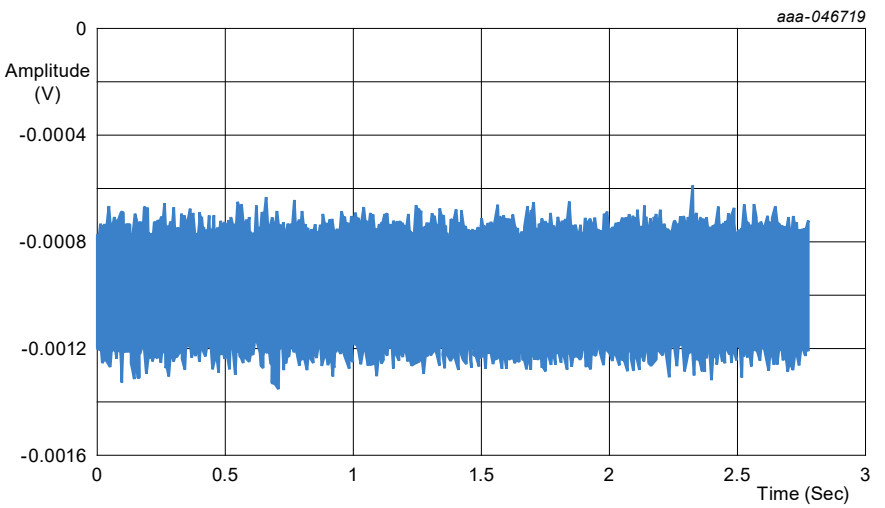


Figure 46. ADC conversion results

11.4 Power supplies and component selection

11.4.1 HV input pin protection and HV supply clamp

When any of the following pins HV AIxP, AIxN or AICOM is driven close to HVDD-0.5 V or HVSS+0.5 V, the internal protection diodes at the input pin may be forward-biased and start to conduct current flow from the input pin to the HVDD or HVSS pins. In general, the required external 2.5 kΩ series resistor is sufficient to limit the current. It is recommended to add supply clamping with Zener diodes at HVDD and HVSS to improve reliability. In case of surge events, TVS diodes could be added at the source side, before the resistor.

11.4.2 Power supply sequencing

As with many multiple-power supply systems, proper sequencing of the different supplies during power up and power down is a common practice to ensure robust device biasing without unnecessary electrical overstress. Though NAFE71388 devices were tested for robustness under various power supply ramping rates and order of sequences, testing is insufficient to cover all applications. Thus, for NAFE71388 devices, it is recommended to ramp up AVDD, DVDD before HVDD and/or HVSS. Ramping down HVDD and/or HVSS to ~3 V or less before starting to ramp down AVDD and DVDD, is also recommended. In most cases, any ramp rate slower than ±10 V/µs on HVDD, HVSS is acceptable.

11.4.3 HV input pin resistor

An external 2.5 kΩ series resistor is required at each of the AIxP, AIxN and AICOM pins. Higher resistance can lower the current limit in case of fault conditions with the expense of higher voltage error due to pin or board leakages and mismatches. Lower resistance is generally not advised in view of system reliability against surge and ESD events.

For precision HV applications, high-pulse load MELF resistors are typically used and often with TC > 100 ppm/ºC. With low input leakage current and the differential input architecture in the NAFE71388, the requirement on the temperature coefficient of the resistor is largely relaxed. If 1 % resistance tolerance is used, it meets the accuracy requirement in most applications.

Note: *For precise, high common-mode rejection single-ended measurement, AICOM pin in series with the same resistor type and value is to be used, instead of internal GND.*

11.4.4 Crystal

The NAFE71388 offers multiple 18.432 MHz clock-source options:

- Internal oscillator
- Crystal oscillator
- External clock source/module

For robustness, a crystal with higher drive level >100 µW is recommended.

11.4.5 Capacitors

Use of high-grade capacitors is recommended for the following pins:

REFP_ADC/REFN_ADC (1 µF, X7R) and CAPP/CAPN (1 nF, C0G).

11.4.6 Grounds and plane

Good layout practices are crucial to realize the full performance of the ADC.

For best performance, dedicate an entire PCB layer to a ground plane. Do not route any other signal traces on this layer.

11.5 System-level calibration

11.5.1 Procedures for gain and offset calibrations

This section describes the steps in performing digital calibration for offset and gain error correction.

11.5.1.1 Transfer characteristics

The NAFE71388 integrates an offset and gain correction circuitry. The offset correction (Oc) precedes the gain correction (Gc) in digital domain.

The ideal transfer characteristic is

$y = x$

The actual transfer characteristic is

$\boldsymbol{y} = G_a{*}x + O_a$

Where Ga and Oa are the actual gain and actual offset respectively.

The calibrated transfer characteristic is

$\boldsymbol{y} = G_a{*}G_c{*}x + G_c{*}(\,O_a - O_c\,)$

Where Gc and Oc are the correction gain and offset coefficients, respectively.

$$\begin{cases} G_c = \frac{1}{G_a} \\ O_c = O_a \end{cases}$$

11.5.1.2 Voltage and current input gain and offset calibration procedures

This section describes the steps for performing offset and gain digital calibration for voltage or current input.

11.5.1.2.1 Steps for gain CAL

1. Set $O_c = 0$
2. Set $G_c = 1$
3. Put a voltage source equals to x1, about +100 % of full-scale.
4. Read $y_1 = Ga{*}1{*}x_1 + 1{*}\left(Oa + 0\right)$
5. Put a voltage source equals to x2, about -100 % of full-scale.
6. Read $y_2 = Ga{*}1{*}x_2 + 1{*}\left(Oa + 0\right)$
7. Calculate $G_a = \frac{y_2 - y_1}{(x_2 - x_1)}$
8. Set $\boldsymbol{G_c} = \frac{1}{\boldsymbol{G_a}}$

11.5.1.2.2 Steps for offset CAL

1. Plug $y_1 = Ga{*}x_1 + Oa$
2. Calculate $Oa = \left(y_1 - Ga{*}x_1\right)$
3. Set $\boldsymbol{Oc} = \boldsymbol{Oa}$

11.5.2 Factory calibration and self-calibration

The NAFE71388 offers different calibration features to improve system accuracy at lower cost.

The NXP factory-calibrated devices increase initial system accuracy while reducing the capital expenditure for expensive test instruments and reducing the production test time. The NAFE71388 stores factory-calibrated coefficients based on two points self-calibration to reduce the gain and offset error.

The NAFE71388 includes two voltage sources to perform built-in or dynamic end-to-end self-calibrations. The ratiometric REFH and REFL voltage sources derived from the REF_BYP in combination with 0 V source (GND-GND) provide a precise and calibrated source for gain and offset calibration of all signal paths except reference voltage. The two points gain and offset calibration is performed measuring REFH-GND (or REFL-GND) and GND-GND and comparing against the internal stored value REFH-GND (or REFL-GND) and GND-GND = 0 V to calculate the gain and offset coefficients. Typically, REFH-GND with a typical value of 2.3 V, is suggested for low-channel gain, while RFEL-GND, with a typical value of 0.2 V, is suggested for high-channel gain.

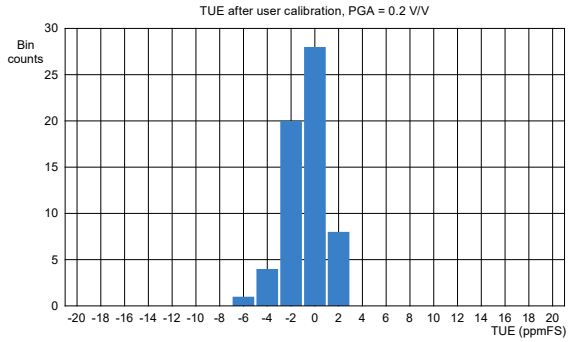
For systems that require low offset, an offset calibration could be performed measuring AICOM-AICOM to calculate and calibrate the offset error. Alternately, the NAFE71388 offers an automatic offset reduction circuit that is enabled by setting, CH_CONFIG1.CH_CHOP = 1, to activate the Precision mode. In this mode, the ADC runs two conversions and takes the average of the difference for offset removal.

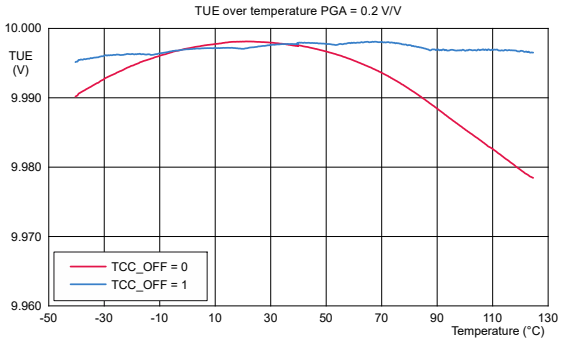
Note: *The output data rate is halved.*

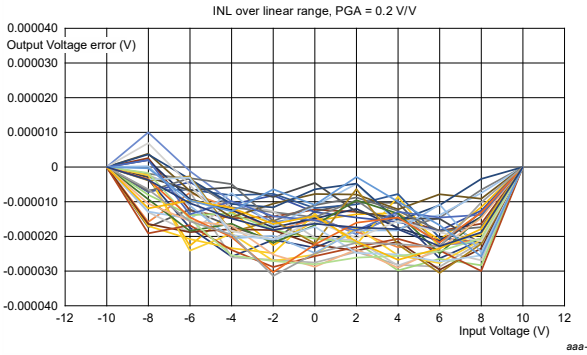
12 Typical operating characteristics

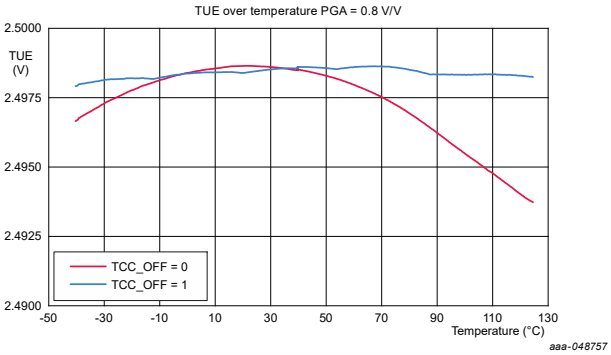
VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, internal 2.5 V reference, TA = 40 ºC, unless otherwise specified.

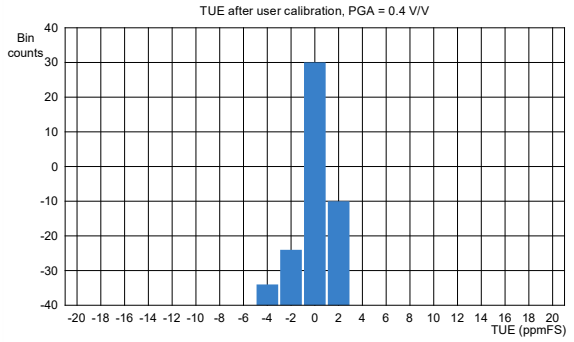
Table 45. Typical operating characteristics

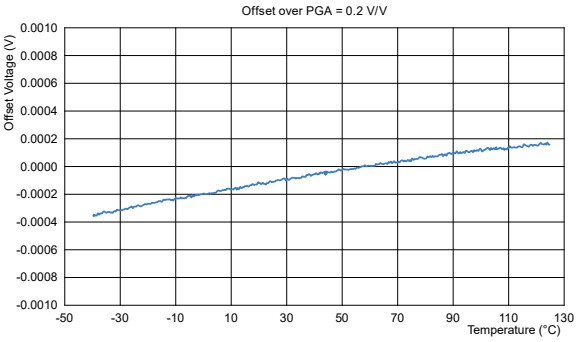


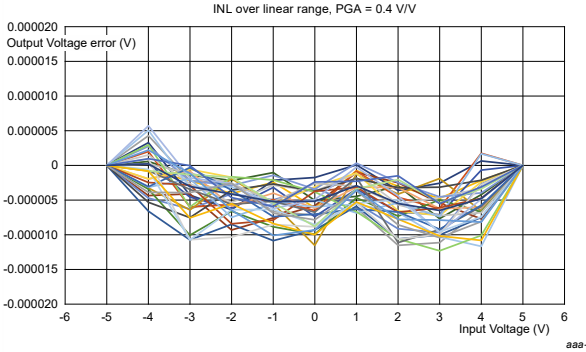


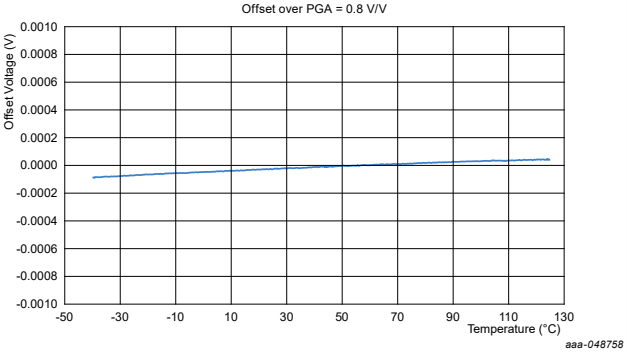












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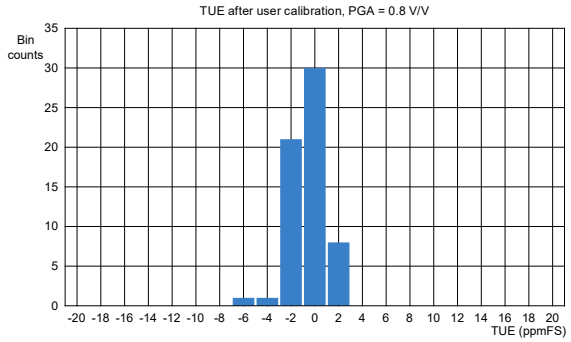

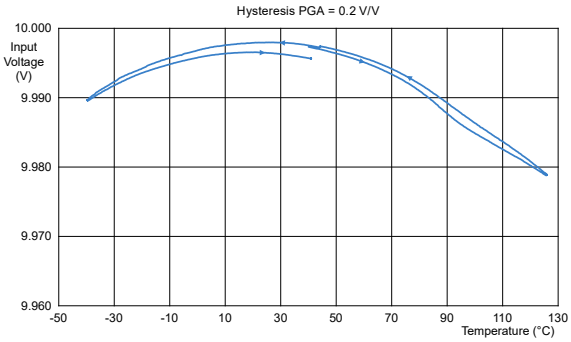

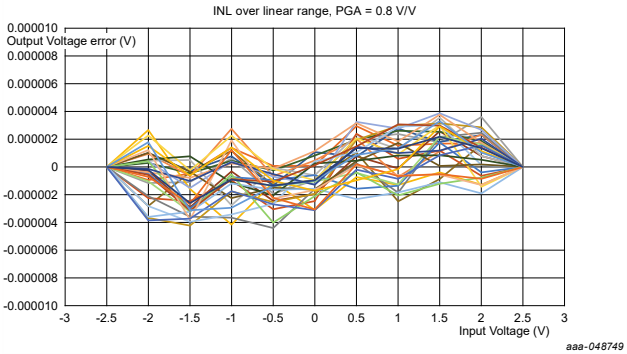

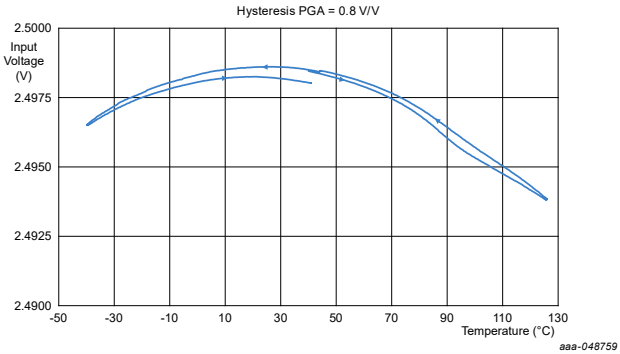

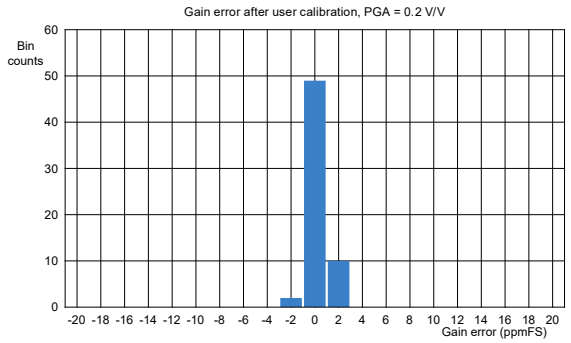

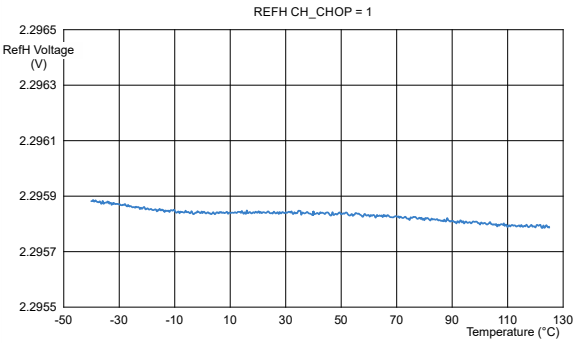

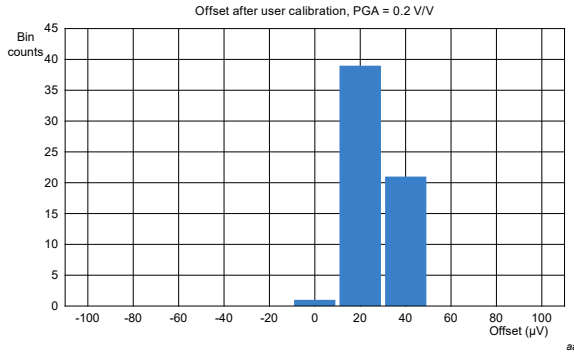

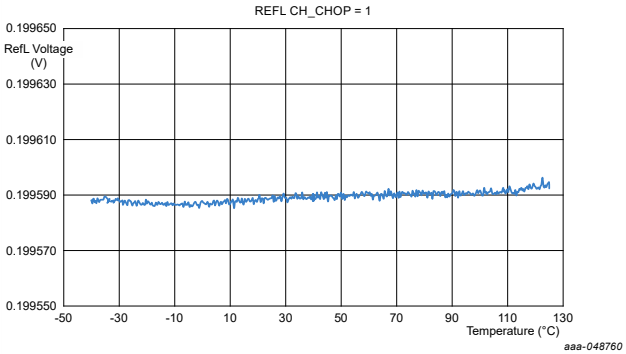

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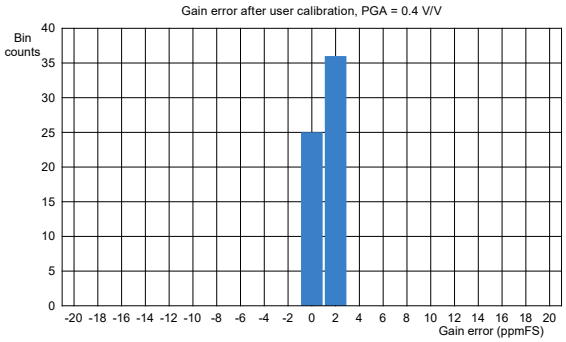

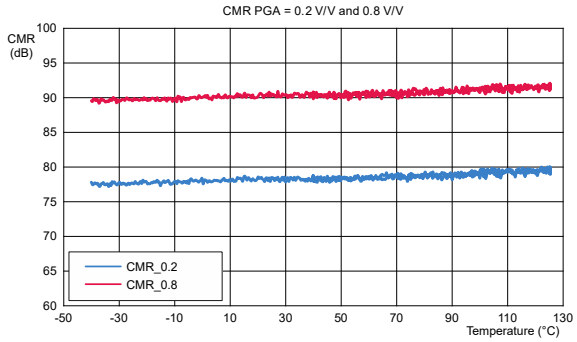

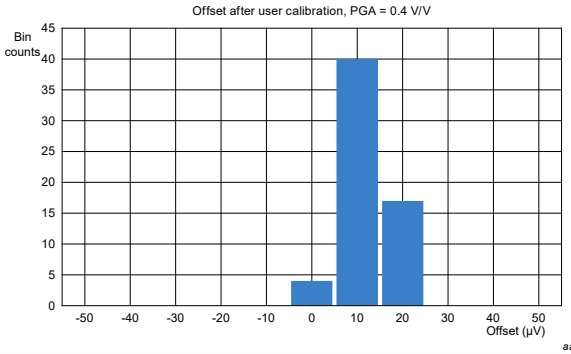

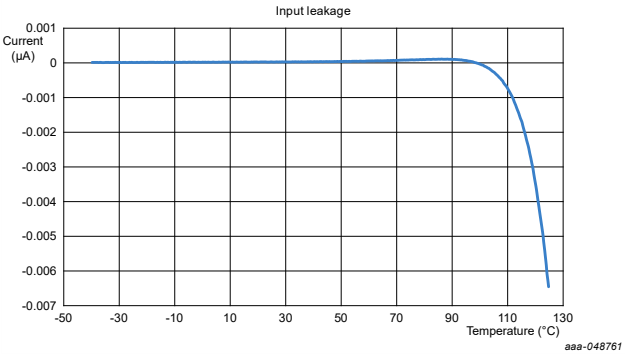

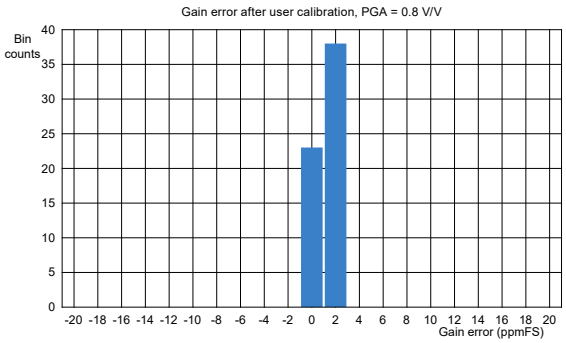

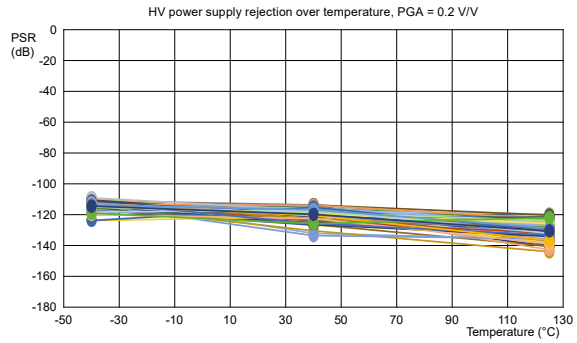

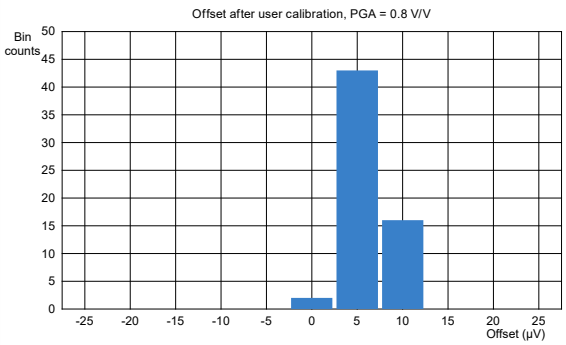

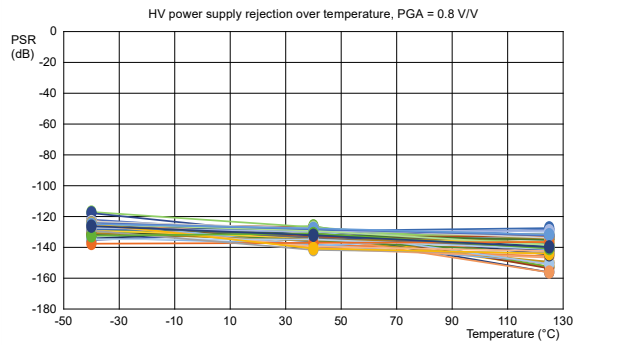

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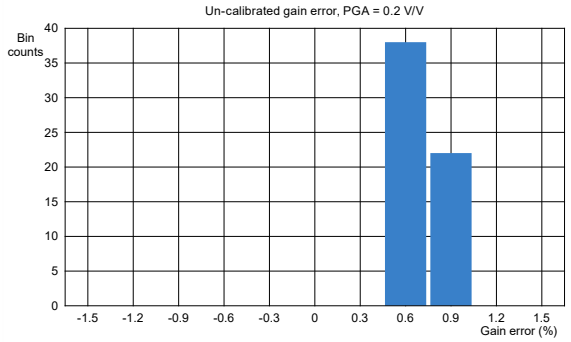

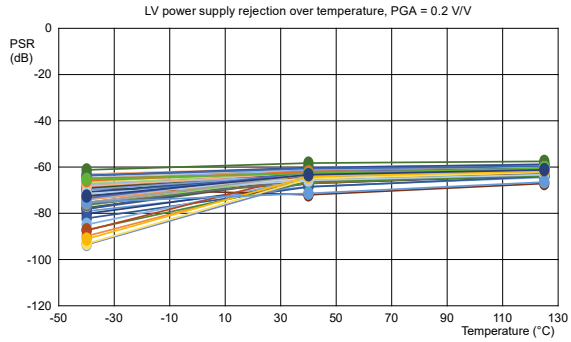

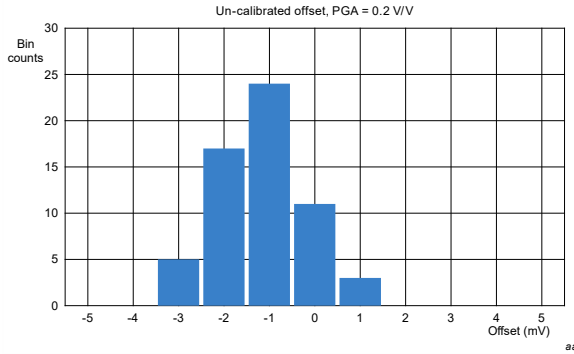

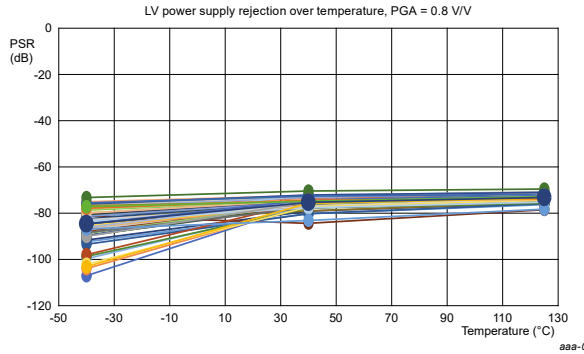

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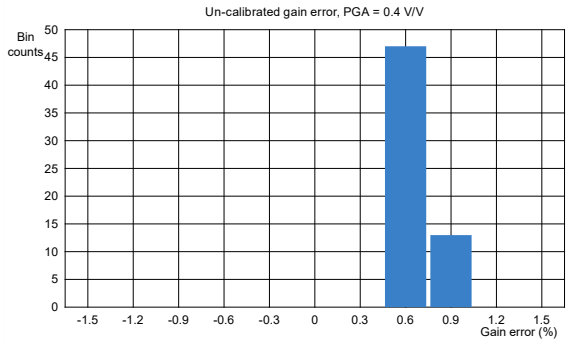

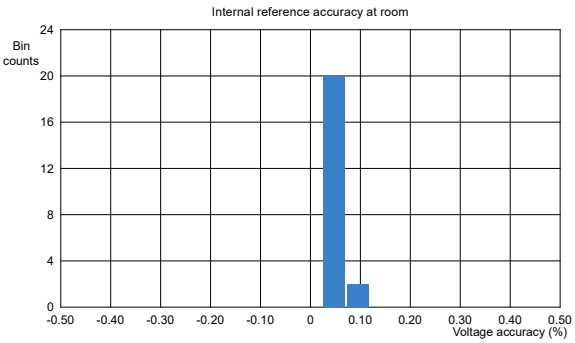

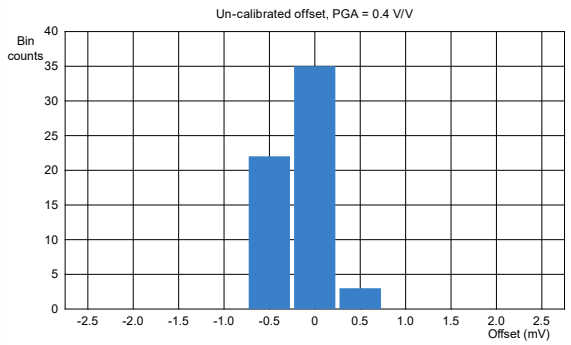

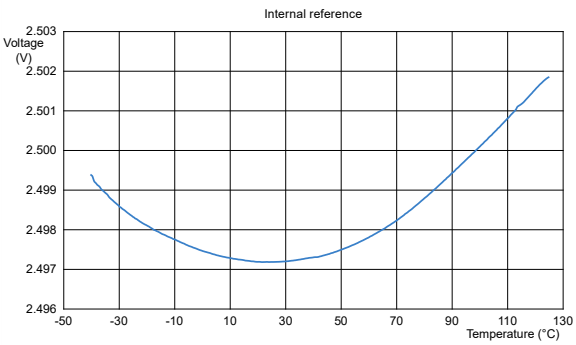

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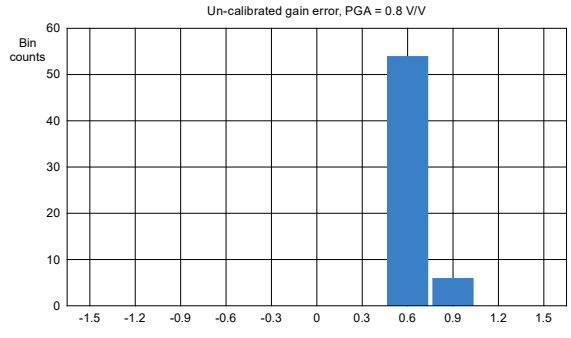

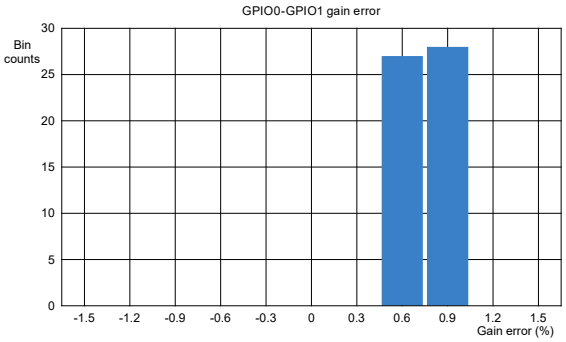

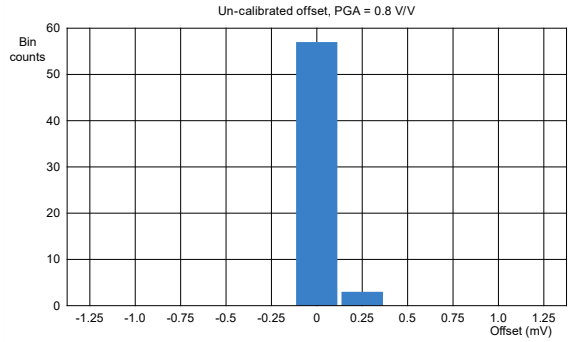

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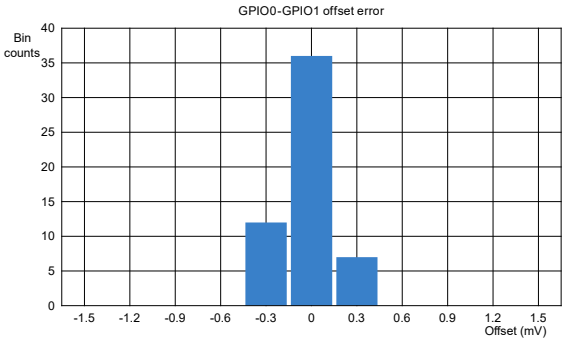

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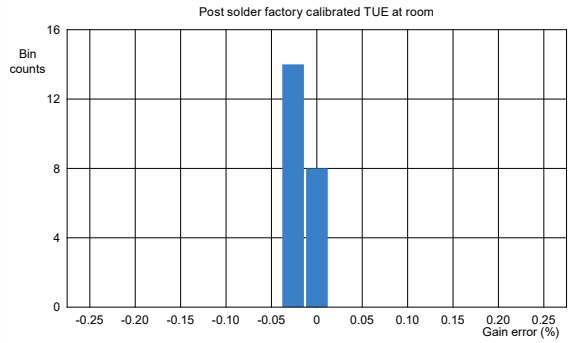

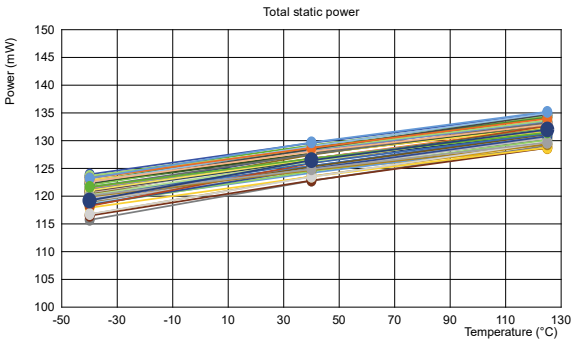

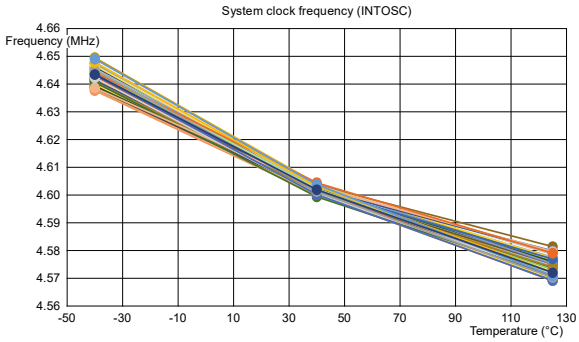

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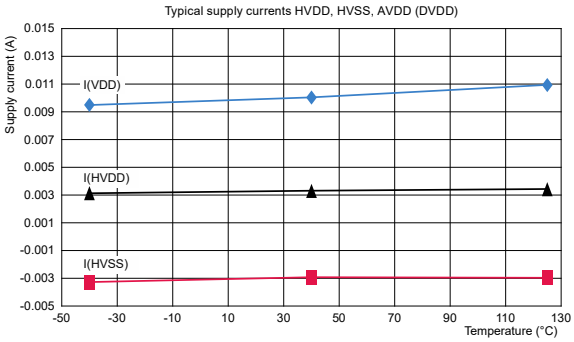

aaa-048767

13 Package outline

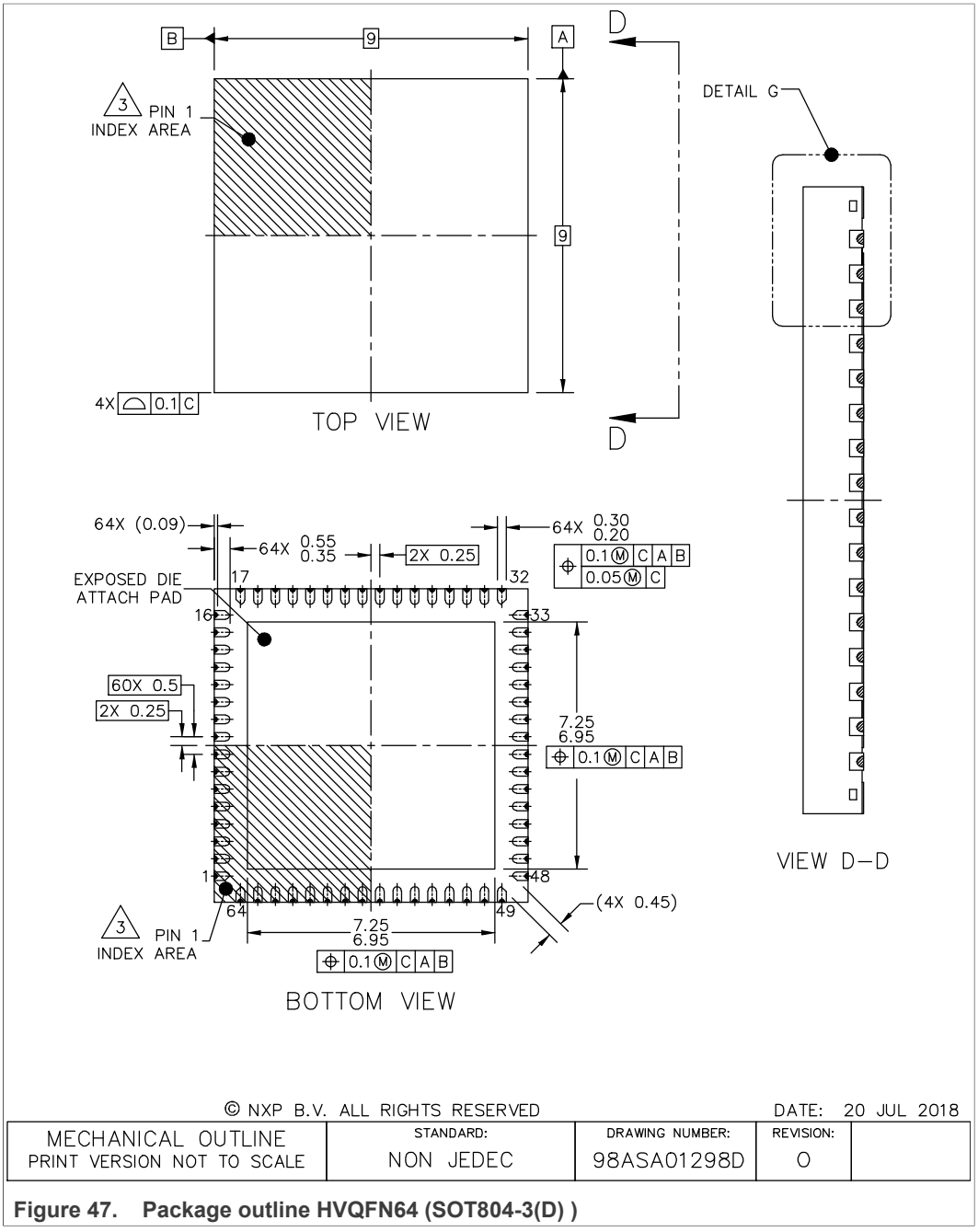

Figure 47. Package outline HVQFN64 (SOT804-3(D))

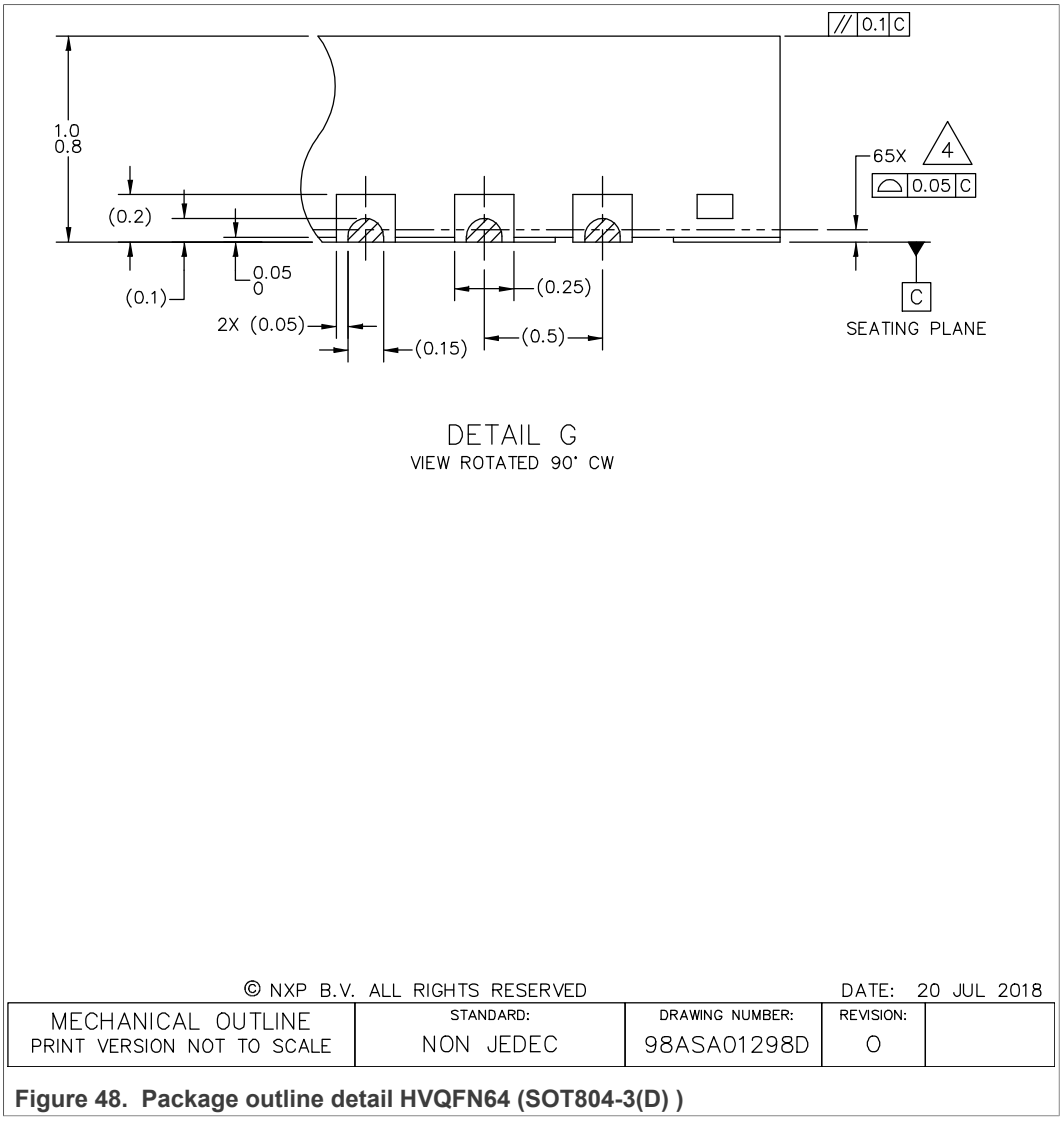

Figure 48. Package outline detail HVQFN64 (SOT804-3(D))

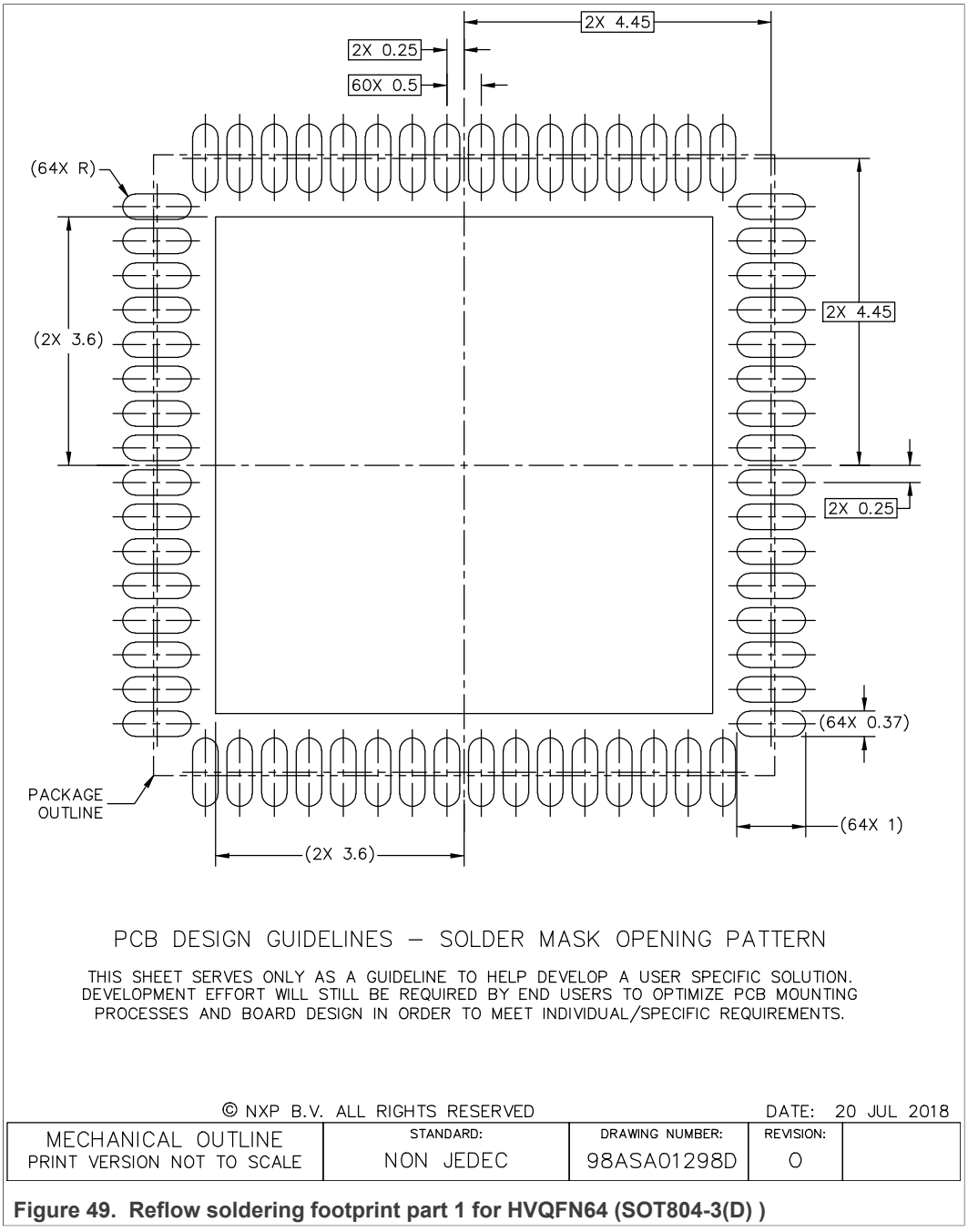

Figure 49. Reflow soldering footprint part 1 for HVQFN64 (SOT804-3(D))

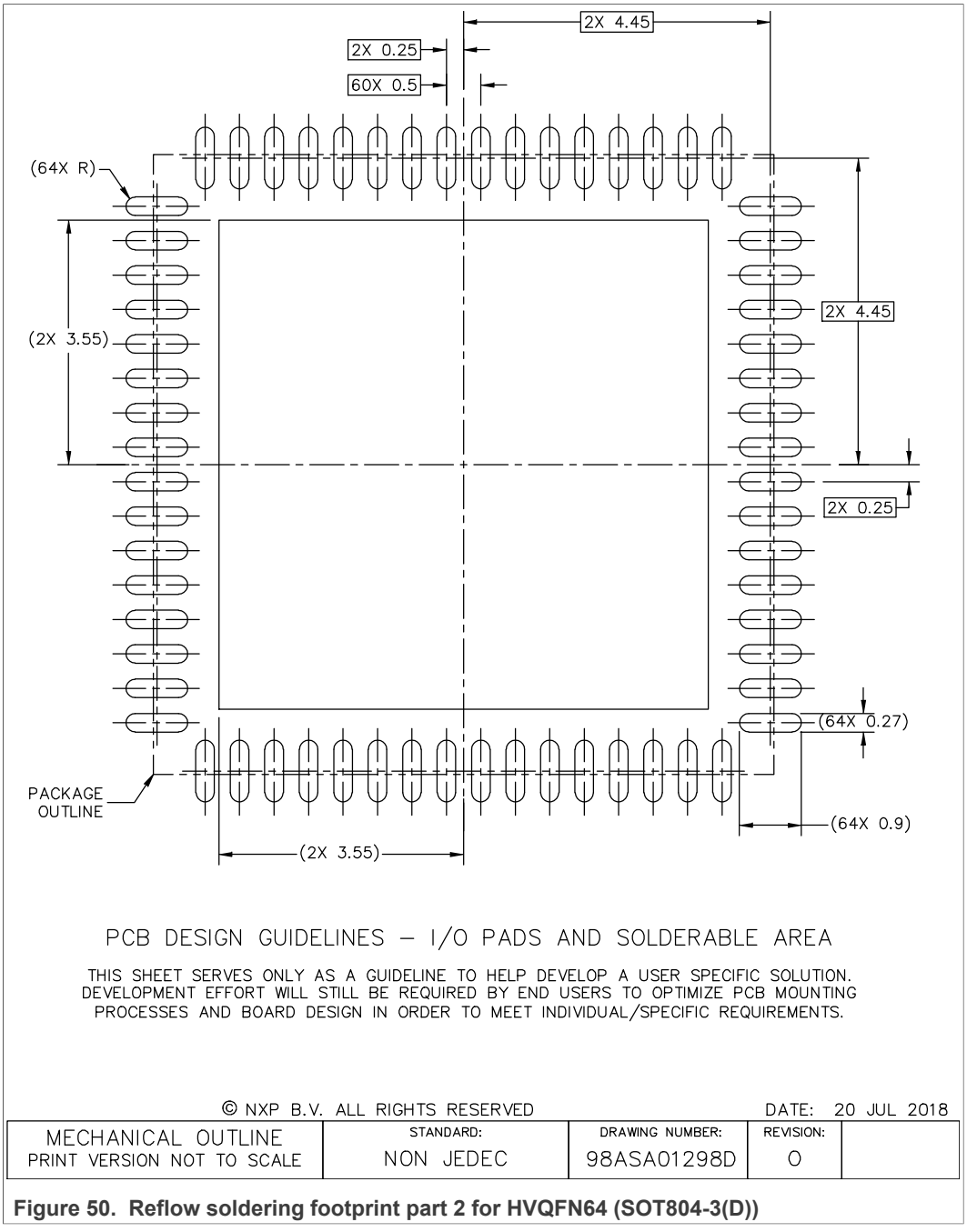

Figure 50. Reflow soldering footprint part 2 for HVQFN64 (SOT804-3(D))

Revision history

Rev	Date	Description
v.1	20221104	Initial version

14 Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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