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NB4N507ADEVB

NB4N507ADEVB Evaluation Board User's Manual

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EVAL BOARD USER'S MANUAL

Description

The NB4N507ADEVB Evaluation Board provides a flexible and convenient platform to quickly evaluate, characterize and verify the performance and operation of the NB4N507A PECL Clock Synthesizer. This user's manual provides detailed information on board contents, layout and its use. It should be used in conjunction with a device datasheet: NB4N507A. (www.onsemi.com)

Board Features

- Accommodates the Electrical Characterization of the NB4N507A in 16−pin 150 mil SOIC Package
- Supports use of a 10 MHz to 27 MHz Through−hole or Surface Mount Crystal
- Incorporates on Board Slide Switch Controlled Multiplier Select and OE Logic Pins, Minimizing Excess Cabling
- SMA Connectors are Provided for Auxiliary Input and Output Interfaces
- Differential PECL Outputs Loaded/Terminated On−board; Output Signals are Monitored via SMA Connectors
- Convenient and Compact Board Layout
- 3.3 V or 5.0 V Single or Split−Power Supply Operation

Board Layout

The evaluation board is constructed with Getek material with 50 Ω trace impedances and is designed to minimize noise, achieve high bandwidth and minimize crosstalk.

The NB4N507A evaluation board is equipped with 3−position slide switches. These switches are used to manipulate the static input logic levels of the Multiplier Select pins, S0 and S1, and Output Enable pin, OE. The H position of the slide switch asserts a logic HIGH on the assigned pin, the L asserts a logic LOW and the M is an open where the pin "floats" to a mid−logic level by way of the device's internal pull−up and pulldown resistors.

Multiplier Select pins, S0 and S1, and Output Enable pin, OE, also have SMA connector provisions, if the application requires them.

Layer Stack

L1 Signal
L2 SMA Ground
L3 V_{CC} (Positive Power Supply) and DUTGND (Device Ground, Negative Power Supply)
L4 Signal

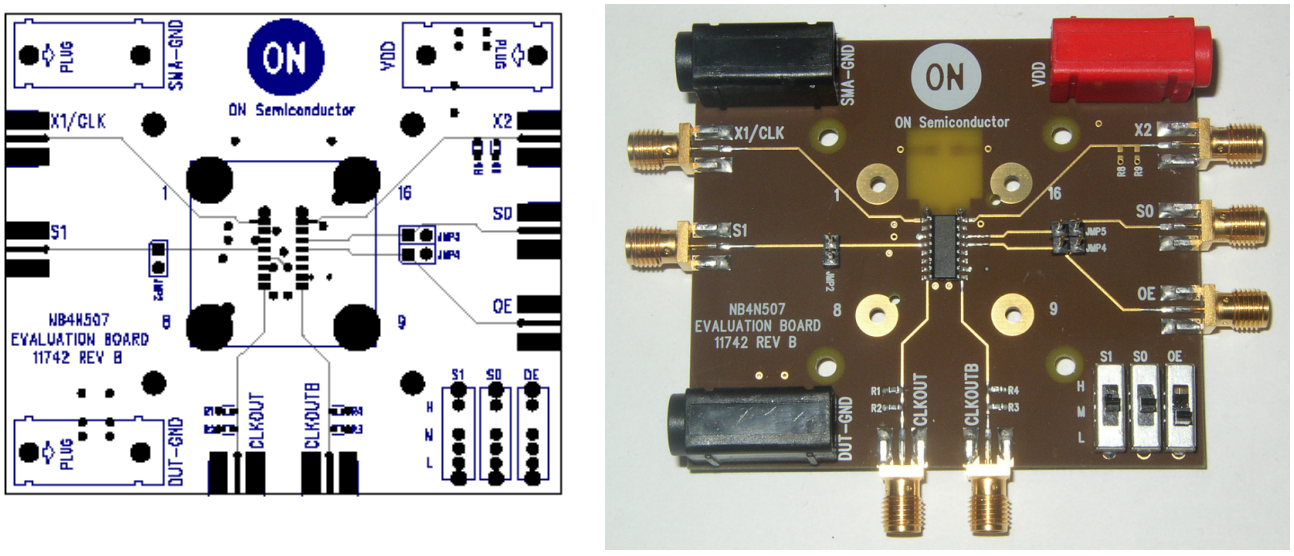

Figure 1. Evaluation Board

LAB SETUP PROCEDURE

Power Supply Connections and Output Termination

The NB4N507A has a positive supply pin, V_{DD}, and a negative supply pin, DUTGND. SMAGND is the ground plane for the SMA connectors.

Power supply banana plug connectors for V_{DD}, DUTGND and SMAGND are provided in the corners of the board. The (LV)PECL CLKOUT outputs have non−standard, open collector outputs and must be externally DC loaded and terminated. Thevenin equivalent load and termination resistors are provided on−board at the output's SMA connector.

Single Supply (Recommended)

Connect a single power supply to the evaluation board. (see Figure 2); Connect V_{DD} to +3.3 V, Connect GND to 0 V.

Use high−impedance probes of the oscilloscope or frequency counter to monitor the (LV)PECL CLKOUT outputs.

"Spilt" Power Supply (Optional)

For some tests, an optional "split" or dual power supply technique can be used, however, doing so will double terminate the (LV)PECL outputs into 50 Ωs of an oscilloscope or a frequency counter, and will therefore, appear to halve the output amplitude. Since $V_{TT} = V_{DD} - 2.0$ V, off setting V_{DD} by +2.0 V yields V_{TT} = 0 V or Ground. The V_{TT} terminal connects to the isolated SMAGND connector ground plane, and is not to be confused with the device ground pin or DUTGND.

Table 1. POWER SUPPLY CONFIGURATIONS

Device Pin	Power Supply	Single Supply	"Spilt" Power Supply (Optional)
V_{DD}	RED	+3.3 V or +5.0 V	V_{DD} = +2.0 V
SMAGND	BLACK	0 V	$V_{TT} = V_{DD} - 2.0$ V = 0 V
DUTGND	BLACK	0 V	DUTGND = −1.3 V (or −3.0 V)

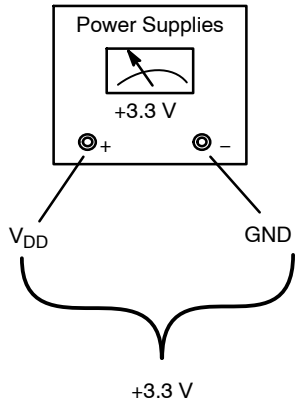

Figure 2. Single Power Supply Configuration

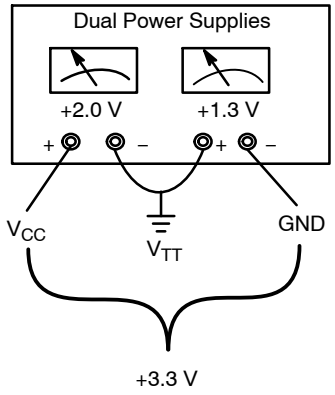

Figure 3. "Split" Power Supply Connections

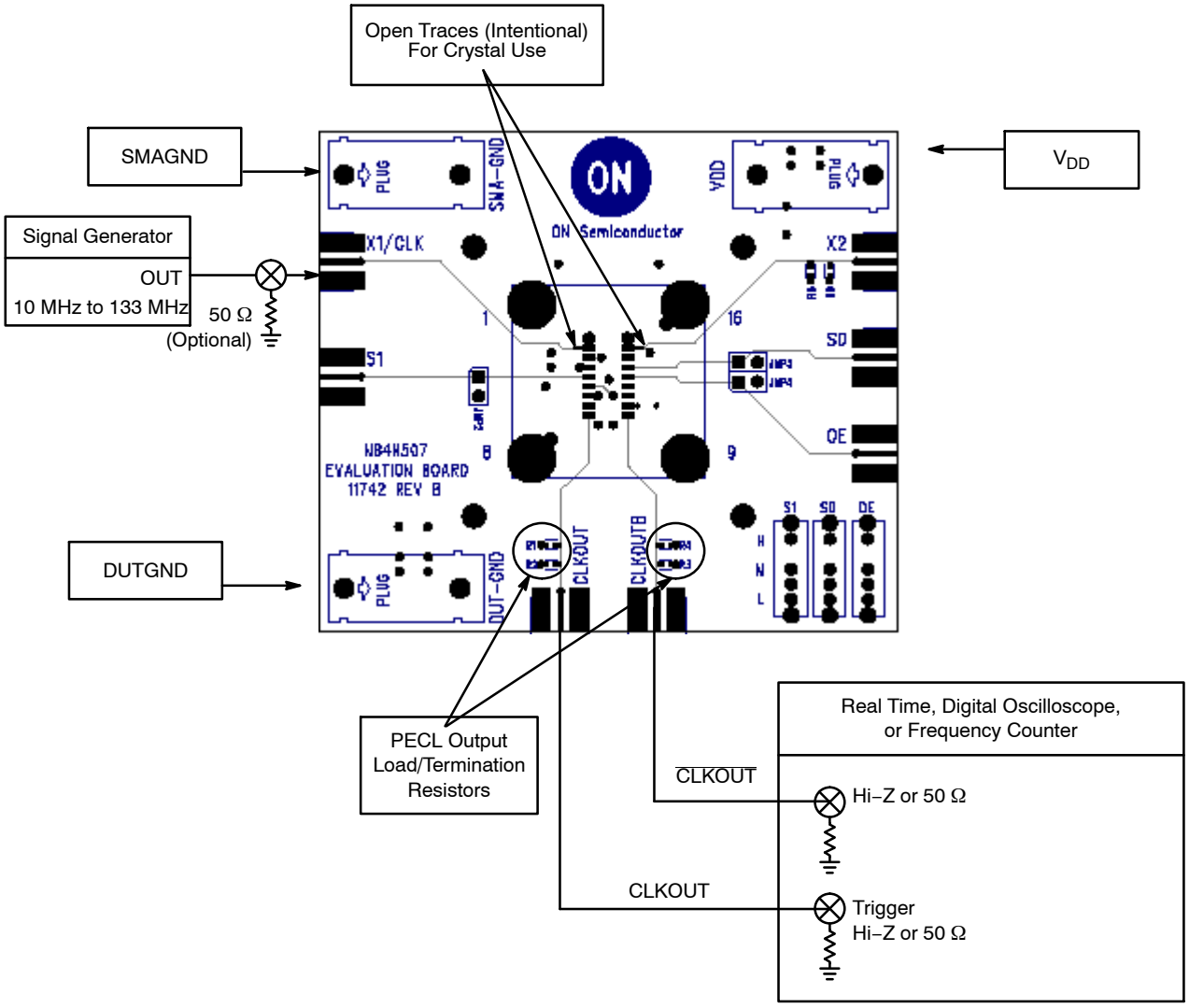

Figure 4. NB4N507A Evaluation Board

LAB SETUP AND MEASUREMENT PROCEDURE

Equipment Used

- Agilent Signal Generator #33250A for CLK, External Clock Source
- Tektronix or LeCroy with High Impedance Probes or TDS8000 Oscilloscope or Frequency Counter
- Agilent #6624A DC Power Supply
- Digital Voltmeter
- Matched High−speed Cables with SMA Connectors for the PECL CLKOUT Pins

In order to get started and demonstrate the NB4N507A, perform the following test setup sequence:

1. To monitor the CLKOUT outputs on an oscilloscope or frequency counter;
   a.. Connect a single power supply to the evaluation board. (see Figure 2)
   Connect V_{DD} to +3.3 V
   Connect GND to 0 V
   b.. or; Connect a “split” power supply to the evaluation board. (see Figure 3)
   Connect V_{CC} banana jack to +2.0 V
   Connect V_{TT} banana jack to SMA_GND= 0 V
   Connect GND banana jack to −1.3 V for 3.3 V operation, or −3.0 V for 5.0 V operation
2. Determine if a crystal or an external clock reference will be used.
   a.. For crystal use, install a crystal

b.. For external clock reference use, short the open trace at Pin 1 and provide an external clock reference from a signal generator (10 − 27 MHz) into the X1/CLK pin. Terminate the signal generator with 50 Ω to SMA ground.

3. Set the programmable S0 and S1 pin switches accordingly to achieve the desired function table logic input levels.
4. Set the OE pin to a logic HIGH
5.
   a.. If a single power supply is used, connect the CLKOUT outputs to the oscilloscope with matched high−impedance probe cables.
   b.. If a split power supply is used, connect the CLKOUT outputs to the oscilloscope with matched cables.
6. Ensure the oscilloscope is triggered properly. Trigger the oscilloscope from the $\overline{\text{CLKOUT}}$ output.

NB4N507A EVALUATION BOARD PIN DESCRIPTIONS AND FEATURES BY PIN

The NB4N507A Evaluation Board was designed to accommodate the test and evaluation of the NB4N507A PECL Clock Synthesizer. Detailed board features by device pin are described below:

Crystal (X1/CLK and X2)

A through−hole or surface mount crystal can be used. The metal traces at the crystal pins are intentionally open for crystal use and will have no impedance affect on the crystal pins.

X1/CLK − External Clock

An SMA connector is provided for X1/CLK if an external clock source is used on Pin 1. The metal trace at the package pin is intentionally open for crystal use, but, must be shorted for a connection to Pin 1 for external clock use. The unused component pad labeled C2 (used for the crystal load capacitor) may be used for a 50 Ω resistor to ground to terminate an external signal generator.

S0 and S1

The S0 and S1 multiplier select pins can be exercised manually with the S0 and S1 slide switches when the jumpers are used across JMP2 and JMP5, or they can be controlled externally via the SMA connectors with the jumpers open.

The H position of the DIP switch asserts a logic HIGH (V_{CC}) on the assigned pin and the L asserts a logic LOW (DUTGND). The S0 and S1 device pins have internal pull−up and pulldown resistors. When left open, the S0 or S1 switch “floats” to mid−logic level. In the M position, the slide switch is an open and the pin “floats” to the mid−logic level.

CLKOUT and $\overline{\text{CLKOUT}}$

The CLKOUT and $\overline{\text{CLKOUT}}$ PECL outputs have equal length, 50 Ω board traces with SMA connectors. Matched cables can connect to an oscilloscope or frequency counter.

The (LV)PECL CLKOUT outputs have nonstandard, open collector outputs and must be externally DC loaded and terminated.

Thevenin equivalent load and termination resistors are provided on board at the output’s SMA connector.

OE

The Output Enable function can be exercised manually with the OE switch when the JMP4 jumper is used, or they can be controlled externally via the SMA connector and the jumper open.

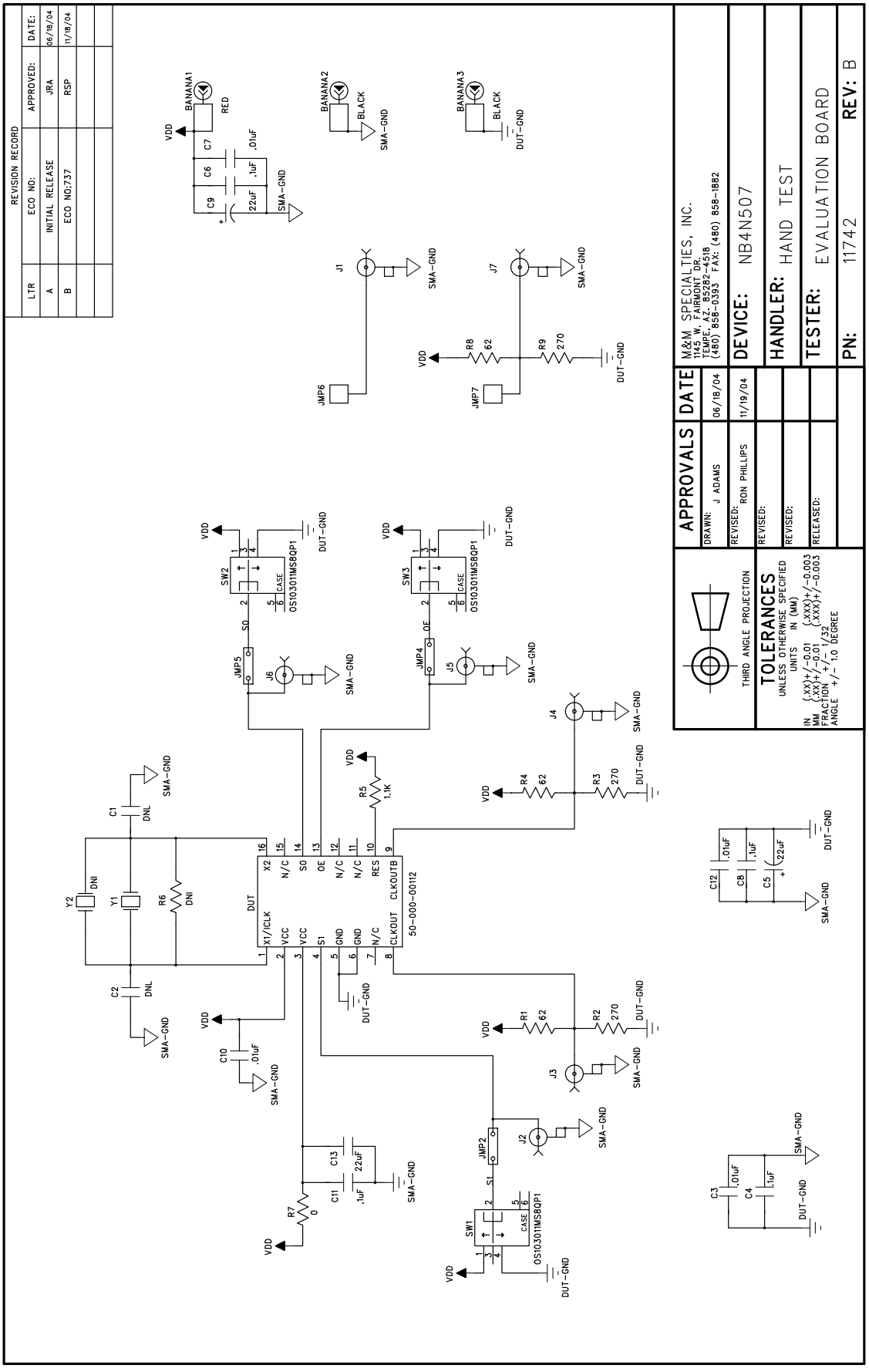

Figure 5. Evaluation Board Schematic