

NB6L572M

2.5V / 3.3V Differential 4:1 Mux to 1:2 CML Clock/Data Fanout / Translator

Multi-Level Inputs w/ Internal Termination

Description

The NB6L572M is a high performance differential 4:1 Clock / Data input multiplexer and a 1:2 CML Clock / Data fanout buffer that operates up to 6 GHz / 8 Gbps respectively with a 2.5 V or 3.3 V power supply.

The differential Clock / Data inputs have internal 50 Ω termination resistors and will accept differential LVPECL, CML, or LVDS logic levels. The NB6L572M incorporates a pair of Select pins that will choose one of four differential inputs and will produce two identical CML output copies of Clock or Data.

As such, the NB6L572M is ideal for SONET, GigE, Fiber Channel, Backplane and other Clock/Data distribution applications.

The two differential CML outputs will swing 400 mV when externally loaded and terminated with a 50 Ω resistor to V_{CC} and are optimized for low skew and minimal jitter.

The NB6L572M is offered in a low profile 5x5mm 32-pin QFN Pb-Free package. Application notes, models, and support documentation are available at www.onsemi.com. The NB6L572M is a member of the ECLinPS MAX™ family of high performance clock products.

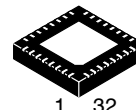
Features

- Input Data Rate > 8 Gb/s Typical
- Data Dependent Jitter < 10 ps
- Maximum Input Clock Frequency > 6 GHz Typical
- Random Clock Jitter < 0.8 ps RMS
- Low Skew 1:2 CML Outputs, < 15 ps max
- 4:1 Multi-Level Mux Inputs, accepts LVPECL, CML, LVDS
- 200 ps Typical Propagation Delay
- 35 ps Typical Rise and Fall Times
- Differential CML Outputs, 400 mV Peak-to-Peak, Typical
- Operating Range: $V_{CC} = 2.375$ V to 3.6 V with $GND = 0$ V
- Internal 50 Ω Input Termination Resistors
- V_{REFAC} Reference Output
- QFN-32 Package, 5mm x 5mm
- 40°C to +85°C Ambient Operating Temperature
- These are Pb-Free Devices



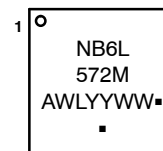
ON Semiconductor®

<http://onsemi.com>



QFN32
MN SUFFIX
CASE 488AM

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

NB6L572M

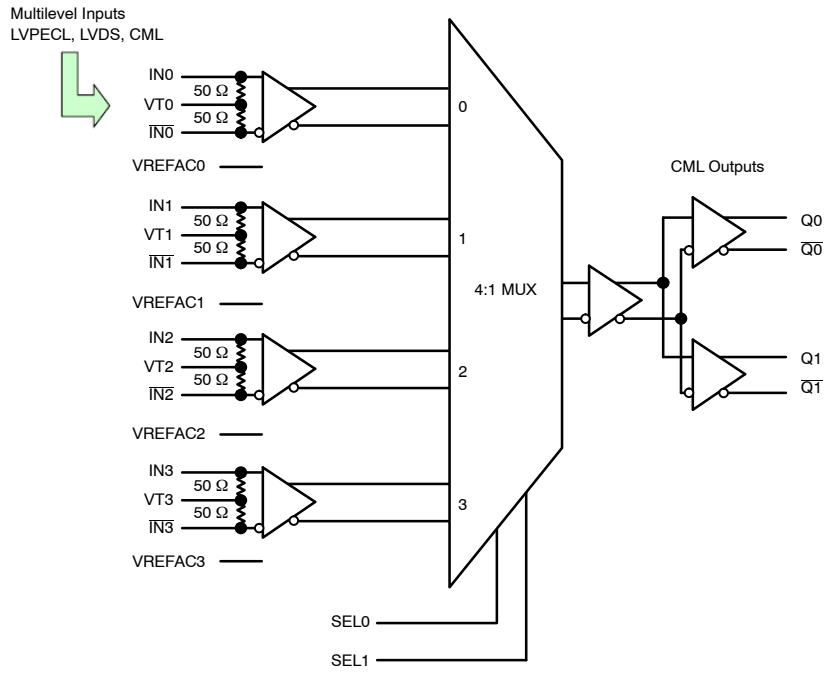


Figure 1. Simplified Block Diagram

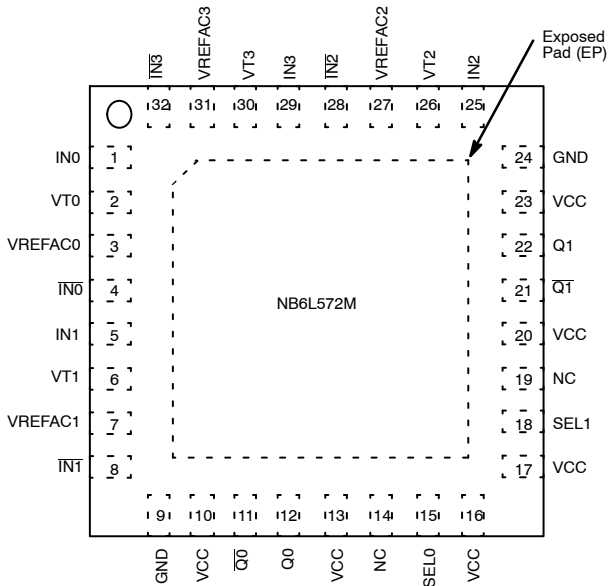


Figure 2. Pinout: QFN-32 (Top View)

Table 1. INPUT SELECT FUNCTION TABLE

| SEL1* | SEL0* | Clock / Data Input Selected |
|-------|-------|-----------------------------|
| 0 | 0 | IN0 Input Selected |
| 0 | 1 | IN1 Input Selected |
| 1 | 0 | IN2 Input Selected |
| 1 | 1 | IN3 Input Selected |

*Defaults HIGH when left open.

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Table 2. PIN DESCRIPTION

| Pin Number | Pin Name | I/O | Pin Description |
|----------------------------------|--|----------------------------|---|
| 1, 4 5, 8 25, 28 29, 32 | IN0, $\overline{IN0}$ IN1, $\overline{IN1}$ IN2, $\overline{IN2}$ IN3, $\overline{IN3}$ | LVPECL, CML, LVDS Input | Non-inverted, Inverted, Differential Clock or Data Inputs |
| 2, 6 26, 30 | VT0, VT1 VT2, VT3 | | Internal 100 Ω Center-tapped Termination Pin for INx/ \overline{INx} |
| 15 18 | SEL0 SEL1 | LVTTTL/LVCMOS Input | Input Select pins, default HIGH when left open through a 131 k Ω pullup resistor. Input logic threshold is $V_{CC}/2$. See Select Function, Table 1. |
| 14, 19 | NC | – | No Connect |
| 10, 13, 16 17, 20, 23 | VCC | – | Positive Supply Voltage. All VCC pins must be connected to the positive power supply for correct DC and AC operation. |
| 11, 12 21, 22 | $\overline{Q0}$, Q0 $\overline{Q1}$, Q1 | CML Output | Non-inverted, Inverted Differential Outputs. |
| 9, 24 | GND | | Negative Supply Voltage, connected to Ground |
| 3 7 27 31 | VREF-AC0 VREF-AC1 VREF-AC2 VREF-AC3 | – | Output Voltage Reference for Capacitor-Coupled Inputs |
| – | EP | – | The Exposed Pad (EP) on the QFN-32 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is electrically connected to the die, and must be electrically connected to GND. |

1. In the differential configuration when the input termination pins (VT0, VT1, VT2, VT3) are connected to a common termination voltage or left open, and if no signal is applied on INx/ \overline{INx} input, then the device will be susceptible to self-oscillation.
2. All VCC, and GND pins must be externally connected to a power supply for proper operation.

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Table 3. ATTRIBUTES

| Characteristics | | Value |
|--|-----------------------------------|----------------------|
| ESD Protection | Human Body Model Machine Model | > 2 kV > 200 V |
| R _{PU} – SELx Input Pull-up Resistor | | 131 kΩ |
| Moisture Sensitivity (Note 3) | QFN-32 | Level 1 |
| Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in |
| Transistor Count | | 275 |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | |

3. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---------------------|--|--------------------|----------------|------------------------------|------|
| V _{CC} | Positive Power Supply | GND = 0 V | | -0.5 V to +4.0 | V |
| V _{IN} | Positive Input Voltage | GND = 0 V | | -0.5 to V _{CC} +0.5 | V |
| V _{INPP} | Differential Input Voltage I _N – I _N \bar | | | 1.89 | V |
| I _{out} | Output Current Through R _T (50 Ω Resistor) | | | ± 40 | mA |
| I _{IN} | Input current Through RT (50 Ω resistor) | | | ± 40 | mA |
| I _{VREFAC} | VREFAC Sink or Source Current | | | ± 1.5 | mA |
| T _A | Operating Temperature Range | | | -40 to +85 | °C |
| T _{stg} | Storage Temperature Range | | | -65 to +150 | °C |
| θ _{JA} | Thermal Resistance (Junction-to-Ambient) (Note 4) | 0 lfpm 500 lfpm | QFN32 QFN32 | 31 27 | °C/W |
| θ _{JC} | Thermal Resistance (Junction-to-Case) (Note 4) | | QFN32 | 12 | °C/W |
| T _{sol} | Wave Solder | ≤ 20 sec | | 265 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

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Table 5. DC CHARACTERISTICS CML OUTPUT $V_{CC} = 2.375 \text{ V to } 3.6 \text{ V}$, $GND = 0 \text{ V}$, $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ (Note 5)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|--------|----------------|-----|-----|-----|------|
|--------|----------------|-----|-----|-----|------|

POWER SUPPLY

| | | | | | | |
|----------|--|--|--------------|------------|--------------|----|
| V_{CC} | Power Supply Voltage | $V_{CC} = 3.3 \text{ V}$ $V_{CC} = 2.5 \text{ V}$ | 3.0 2.375 | 3.3 2.5 | 3.6 2.625 | V |
| I_{CC} | Power Supply Current for V_{CC} (Inputs and Outputs Open) | $V_{CC} = 3.3 \text{ V}$ $V_{CC} = 2.5 \text{ V}$ | | 130 115 | 165 150 | mA |

CML OUTPUTS (Note 6)

| | | | | | | |
|----------|---------------------|--|--|--|--|----|
| V_{OH} | Output HIGH Voltage | $V_{CC} = 3.3 \text{ V}$ $V_{CC} = 2.5 \text{ V}$ | $V_{CC} - 30$ 3270 2470 | $V_{CC} - 10$ 3290 2490 | V_{CC} 3300 2500 | mV |
| V_{OL} | Output LOW Voltage | $V_{CC} = 3.3 \text{ V}$ $V_{CC} = 2.5 \text{ V}$ | $V_{CC} - 650$ 2650 $V_{CC} - 650$ 1850 | $V_{CC} - 450$ 2850 $V_{CC} - 450$ 2050 | $V_{CC} - 300$ 3000 $V_{CC} - 300$ 2200 | mV |

DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED (Figures 5 & 6) (Note 8)

| | | | | | | |
|-----------|--|--|----------------|--|----------------|----|
| V_{IH} | Single-ended Input HIGH Voltage | | $V_{th} + 100$ | | V_{CC} | mV |
| V_{IL} | Single-ended Input LOW Voltage | | GND | | $V_{th} - 100$ | mV |
| V_{th} | Input Threshold Reference Voltage Range (Note 8) | | 1100 | | $V_{CC} - 100$ | mV |
| V_{ISE} | Single-ended Input Voltage ($V_{IH} - V_{IL}$) | | 200 | | 1200 | mV |

VREFAC

| | | | | | | |
|--------------|---|--|------|-----------------|-----------------|----|
| V_{REF-AC} | Output Reference Voltage (100 μA Load) | | 1050 | $V_{CC} - 1250$ | $V_{CC} - 1050$ | mV |
|--------------|---|--|------|-----------------|-----------------|----|

DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 7 & 8) (Note 9)

| | | | | | | |
|-----------|--|--|------|--|-----------------|---------------|
| V_{IHD} | Differential Input HIGH Voltage ($I_N, \overline{I_N}$) | | 1200 | | V_{CC} | mV |
| V_{ILD} | Differential Input LOW Voltage ($I_N, \overline{I_N}$) | | 0 | | $V_{IHD} - 100$ | mV |
| V_{ID} | Differential Input Voltage ($I_N, \overline{I_N}$) ($V_{IHD} - V_{ILD}$) | | 100 | | 1200 | mV |
| V_{CMR} | Input Common Mode Range (Differential Configuration, Note 10) (Figure 9) | | 1050 | | $V_{CC} - 50$ | mV |
| I_{IH} | Input HIGH Current $I_N / \overline{I_N}$ ($V_{TIN} / \overline{V_{TIN}}$ Open) | | -150 | | 150 | μA |
| I_{IL} | Input LOW Current $I_N / \overline{I_N}$ ($V_{TIN} / \overline{V_{TIN}}$ Open) | | -150 | | 150 | μA |

CONTROL INPUT (SELx Pin)

| | | | | | | |
|----------|------------------------------------|--|----------------------|--|----------------------|---------------|
| V_{IH} | Input HIGH Voltage for Control Pin | | $V_{CC} \times 0.65$ | | V_{CC} | V |
| V_{IL} | Input LOW Voltage for Control Pin | | GND | | $V_{CC} \times 0.35$ | V |
| I_{IH} | Input HIGH Current | | -150 | | 150 | μA |
| I_{IL} | Input LOW Current | | -150 | | 150 | μA |

TERMINATION RESISTORS

| | | | | | | |
|------------|---|--|----|----|----|----------|
| R_{TIN} | Internal Input Termination Resistor (Measured from I_{Nx} to V_{Tx}) | | 45 | 50 | 55 | Ω |
| R_{TOUT} | Internal Output Termination Resistor | | 45 | 50 | 55 | Ω |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and Output parameters vary 1:1 with V_{CC} .
- CML outputs loaded with 50 Ω to V_{CC} for proper operation.
- V_{th} is applied to the complementary input when operating in single-ended mode.
- V_{th} , V_{IH} , V_{IL} , and V_{ISE} parameters must be complied with simultaneously.
- V_{IHD} , V_{ILD} , V_{ID} and V_{CMR} parameters must be complied with simultaneously.
- V_{CMR} min varies 1:1 with GND, V_{CMR} max varies 1:1 with V_{CC} . The V_{CMR} range is referenced to the most positive side of the differential input signal.

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Table 6. AC CHARACTERISTICS $V_{CC} = 2.375\text{ V to }3.6\text{ V}$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$ (Note 11)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|--------------------------|--|---|----------|-----------|----------------------|
| f_{MAX} | Maximum Input Clock Frequency $V_{OUT} \geq 250\text{ mV}$ | 5 | 6 | | GHz |
| $f_{DATAMAX}$ | Maximum Operating Data Rate NRZ, (PRBS23) | 6.5 | 8 | | Gbps |
| f_{SEL} | Maximum Toggle Frequency, SELx | 20 | 40 | | MHz |
| V_{OUTPP} | Output Voltage Amplitude (@ $V_{INPPmin}$) $f_{in} \leq 5\text{ GHz}$ (Note 12) (Figure 10) | 250 | 400 | | mV |
| t_{PLH} , t_{PHL} | Propagation Delay to Differential Outputs Measured at Differential Crosspoint | @ 1 GHz INx/\overline{INx} to Qx/\overline{Qx} @ 50 MHz SELx to Qx | 125 4 | 200 10 | ps ns |
| t_{PD} Tempco | Differential Propagation Delay Temperature Coefficient | | 100 | | $\Delta fs/^\circ C$ |
| tskew | Output – Output skew (within device) (Note 13) Device – Device skew ($tpdmax - tpdmin$) | | 0 5 | 15 25 | ps |
| t_{DC} | Output Clock Duty Cycle (Reference Duty Cycle = 50%) $f_{in} = 1\text{ GHz}$ | 45 | 50 | 55 | % |
| Φ_N | Phase Noise, $f_{in} = 1\text{ GHz}$ | | | | dBc |
| | | 10 kHz | -134 | | |
| | | 100 kHz | -136 | | |
| | | 1 MHz | -149 | | |
| | | 10 MHz | -150 | | |
| | | 20 MHz | -150 | | |
| | | 40 MHz | -150 | | |
| $t_{J\Phi N}$ | Integrated Phase Jitter (Figure x) $f_{in} = 1\text{ GHz}$, 12 kHz – 20 MHz Offset (RMS) | | 35 | | fs |
| t_{JITTER} | Random Clock Jitter, RJ(RMS) (Note 14) $f_{in} \leq 5\text{ GHz}$ Deterministic Jitter, DJ (Note 15) ($FR4 \leq 12'$) $f_{in} \leq 6.5\text{ Gbps}$ | | 0.2 1 | 0.8 5 | ps RMS ps pk-pk |
| | Crosstalk Induced Jitter (Adjacent Channel) (Note 16) | | 0.35 | 0.7 | ps RMS |
| V_{INPP} | Input Voltage Swing (Differential Configuration) (Note 17) | 100 | | 1200 | mV |
| t_r, t_f | Output Rise/Fall Times @ 1 GHz; (20% – 80%), $V_{IN} = 400\text{ mV } Qx, \overline{Qx}$ | 20 | 35 | 50 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

11. Measured using a 100 mVpk-pk source, 50% duty cycle clock source. All output loading with external 50 Ω to V_{CC} . Input edge rates 40 ps (20% – 80%).
12. Output voltage swing is a single-ended measurement operating in differential mode.
13. Skew is measured between outputs under identical transitions and conditions. Duty cycle skew is defined only for differential operation when the delays are measured from cross-point of the inputs to the cross-point of the outputs.
14. Additive RMS jitter with 50% duty cycle clock signal.
15. Additive Peak-to-Peak data dependent jitter with input NRZ data at PRBS23.
16. Crosstalk is measured at the output while applying two similar clock frequencies that are asynchronous with respect to each other at the inputs.
17. Input voltage swing is a single-ended measurement operating in differential mode.

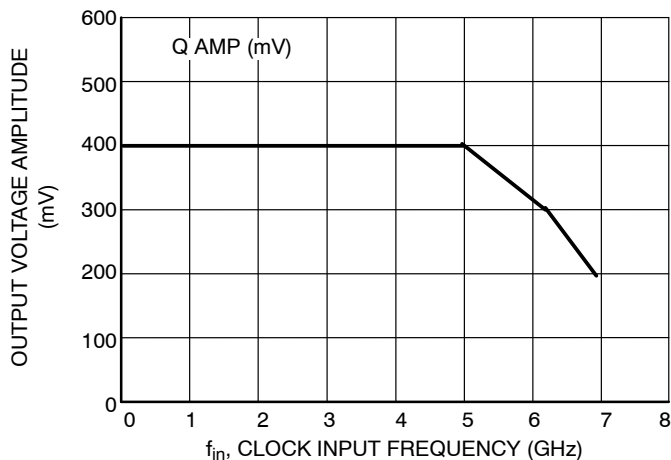


Figure 3. Clock Output Voltage Amplitude (V_{OUTPP}) vs. Input Frequency (f_{in}) at Ambient Temperature (Typical)

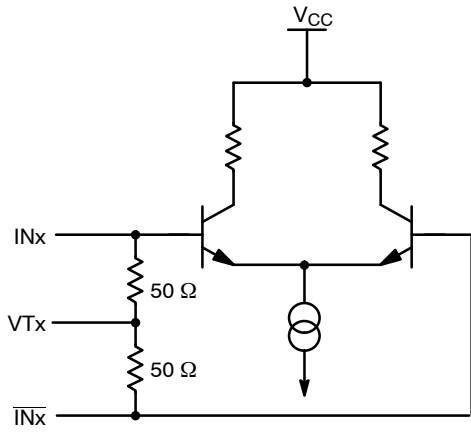


Figure 4. Input Structure

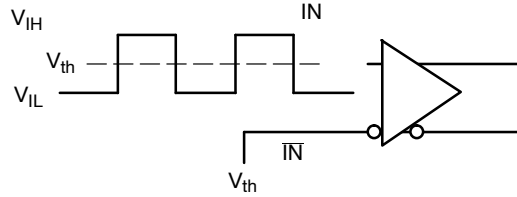


Figure 5. Differential Input Driven Single-Ended

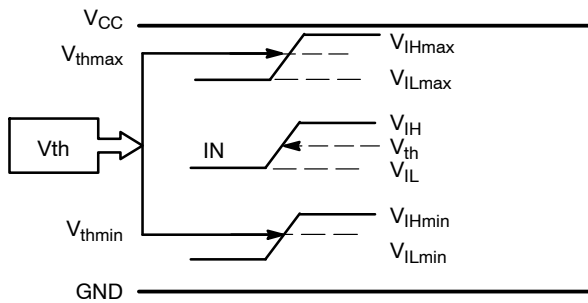


Figure 6. V_{th} Diagram

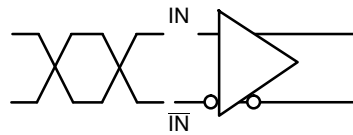


Figure 7. Differential Inputs Driven Differentially

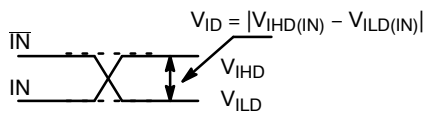


Figure 8. Differential Inputs Driven Differentially

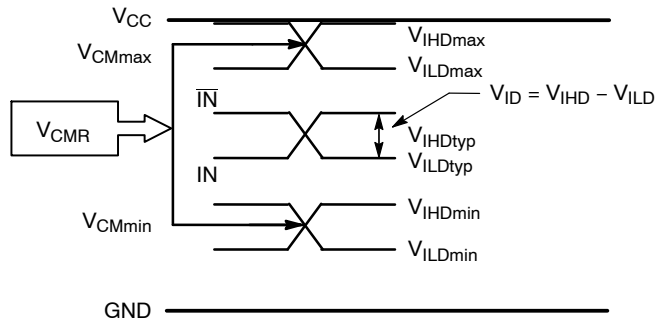


Figure 9. V_{CMR} Diagram

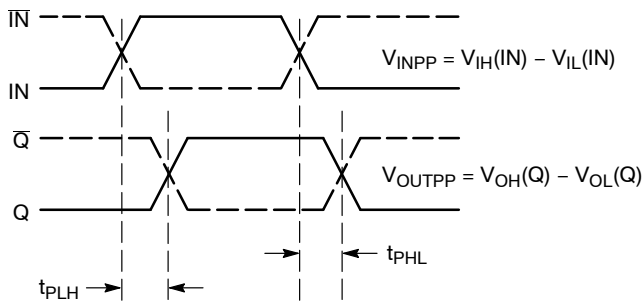


Figure 10. AC Reference Measurement

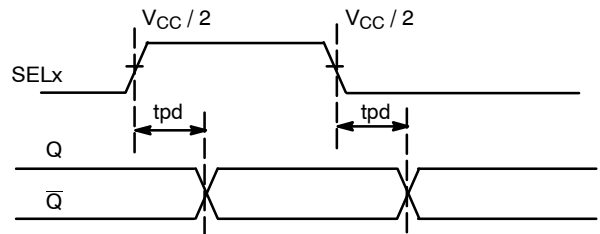


Figure 11. SELx to Qx Timing Diagram

NB6L572M

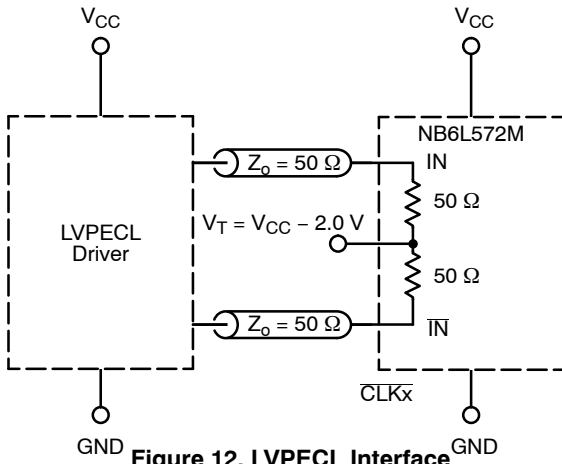


Figure 12. LVPECL Interface

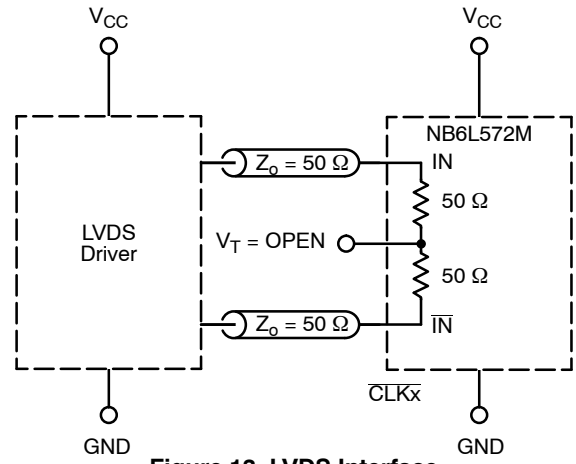


Figure 13. LVDS Interface

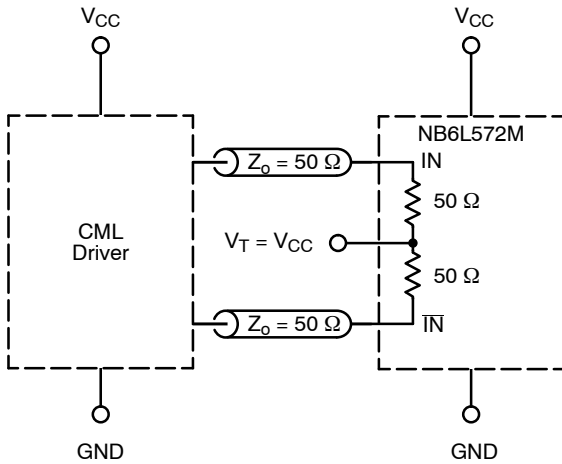


Figure 14. Standard 50 Ω Load CML Interface

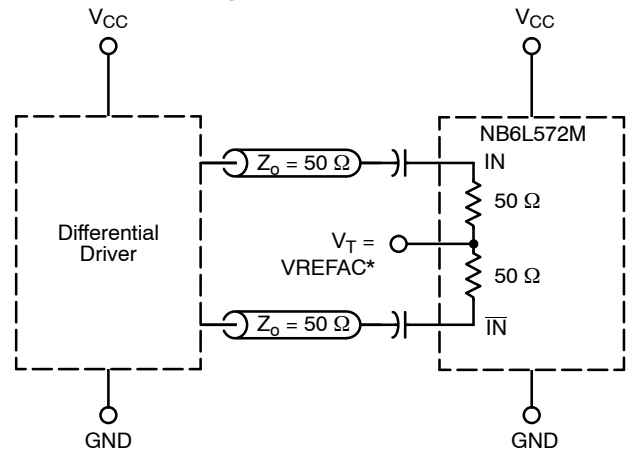


Figure 15. Capacitor-Coupled Differential Interface (V_T Connected to External V_{REFAC})

* V_{REFAC} bypassed to ground with a 0.01 μF capacitor.

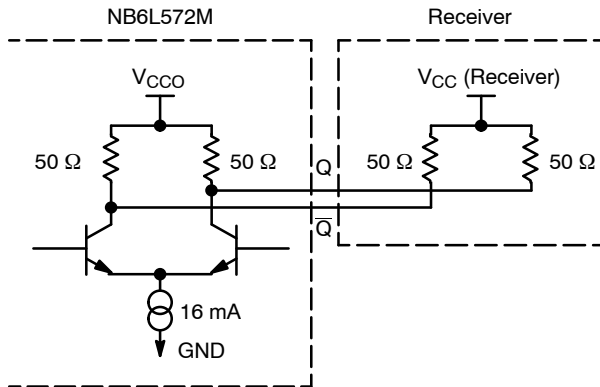


Figure 16. Typical CML Output Structure and Termination ($V_{CC} = 2.5 \text{ V}$ or 3.3 V)

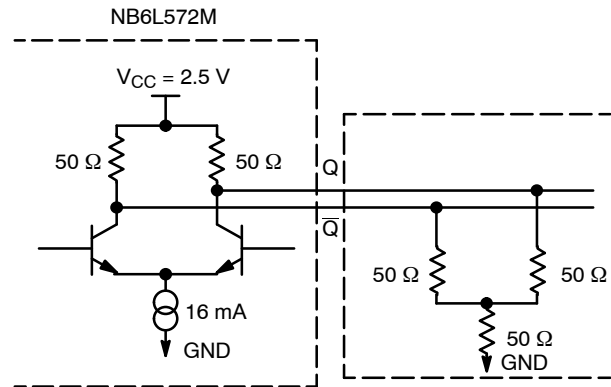


Figure 17. Alternative Output Termination ($V_{CC} = 2.5 \text{ V}$, Only)

DEVICE ORDERING INFORMATION

| Device | Package | Shipping [†] |
|---------------|---------------------|-----------------------|
| NB6L572MMNG | QFN-32 (Pb-Free) | 74 Units / Rail |
| NB6L572MMNR4G | QFN-32 (Pb-Free) | 1000 / Tape & Reel |

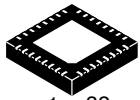
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

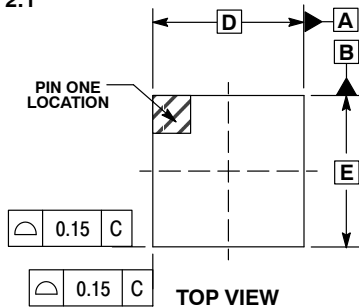


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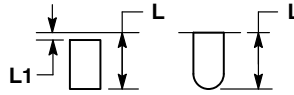
SCALE 2:1

QFN32 5x5, 0.5P
CASE 488AM
ISSUE A

DATE 23 OCT 2013



TOP VIEW

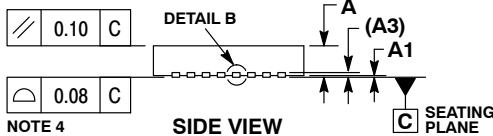


DETAIL A
ALTERNATE TERMINAL
CONSTRUCTIONS

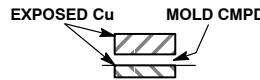
NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| MILLIMETERS | | |
|-------------|------|------|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | --- | 0.05 |
| A3 | 0.20 | REF |
| b | 0.18 | 0.30 |
| D | 5.00 | BSC |
| D2 | 2.95 | 3.25 |
| E | 5.00 | BSC |
| E2 | 2.95 | 3.25 |
| e | 0.50 | BSC |
| K | 0.20 | --- |
| L | 0.30 | 0.50 |
| L1 | --- | 0.15 |

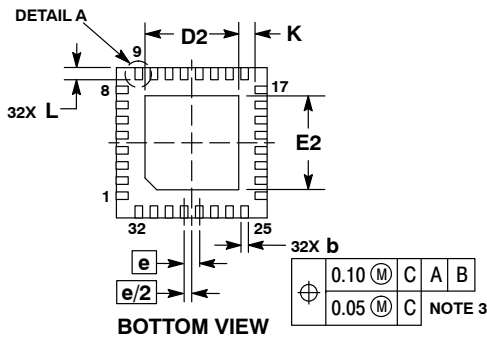


SIDE VIEW

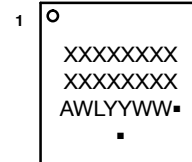


DETAIL B
ALTERNATE
CONSTRUCTION

GENERIC
MARKING DIAGRAM*



BOTTOM VIEW



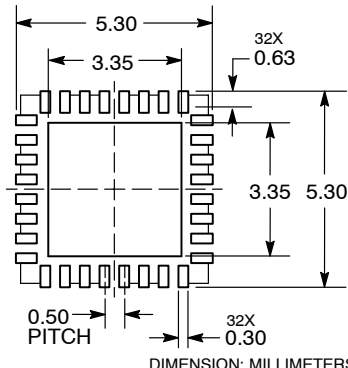
- XXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.

Pb-Free indicator, "G" or microdot "▪", may or may not be present.

RECOMMENDED
SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|------------------|----------------|--|
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