TinyLogic UHS Universal Configurable Two-Input Logic Gates

NC7SZ57, NC7SZ58

ON Semiconductor®

www.onsemi.com

Description

The NC7SZ57 and NC7SZ58 are universal configurable two−input logic gates. Each device is capable of being configured for 1 of 5 unique two−input logic functions. Any possible two−input combinatorial logic function can be implemented, as shown in the *Function Selection Table*. Device functionality is selected by how the device is wired at the board level. *Figures 4 through 13* illustrate how to connect the NC7SZ57 and NC7SZ58, respectively, for the desired logic function. All inputs have been implemented with hysteresis.

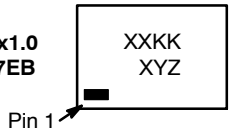
The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a broad V_{CC} operating range. The device is specified to operate over the 1.65 V to 5.5 V V_{CC} operating range. The input and output are high impedance when V_{CC} is 0 V. Inputs tolerate voltages up to 5.5 V independent of V_{CC} operating range.

Features

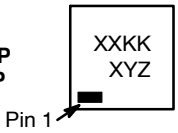
- Ultra High−Speed
- Capable of Implementing any Two−Input Logic Functions
- Typical Usage Replaces Two (2) TinyLogic Gate Devices
- Reduces Part Counts in Inventory
- Broad V_{CC} Operating Range: 1.65 V to 5.5 V
- Power Down High Impednce Input / Output
- Over−Voltage Tolerant Inputs Facilitate 5 V to 3 V Translation
- Proprietary Noise / EMI Reduction Circuitry Implemented
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

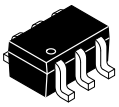
MARKING DIAGRAMS

SIP6 1.45x1.0
CASE 127EB

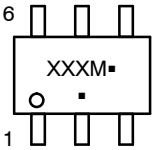


UDFN6
1.0X1.0, 0.35P
CASE 517DP





SC−88
DF SUFFIX
CASE 419B−02



XX, XXX	= Specific Device Code
KK	= 2−Digit Lot Run Traceability Code
XY	= 2−Digit Date Code Format
Z	= Assembly Plant Code
M	= Date Code*
▪	= Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 9 of this data sheet.

Pin Configurations

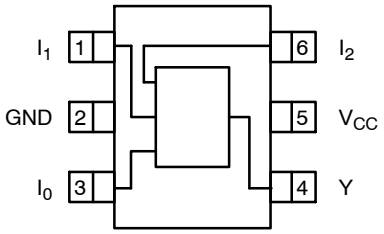


Figure 1. SC70 (Top View)

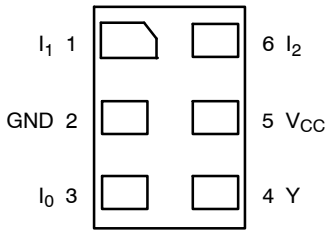
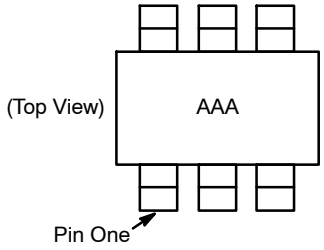


Figure 3. MicroPak™ (Top Through View)



NOTES:
1. AAA represents product code top mark (*see* *Ordering Information*).
2. Orientation of top mark determines pin one location.
3. Reading the top mark left to right, pin one is the lower left pin.

Figure 2. Pin 1 Orientation

PIN DEFINITIONS

Pin # SC70	Pin # MicroPak	Name	Description
1	1	I_1	Data Input
2	2	GND	Ground
3	3	I_0	Data Input
4	4	Y	Output
5	5	V_{CC}	Supply Voltage
6	6	I_2	Data Input

FUNCTION TABLE

Inputs			NC7SZ57	NC7SZ58
I_2	I_1	I_0	$Y = \overline{(I_0)} \cdot \overline{(I_2)} + (I_1) \cdot (I_2)$	$Y = (I_0) \cdot \overline{(I_2)} + \overline{(I_1)} \cdot (I_2)$
L	L	L	H	L
L	L	H	L	H
L	H	L	H	L
L	H	H	L	H
H	L	L	L	H
H	L	H	L	H
H	H	L	H	L
H	H	H	H	L

H = HIGH Logic Level
L = LOW Logic Level

FUNCTION SELECTION TABLE

2−Input Logic Function	Device Selection	Connection Configuration
2−Input AND	NC7SZ57	Figure 4
2−Input AND with Inverted Input	NC7SZ58	Figure 10, Figure 11
2−Input AND with Both Inputs Inverted	NC7SZ57	Figure 7
2−Input NAND	NC7SZ58	Figure 9
2−Input NAND with Inverted Input	NC7SZ57	Figure 5, Figure 6
2−Input NAND with Both Inputs Inverted	NC7SZ58	Figure 12
2−Input OR	NC7SZ58	Figure 12
2−Input OR with Inverted Input	NC7SZ57	Figure 5, Figure 6
2−Input OR with Both Inputs Inverted	NC7SZ58	Figure 9
2−Input NOR	NC7SZ57	Figure 7
2−Input NOR with Inverted Input	NC7SZ58	Figure 9, Figure 10
2−Input NOR with Both Inputs Inverted	NC7SZ57	Figure 4
2−Input XOR	NC7SZ58	Figure 13
2−Input XNOR	NC7SZ57	Figure 8

NC7SZ57 Logic Configurations

Figure 4 through Figure 8 show the logical functions that can be implemented using the NC7SZ57. The diagrams show the DeMorgan's equivalent logic duals for a given two−input function. The logical implementation is next to the board−level physical implementation of how the pins of the function should be connected.

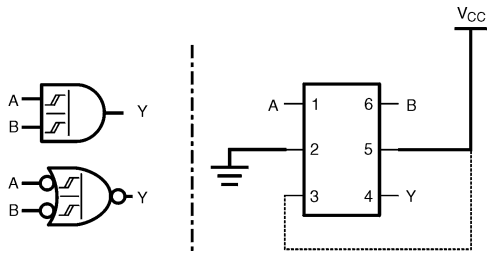


Figure 4. 2−Input AND Gate

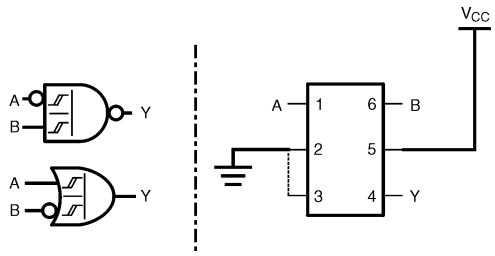


Figure 5. 2−Input NAND with Inverted A Input

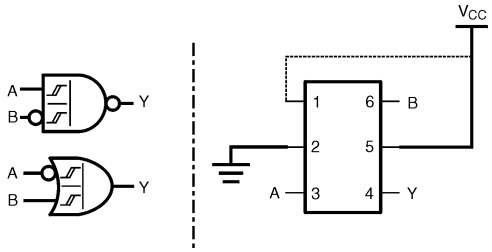


Figure 6. 2−Input NAND with Inverted B Input

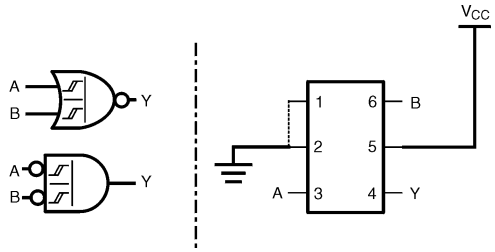


Figure 7. 2−Input NOR Gate

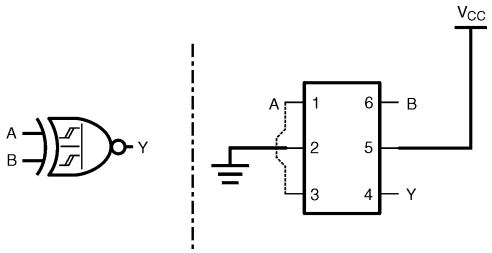


Figure 8. 2−Input XNOR Gate

NC7SZ58 Logic Configurations

Figure 9 through Figure 13 show the logical functions that can be implemented using the NC7SZ58. The diagrams show the DeMorgan's equivalent logic duals for a given two−input function. The logical implementation is next to the board−level physical implementation of how the pins of the function should be connected.

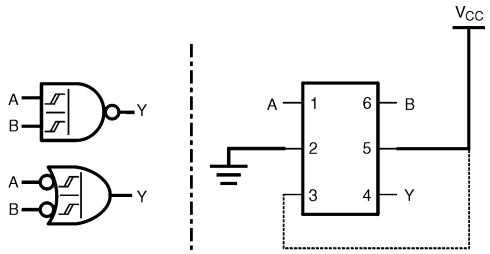


Figure 9. 2−Input NAND Gate

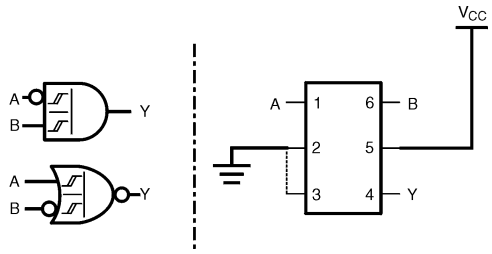


Figure 10. 2−Input AND with Inverted A Input

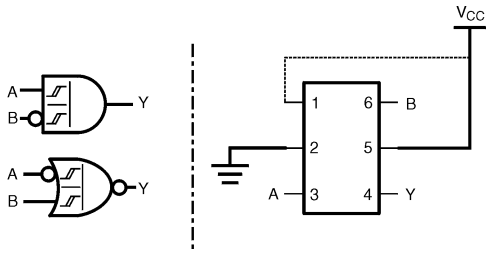


Figure 11. 2−Input AND with Inverted B Input

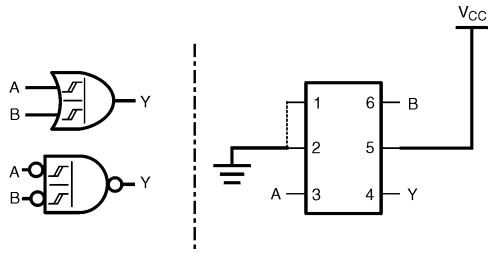


Figure 12. 2−Input OR Gate

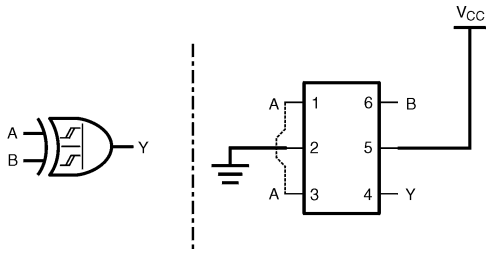


Figure 13. 2−Input XOR Gate

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		−0.5	6.5	V
V_{IN}	DC Input Voltage		−0.5	6.5	V
V_{OUT}	DC Output Voltage		−0.5	6.5	V
I_{IK}	DC Input Diode Current	V_{IN} < 0 V	−	−50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < 0 V	−	−50	mA
I_{OUT}	DC Output Source / Sink Current		−	±50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current		−	±50	mA
T_{STG}	Storage Temperature Range		−65	+150	°C
T_J	Maximum Junction Temperature under Bias		−	+150	°C
T_L	Lead Temperature, Soldering, 10 Seconds		−	+260	°C
P_D	Power Dissipation in Still Air	SC70−6	−	332	mW
		MicroPak−6	−	812	
		MicroPak2™ −6	−	812	
ESD	Human Body Model, JEDEC: JESD22−A114		−	4000	V
	Charge Device Model, JEDEC: JESD22−C101		−	2000	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage Operating		1.65	5.5	V
	Supply Voltage Data Retention		1.5	5.5	
V_{IN}	Input Voltage		0	5.5	V
V_{OUT}	Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		−40	+85	°C
θ_{JA}	Thermal Resistance	SC70−6	−	377	°C/W
		MicroPak−6	−	154	
		MicroPak2−6	−	154	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTICAL CHARACTERISTICS

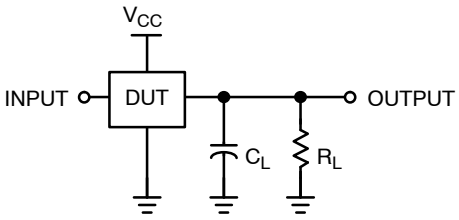
Symbol	Parameter	V_{CC} (V)	Conditions		T_A = +25°C			T_A = −40 to +85°C		Unit
					Min	Typ	Max	Min	Max	
V_P	Positive Threshold Voltage	1.65			–	0.99	1.40	–	1.40	V
		2.30			–	1.39	1.80	–	1.80	
		3.00			–	1.77	2.20	–	2.20	
		4.50			–	2.49	3.10	–	3.10	
		5.50			–	2.95	3.60	–	3.60	
V_N	Negative Threshold Voltage	1.65			0.20	0.50	–	0.20	–	V
		2.30			0.40	0.75	–	0.40	–	
		3.00			0.60	0.99	–	0.60	–	
		4.50			1.00	1.43	–	1.00	–	
		5.50			1.20	1.70	–	1.20	–	
V_H	Hysteresis Voltage	1.65			0.15	0.48	0.90	0.15	0.90	V
		2.30			0.25	0.64	1.10	0.25	1.10	
		3.00			0.40	0.78	1.20	0.40	1.20	
		4.50			0.60	1.06	1.50	0.60	1.50	
		5.50			0.70	1.25	1.70	0.70	1.70	
V_{OH}	HIGH Level Output Voltage	1.65	V_{IN} = V_{IH} or V_{IL} I_{OH} = −100 μA		1.55	1.65	–	1.55	–	V
		2.30			2.20	2.30	–	2.20	–	
		3.00			2.90	3.00	–	2.90	–	
		4.50			4.40	4.50	–	4.40	–	
		1.65	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −4 mA	1.29	1.52	–	1.29	–	
		2.30		I_{OH} = −8 mA	1.90	2.15	–	1.90	–	
		3.00		I_{OH} = −16 mA	2.40	2.80	–	2.40	–	
		3.00		I_{OH} = −24 mA	2.30	2.68	–	2.30	–	
		4.50		I_{OH} = −32 mA	3.80	4.20	–	3.80	–	
V_{OL}	LOW Level Output Voltage	1.65	V_{IN} = V_{IH} or V_{IL} I_{OL} = 100 μA		–	–	0.10	–	0.10	V
		2.30			–	–	0.10	–	0.10	
		3.00			–	–	0.10	–	0.10	
		4.50			–	–	0.10	–	0.10	
		1.65	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4 mA	–	0.08	0.24	–	0.24	
		2.30		I_{OL} = 8 mA	–	0.10	0.30	–	0.30	
		3.00		I_{OL} = 16 mA	–	0.15	0.40	–	0.40	
		3.00		I_{OL} = 24 mA	–	0.22	0.55	–	0.55	
		4.50		I_{OL} = 32 mA	–	0.22	0.55	–	0.55	
I_{IN}	Input Leakage Current	1.65 to 5.50	V_{IN} = 5.5 V, GND		–	–	±0.1	–	±1.0	μA
I_{OFF}	Power Off Leakage Current	0	V_{IN} or V_{OUT} = 5.5 V		–	–	1	–	10	μA
I_{CC}	Quiescent Supply Current	1.65 to 5.5	V_{IN} = 5.5 V, GND		–	–	1	–	10	μA

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C			T_A = −40 to +85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay I_n to Y (Figure 14, 16)	1.8 ±0.15	C_L = 15 pF, R_L = 1 MΩ	–	8.0	14.0	–	14.5	ns
		2.5 ±0.2		–	4.9	8.0	–	8.5	
		3.3 ±0.3		–	3.7	5.3	–	5.7	
		5.0 ±0.5		–	2.8	4.3	–	4.6	
		3.3 ±0.3	C_L = 50 pF, R_L = 500 Ω	–	4.2	6.0	–	6.5	ns
		5.0 ±0.5		–	3.4	4.9	–	5.3	
C_{IN}	Input Capacitance	0		–	2	–	–	–	pF
C_{PD}	Power Dissipation Capacitance (Figure 15)	3.3	(Note 4)	–	14	–	–	–	pF
		5.0		–	17	–	–	–	

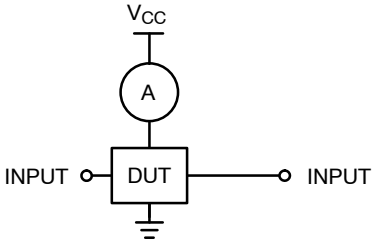
4. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. *(See Figure 12)* C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD} = (C_{PD})\ (V_{CC})\ (f_{IN}) + (I_{CC}static)$.

AC Loading and Waveforms



NOTE:
5. C_L includes load and stray capacitance.
6. Input PRR = 1.0 MHz, t_W = 500 ns.

Figure 14. AC Test Circuit



NOTE:
7. Input = AC Waveforms.
8. PRR = Variable; Duty Cycle = 50%.

Figure 15. I_{CCD} Test Circuit

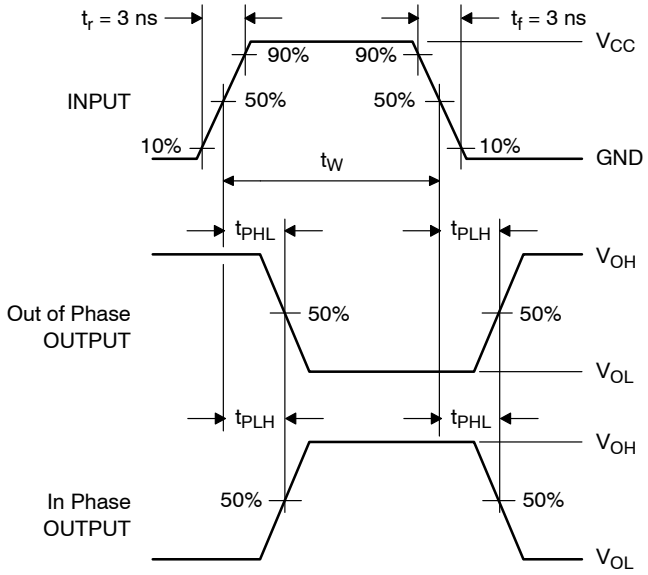


Figure 16. AC Waveforms

ORDERING INFORMATION

Device	Top Mark	Package	Shipping†
NC7SZ57P6X	Z57	6−Lead SC70, EIAJ SC−88, 1.25 mm Wide	3000 / Tape & Reel
NC7SZ57L6X	KK	6−Lead Micropak, 1.0 mm Wide	5000 / Tape & Reel
NC7SZ57FHX	KK	6−Lead, MicroPak2, 1x1 mm Body, .35 mm Pitch	5000 / Tape & Reel
NC7SZ58P6X	Z58	6−Lead SC70, EIAJ SC−88, 1.25 mm Wide	3000 / Tape & Reel
NC7SZ58L6X	LL	6−Lead Micropak, 1.0 mm Wide	5000 / Tape & Reel
NC7SZ58FHX	LL	6−Lead, MicroPak2 , 1x1 mm Body, .35 mm Pitch	5000 / Tape & Reel

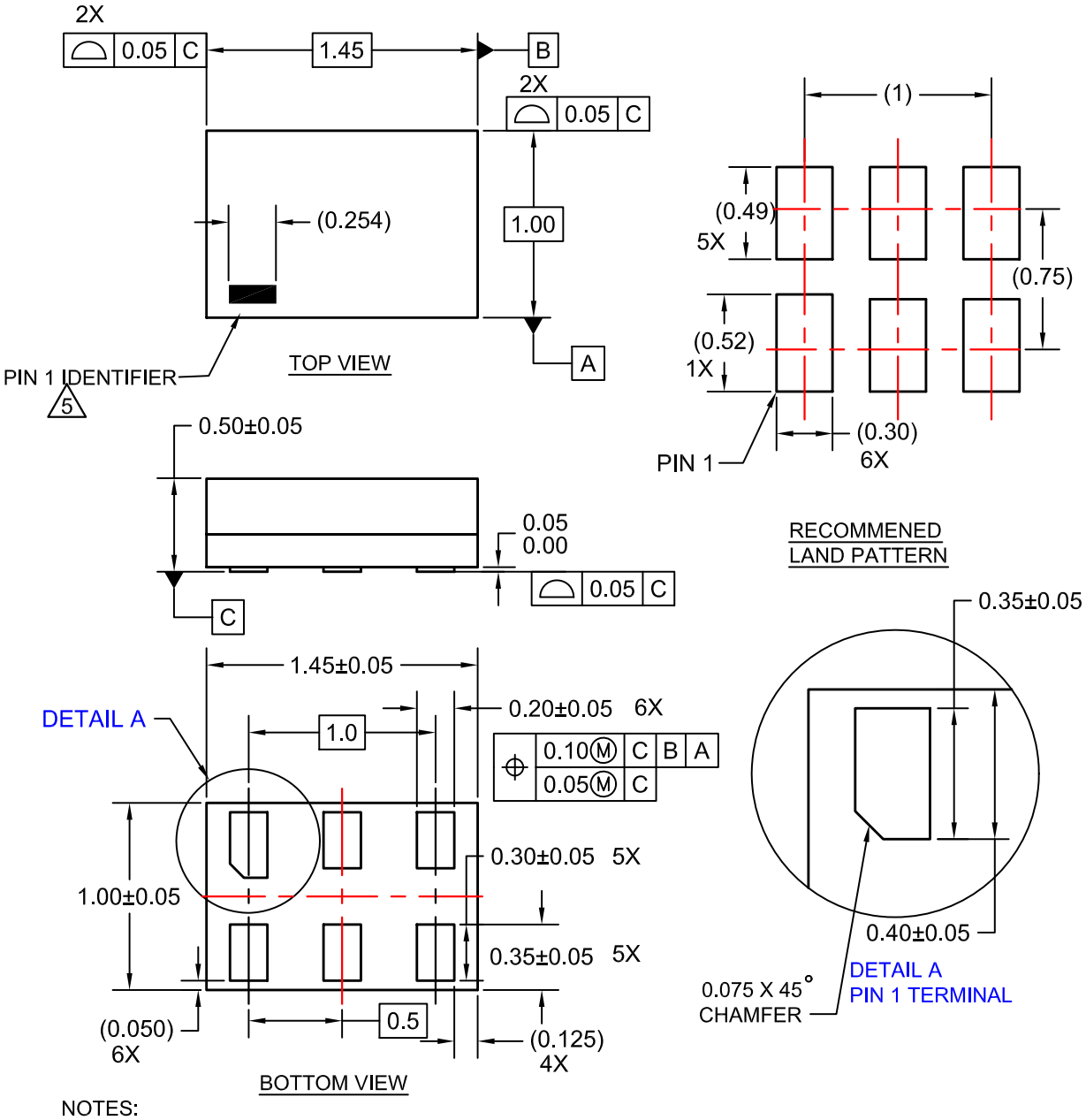
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SIP6 1.45X1.0
CASE 127EB
ISSUE O

DATE 31 AUG 2016



NOTES:

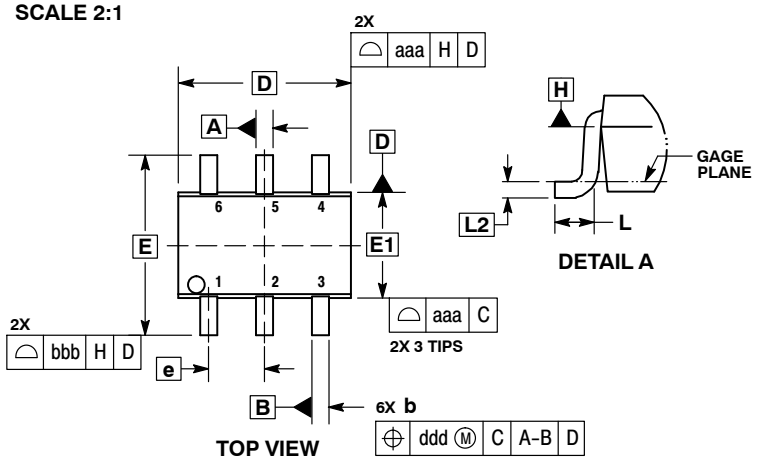
1. CONFORMS TO JEDEC STANDARD MO-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-2009
4. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

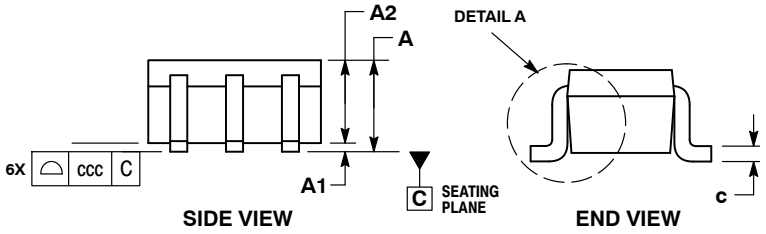
DOCUMENT NUMBER:	**98AON13590G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SIP6 1.45X1.0**	**PAGE 1 OF 1**

SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE Y

DATE 11 DEC 2012

1
SCALE 2:1

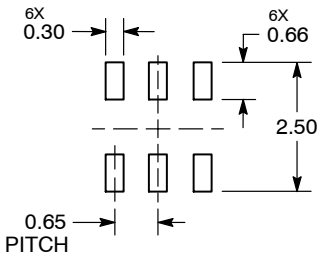




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

	MILLIMETERS			INCHES		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	−−−	−−−	1.10	−−−	−−−	0.043
A1	0.00	−−−	0.10	0.000	−−−	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

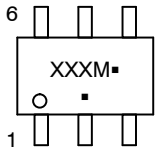
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE Y

DATE 11 DEC 2012

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. COLLECTOR
4. EMITTER
5. BASE
6. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 6:
PIN 1. ANODE 2
2. N/C
3. CATHODE 1
4. ANODE 1
5. N/C
6. CATHODE 2

STYLE 7:
PIN 1. SOURCE 2
2. DRAIN 2
3. GATE 1
4. SOURCE 1
5. DRAIN 1
6. GATE 2

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. EMITTER 2
2. EMITTER 1
3. COLLECTOR 1
4. BASE 1
5. BASE 2
6. COLLECTOR 2

STYLE 10:
PIN 1. SOURCE 2
2. SOURCE 1
3. GATE 1
4. DRAIN 1
5. DRAIN 2
6. GATE 2

STYLE 11:
PIN 1. CATHODE 2
2. CATHODE 2
3. ANODE 1
4. CATHODE 1
5. CATHODE 1
6. ANODE 2

STYLE 12:
PIN 1. ANODE 2
2. ANODE 2
3. CATHODE 1
4. ANODE 1
5. ANODE 1
6. CATHODE 2

STYLE 13:
PIN 1. ANODE
2. N/C
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 14:
PIN 1. VREF
2. GND
3. GND
4. IOUT
5. VEN
6. VCC

STYLE 15:
PIN 1. ANODE 1
2. ANODE 2
3. ANODE 3
4. CATHODE 3
5. CATHODE 2
6. CATHODE 1

STYLE 16:
PIN 1. BASE 1
2. EMITTER 2
3. COLLECTOR 2
4. BASE 2
5. EMITTER 1
6. COLLECTOR 1

STYLE 17:
PIN 1. BASE 1
2. EMITTER 1
3. COLLECTOR 2
4. BASE 2
5. EMITTER 2
6. COLLECTOR 1

STYLE 18:
PIN 1. VIN1
2. VCC
3. VOUT2
4. VIN2
5. GND
6. VOUT1

STYLE 19:
PIN 1. I OUT
2. GND
3. GND
4. V CC
5. V EN
6. V REF

STYLE 20:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 21:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. N/C
6. CATHODE 1

STYLE 22:
PIN 1. D1 (i)
2. GND
3. D2 (i)
4. D2 (c)
5. VBUS
6. D1 (c)

STYLE 23:
PIN 1. Vn
2. CH1
3. Vp
4. N/C
5. CH2
6. N/C

STYLE 24:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 25:
PIN 1. BASE 1
2. CATHODE
3. COLLECTOR 2
4. BASE 2
5. EMITTER
6. COLLECTOR 1

STYLE 26:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 27:
PIN 1. BASE 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. EMITTER 2
6. COLLECTOR 2

STYLE 28:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 29:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE/ANODE
6. CATHODE

STYLE 30:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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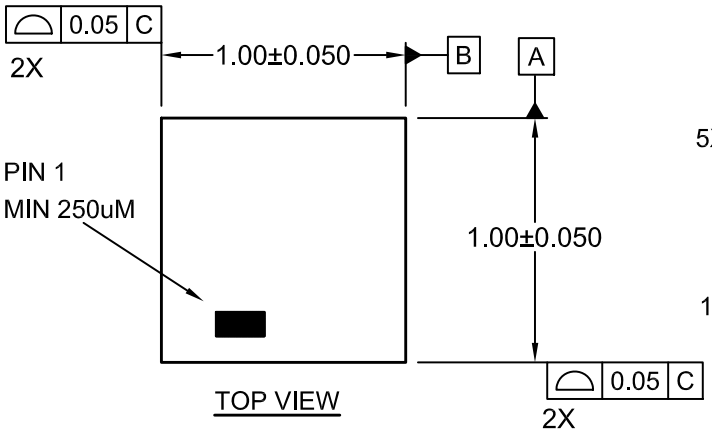
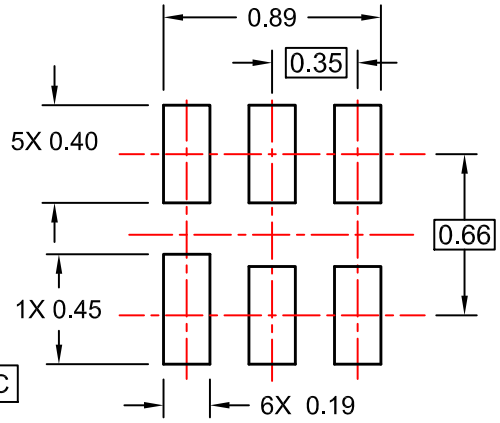
DESCRIPTION:	**SC−88/SC70−6/SOT−363**	**PAGE 2 OF 2**

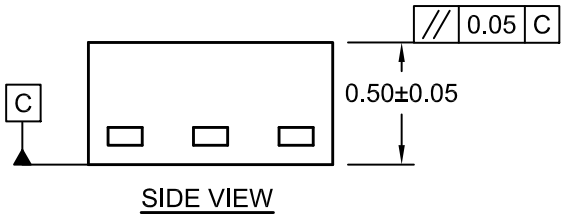
UDFN6 1.0X1.0, 0.35P
CASE 517DP
ISSUE O

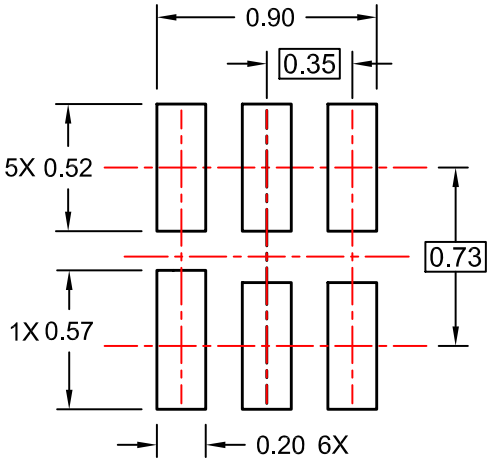
DATE 31 AUG 2016



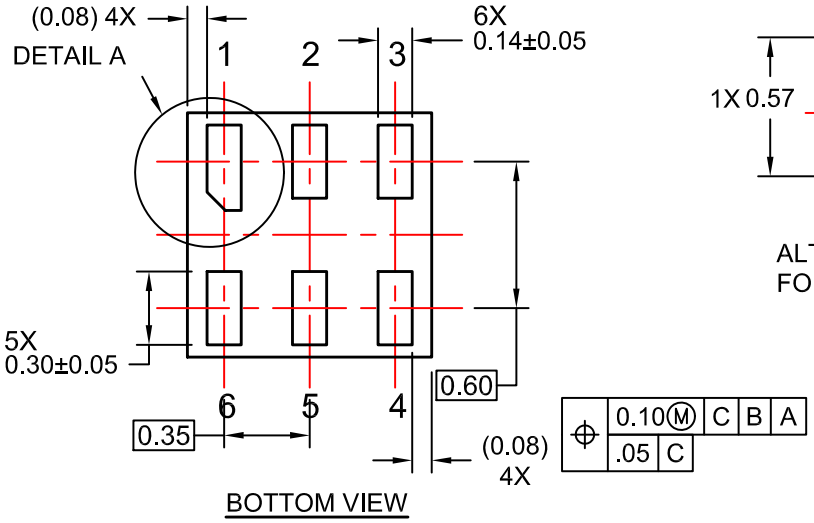


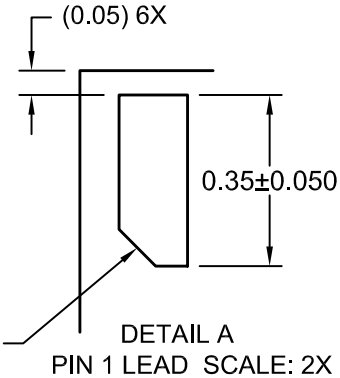
RECOMMENDED LAND PATTERN
FOR SPACE CONSTRAINED PCB





ALTERNATIVE LAND PATTERN
FOR UNIVERSAL APPLICATION





NOTES:

A. COMPLIES TO JEDEC MO-252 STANDARD
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009

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DESCRIPTION:	**UDFN6 1.0X1.0, 0.35P**	**PAGE 1 OF 1**