NCL30388LED1GEVB

NCL30388LED1 60 W High Power Factor LED Driver Evaluation Board User’s Manual

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EVAL BOARD USER’S MANUAL

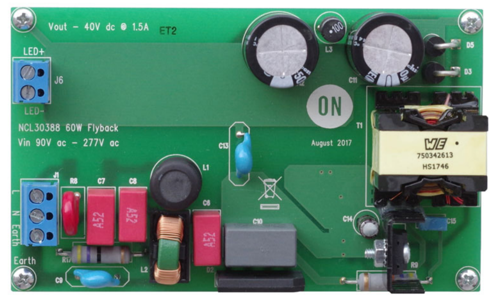


Figure 1. NCL30388LED1 Evaluation Board

Evaluation Board Overview

This manual covers the specification, theory of operation, testing and construction of the NCL30388LED1GEVB demonstration board. The NCL30388 board demonstrates an isolated Primary Side Regulation 60 W high PF flyback LED driver for a typical troffer application.

The Key Features of this Demo Board

- Low THD
- High Power Factor
- Fast Startup
- CC/CV Operation
- Integrated Fault Protection
  - Brown−Out Protection
  - Winding and Diode Short Circuit Protection
  - Over Temperature
  - Output Over Current
  - Output Over Voltage

Specifications

Input Voltage	100 − 265 V ac	
Line Frequency	50/60 Hz	
Power Factor (100% Load)	0.9	Min.
THD (Load > 20%)	20%	Max.
Output Voltage	40 V dc	
Output Ripple	50%	Pk − Pk
Output Current	1.5 A dc	±5%
Efficiency	92%	Max.
Start Up Time	< 250 ms	

April, 2018 − Rev.0
Publication Order Number:
EVBUM2558/D

THEORY OF OPERATION

Power Stage

The power stage is a PSR flyback design. No direct connection to the output is required for regulation with a PSR. The power stage operates as a QR power stage. The QR operation allows for optimum commutation of the output diode for good EMI performance and high efficiency. The power stage operates in CrM at loads above 80%. Below 80% load, the power stage goes into valley skip. A line range selector skips an extra valley for line voltages above about 150 V ac. This maintains a more constant operating frequency and improves efficiency.

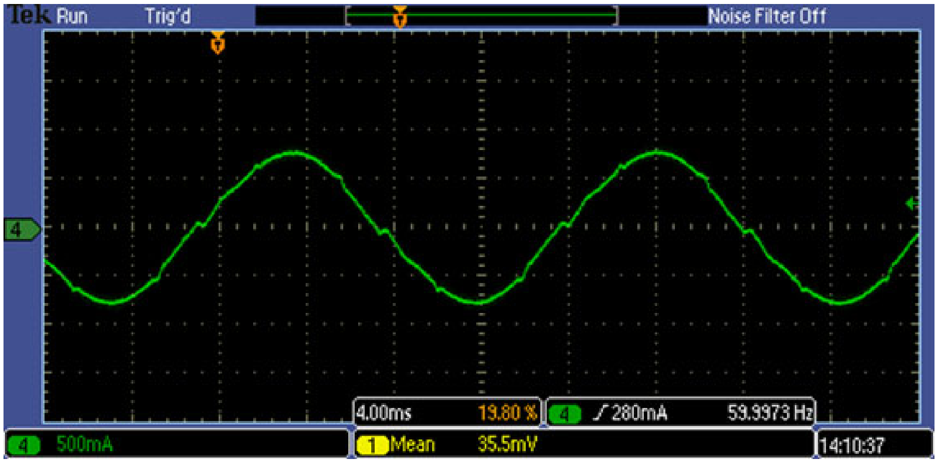


Figure 2. Input Current

HV Pin Functions

The HV Pin provides 3 Essential Functions:

1. HV Start Current
2. Rectified Line Voltage Sensing
   a. PFC Loop Reference
   b. Line Range Selection

HV Start

The HV pin sources current to C14 to until V_{CC} reaches 18 V. The controller starts up at 18 V and begins switching. D4 supplies V_{CC} power from the aux winding to power the NCL30388 and the HV start current source switches off to reduce power losses. The constant current charge of C14 makes the startup time very consistent over line. The HV startup will supply V_{CC} power when the V_{CC} reaches 8.6 V to maintain operation in extreme light load conditions. The HV pin's 700 V rating is robust for applications above 265 V ac.

Rectified Line Sensing

The rectified AC line supplies the HV pin a reference for the PFC loop. The signal is internally scaled for the control circuit. As such, distortion on this pin will result in distortion in the input current. Low distortion over a wide mains is best achieved with a small capacitor on the HVDC or even placed on the AC side of the bridge rectifier. L1 attenuates EMI because the value of C10 is small to preserve high PF and low THD. C7 & R17 form a damper to dampen out resonances in the EMI filter.

Line Range Selection

Internally the HV pin changes gain in the feedback loop to dynamically adjust the control for optimum PF, THD, and regulation. Unlike controllers such as NCL30188, the range selection voltage is not user adjustable because the division from HVDC in set internally rather than externally. While this may seem to be a loss of adjustability, the range selection is set to a voltage that is not within any normal operating range worldwide.

ZCD Pin

The ZCD pin senses zero current point to restart the switch cycle and counts the valleys for valley selection. Additionally the ZCD pin senses the output voltage from the aux winding for short circuit detection and CV set voltage. If the ZCD pin does not measure a voltage greater than 1 V in the off time, the controller shuts down because it interprets this as a short circuit. The controller will restart in 4s. The CV set voltage is 2.48 V on the ZCD pin during the off time. This voltage is scaled through the turns ratio of the flyback transformer and the resistor divider on ZCD to regulate the output voltage in case of an open load. The voltage is constantly regulated rather than switching off as an OVP event. This allows the output to be used as a CV output as well as a CC output. Care must be taken to ensure that the CV set point is above the maximum LED voltage or the LED will dim as the CV loop limits the output voltage. We can see that the ZCD voltage is limited to the range of 1 V to 2.48 V in normal operation. This gives a practical LED output voltage range of 2:1.

Output Current regulation

Output current regulation is set by the primary sense resistor R15 & R14 according to this equation:

$$I_{out} = \frac{V_{REF}}{8 N_{sp} R_{sense}} \qquad \text{(eq. 1)}$$

Where Vref = 0.33 V and Nsp = Secondary/Primary turns ratio.

The internal control algorithm computes the output current based on measured parameters on the primary side which eliminates the need for secondary side controls circuits.

Comp Pin

The Comp pin is the output from the OTA that regulates current or voltage. As with any PFC, the bandwidth of this feedback loop must be less than the line frequency. R11, C17, & C18 make up the compensation network. The network can be as simple as a single capacitor but better dynamic response is achieved with this network configuration. The NCL30388 samples the max and min values on the comp pin and averages them mathematically. This makes the PF and THD much less dependent on the line frequency ripple on comp.

CS Pin

The current sense pin controls the peak primary current. The maximum threshold in normal operation is 1.38 V with an LEB of 330 ns. In case of extreme faults such as a shorted rectifier, the threshold for immediate stop is 1.99 V with an LEB of 170 ns. R13 provides 2 important functions:

1. CS Short Detection
2. Line Feedforward Compensation

CS Short Detection

During startup, CS sources a small current to check if the CS pin is accidently shorted to ground. In reality, this is usually a manufacturing defect. Typically a shorted CS pin would result in catastrophic failure if undetected. Thanks to this protection feature, a failure can be avoided. R13 must be greater than 250 Ω or CS will detect a short. Note that this short circuit checking is turned off during normal switching operation.

Line Feedforward

The PSR control compensates for many errors in computing the output current such as leakage inductance. Some error sources are variable with line such as the effect of delays in the power stage. As the input voltage increases, the power stage delays cause the peak current to overshoot slightly the intended target peak current. This results in output current increasing with line. While this is not usually a very large increase in output current, the control can compensate for this by sourcing a current into CS that is proportional to the input voltage. This reduces the target peak current slightly such that the effect of the delay is cancelled and regulation is improved. Finding the optimum value of R13 is a bit of trial and error. Also any impedance between DRV and the FET, will degrade regulation.

Protection

Thermal Protection

The thermal protection based on internal die temperature is built into the NCL30388.

OVP

An OVP is activated if V_{CC} exceeds 26.5 V. The NCL30388 will timeout for 4 s and attempt to restart.

SCHEMATIC

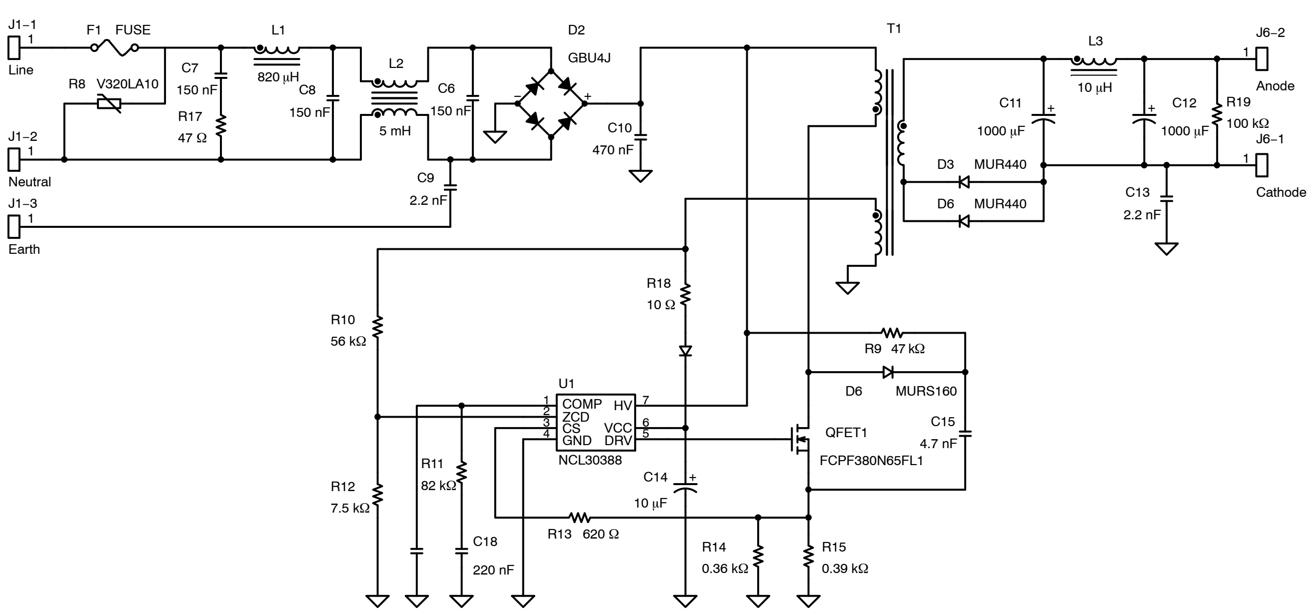


Figure 3. Schematic

GERBER VIEWS

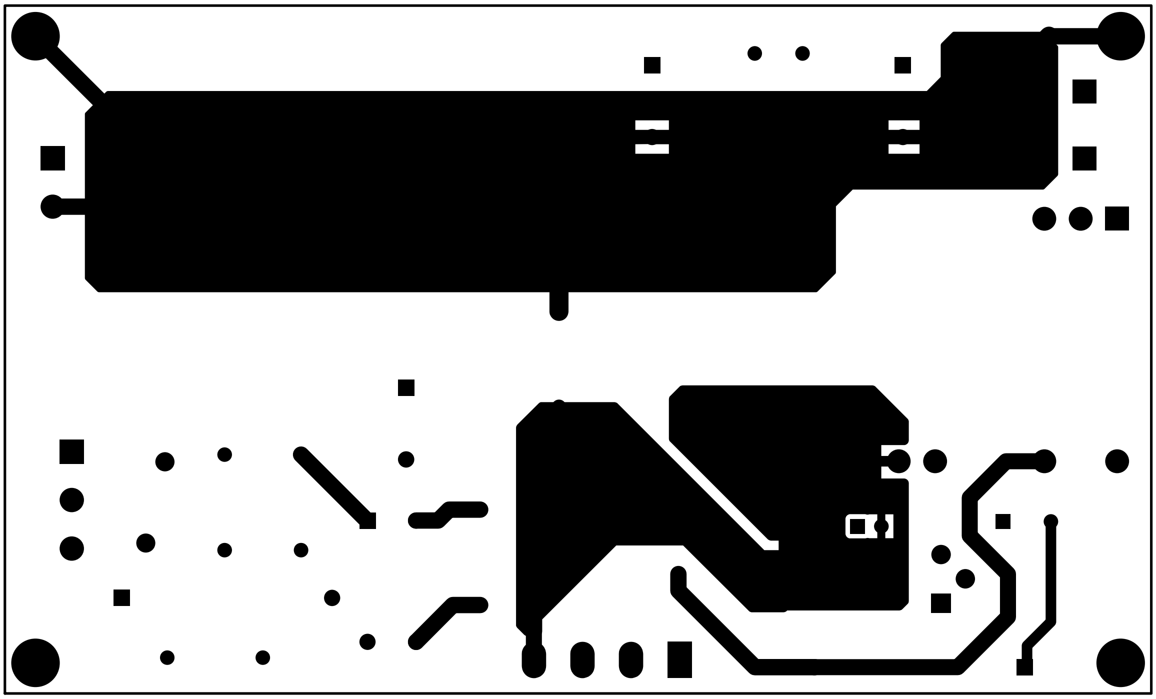


Figure 4. Top Side PCB

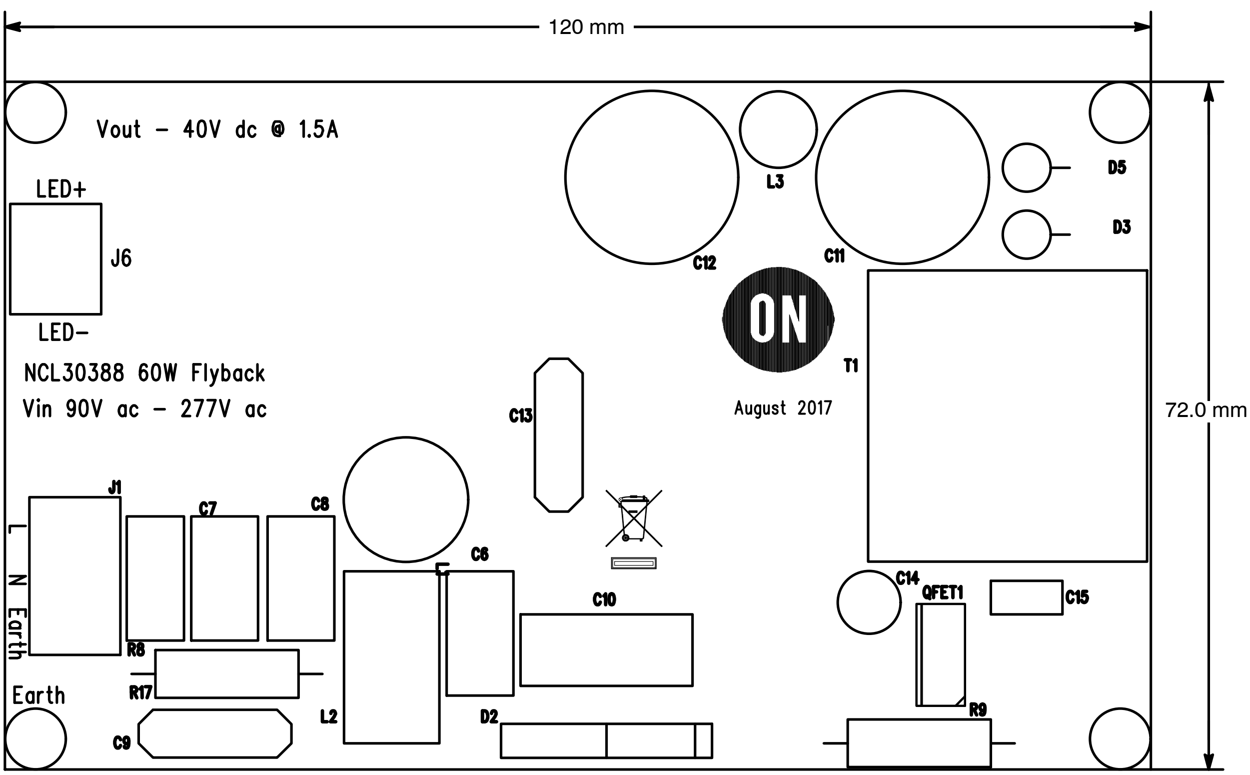


Figure 5. PCB Outline

CIRCUIT BOARD FABRICATION NOTES

1. Fabricate per IPC−6011 and IPC6012. Inspect to IPA−A−600 Class 2 or updated standard.
2. Printed Circuit Board is defined by files listed in fileset.
3. Modification to copper within the PCB outline is not allowed without permission, except where noted otherwise. The manufacturer may make adjustments to compensate for manufacturing process, but the final PCB is required to reflect the associated gerber file design ±0.001 in. for etched features within the PCB outline.
4. Material in accordance with IPC−4101/21, FR4, Tg 125°C min.
5. Layer to layer registration shall not exceed ±0.004 in.
6. External finished copper conductor thickness shall be 0.0026 in. min. (ie 2 oz)
7. Copper plating thickness for through holes shall be 0.0013 in. min. (ie 1 oz)
8. All holes sizes are finished hole size.
9. Finished PCB thickness 0.062 in.
10. All un-dimensioned holes to be drilled using the NC drill data.
11. Size tolerance of plated holes: ±0.003 in.: non−plated holes ±0.002 in.
12. All holes shall be ±0.003 in. of their true position U.D.S.
13. Construction to be SMOBC, using liquid photo image (LPI) solder mask in accordance with IPC−SM−B40C, Type B, Class 2, and be green in color.
14. Solder mask mis-registration ±0.004 in. max.
15. Silkscreen shall be permanent non−conductive white ink.
16. The fabrication process shall be UL approved and the PCB shall have a flammability rating of UL94V0 to be marked on the solder side in silkscreen with date, manufactures approved logo, and type designation.
17. Warp and twist of the PCB shall not exceed 0.0075 in. per in.
18. 100% electrical verification required.
19. Surface finish: electroless nickel immersion gold (ENIG)
20. RoHS 2002/95/EC compliance required.

ECA PICTURE

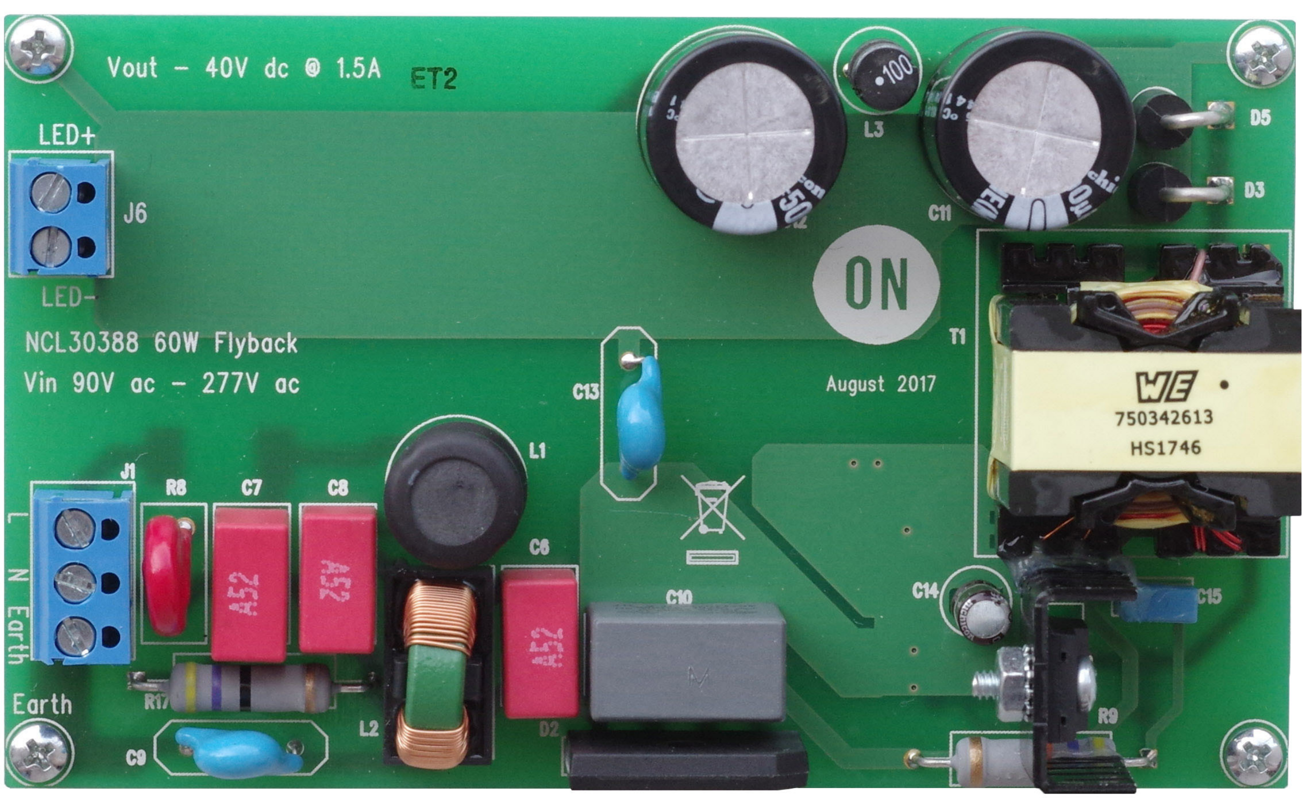


Figure 6. Top View

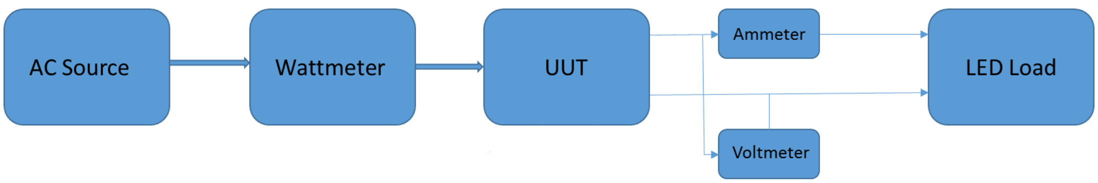
TEST PROCEDURE

Equipment Needed

- AC Source – 90 to 265 V ac 50/60 Hz Minimum 100 W capability
- AC Wattmeter – 100 W Minimum, True RMS Input Voltage, Current, and Power Factor 0.2% accuracy or better
- DC Voltmeter – 100 V dc minimum 0.1% accuracy or better
- DC Ammeter – 2 A dc minimum 0.1% accuracy or better
- LED Load – 35 V to 40 V @ 1.5 A
- Resistor Load – 100 Ω, 30 Watt minimum

Test Connections

1. Connect the LED Load to J6 ‘LED+’ and ‘LED−’ terminals through the ammeter shown in Figure 7. ***Caution: Observe the correct polarity or the load may be damaged.***
2. Connect the AC power to the input of the AC wattmeter shown in Figure 7. Connect J1 ‘L’ and ‘N’ terminals to the output of the AC wattmeter. Connect J1 Earth to ground for safety.
3. Connect the DC voltmeter as shown in Figure 7.



NOTE: Unless otherwise specified, all voltage measurements are taken at the terminals of the UUT.

Figure 7. Test Set Up

Constant Current Regulation

Functional Test Procedure

1. Set the LED Load between 36 and 40 Volts.
2. Set the input voltage as indicated. ***Caution: Do not touch the ECA once it is energized because there are hazardous voltages present.***

Max Load:

- Enter ‘P’ or ‘F’ in column depending on test result

	Input Power	Power Factor		Output Current		Output Voltage
		Reading	Pass/Fail (>0.9)	Reading	Pass/Fail (1.35 A to 1.55 A)	
90 V						
120 V						
230 V						
265 V						

$$\text{Efficiety} = \frac{V_{out} \times I_{out}}{\text{Pin}} \times 100\% \qquad \text{(eq. 2)}$$

3. Set input voltage to zero after completing tests above.

Constant Voltage Regulation

Functional Test Procedure

1. Remove LED load and replace with 100 Ω resistor to J6 ‘LED+’ and ‘LED−’ terminals.
2. Set the input voltage as indicated. ***Caution: Do not touch the ECA once it is energized because there are hazardous voltages present.***

- Enter ‘P’ or ‘F’ in column depending on test result

Input Voltage	Output Voltage	
	Reading	Pass/Fail (<43 V dc)
120 V		
230 V		

3. Turn off all power sources at end of test.

TEST DATA

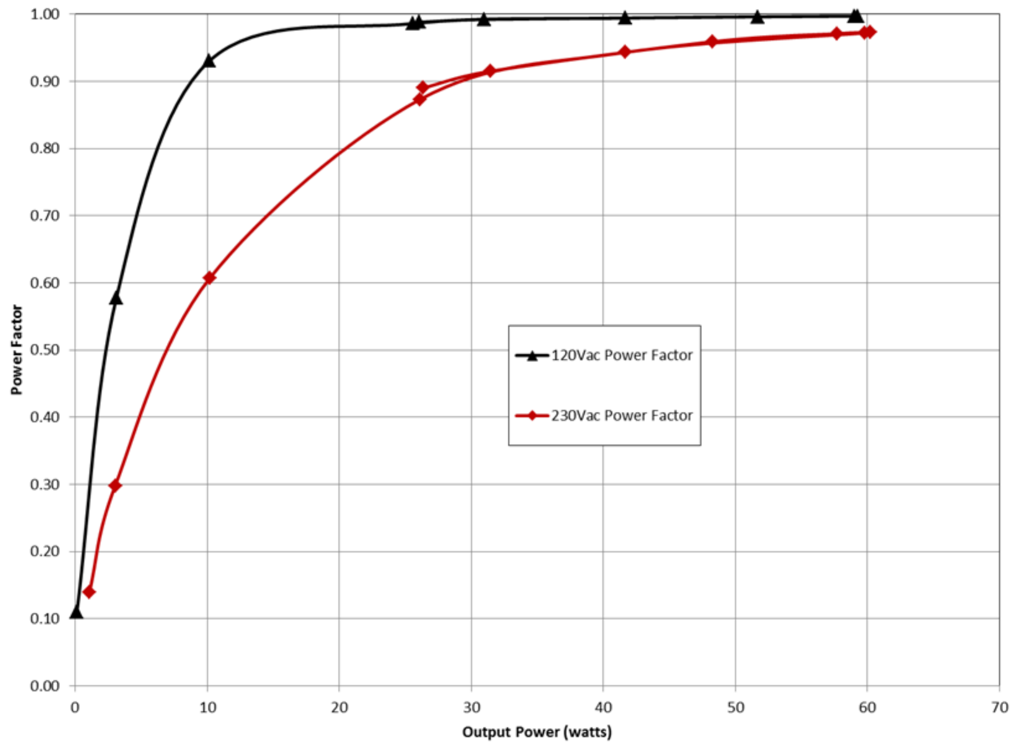


Figure 8. Power Factor over Load

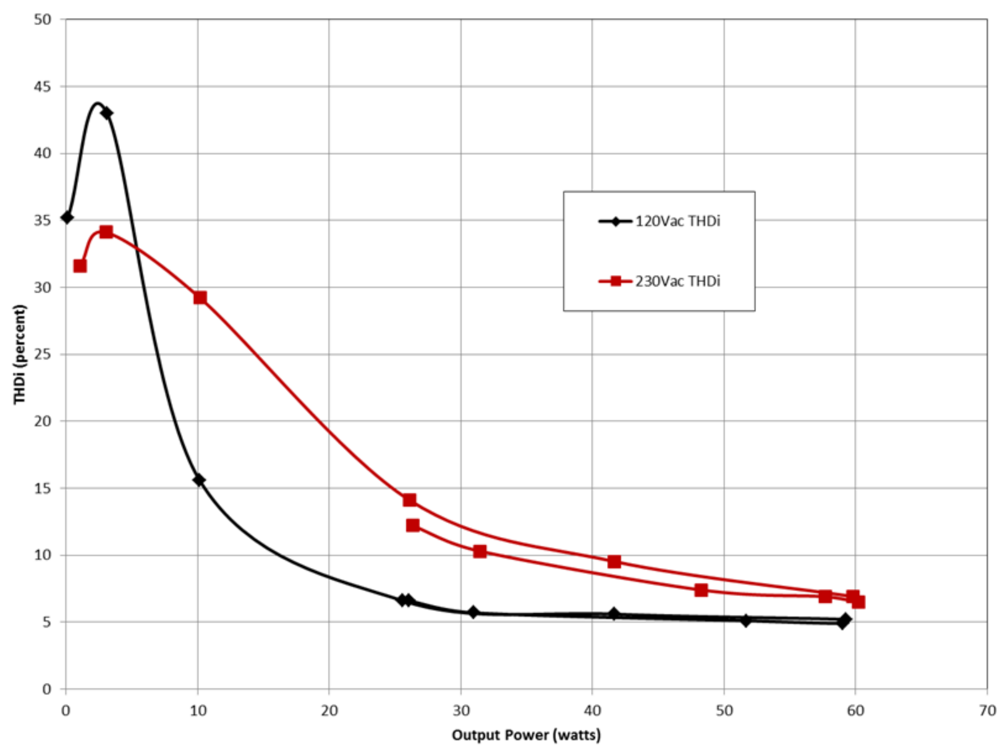


Figure 9. THD over Load

TEST DATA

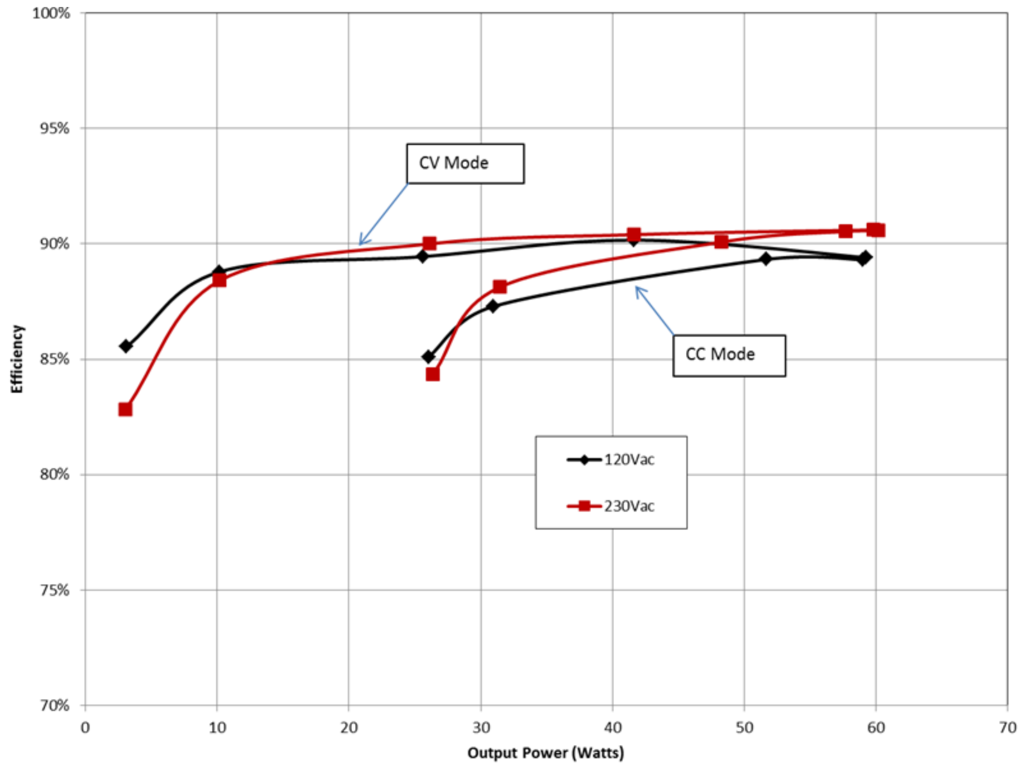


Figure 11. Efficiency

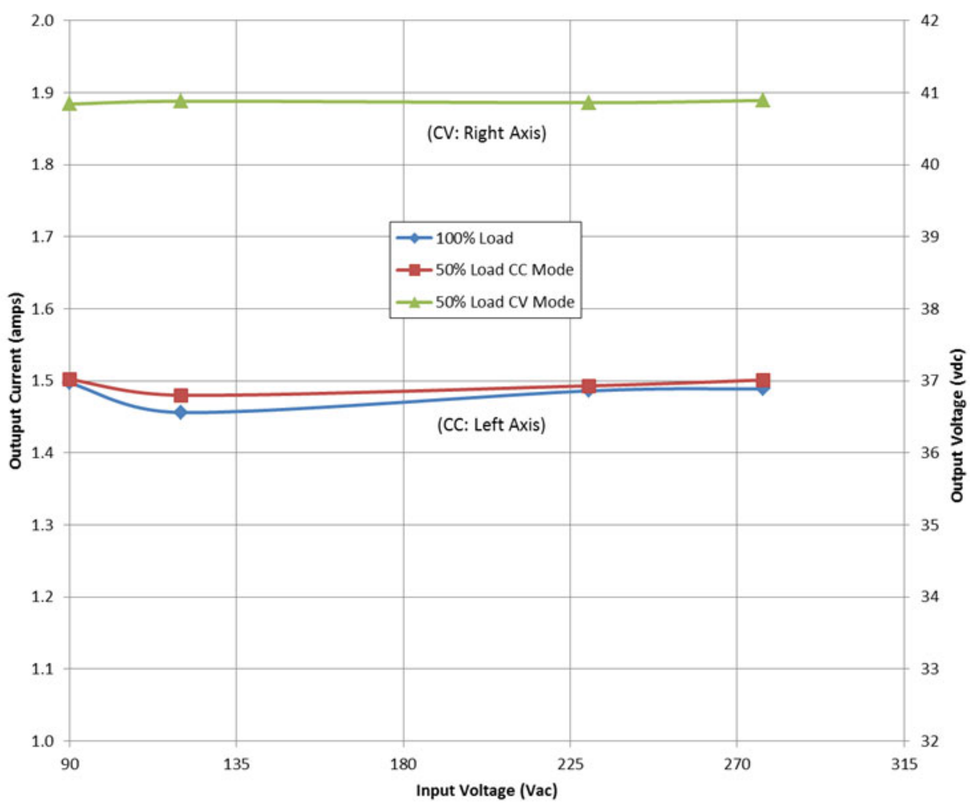


Figure 10. Regulation over Line

TEST DATA

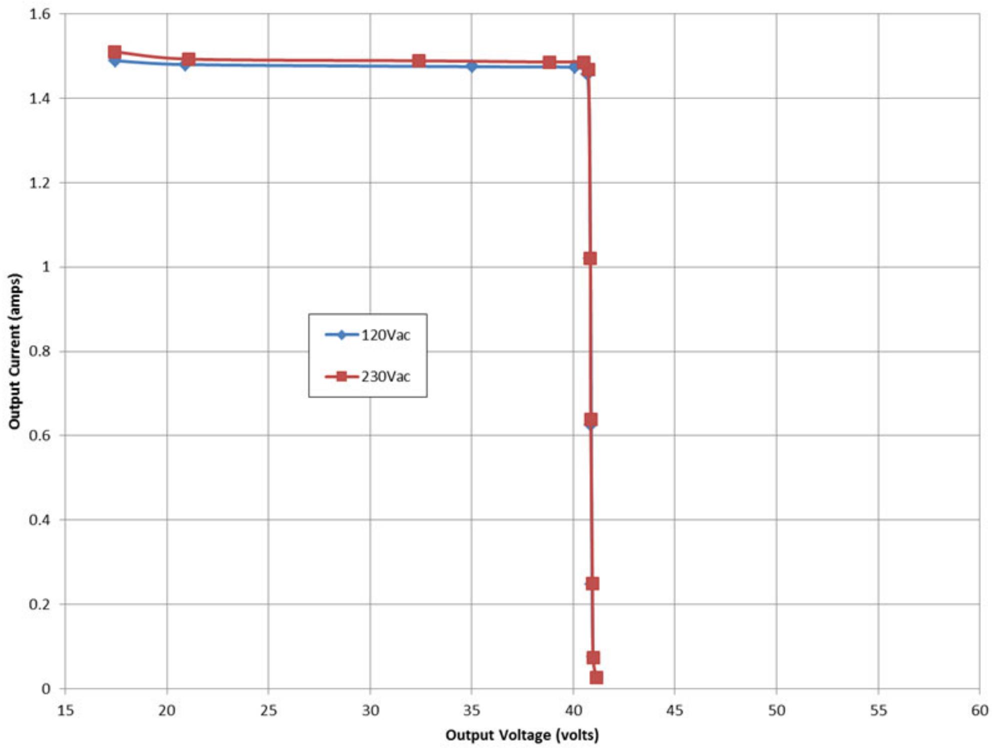


Figure 12. Output Regulation

TEST DATA

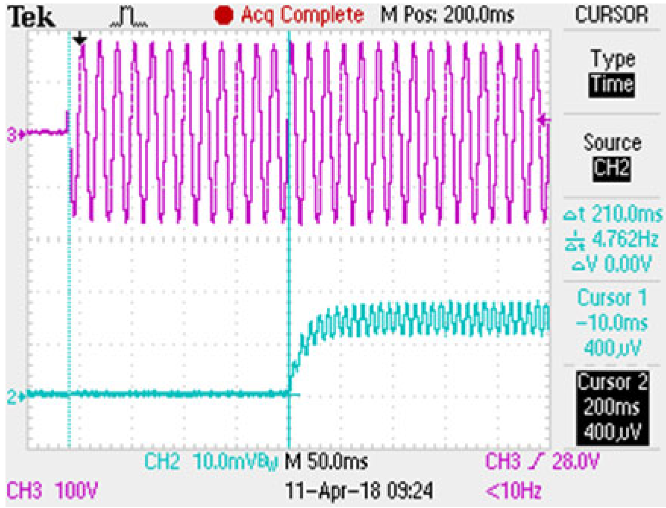


Figure 13. Start Up with AC Applied 120 V

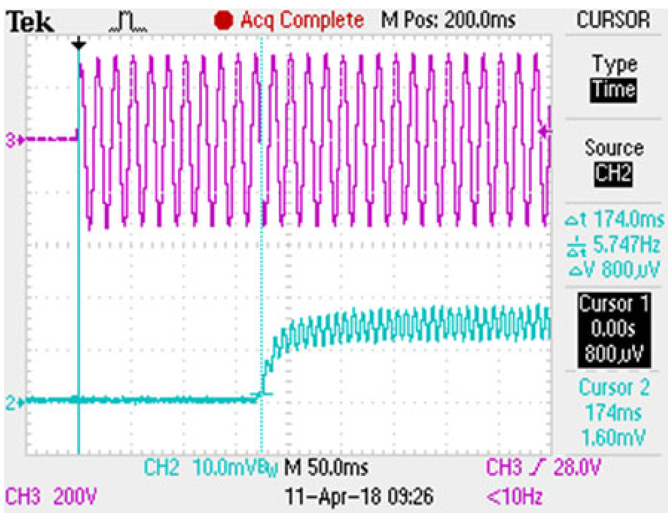


Figure 14. Start Up with AC Applied 230 V

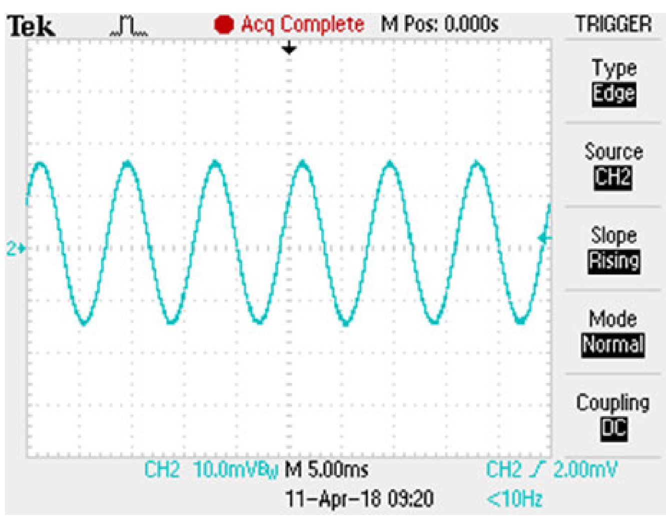


Figure 15. Output Ripple 42% P−P

TEST DATA

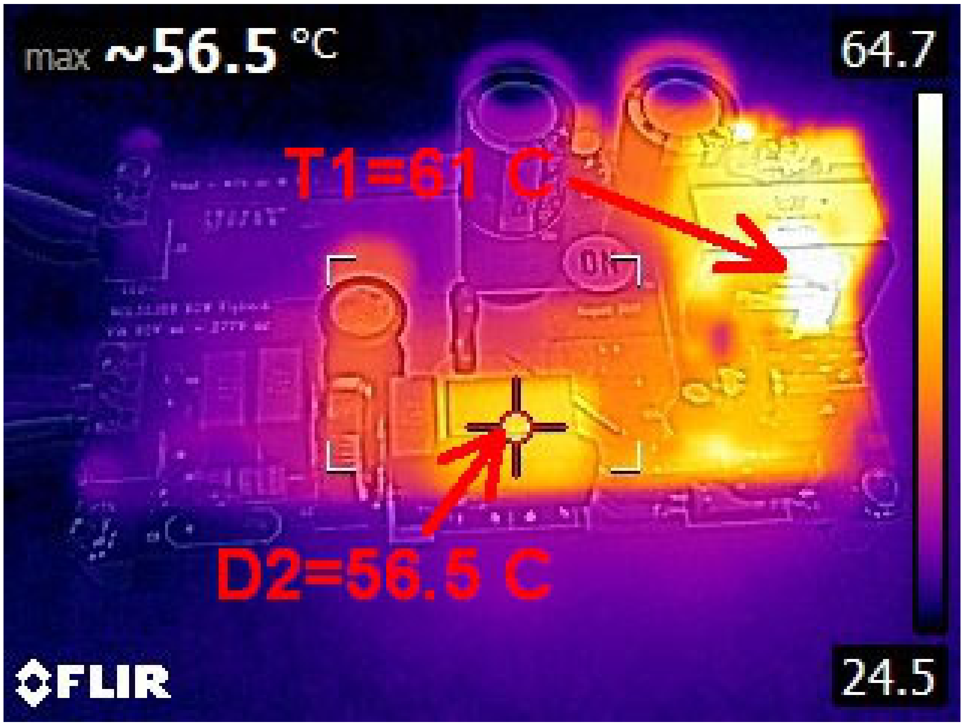


Figure 16. Thermal Image Side View

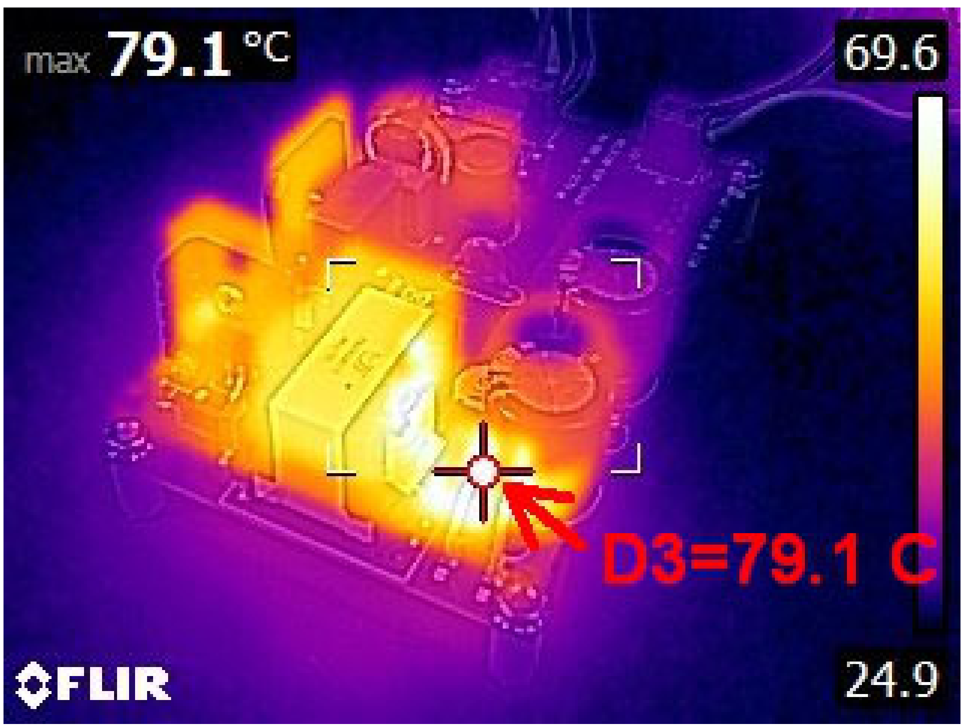


Figure 17. Thermal Image End View

Table 1. BILL OF MATERIALS

Quantity	Reference	Part	Manufacturer	Part Number
1	C17	22 nF	Wurth	885012207094
1	C18	220 nF	Wurth	885012207100
3	C6,C7,C8	150 nF	Wurth	890334023025
2	C9,C13	2.2 nF	Murata	DE1E3KX222MA4BP01F
1	C10	470 nF	Wurth	890334025039
2	C11,C12	1000 μF 50 V	Wurth	860160680034
1	C14	10 μF 35 V	Nichicon	USV1V100MFD
1	C15	4.7 nF 630 V	Kemet	B32529C8472J000
1	D2	GBU4J	On Semiconductor	GBU4J
2	D3,D5	MUR440RLG	On Semiconductor	MUR440RLG
1	D4	ES1JFL	On Semiconductor	ES1JFL
1	D6	MURS160T3G	On Semiconductor	MURS160T3G
1	F1	1A6 Slo	Belfuse	UMTS 1.6
1	J1	CON3	Wurth	691101710003
1	J6	CON2	Wurth	691101710002
1	L1	820 μH	Abracon	AIUR−06−821K
1	L2	5 mH	Murata	51505C
1	L3	10 μH	Wurth	744779100
1	QFET1	FCPF380N65FL1	ON Semiconductor	FCPF380N65FL1
1	Heatsink		Aavid Thermalloy	507302B00000G
1	R19	100 kΩ	Yaego	RC0805FR−07100KL
1	R8	320 V	Littelfuse	V320LA10P
1	R9	47 kΩ 2 W	Yageo	RSF200JB−73−47K
1	R10	56 kΩ	Yaego	RC0805FR−0756KL
1	R11	82 kΩ	Yaego	RC0805FR−0782KL
1	R12	7.5 kΩ	Yaego	RC0805FR−077K5L
1	R13	620 Ω	Yaego	RC0805FR−07620RL
1	R14	0.36 Ω 1 W	Panasonic	ERJ−1TRQFR36U
1	R15	0.39 Ω 1 W	Yageo	RL2512FK−070R39L
1	R17	47 Ω 2 W	Yageo	RSF200JB−73−47R
1	R18	10 Ω	Yaego	RC0805FR−0710RL
1	T1	750342613	Wurth	750342613
1	U2	NCL30388	On Semiconductor	NCL30388A1

NOTES: All Components to comply with RoH 2002/95/EC