# NCN9252MUGEVB

# High-Speed USB 2.0 (480 Mbps) DP3T Switch for USB/UART/Data Multiplexing Evaluation Board User's Manual

**ON Semiconductor®**

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## EVAL BOARD USER'S MANUAL

## OVERVIEW

The NCN9252 is a DP3T switch for combined UART and USB 2.0 high−speed data applications. It allows portable systems to use a single external port to transmit and receive signals to and from three separate locations within the portable system. It is comprised of two switches, each with a single common I/O that alternates between three terminals. They are operated together to allow three data sources, such as a USB or UART transceiver, to pass differential data through a shared USB connector port.

The NCN9252 features low RON− 4 Ω (max) at 4.2 V $V_{CC}$, 5 Ω (typ) at a 3.3 V $V_{CC}$. It also features low CON,

< 30 pF (max) across the supply voltage range. This performance makes it ideal for both USB full−speed and high−speed applications that require both low RON and CON for effective signal transmission. The NCN9252 is capable of accepting control input signals down to 1.4 V, over a range of $V_{CC}$ supply voltages with minimal leakage current. The NCN9252 is offered in a Pb−Free, 12 pin, 1.7 x 2.0 x 0.5 mm, UQFN package.



**Figure 1. Board Photo**

# NCN9252MUGEVB
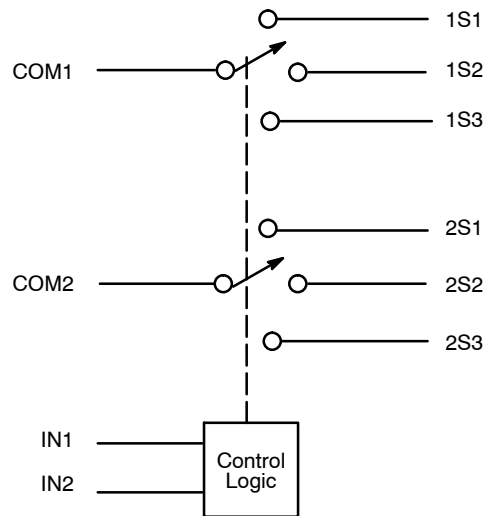


**Figure 2. Functional Block Diagram**

**Table 1. FUNCTION TABLE**

| IN1 [0] | IN2 [1] | COM1 Closed to: | COM2 Closed to: |
|---------|---------|-----------------|-----------------|
| 0 | 0 | No Connect | No Connect |
| 1 | 0 | 1S1 | 2S1 |
| 0 | 1 | 1S2 | 2S2 |
| 1 | 1 | 1S3 | 2S3 |

**Get Started...**

Equipment needed
- Power Supply
- 2 Banana Cables
- Computer
- USB Flash Drive
- USB Cable

Procedure

1. Set the power supply to 3.3 V. Connect the power supply from $V_{CC}$ to GND using the banana cables. The supply current should be less than 1 μA.
2. Connect the USB drive to the common I/O USB port, J1.
3. Connect the USB cable from the desired output port to the computer
4. Select the output port by moving the jumpers to the appropriate logic level for IN1 and IN2, as shown in the function table in Table 1.
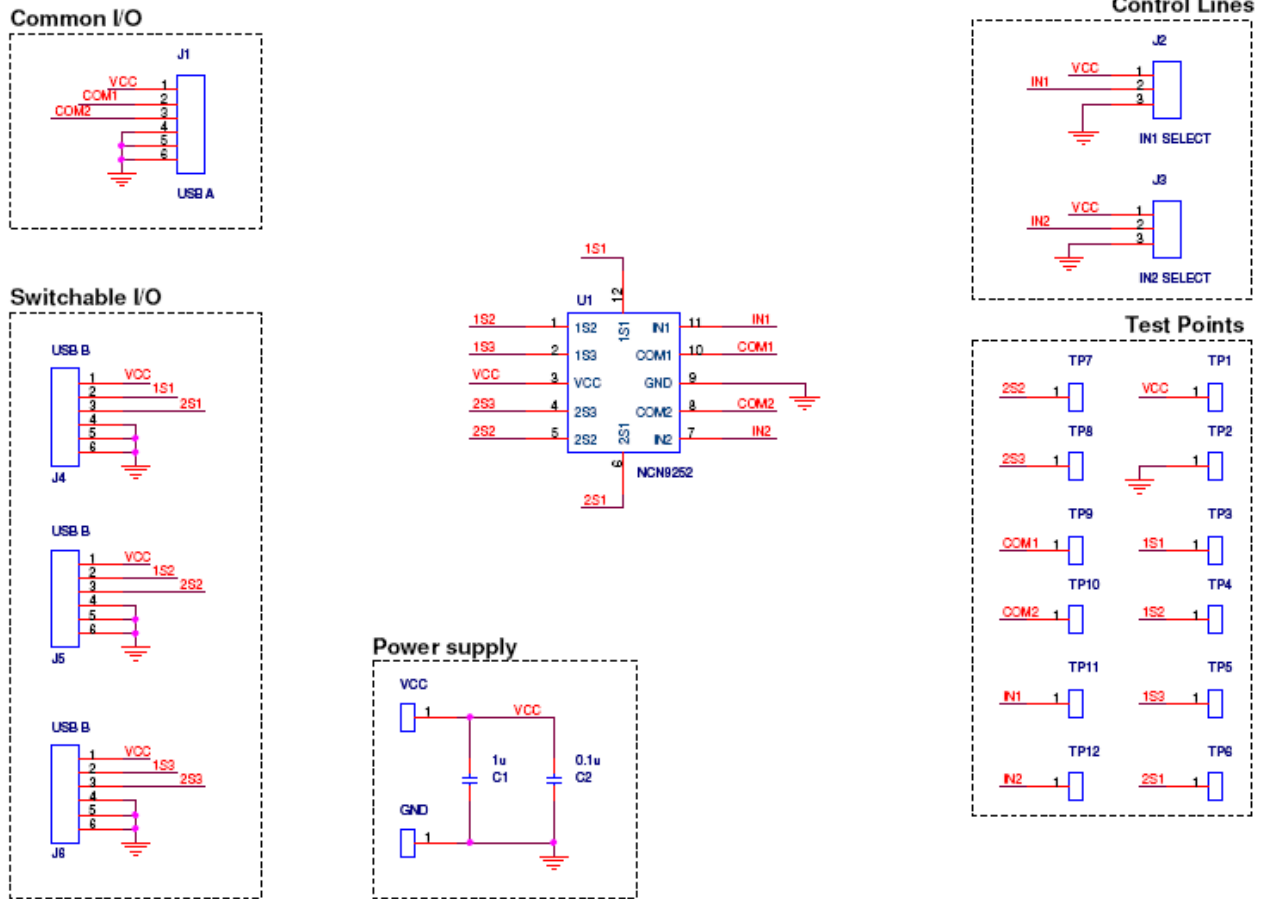
# NCN9252MUGEVB

## BOARD SCHEMATIC



**Figure 3. Board Schematic**

## Table 2. BILL OF MATERIALS

| Designator | Qty | Description | Value | Tolerance | Footprint | Manufacturer | Manufacturer Part Number | Substitution Allowed | Lead Free |
|---|---|---|---|---|---|---|---|---|---|
| C1 | 1 | Ceramic Capacitor SMD | 1μF | 10% | 805 | AVX Corporation | GRM155R60J105 | Yes | Yes |
| C2 | 1 | Ceramic Capacitor SMD | 0.1μF | 10% | 603 | AVX Corporation | 0603YC104KAT2A | Yes | Yes |
| J1 | 1 | USB TypeA connector surface mount | n/a | n/a | USB TypeA | Mill–Max | 896–43–004–00–000000 | Yes | Yes |
| J2, J3 | 2 | 3–pin header | n/a | n/a | Header3 | Tyco Electronics | 5–826629–0 | Yes | Yes |
| J2, J4 | 2 | 2–pin jumper | n/a | n/a | n/a | Tyco Electronics | 4–881545–2 | Yes | Yes |
| J4, J5, J6 | 3 | USB TypeB Connector through–hole | n/a | n/a | USB TypeB | Adam Tech | USB–B–S–RA | Yes | Yes |
| J7, J8 | 2 | Banana Connector | n/a | n/a | 7mm Hole | Johnson Components | 111–2223–001 | Yes | Yes |
| J9, J10, J11, J12 | 4 | Standoff nut | n/a | n/a | n/a | Keystone Electronics | 1903C | Yes | Yes |
| J9, J10, J11, J13 | 4 | Standoff screw | n/a | n/a | n/a | Keystone Electronics | 4814K–ND | Yes | Yes |
| TP1, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12 | 11 | Test Point PC Multi Purpose | n/a | n/a | 1mm hole | Keystone Electronics | 5000 | Yes | Yes |
| TP2 | 1 | PCB shorting link | n/a | n/a | GND_Strap | Harwin | D3082–46 | Yes | Yes |
| U1 | 1 | NCN9252 | n/a | n/a | UQFN12 | ON Semiconductor | NCN9252MUTAG | No | Yes |

## PCB LAYOUT GUIDELINES

### Electrical Layout Considerations

Implementing a high speed USB device requires paying attention on USB lines and traces to preserve signal integrity. The demonstration board serves as a layout example and can support the design engineers to preserve high speed performances.

Electrical layout guidelines are:

- The bypass capacitor must be placed as close as possible to the $V_{CC}$ input pin for noise immunity.
- The characteristic impedance of each High Speed USB segment must be 45 Ω.

- The ground plane of the PCB will be used to determine the characteristic impedance of each line.
- All corresponding D+ / D− line segment pairs must be the same length.
- The use of vias to route these signals should be avoided when possible.
- The use of turns or bends to route these signal should be avoided when possible.
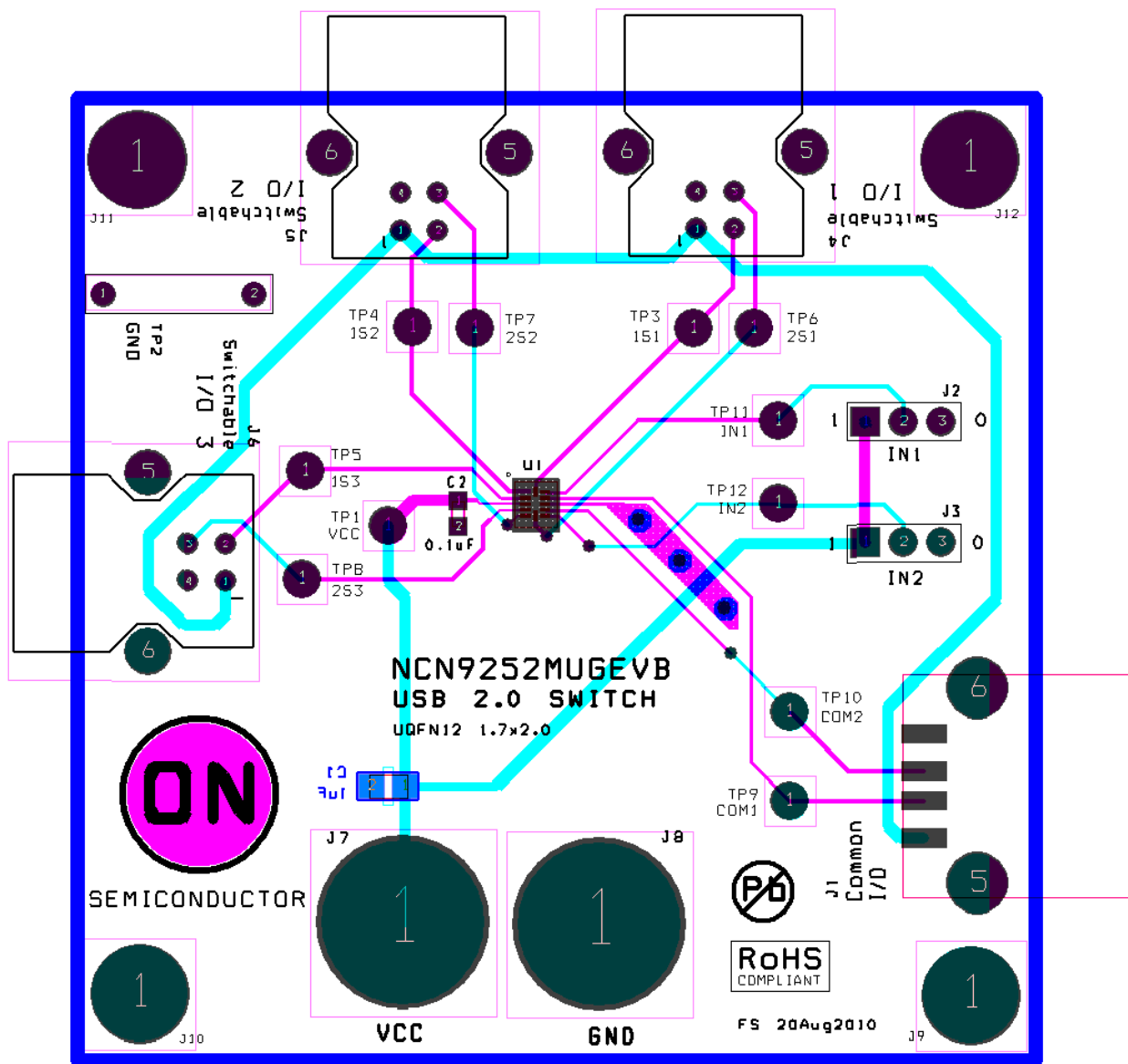
## EVALUATION BOARD PCB LAYOUT



**Figure 4. Evaluation Board Layout. Top Layer: Magenta. Bottom Layer: Cyan.**