NCP1075A/B, NCP1076A/B, NCP1077A/B, NCP1079A/B

Enhanced Off-line Switcher for Robust and Highly Efficient Power Supplies

ON Semiconductor®

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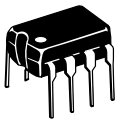
The NCP107xuz products integrate a fixed frequency current mode controller with a 700 V MOSFET. Available in a two different pin−out of the very common PDIP−7 package, the NCP107xuz offers a high level of integration, including soft−start, frequency−jittering, short−circuit protection, skip−cycle, a maximum peak current set−point, ramp compensation, and a dynamic self−supply (DSS, eliminating the need for an auxiliary winding).

Unlike other monolithic solutions, the NCP107xuz is quiet by nature: during nominal load operation, the part switches at one of the available frequencies (65, 100 or 130 kHz). When the output power demand diminishes, the IC automatically enters frequency foldback mode and provides excellent efficiency at light loads. When the power demand reduces further, it enters into a skip mode to reduce the standby consumption down to a no load condition.

Protection features include: a timer to detect an overload or a short−circuit event, Over−voltage Protection with auto−recovery. Ac input line voltage detection prevents lethal runaway in low input voltage conditions (Brown−out) as well as too high an input line (Ac line Over−voltage Protection). This also allows an Over−power Protection to compensate all internal delays in high input voltage conditions and optimize the maximum output current capability.

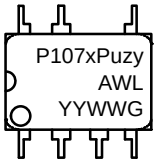
For improved standby performance, the connection of an auxiliary winding stops the DSS operation and helps to reduce input power consumption below 50 mW at high line.

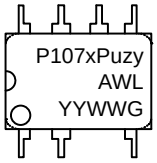


PDIP−7
(PDIP−8 LESS PIN 6)
CASE 626A

PDIP−7
(PDIP−8 LESS PIN 3)
CASE 626AS

MARKING DIAGRAMS





x	= Power Version (5, 6, 7, 9)
u	= Pin Connections (A, B)
z	= 2nd level OCP enabled/disabled (A, B)
y	= Oscillator Frequency 65, 100, 130 (A, B, C)
A	= Assembly Location
WL	= Wafer Lot
Y, YY	= Year
W, WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 31 of this data sheet.

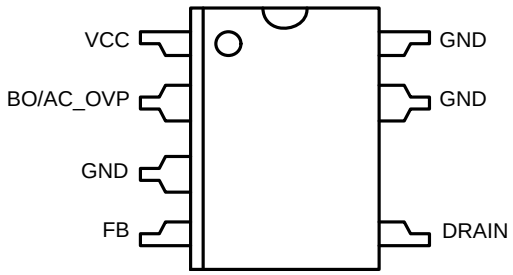
Features

- Built−in 700 V MOSFET with $R_{DS(ON)}$ of 13.5 Ω (NCP1075uz), 4.8 Ω (NCP1076uz/77uz) and 2.9 Ω (NCP1079uz)
- Large Creepage Distance Between High Voltage Pins
- Current−mode Fixed Frequency Operation – 65 / 100 / 130 kHz
- Various Options for Maximum Peak Current: see below table
- Fixed Slope Compensation
- Skip−cycle Operation at Low Peak Currents Only
- Dynamic Self−supply: No Need for an Auxiliary Winding
- Internal 10 ms Soft−start
- Auto−recovery Output Short−circuit Protection with Timer−based Detection
- Auto−recovery Over−voltage Protection with Auxiliary Winding Operation
- Adjustable Brown−out Protection and OVP
- 2nd Leading Edge Blanking – Current Protection (NCP107xuA version only)
- Over Power Protection
- Frequency Jittering for Better EMI Signature
- No Load Input Consumption < 50 mW
- Frequency Foldback to Improve Efficiency at Light Load
- These are Pb−free Devices

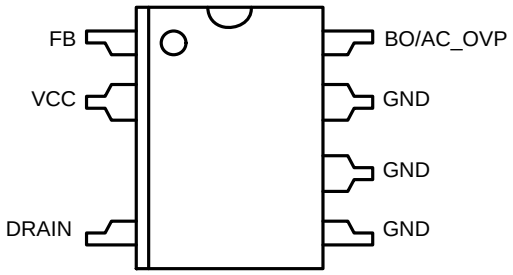
Typical Applications

- Auxiliary / Standby Isolated Power Supplies
- Major Home Appliances Power Supplies
- Power Meter SMPS
- Wide Input Industrial SMPS

PIN CONNECTIONS



(Top View)
PDIP−7
NCP107xA



(Top View)
PDIP−7
NCP107xB

PIN FUNCTION DESCRIPTION

Pin No		Pin Name	Function	Pin Description
PDIP 7 A	PDIP 7 B			
1	2	VCC	IC supply pin	This pin is connected to an external capacitor. The V_{CC} management includes an auto−recovery over−voltage protection.
2	8	BO/AC_OVP	Brown−out / Ac Line Over−voltage protection	Detects both input voltage conditions (Brown−out) and too high an input voltage (Ac line OVP). Do not leave this pin floating – if this pin is not used it should be directly connected do GND.
3	5	GND	The IC Ground	
4	1	FB	Feedback signal input	By connecting an opto−coupler to this pin, the peak current set−point is adjusted accordingly to the output power demand.
5	4	DRAIN	Drain connection	The internal drain MOSFET connection
6	3	NC		This un−connected pin ensures adequate creepage distance
7	6	GND	The IC Ground	
8	7	GND	The IC Ground	

PRODUCTS INFOS & INDICATIVE MAXIMUM OUTPUT POWER

Product	$R_{DS(ON)}$	I_{PK}	230 Vrms ±15%		85−265 Vrms	
			Adapter	Open Frame	Adapter	Open Frame
NCP1075uz	13.5 Ω	400 mA	8.5 W	14 W	6 W	10 W
NCP1076uz / NCP1077uz	4.8 Ω	800 mA	19 W	31 W	14 W	23 W
NCP1079uz	2.9 Ω	1050 mA	25 W	41 W	18 W	30 W

NOTE: Informative values only, with T_{amb} = 25°C, T_{case} = 100°C, PDIP−7 package, Self−supply via Auxiliary winding and circuit mounted on minimum copper area as recommended.

QUICK SELECTION TABLE

Device	Frequency [kHz]	$R_{DS(ON)}$ [Ω]	I_{PK} [mA]	Package type
NCP1075uz	65, 100, 130*	13.5	400	PDIP−7 (Pb−Free)
NCP1076uz	65, 100, 130*	4.8	650	
NCP1077uz	65, 100, 130*	4.8	800	
NCP1079uz	65, 100, 130*	2.9	1050	

*NOTE: 130 kHz option available in pin connection B only

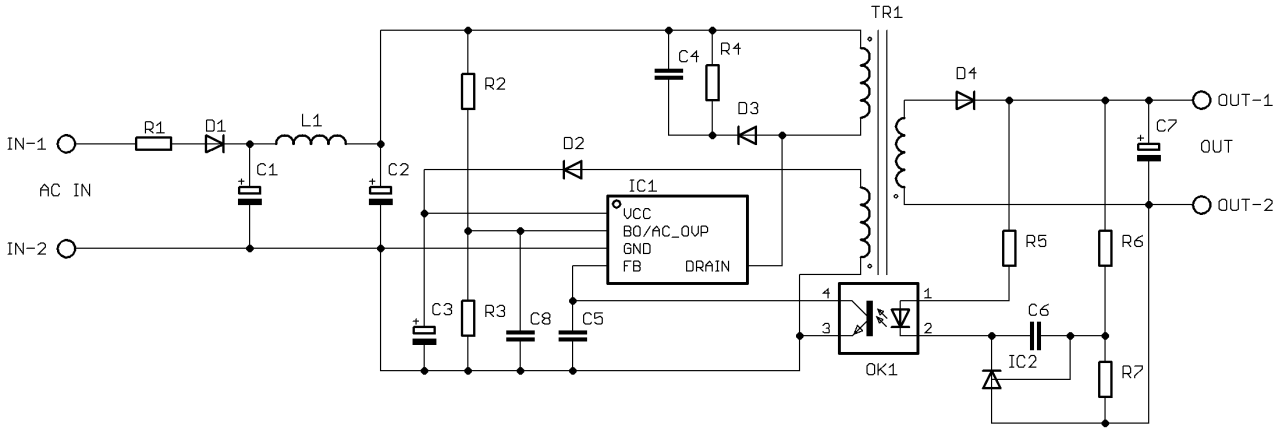


Figure 1. Typical Isolated Application (Flyback Converter), Enable Brown−out, Ac Line OVP and OPP Functions

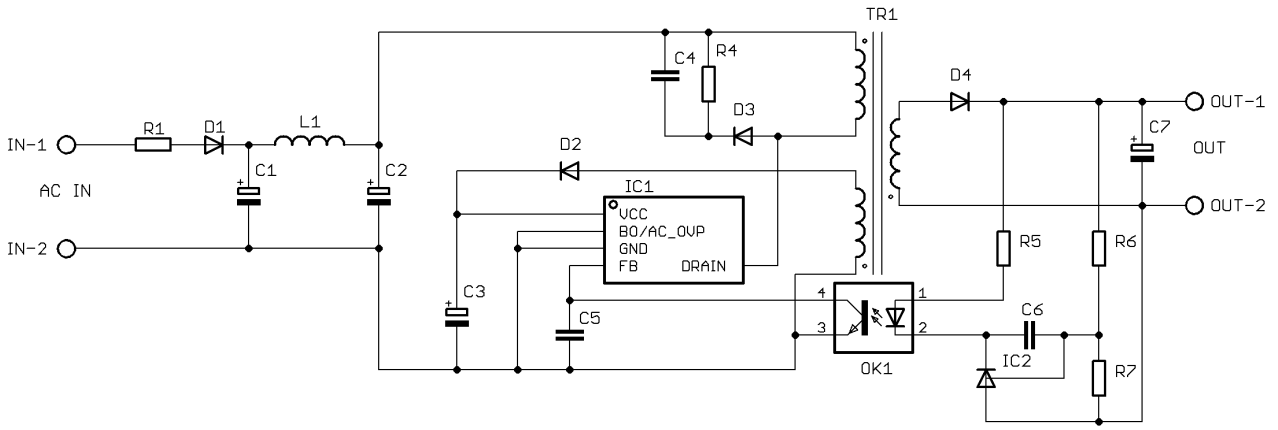


Figure 2. Typical Isolated Application (Flyback Converter), Disabled Brown−out Function – Against Line Detection

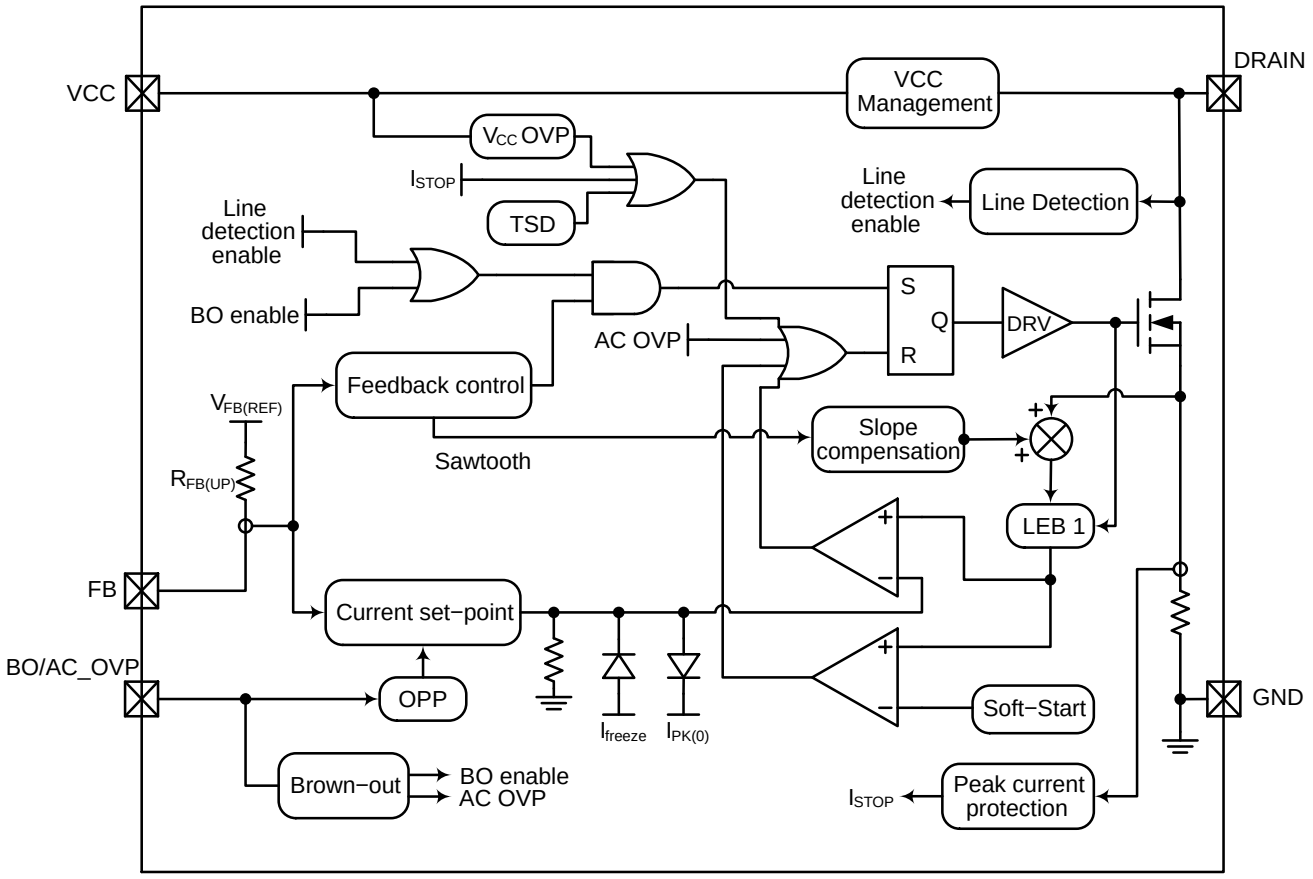


Figure 3. Simplified Internal Circuit Architecture

MAXIMUM RATINGS TABLE (All voltages related to GND terminal)

Rating		Symbol	Value	Unit
Power supply voltage, VCC pin, continuous voltage		V_{CC}	−0.3 to 20	V
Voltage on all pins, except DRAIN and VCC pin		Vinmax	−0.3 to 10	V
DRAIN voltage		BV_{DSS}	−0.3 to 700	V
Maximum Current into VCC pin		I_{CC}	15	mA
Drain Current Peak during Transformer Saturation (T_J = 150°C): NCP1075uz NCP1076uz/77uz NCP1079uz Drain Current Peak during Transformer Saturation (T_J = 25°C): NCP1075uz NCP1076uz/77uz NCP1079uz		$I_{DS(PK)}$	 0.9 2.2 3.6 1.5 3.9 6.4	A
Thermal Resistance Junction−to−Air – PDIP7	0.36 Sq. Inch	$R_{\theta J-A}$	77	°C/W
	1.0 Sq. Inch		68	
Maximum Junction Temperature		T_{JMAX}	150	°C
Storage Temperature Range			−60 to +150	°C
Human Body Model ESD Capability (All pins except HV pin) per JEDEC JESD22−A114F		HBM	2	kV
Human Body Model ESD Capability (Drain pin) per JEDEC JESD22−A114F		HBM	1	kV
Charged−Device Model ESD Capability per JEDEC JESD22−C101E		CDM	1	kV
Machine Model ESD Capability per JEDEC JESD22−A115−A		MM	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.
2. Maximum drain current $I_{DS(PK)}$ is obtained when the transformer saturates. It should not be mixed with short pulses that can be seen at turn on. Figure 4 below provides spike limits the device can tolerate.

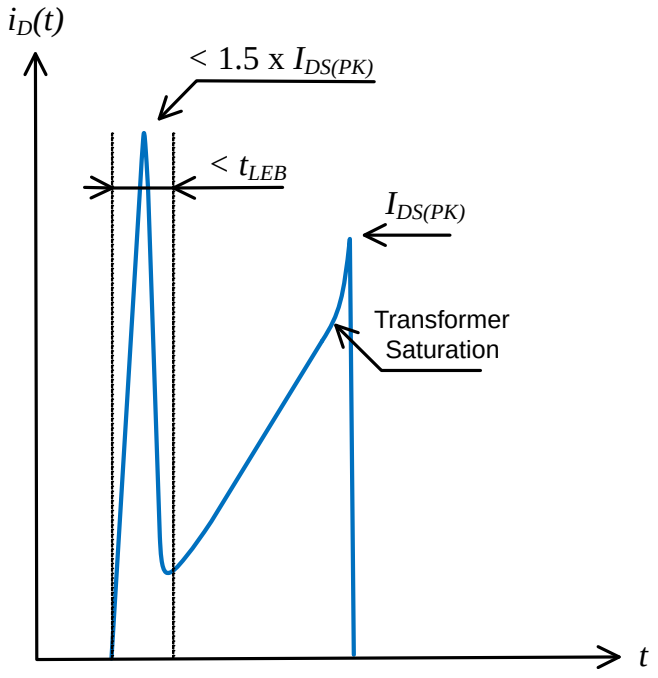


Figure 4. Spike Limits

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{CC} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
SUPPLY SECTION AND VCC MANAGEMENT						
$V_{CC(ON)}$	V_{CC} increasing level at which the switcher starts operation	1 (2)	8.0	8.4	8.9	V
$V_{CC(MIN)}$	V_{CC} decreasing level at which the HV current source restarts	1 (2)	6.5	6.9	7.3	V
$V_{CC(OFF)}$	V_{CC} decreasing level at which the switcher stops operation (UVLO)	1 (2)	6.1	6.5	6.9	V
$V_{CC(reset)}$	V_{CC} voltage at which the internal latch is reset (Guaranteed by design)	1 (2)		4		V
I_{CC1}	Internal IC consumption, MOSFET switching (f_{SW} = 65 kHz)	1 (2)				mA
	NCP1075uz		−	1.10	−	
	NCP1076uz/77uz		−	1.26	−	
	NCP1079uz		−	1.40	−	
$I_{CC(skip)}$	Internal IC consumption, V_{FB} is 0 V (No switching on MOSFET)	1 (2)	−	400	−	μA
POWER SWITCH CIRCUIT						
$R_{DS(ON)}$	Power Switch Circuit on−state resistance (I_{DRAIN} = 50 mA)	5 (4)				Ω
	NCP1075uz					
	T_J = 25°C		−	13.5	16.8	
	T_J = 125°C		−	26.0	31.6	
	NCP1076uz/77uz					
	T_J = 25°C		−	4.8	6.8	
	T_J = 125°C		−	9.3	11.6	
	NCP1079uz					
	T_J = 25°C		−	2.9	3.9	
	T_J = 125°C		−	5.3	7.5	
BV_{DSS}	Power Switch Circuit & Start−up breakdown voltage ($I_{DRAIN(OFF)}$ = 120 μA, T_J = 25°C)	5 (4)	700	−	−	V
$I_{DSS(OFF)}$	Power Switch & Start−up breakdown voltage off−state leakage current T_J = 125°C (V_{DS} = 700 V)	5 (4)	−	85	−	μA
	Switching characteristics (R_L = 50 Ω, V_{DS} set for I_{DRAIN} = 0.7 x I_{lim})	5 (4)				ns
t_R	Turn−on time (90% − 10%)		−	20	−	
t_F	Turn−off time (10% − 90%)		−	10	−	
INTERNAL START−UP CURRENT SOURCE						
I_{start1}	High−voltage current source, V_{CC} = $V_{CC(ON)}$ − 200 mV	5 (4)	4.0	9.0	12.0	mA
I_{start2}	High−voltage current source, V_{CC} = 0 V	5 (4)	−	0.5	−	mA
$V_{HV(MIN)}$	Minimum start−up voltage, V_{CC} = 0 V	5 (4)	−	21	−	V
$V_{CC(TH)}$	V_{CC} Transient level for I_{start1} to I_{start2} toggling point	1 (2)	−	1.6	−	V
CURRENT COMPARATOR						
I_{PK}	Maximum internal current set−point at 50% duty−cycle FB pin open, T_J = 25°C					mA
	NCP1075uz	−	−	400	−	
	NCP1076uz	−	−	650	−	
	NCP1077uz	−	−	800	−	
	NCP1079uz	−	−	1050	−	
$I_{PK(0)}$	Maximum internal current set−point at beginning of switching cycle FB pin open, BO/AC_OVP pin voltage ≤ 0.8 V, T_J = 25°C					mA
	NCP1075uz	−	420	470	520	
	NCP1076uz	−	690	765	840	
	NCP1077uz	−	850	940	1030	
	NCP1079uz	−	1110	1230	1350	

3. The final switch current is: $I_{PK(0)}$ / (V_{in}/L_P + S_a) x V_{in}/L_P + V_{in}/L_P x t_{prop}, with S_a the built−in slope compensation, V_{in} the input voltage, L_P the primary inductor in a flyback, and t_{prop} the propagation delay.
4. Oscillator frequency is measured with disabled jittering.

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{CC} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
CURRENT COMPARATOR						
$I_{PKSW(65)}$	Final switch current with a primary slope of 200 mA/μs, f_{SW} = 65 kHz (Note 3)					mA
	NCP1075uz	−	−	450	−	
	NCP1076uz	−	−	710	−	
	NCP1077uz	−	−	860	−	
	NCP1079uz	−	−	1100	−	
$I_{PKSW(100)}$	Final switch current with a primary slope of 200 mA/μs, f_{SW} =100 kHz (Note 3)					mA
	NCP1075uz	−	−	440	−	
	NCP1076uz	−	−	685	−	
	NCP1077uz	−	−	825	−	
	NCP1079uz	−	−	1040	−	
$I_{PKSW(130)}$	Final switch current with a primary slope of 200 mA/μs, f_{SW} =130 kHz (Note 3)					mA
	NCP1075uz	−	−	450	−	
	NCP1076uz	−	−	685	−	
	NCP1077uz	−	−	820	−	
	NCP1079uz	−	−	1020	−	
$I_{PK(OPP)}$	Maximum internal current set−point at beginning of switching cycle FB pin open, BO/AC_OVP pin voltage = 2.65 V, T_J = 25°C					mA
	NCP1075uz	−	−	375	−	
	NCP1076uz	−	−	610	−	
	NCP1077uz	−	−	750	−	
	NCP1079uz	−	−	985	−	
t_{SS}	Soft−start duration (Guaranteed by design)	−	−	10	−	ms
t_{prop}	Propagation delay from current detection to drain OFF state	−	−	100	−	ns
t_{LEB1}	Leading Edge Blanking Duration 1	−	−	300	−	ns
t_{LEB2}	Leading Edge Blanking Duration 2 (NCP107xuA version only)	−	−	100	−	ns
INTERNAL OSCILLATOR						
$f_{OSC(65)}$	Oscillation frequency, 65 kHz version, T_J = 25°C (Note 4)	−	59	65	71	kHz
$f_{OSC(100)}$	Oscillation frequency, 100 kHz version, T_J = 25°C (Note 4)	−	90	100	110	kHz
$f_{OSC(130)}$	Oscillation frequency, 130 kHz version, T_J = 25°C (Note 4)	−	117	130	143	kHz
f_{jitter}	Frequency jittering in percentage of f_{OSC}	−	−	±6	−	%
f_{swing}	Jittering modulation frequency	−	−	300	−	Hz
D_{MAX}	Maximum duty−cycle	−	64	68	72	%
FEEDBACK SECTION						
$I_{FB(fault)}$	FB current for which Fault is detected	4 (1)	−	−35	−	μA
$I_{FB100\%}$	FB current for which internal current set−point is 100% ($I_{PK(0)}$)	4 (1)	−	−44	−	μA
$I_{FB(freeze)}$	FB current for which internal current set-point is I_{freeze}	4 (1)	−	−90	−	μA
$V_{FB(REF)}$	Equivalent pull−up voltage in linear regulation range (Guaranteed by design)	4 (1)	−	3.3	−	V
$R_{FB(UP)}$	Equivalent feedback resistor in linear regulation range (Guaranteed by design)	4 (1)	−	19.5	−	kΩ
FREQUENCY FOLDBACK & SKIP						
I_{FBfold}	Start of frequency foldback FB pin current level	4 (1)	−	−68	−	μA
$I_{FBfold(END)}$	End of frequency foldback FB pin current level, $f_{SW} = f_{MIN}$	4 (1)	−	−100	−	μA

3. The final switch current is: $I_{PK(0)} / (V_{in}/L_P + S_a) \times V_{in}/L_P + V_{in}/L_P \times t_{prop}$, with S_a the built−in slope compensation, V_{in} the input voltage, L_P the primary inductor in a flyback, and t_{prop} the propagation delay.
4. Oscillator frequency is measured with disabled jittering.

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{CC} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
FREQUENCY FOLDBACK & SKIP						
f_{MIN}	The frequency below which skip−cycle occurs, T_J = 25°C (Note 4)	−	23	27	31	kHz
$I_{FB(skip)}$	The FB pin current level to enter skip mode	4 (1)	−	−120	−	μA
I_{freeze}	Internal minimum current set−point ($I_{FB} = I_{FB(freeze)}$)					mA
	NCP1075uz	−	−	165	−	
	NCP1076uz	−	−	270	−	
	NCP1077uz	−	−	330	−	
	NCP1079uz	−	−	430	−	
SLOPE COMPENSATION						
$S_{a(65)}$	The internal slope compensation @ 65 kHz:					mA/μs
	NCP1075uz	−	−	9	−	
	NCP1076uz	−	−	15	−	
	NCP1077uz	−	−	18	−	
	NCP1079uz	−	−	23	−	
$S_{a(100)}$	The internal slope compensation @ 100 kHz:					mA/μs
	NCP1075uz	−	−	14	−	
	NCP1076uz	−	−	23	−	
	NCP1077uz	−	−	28	−	
	NCP1079uz	−	−	36	−	
$S_{a(130)}$	The internal slope compensation @ 130 kHz:					mA/μs
	NCP1075uz	−	−	18	−	
	NCP1076uz	−	−	30	−	
	NCP1077uz	−	−	36	−	
	NCP1079uz	−	−	46	−	
PROTECTIONS						
t_{SCP}	Fault validation further to error flag assertion	−	35	48	−	ms
$t_{recovery}$	OFF phase in fault mode	−	−	420	−	ms
V_{OVP}	V_{CC} voltage at which the switcher stops pulsing	1 (5)	17.0	18.0	18.8	V
t_{OVP}	The filter of V_{CC} OVP comparator	−	−	80	−	μs
$V_{BO(EN)}$	Brown−out level detection	2 (8)	−	50	−	mV
$V_{BO(ON)}$	Brown−out level, the switcher starts pulsing, OPP starts to decrease I_{PK}	2 (8)	0.76	0.80	0.84	V
$V_{BO(HYST)}$	Brown−out hysteresis (Guaranteed by design)	2 (8)	−	100	−	mV
$V_{ACOVP(ON)}$	OVP level when the switcher stops pulsing	2 (8)	2.755	2.900	3.045	V
$V_{ACOVP(OFF)}$	OVP level when the switcher starts pulsing	2 (8)	2.3	2.6	2.9	V
$t_{BOfilter}$	V_{BO} filter	−	−	20	−	μs
t_{BO}	Brown−out timer	−	−	50	−	ms
$V_{HV(EN)}$	The drain pin voltage above which the MOSFET operates. Checked after one of the following events: TSD, UVLO, SCP, or V_{CC} OVP mode, BO/AC_OVP pin = 0 V	5 (4)	72	91	110	V
$I_{PK(150)}$	High current protection, percent of max limit I_{PK} (NCP107xuA version only)	−	−	150	−	%
TEMPERATURE MANAGEMENT						
TSD	Temperature shutdown (Guaranteed by design)	−	150	−	−	°C
TSD_{HYST}	Hysteresis in shutdown (Guaranteed by design)	−	−	20	−	°C

3. The final switch current is: $I_{PK(0)}$ / ($V_{in}/L_P + S_a$) x V_{in}/L_P + V_{in}/L_P x t_{prop}, with S_a the built−in slope compensation, V_{in} the input voltage, L_P the primary inductor in a flyback, and t_{prop} the propagation delay.
4. Oscillator frequency is measured with disabled jittering.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

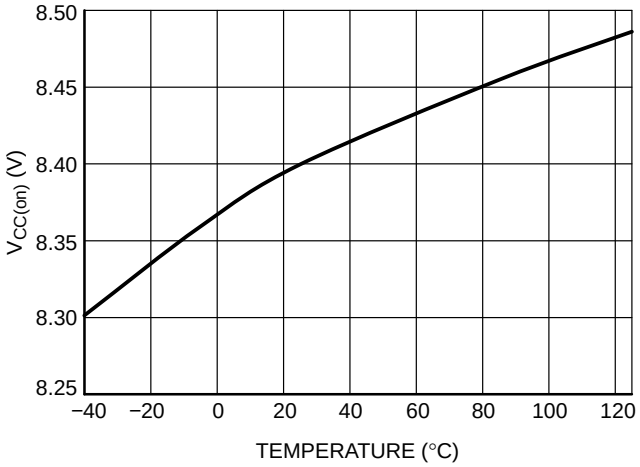


Figure 5. $V_{CC(on)}$ vs. Temperature

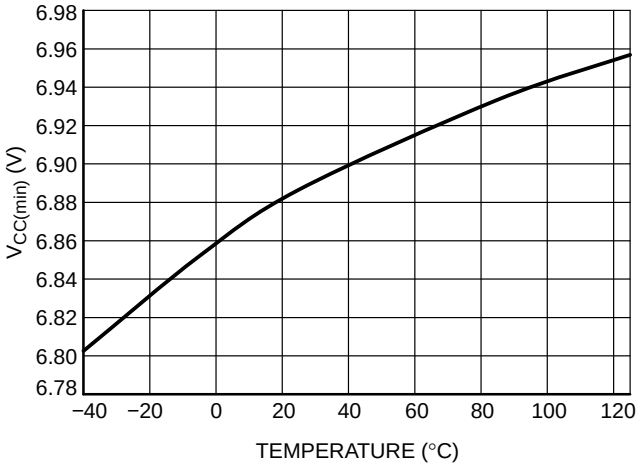


Figure 6. $V_{CC(min)}$ vs. Temperature

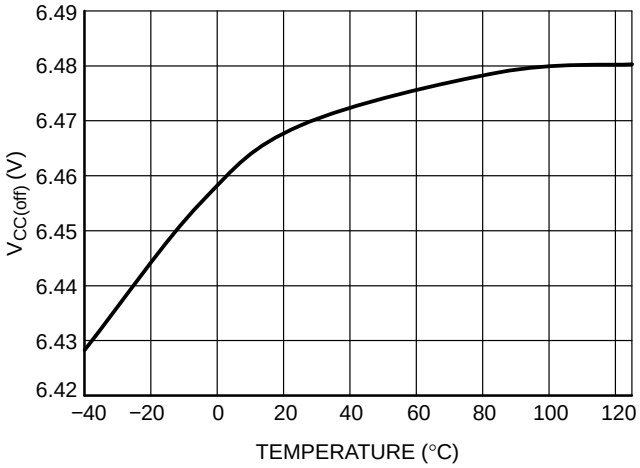


Figure 7. $V_{CC(off)}$ vs. Temperature

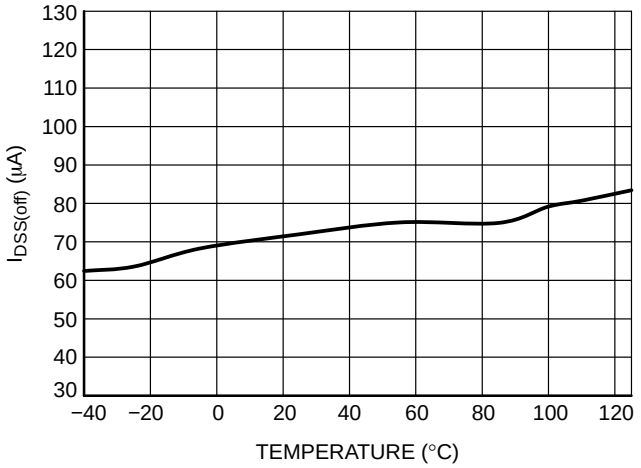


Figure 8. $I_{DSS(off)}$ vs. Temperature

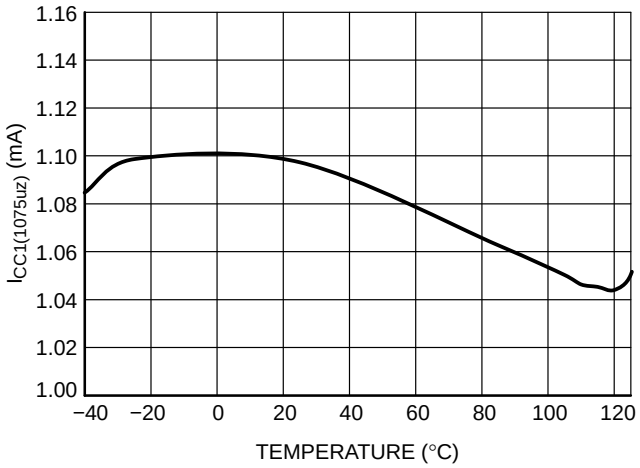


Figure 9. $I_{CC1(1075uz)}$ vs. Temperature

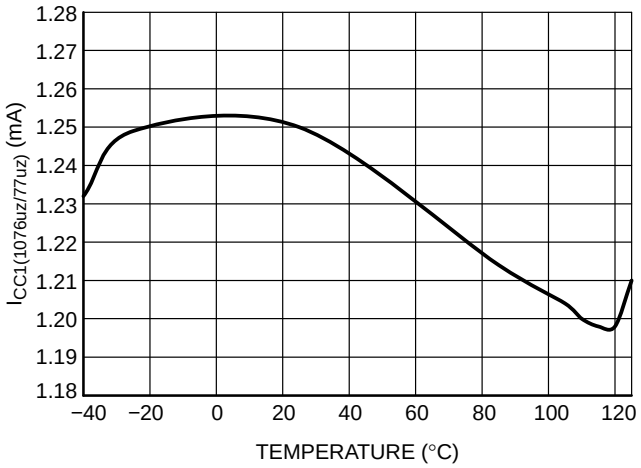


Figure 10. $I_{CC1(1076uz/77uz)}$ vs. Temperature

TYPICAL CHARACTERISTICS

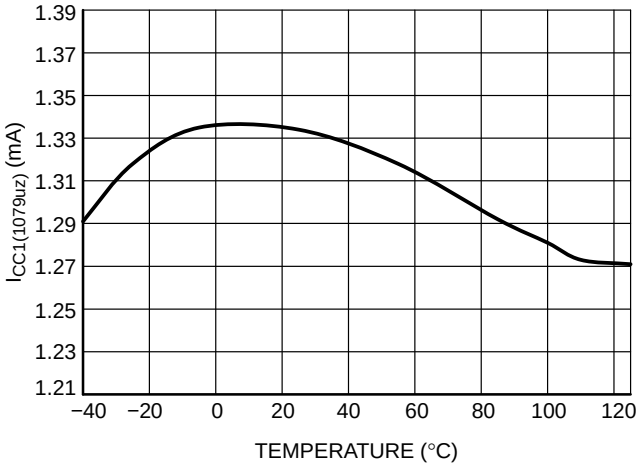


Figure 11. $I_{CC1(1079uz)}$ vs. Temperature

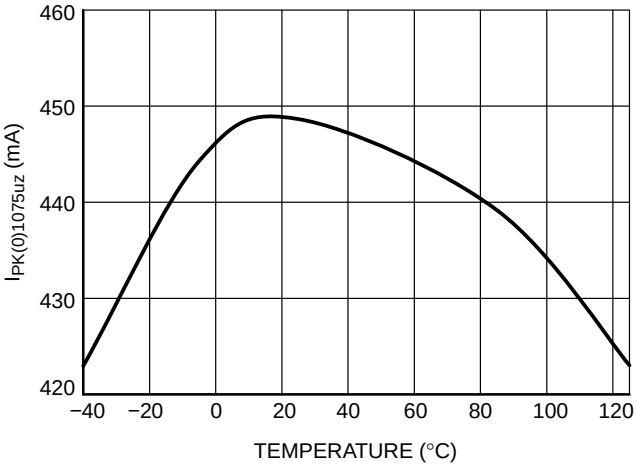


Figure 12. $I_{PK(0)1075uz}$ vs. Temperature

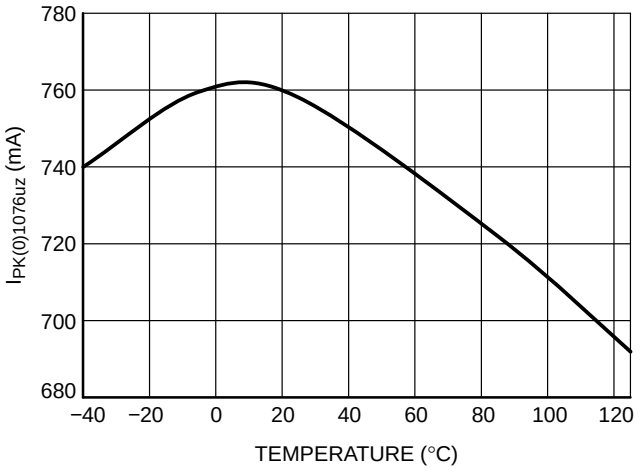


Figure 13. $I_{PK(0)1076uz}$ vs. Temperature

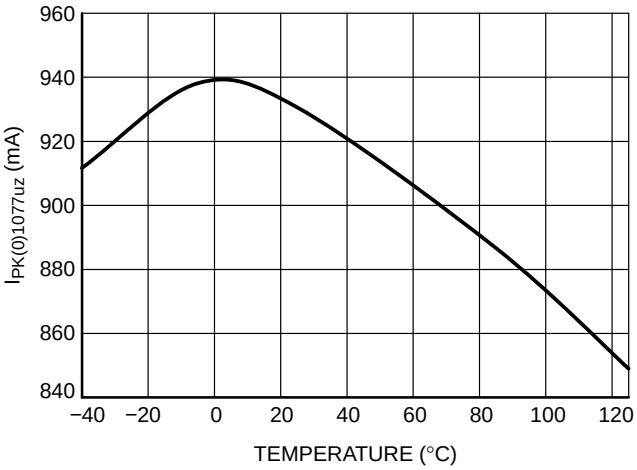


Figure 14. $I_{PK(0)1077uz}$ vs. Temperature

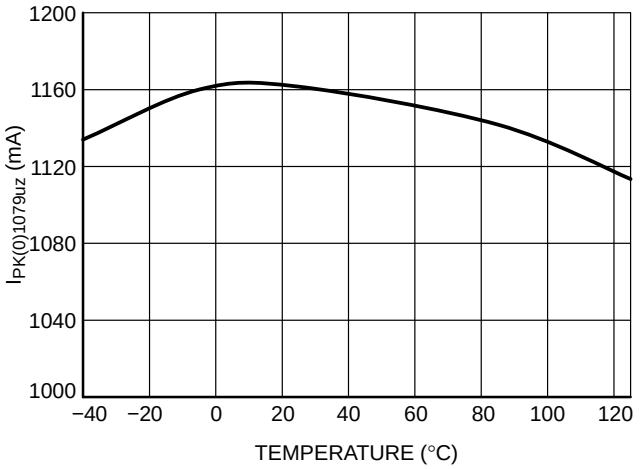


Figure 15. $I_{PK(0)1079uz}$ vs. Temperature

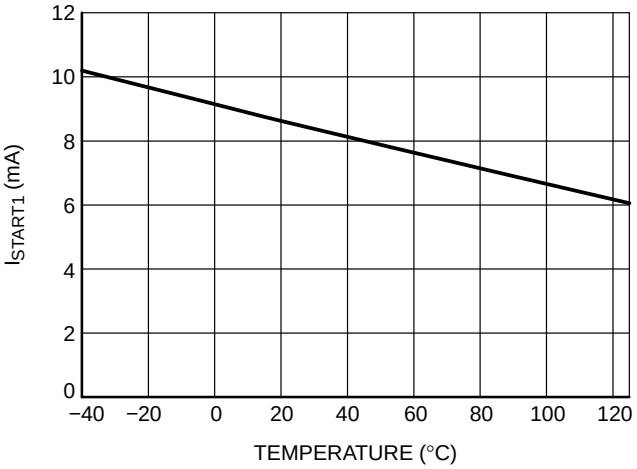


Figure 16. I_{START1} vs. Temperature

TYPICAL CHARACTERISTICS

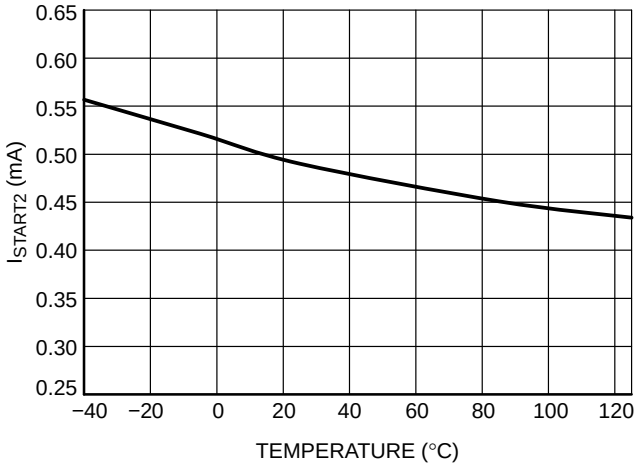


Figure 17. I_{START2} vs. Temperature

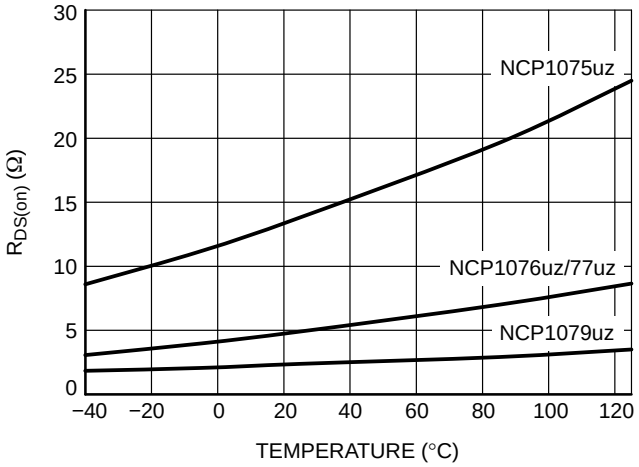


Figure 18. $R_{DS(on)}$ vs. Temperature

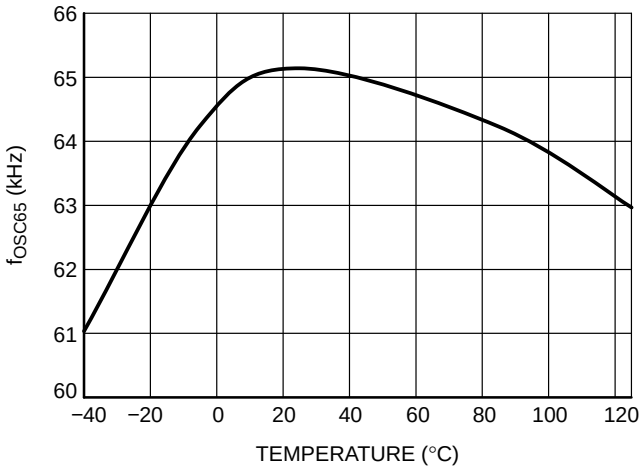


Figure 19. f_{OSC65} vs. Temperature

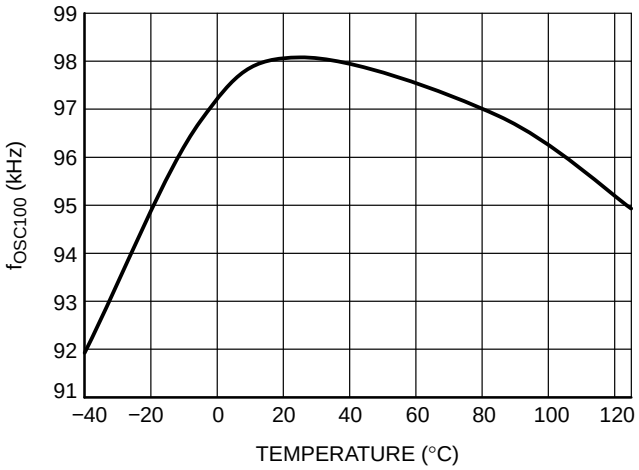


Figure 20. f_{OSC100} vs. Temperature

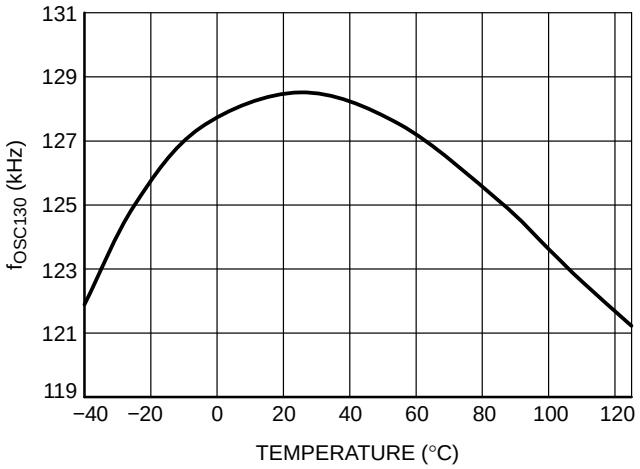


Figure 21. f_{OSC130} vs. Temperature

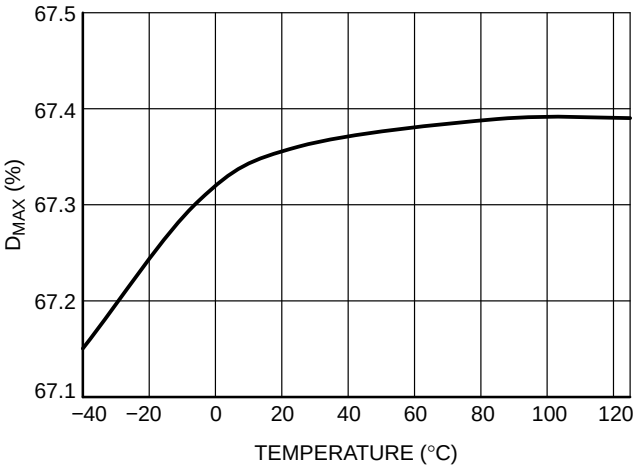


Figure 22. D_{MAX} vs. Temperature

TYPICAL CHARACTERISTICS

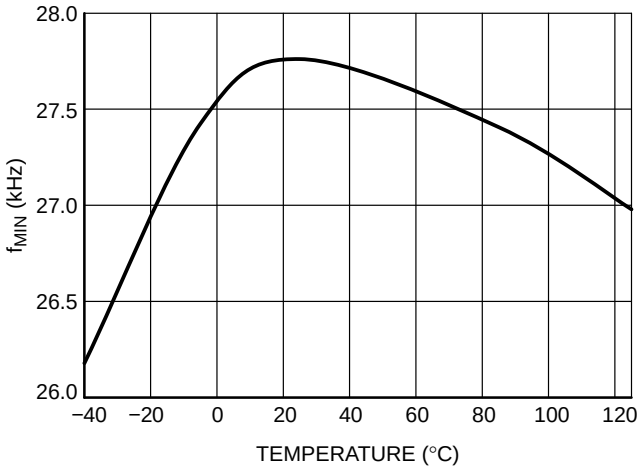


Figure 23. f_{MIN} vs. Temperature

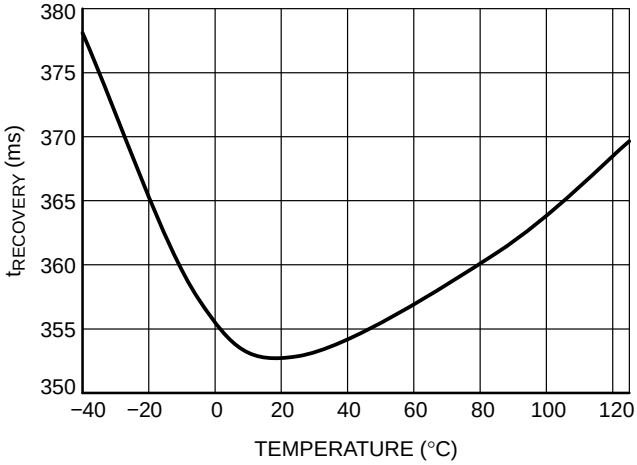


Figure 24. $t_{RECOVERY}$ vs. Temperature

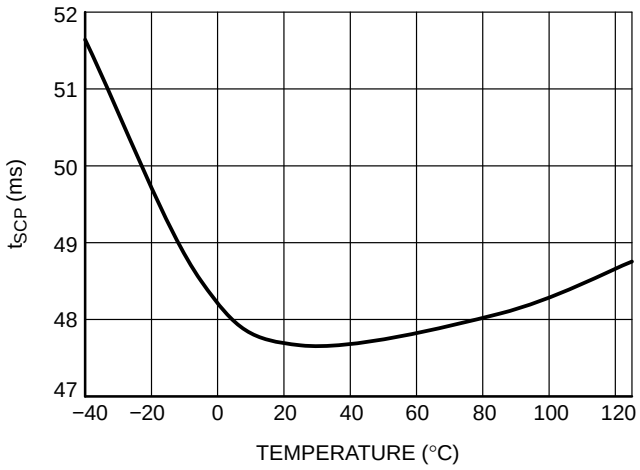


Figure 25. t_{SCP} vs. Temperature

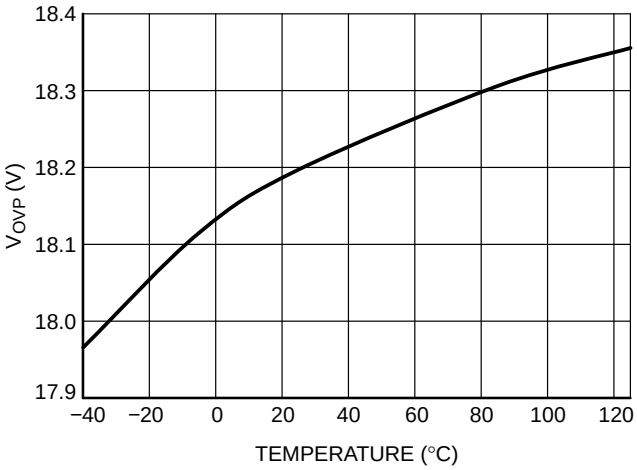


Figure 26. V_{OVP} vs. Temperature

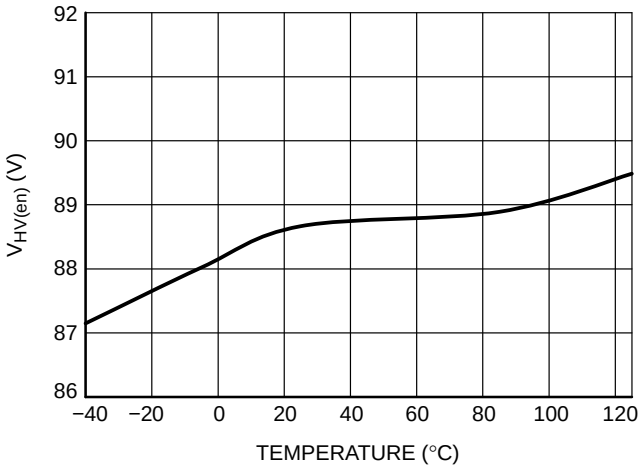


Figure 27. $V_{HV(en)}$ vs. Temperature

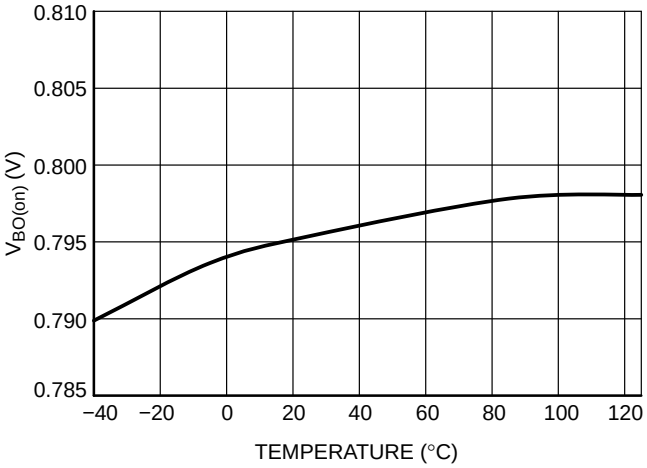


Figure 28. $V_{BO(on)}$ vs. Temperature

TYPICAL CHARACTERISTICS

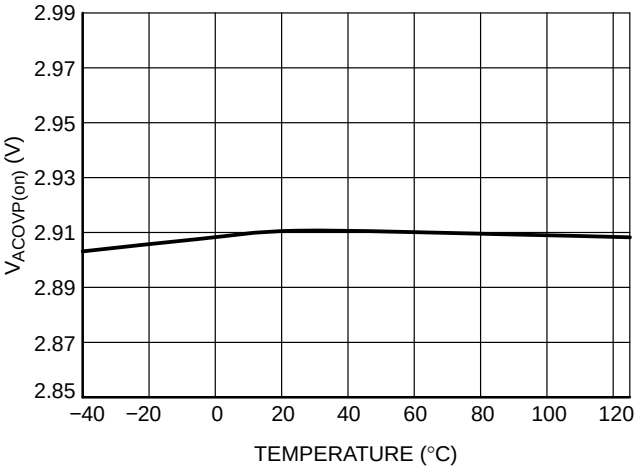


Figure 29. $V_{ACOVP(on)}$ vs. Temperature

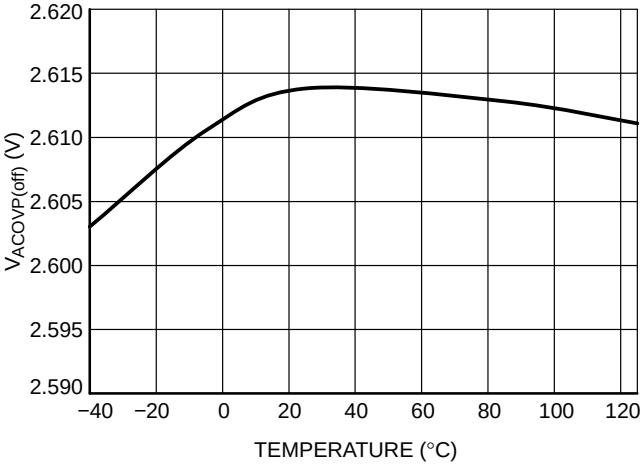


Figure 30. $V_{ACOVP(off)}$ vs. Temperature

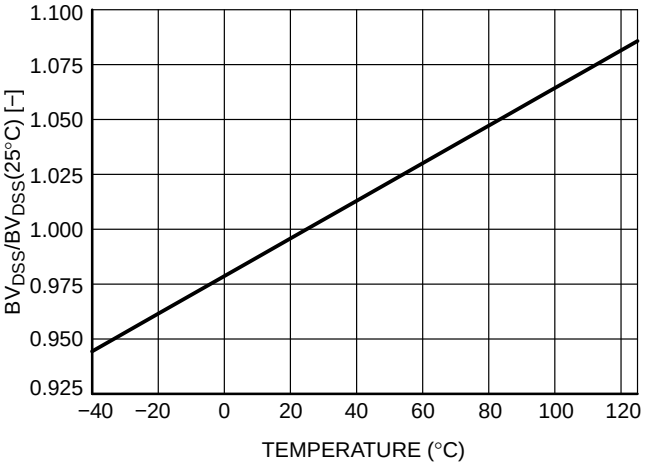


Figure 31. BV_{DSS}/BV_{DSS}(25°C) vs. Temperature

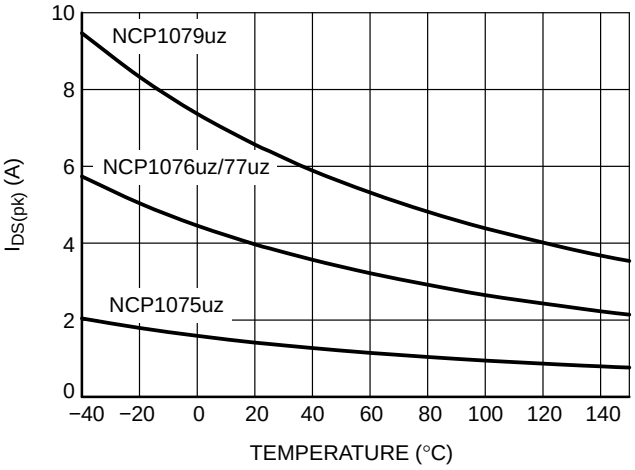


Figure 32. Drain Current Peak during Transformer Saturation vs. Junction Temperature

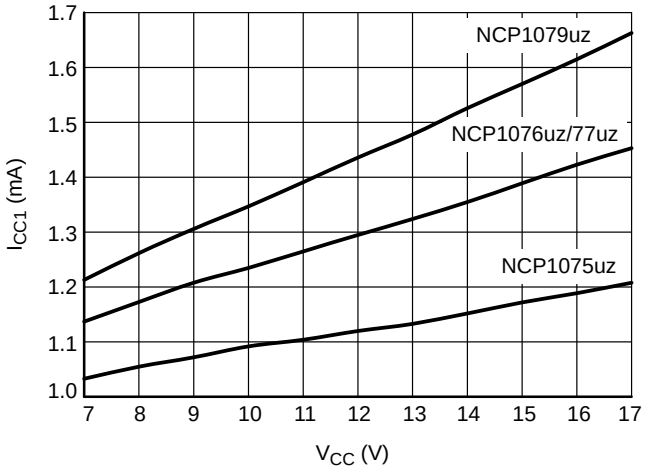


Figure 33. I_{CC1} vs. V_{CC}

APPLICATION INFORMATION

Introduction

Thanks to ON Semiconductor Very High Voltage Integrated Circuit technology, the circuit hosts a high−voltage power MOSFET featuring a 13.5/4.8/2.9 Ω $R_{DS(ON)}$ − T_J = 25°C. An internal current source delivers the start−up current, necessary to crank the power supply.

- **Current−mode operation:** The controller uses current−mode control architecture.
- **700 V Power MOSFET:** Thanks to ON Semiconductor Very High Voltage Integrated Circuit technology, the circuit hosts a high−voltage power MOSFET featuring a 4.8 and 2.9 Ω $R_{DS(ON)}$ − T_J = 25°C. This value lets the designer build a power supply up to 28 W operated on universal mains. An internal current source delivers the start−up current, necessary to crank the power supply.
- **Dynamic Self−Supply:** This device could be used in an application without an auxiliary winding to provide supply voltage via an internal high−voltage current source.
- **Short−circuit protection:** By permanently monitoring the feedback line activity, the IC is able to detect the presence of a short−circuit, immediately reducing the output power for a total system protection. A t_{SCP} timer is started as soon as the feedback current is below threshold, $I_{FB(fault)}$, which indicates a maximum peak current condition. If at the end of this timer the fault is still present, then the device enters a safe, auto−recovery burst mode, affected by a fixed timer recurrence, $t_{recovery}$. Once the short has disappeared, the controller resumes and goes back to normal operation.
- **Built−in VCC Over−Voltage Protection:** When the auxiliary winding is used to bias the VCC pin (no DSS), an internal comparator is connected to VCC pin. In case the voltage on the pin exceeds the V_{OVP} level (18 V typically), the controller immediately stops switching and awaits a full timer period ($t_{recovery}$) before attempting to re−start. If the fault is gone, the controller resumes operation. If the fault is still there, e.g. in the case of a broken opto−coupler, the controller protects the load through a safe burst mode.
- **Line detection:** An internal comparator monitors the drain voltage. If the drain voltage is lower than the internal threshold ($V_{HV(EN)}$), the internal power switch is inhibited. This avoids operating at too low an ac input. Line detection is active, when BO/AC_OVP pin is grounded.
- **Brown−out detection and AC line Over−Voltage Protection:** The BO/AC_OVP input monitors bulk voltage level via resistive divider and thus assures that the application is working only for designed bulk voltage. When BO/AC_OVP pin is connected to ground, Line detection is inhibited.
- **Internal OPP:** An internal function using the bulk voltage to program the maximum current reduction for a given input voltage. Internal OPP is active when BO/AC_OVP pin is connected via resistive divider to the bulk voltage.
- **2nd LEB (NCP107xuA only):** Second level of current protection. If peak current is 150% max peak current limit, then the controller stops switching after three pulses and waits for an auto−recovery period ($t_{recovery}$) before attempting to re−start.
- **Frequency jittering:** An internal low−frequency modulation signal varies the pace at which the oscillator frequency is modulated. This helps spreading out energy in conducted noise analysis. To improve the EMI signature at low power levels, the jittering remains active in frequency foldback mode.
- **Soft−Start:** A 10 ms soft−start ensures a smooth start−up sequence, reducing output overshoots.
- **Frequency foldback capability:** A continuous flow of pulses is not compatible with no−load/light−load standby power requirements. To excel in this domain, the controller observes the feedback current information and when it reaches a level of I_{FBfold}, the oscillator then starts to reduce its switching frequency as the feedback current continues to increase (the power demand continues to reduce). It can go down to 27 kHz (typical) reached for a feedback level of $I_{FBfold(END)}$ (100 μA roughly). At this point, if the power continues to drop, the controller enters classical skip−cycle mode.
- **Skip:** If SMPS naturally exhibits a good efficiency at nominal load, they begin to be less efficient when the output power demand diminishes. By skipping un−needed switching cycles, the NCP107xuz drastically reduces the power wasted during light load conditions.

Start−up Sequence

When the power supply is first powered from the mains outlet, the internal current source (typically 9.2 mA) is biased and charges up the V_{CC} capacitor from the drain pin. Once the voltage on this V_{CC} capacitor reaches the $V_{CC(ON)}$ level (typically 8.4 V), the current source turns off and pulses are delivered by the output stage: the circuit is awake and activates the power MOSFET if the bulk voltage is above $V_{HV(EN)}$ level (Brown−in protection) or voltage on BO/AC_OVP pin is above $V_{BO(ON)}$ level (Brown−out protection). Figure 34 details the simplified internal circuitry.

Being loaded by the circuit consumption, the voltage on the V_{CC} capacitor goes down. When V_{CC} is below $V_{CC(MIN)}$ level (7 V typically), it activates the internal current source to bring V_{CC} toward $V_{CC(ON)}$ level and stops again: a cycle takes place whose low frequency depends on the V_{CC} capacitor and the IC consumption. A 1.5 V ripple takes place on the VCC pin whose average value equals ($V_{CC(ON)}$ + $V_{CC(MIN)}$)/2. Figure 35 portrays a typical operation of the DSS.

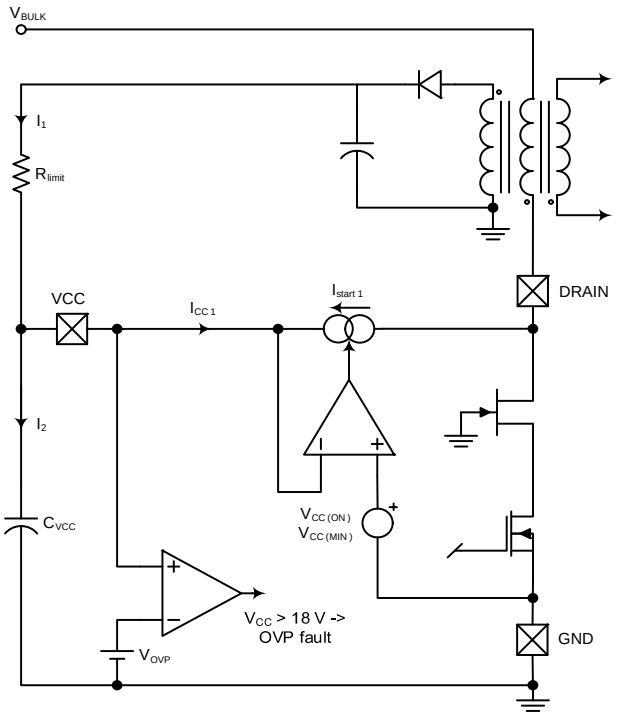


Figure 34. The Internal Arrangement of the Start−up Circuitry

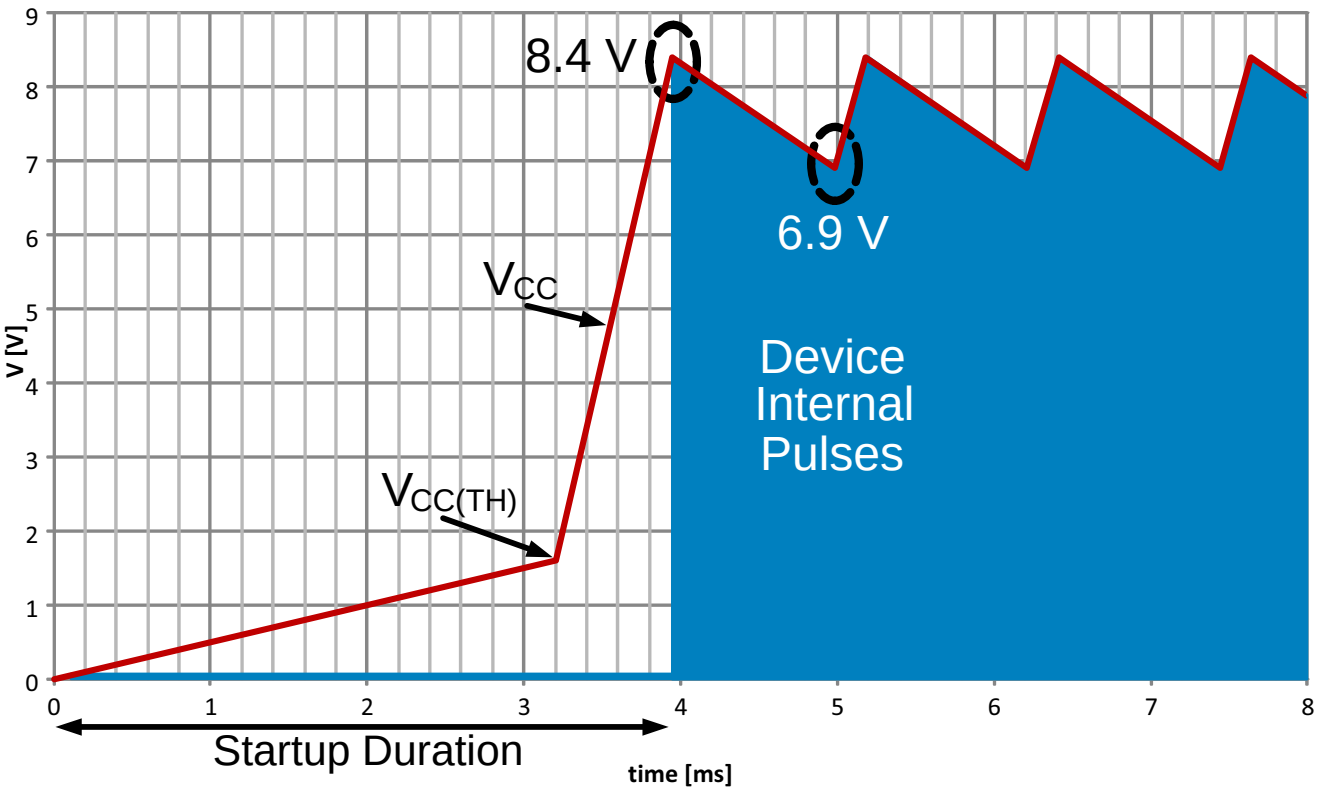


Figure 35. The Charge / Discharge Cycle Over a 1 μF V_{CC} Capacitor

As one can see, even if there is auxiliary winding to provide energy for V_{CC}, it happens that the device is still biased by DSS during start−up time or some fault mode when the voltage on auxiliary winding is not ready yet. The V_{CC} capacitor shall be dimensioned to avoid V_{CC} crosses $V_{CC(OFF)}$ level, which stops operation. The ΔV between $V_{CC(MIN)}$ and $V_{CC(OFF)}$ is 0.5 V. There is no current source to charge V_{CC} capacitor when driver is on, i.e. drain voltage is close to zero. Hence the V_{CC} capacitor can be calculated using

$$C_{VCC} \geq \frac{I_{CC1} \cdot D_{MAX}}{f_{OSC} \cdot \Delta V} \qquad \text{(eq. 1)}$$

Take the 65 kHz device as an example. C_{VCC} should be above

$$C_{VCC} = \frac{1.45 \cdot 10^{-3} \cdot 0.73}{59 \cdot 10^{3} \cdot 0.5} = 36\ \text{nF}$$

A margin that covers the temperature drift and the voltage drop due to switching inside FET should be considered, and thus a capacitor above 0.1 μF is appropriate.

The V_{CC} capacitor has only a supply role and its value does not impact other parameters such as fault duration or the frequency sweep period for instance. As one can see on Figure 34, an internal OVP comparator protects the switcher against lethal V_{CC} runaways. This situation can occur if the feedback loop opto−coupler fails, for instance, and you would like to protect the converter against an over−voltage event. In that case, the over−voltage protection (OVP) circuit immediately stops the output pulses for $t_{recovery}$ duration (420 ms typically). Then a new start−up attempt takes place to check whether the fault has disappeared or not. The OVP paragraph gives more design details on this particular section.

Fault Condition – Short−circuit on VCC

In some fault situations, a short−circuit can purposely occur between V_{CC} and GND. In high line conditions (V_{HV} = 370 V dc) the current delivered by the start−up device will seriously increase the junction temperature. For instance, since I_{start1} equals 4.9 mA (the min corresponds to the highest T_J), the device would dissipate 370 x 4.9 x 10^{-3} = 1.81 W. To avoid this situation, the controller includes a novel circuitry made of two start−up levels, I_{start1} and I_{start2}. At power−up, as long as V_{CC} is below a 1.6 V level, the source delivers I_{start2} (around 500 μA typical), then, when V_{CC} reaches 1.6 V, the source smoothly transitions to I_{start1} and delivers its nominal value. As a result, in case of short−circuit between V_{CC} and GND, the power dissipation will drop to 370 x 500 x 10^{-6} = 185 mW. Figure 35 portrays this particular behavior.

The first start−up period is calculated by the formula C x V = I x t, which implies a 1 x 10^{-6} x 1.6 / (500 x 10^{-6}) = 3.2 ms start−up time for the first sequence. The second sequence is obtained by toggling the source to 8.9 mA with a ΔV of $V_{CC(ON)} - V_{CC(TH)}$ = 8.4 V – 1.6 V = 6.8 V, which finally leads to a second start−up time of 1 x 10^{-6} x 6.8 / (8.9 x 10^{-3}) = 0.76 ms. The total start−up time becomes 3.2 ms + 0.76 ms = 3.96 ms. Please note that this calculation is approximated by the presence of the knee in the vicinity of the transition.

Fault Condition – Output Short−circuit

As soon as V_{CC} reaches $V_{CC(ON)}$, drive pulses are internally enabled. If everything is correct, the auxiliary winding increases the voltage on the VCC pin as the output voltage rises. During the start−sequence, the controller smoothly ramps up the peak drain current to maximum setting, i.e. I_{PK}, which is reached after a typical period of 10 ms. When the output voltage is not regulated, the current coming through FB pin is below $I_{FBfault}$ level (35 μA typically), which is not only during the start−up period but also anytime an overload occurs, an internal error flag is asserted, I_{pFlag}, indicating that the system has reached its maximum current limit set−point. The assertion of this flag triggers a fault counter t_{SCP} (48 ms typically). If at counter completion, I_{pFlag} remains asserted, all driving pulses are stopped and the part stays off in $t_{recovery}$ duration (about 420 ms). A new attempt to re−start occurs and will last 48 ms providing the fault is still present. If the fault still affects the output, a safe burst mode is entered, affected by a low duty−cycle operation (11%). When the fault disappears, the power supply quickly resumes operation. Figure 36 depicts this particular mode:

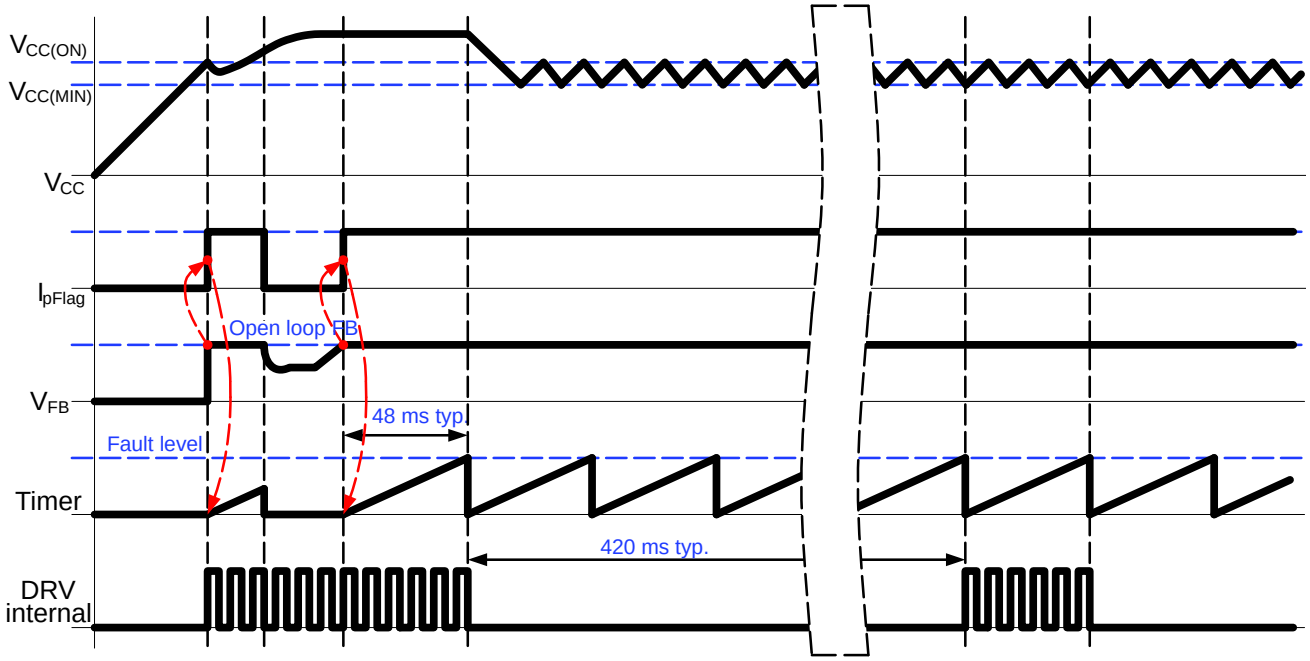


Figure 36. In Case of Short−circuit or Overload, the NCP107xuz Protects Itself and the Power Supply Via a Low Frequency Burst Mode. The V_{CC} is Maintained by the Current Source and Self−supplies the Controller.

Auto−recovery Over−voltage Protection

The particular NCP107xuz arrangement offers a simple way to prevent output voltage runaway when the opto−coupler fails. As Figure 37 shows, a comparator monitors the VCC pin. If the auxiliary winding delivers too much voltage to the C_{VCC} capacitor, then the controller considers an OVP situation and stops the internal drivers. When an OVP occurs, all switching pulses are permanently disabled. After $t_{recovery}$ delay, the circuit resumes operations. If the failure symptom still exists, e.g. feedback opto−coupler fails, the device keeps the auto−recovery OVP mode. We recommend the insertion of a resistor (R_{limit}) between the auxiliary dc level and the VCC pin to protect the IC against high voltage spikes, which can damage the IC. It is also recommended to filter out the VCC line to avoid undesired OVP activations. R_{limit} should be carefully selected to suppress false−triggers of the OVP as we discussed, but also to avoid disturbing the V_{CC} in low / light load conditions.

Self−supplying controllers in extremely low−standby applications often puzzles the designer. Actually, if a SMPS operated at nominal load can deliver an auxiliary voltage of an arbitrary 16 V (V_{nom}), this voltage can drop below 10 V (V_{stby}) when entering standby. This is because the recurrence of the switching pulses expands so much that the low frequency re−fueling rate of the V_{CC} capacitor is not enough to keep a proper auxiliary voltage.

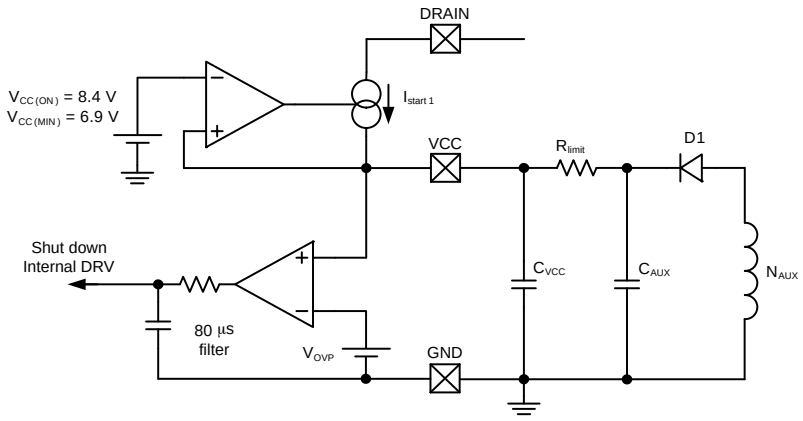


Figure 37. A More Detailed View of the NCP107xuz Offers Better Insight on How to Properly Wire an Auxiliary Winding

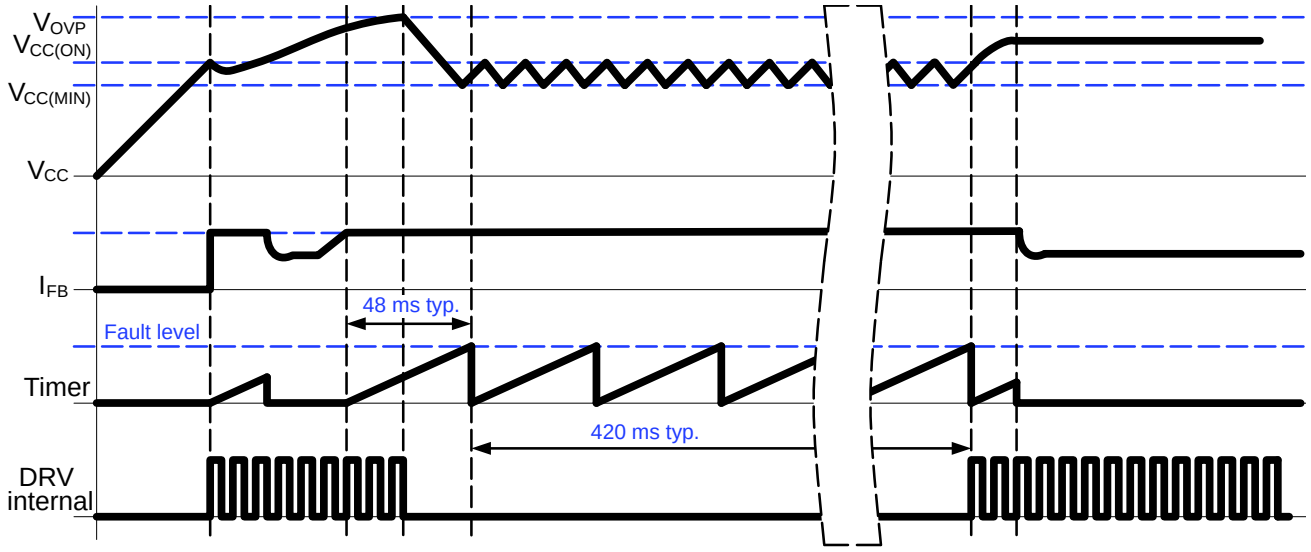


Figure 38. Describes the Main Signal Variations When the Part Operates in Auto−recovery OVP

Soft−start

The NCP107xuz features a 10 ms soft−start which reduces the power−on stress but also contributes to lower the output overshoot. Soft−start is running every time when IC starts switching. It means a first start, a new start after OVP, TSD, Brown−out, etc. Figure 39 shows a typical operating waveform. The NCP107xuz features a novel patented structure which offers a better soft−start ramp, almost ignoring the start−up pedestal inherent to traditional current−mode supplies:

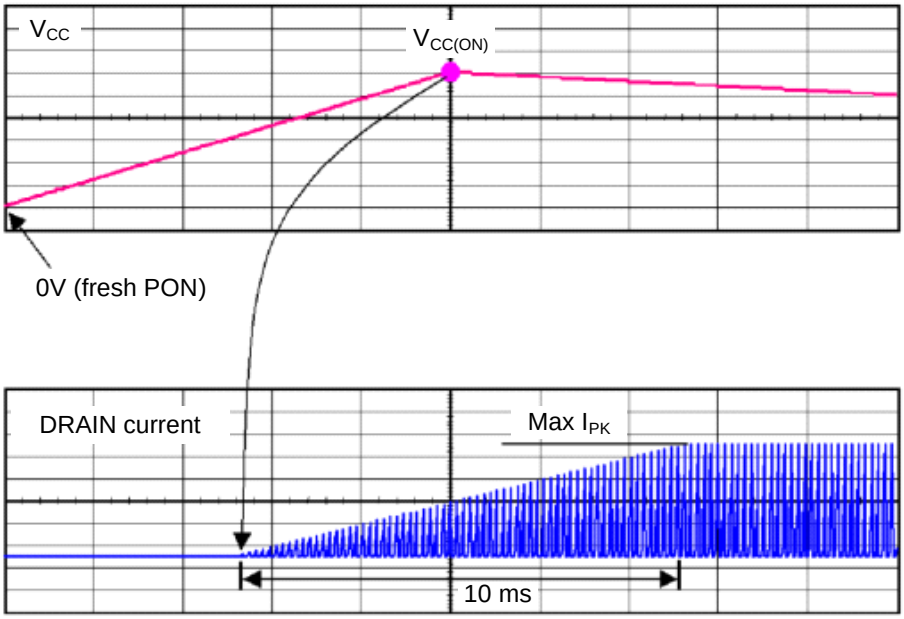


Figure 39. The 10 ms Soft−start Sequence

Jittering

Frequency jittering is a method used to soften the EMI signature by spreading the energy in the vicinity of the main switching component. The NCP107xuz offers a ±6% deviation of the nominal switching frequency. The sweeping sawtooth is internally generated and modulates the clock up and down with a fixed frequency of 300 Hz. Figure 40 shows the relationship between the jitter ramp and the frequency deviation. It is not possible to externally disable the jitter.

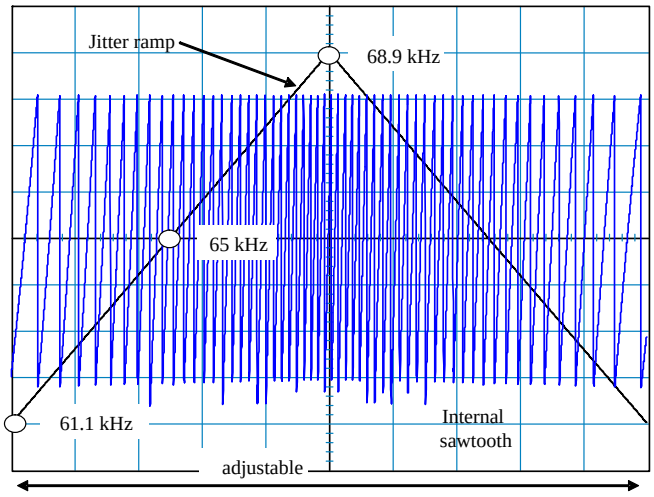


Figure 40. Modulation Effects on the Clock Signal by the Jittering Sawtooth

Line Detection

When BO/AC_OVP pin is grounded (voltage on this pin is below $V_{BO(EN)}$) Figure 2, then an internal comparator monitors the drain voltage as recovering from one of the following situations:

- Short−Circuit Protection,
- V_{CC} OVP is Confirmed,
- UVLO
- TSD

If the drain voltage is lower than the internal threshold $V_{HV(EN)}$ (91 V dc typically), the internal power switch is inhibited. This avoids operating at too low ac input.

Brown−out Function, Ac Line Over−voltage Protection

The Brown−out circuitry offers a way to protect the application from operation under too low an input voltage. Below a given level, the controller blocks the output pulses, above it, it authorizes them. The internal circuitry, depicted by Figure 41, offers a way to observe the high−voltage (HV) rail.

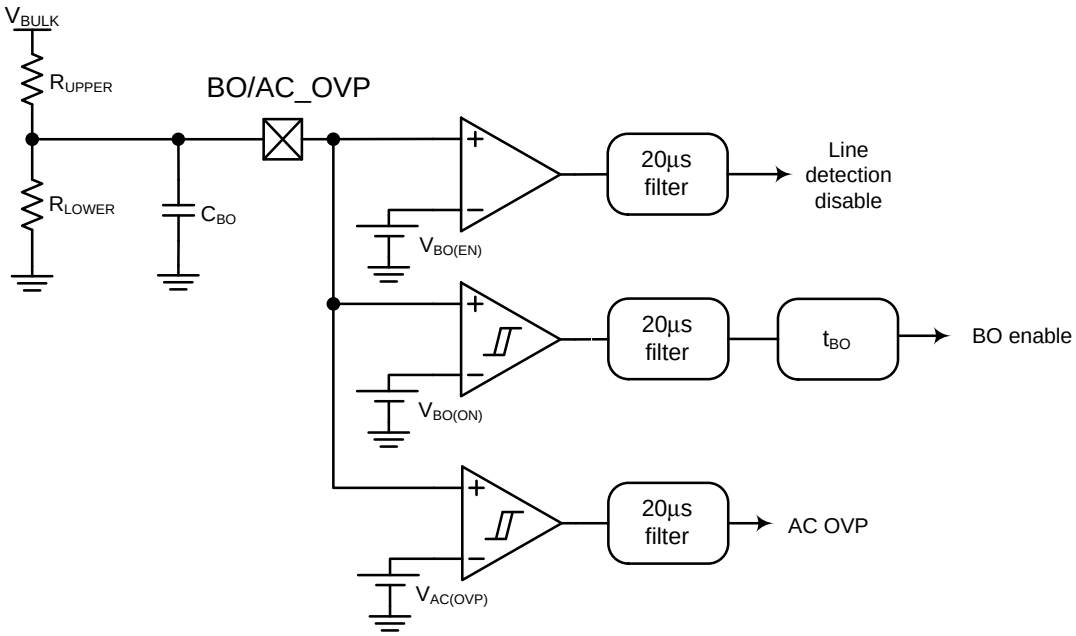


Figure 41. The Internal Brown−out Configuration

A resistive divider made of R_{UPPER} and $R_{LOWER,}$ brings a portion of the HV rail on BO/AC_OVP pin. Below the $V_{BO(EN)}$ = 50 mV is the Brown−out function disabled, over the $V_{BO(EN)}$ Brown−out function is enable and against Line detection is inhibited. If voltage on BO/AC_OVP pin is higher than $V_{BO(ON)}$, switcher starts pulsing. If voltage falls down under $V_{BO(OFF)}$ − level $V_{BO(ON)}$ minus $V_{BO(HYST)}$, the switcher waits 50 ms and then stops pulsing, depicted by Figure 42. Bulk voltage at which IC starts switching is set by resistive divider.

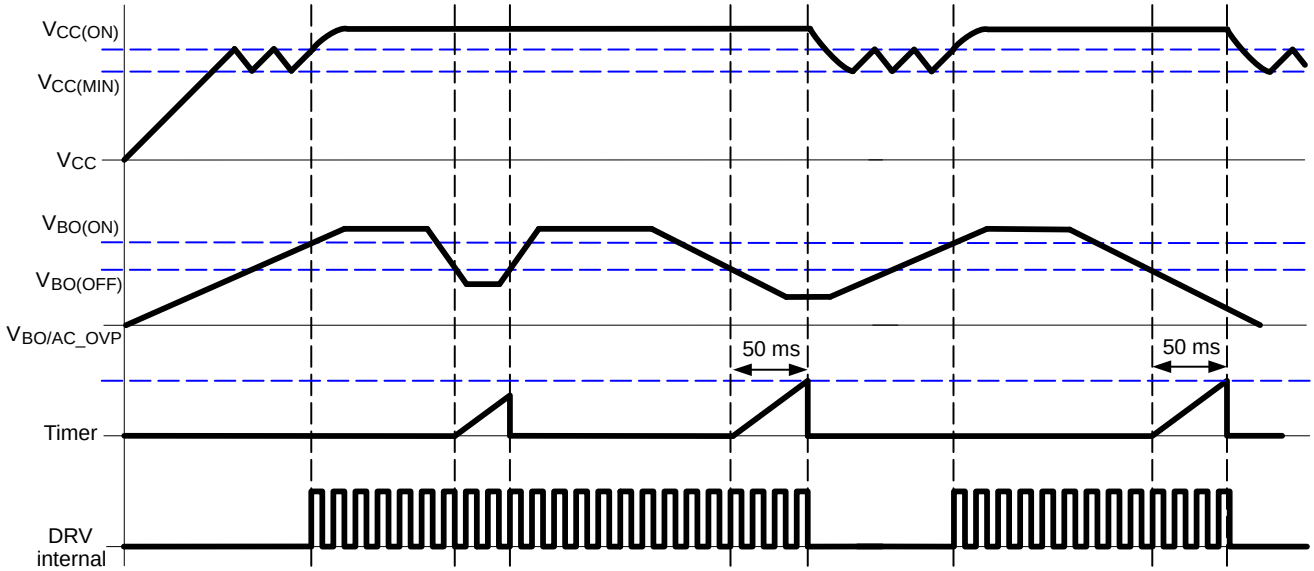


Figure 42. Brown−out Input Functionality with 50 ms Timer

The IC also includes over−voltage protection. If the voltage on BO/AC_OVP pin exceed $V_{ACOVP(ON)}$, the switcher immediately stops pulsing until the voltage on BO/AC_OVP pin drops under $V_{ACOVP(OFF)}$, depicted by Figure 43.

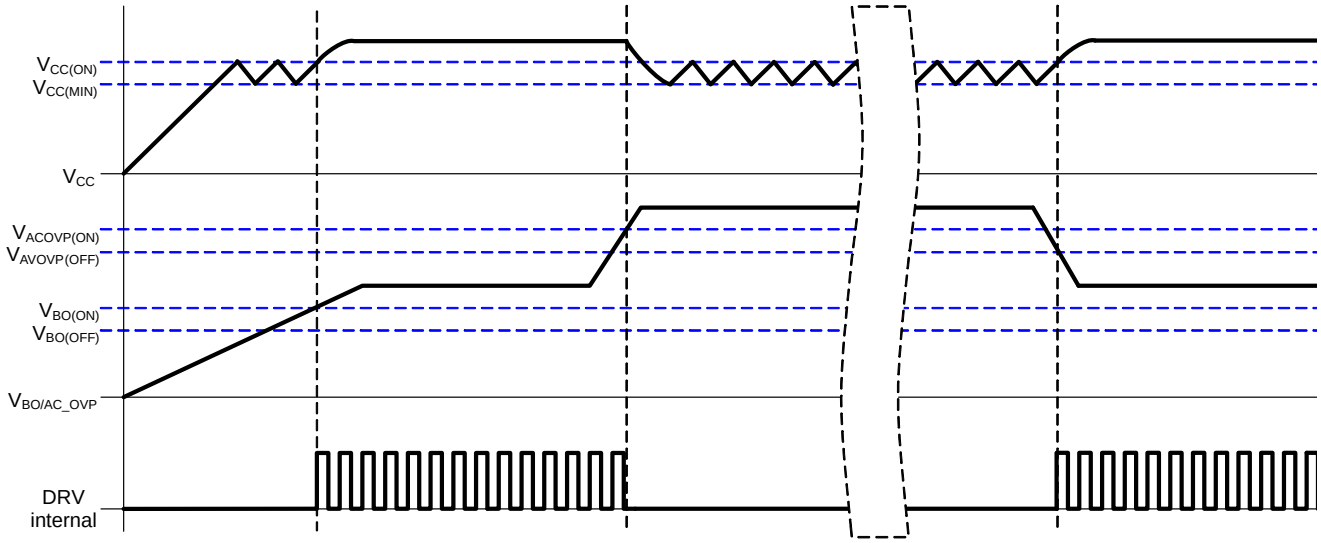


Figure 43. Brown−out Input Functionality with Ac Line OVP Function

Calculation of the resistive divider:

$$\frac{R_{LOWER}}{R_{UPPER}} = \frac{V_{BO(ON)}}{V_{BULK} - V_{BO(ON)}} \quad \text{(eq. 2)}$$

If we decide to start pulsing at $V_{BULK(ON)}$ = 113 V dc (80 V rms at ac mains):

$$\frac{R_{LOWER}}{R_{UPPER}} = \frac{V_{BO(ON)}}{V_{BULK(ON)} - V_{BO(ON)}} = \frac{0.8}{113 - 0.8} \approx 7.1\ m$$

We choose R_{LOWER} = 100 kΩ

$$R_{UPPER} = \frac{100 \cdot 10^3}{7.1 \cdot 10^{-3}} = 14\ M\Omega$$

Then power losses on resistive divider for worst case (V_{BULK} = 409 V dc)

$$P = U \cdot I = \frac{U^2}{R} = \frac{U^2}{R_{UPPER} + R_{LOWER}} = \frac{409^2}{14 \cdot 10^6 + 100 \cdot 10^3} = 12\ mW \quad \text{(eq. 3)}$$

For $V_{BULK(ON)}$ = 113 V dc will be over−voltage protection (voltage when the switcher stops pulsing):

$$V_{BULK(OVP)} = V_{ACOVP(ON)} \cdot \frac{R_{LOWER} + R_{UPPER}}{R_{LOWER}} = V_{ACOVP(ON)} \cdot \frac{V_{BULK(ON)}}{V_{BO(ON)}} = 29 \cdot \frac{113}{0.8} = 409\ Vdc = 290\ Vrms \quad \text{(eq. 4)}$$

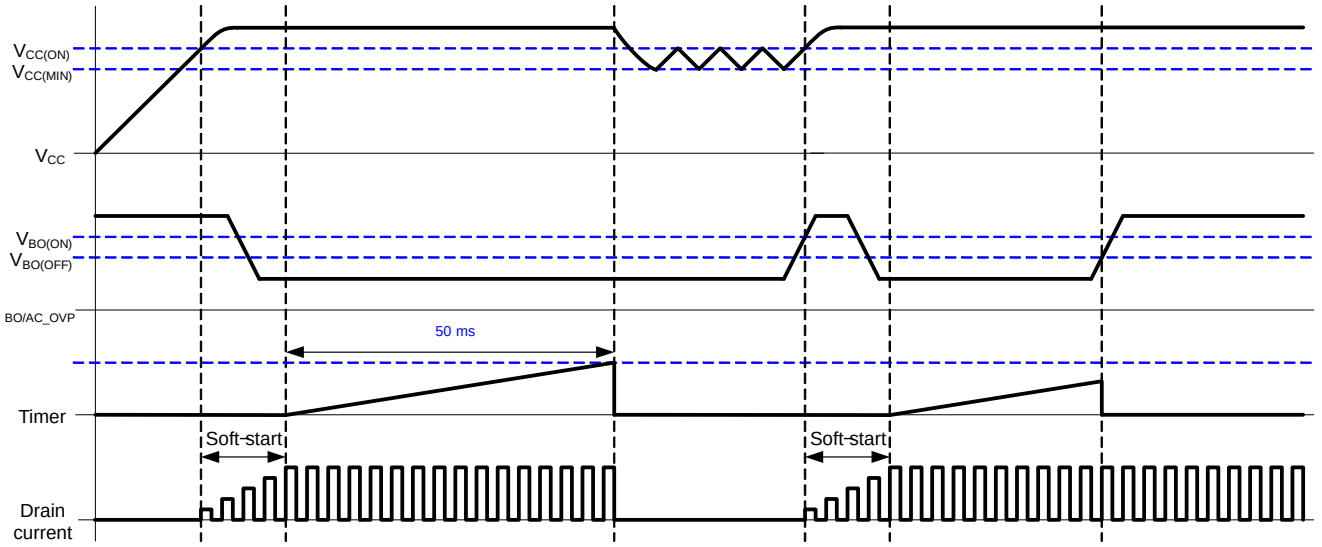


Figure 44. Brown−out Functionality in Soft−start

If voltage on VCC pin is higher than $V_{CC(ON)}$ and voltage on BO/AC_OVP pin is higher than $V_{BO(ON)}$ then IC starts pulsing, drain current is increasing for 10 ms (Soft−start). Brown−out is inhibited during Soft−start, when Soft−start ended, Brown−out checked if is voltage on BO/AC_OVP pin higher than $V_{BO(OFF)}$. If the voltage is lower, timer count 50 ms and if the voltage don't increase over $V_{BO(OFF)}$ then IC stops switching as one can see on Figure 44.

Frequency Foldback

The reduction of no−load standby power associated with the need for improving the efficiency, requires to change the traditional fixed−frequency type of operation. This device implements a switching frequency folback when the feedback current passes above a certain level, I_{FBfold}, set around 68 μA. At this point, the oscillator enters frequency foldback and reduces its switching frequency.

The internal peak current set−point is following the feedback current information until its level reaches the minimal freezing level point of I_{freeze}. Below this value, the peak current set−point is frozen to 30% of the $I_{PK(0)}$. The only way to further reduce the transmitted power is to diminish the operating frequency down to f_{MIN} (27 kHz typically). This value is reached at a feedback current level of $I_{FBfold(END)}$ (100 μA typically). Below this point, if the output power continues to decrease, the part enters skip cycle for the best noise−free performance in no−load conditions. Figures 45 and 46 depict the adopted scheme for the part.

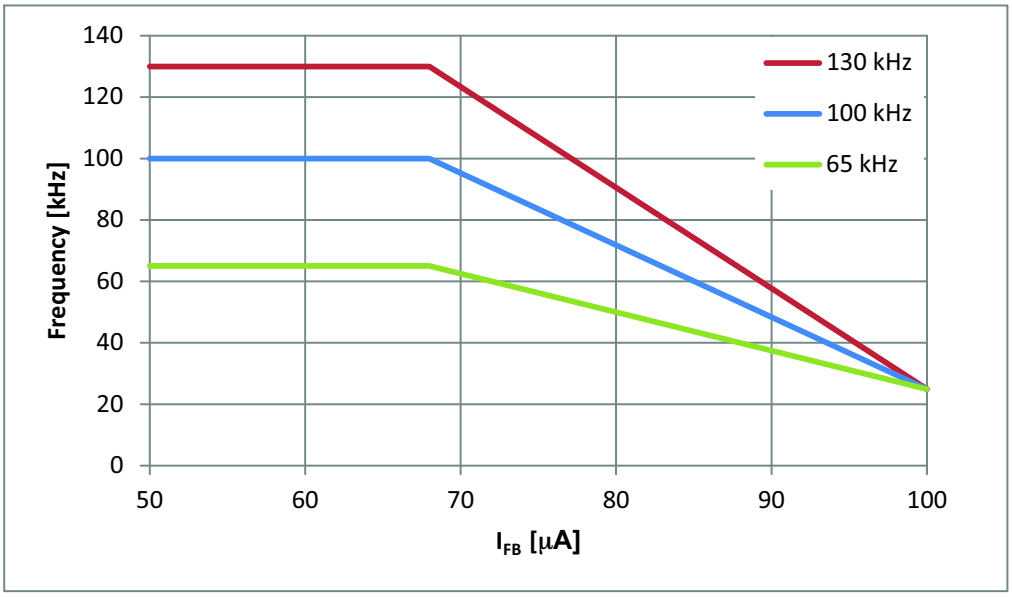


Figure 45. By Observing the Current on the FB pin, the Controller Reduces its Switching Frequency for an Improved Performance at Light Load

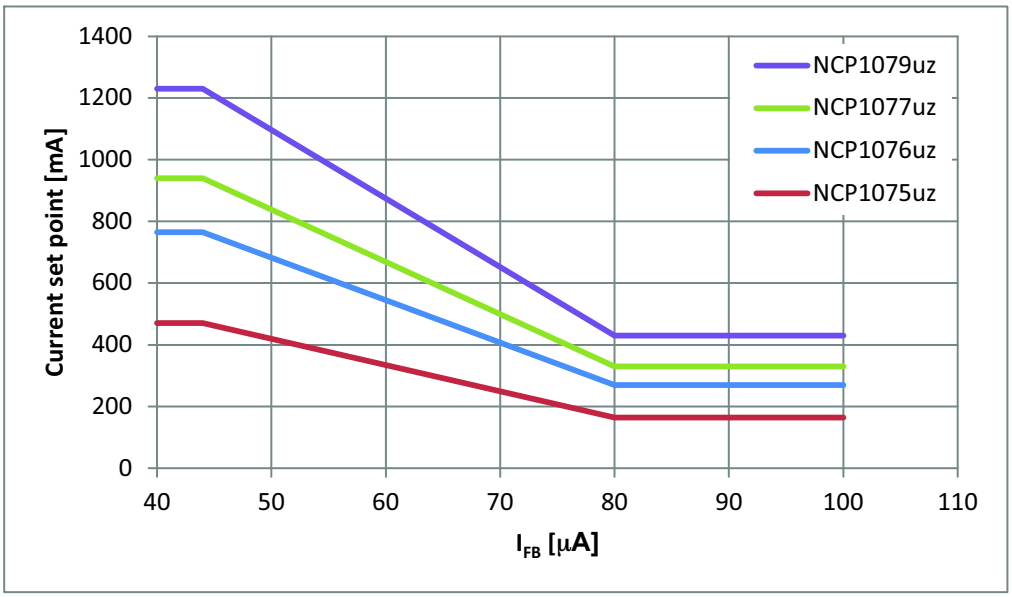


Figure 46. I_{PK} Set−point is Frozen at Lower Power Demand

Feedback and Skip

The FB pin operates linearly as the absolute value of feedback current (I_{FB}) is above 40 μA. In this linear operating range, the dynamic resistance is 19.5 kΩ typically ($R_{FB(UP)}$) and the effective pull up voltage is 3.3 V typically ($V_{FB(REF)}$). When I_{FB} is decreased, the FB voltage will increase to 3.3 V.

Figure 47 depicts the skip mode block diagram. When the FB current information reaches $I_{FB(skip)}$, the internal clock to set the flip−flop is blanked and the internal consumption of the controller is decreased. The hysteresis of internal skip comparator is minimized to lower the ripple of the auxiliary voltage for VCC pin and V_{OUT} of power supply during skip mode. It easies the design of V_{CC} overload range.

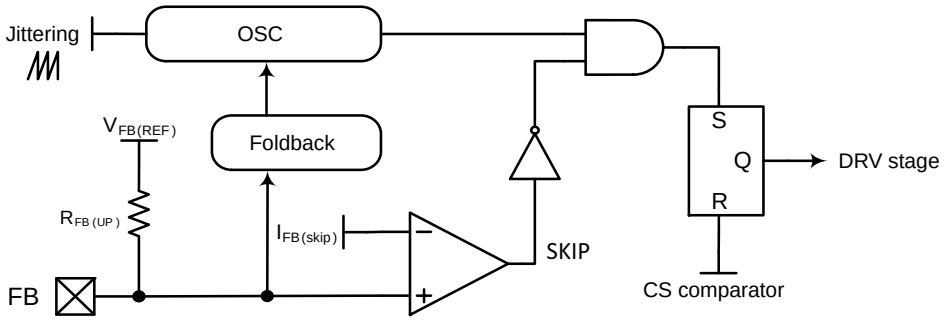


Figure 47. Skip Cycle Schematic

Over−power Protection

This function lets you limit the maximum dc output current regardless of the operating input voltage. For a correct operation, the BO/AC_OVP pin must be connected via a resistive divider to observe the bulk voltage.

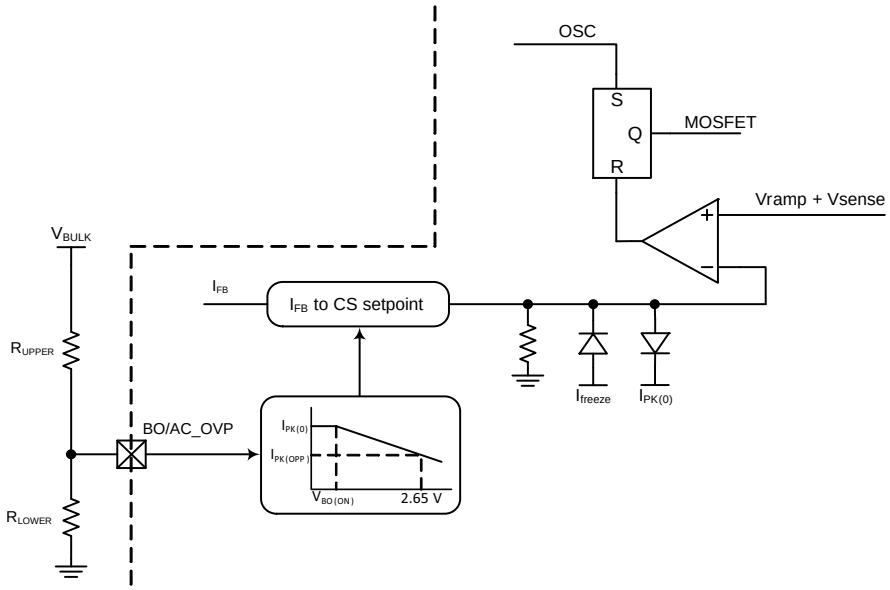


Figure 48. The OPP Circuity Affects the Maximum Peak Current Set−point in Relationship to the Input Voltage.

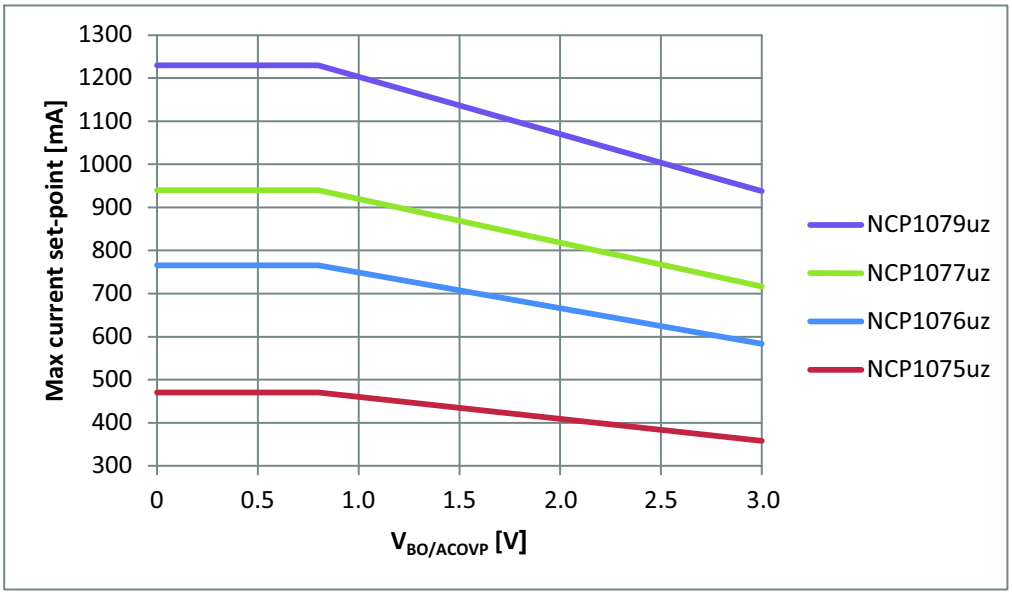


Figure 49. Current Set−point Dependence on BO/AC_OVP Pin Voltage

There are several known ways to implement Over−power Protection (OPP), all suffering from particular problems. These problems range from the added consumption burden on the converter or the skip−cycle disturbance brought by the current−sense offset. In this case is added consumption due to resistive divider (Equation 2).

Maximum peak current is reduced internally according to bulk voltage. When $V_{BO(OPP)}$ is maximum, the peak current set−point is reduced by 10%. Bulk voltage at which will be maximum current peak reduced by 20% (10% in NCP1075uz):

$$V_{BULK(OPP)} = V_{BO(OPP)} \cdot \frac{V_{BULK(ON)}}{V_{BO(ON)}} = V_{BO(OPP)} \cdot \frac{R_{LOWER} + R_{UPPER}}{R_{LOWER}} = 2.65 \cdot \frac{100 \cdot 10^3 + 14 \cdot 10^6}{100 \cdot 10^3} = 375\ \text{Vdc} = 265\ \text{Vrms} \quad \text{(eq. 5)}$$

Second LEB – Peak Current Protection (NCP107xuA only)

There is a second level of current protection with 100 ns propagation delay to prevent IC against high peak current. If peak current is 150% max peak current limit, then the controller stops switching after three pulses and waits for an auto−recovery period ($t_{recovery}$) before attempting to re−start.

Slope Compensation and I_{PK} Set−point

In order to let the NCP107xuz operate in CCM with a duty−cycle above 50%, a fixed slope compensation is internally applied to the current−mode control.

Below appears a table of the slope compensation level, the initial current set−point, and the final current set−point of different versions of switcher.

	NCP1075uz			NCP1076uz			NCP1077uz			NCP1079uz		
f_{SW} [kHz]	65	100	130	65	100	130	65	100	130	65	100	130
S_a [mA/μs]	9	14	18	15	23	30	18	28	36	24	37	46
I_{PK} (Duty−cycle = 50%) [mA]	400			600			800			1050		
$I_{PK(0)}$ [mA]	470			765			940			1230		

Figure 50 depicts the variation of I_{PK} set−point vs. the power switcher duty ratio, which is caused by the internal ramp compensation.

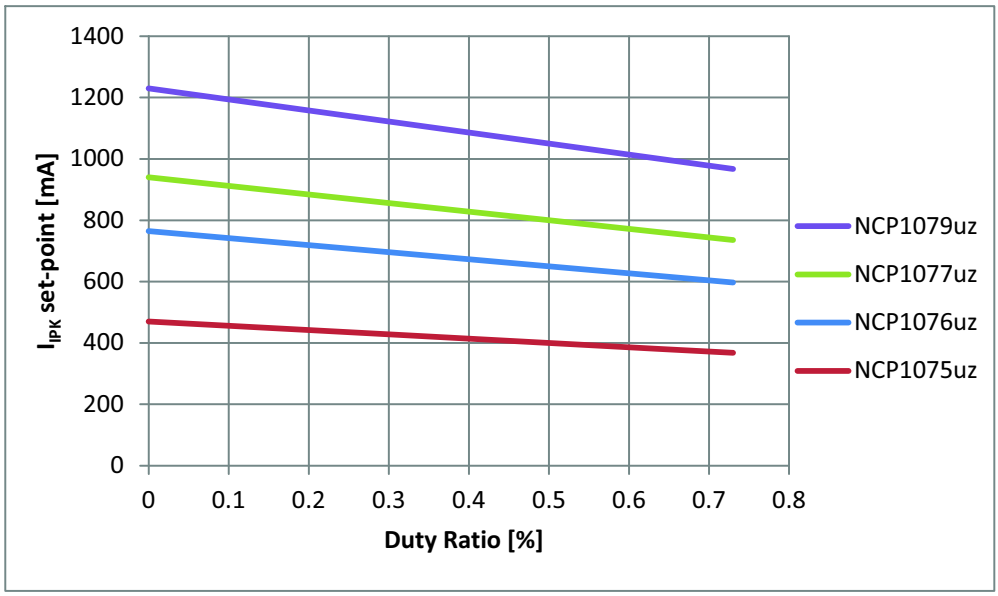


Figure 50. I_{PK} Set−point varies with Power Switch On Time, which is Caused by the Ramp Compensation

Design Procedure

The design of an SMPS around a monolithic device does not differ from that of a standard circuit using a controller and a MOSFET. However, one needs to be aware of certain characteristics specific of monolithic devices. Let us follow the steps:

$V_{IN,MIN}$ = 90 V rms or 127 V dc once rectified, assuming a low bulk ripple
$V_{IN,MAX}$ = 265 V rms or 375 V dc
V_{OUT} = 12 V
P_{OUT} = 10 W
Operating mode is CCM
η = 0.8

1. The lateral MOSFET body−diode shall never be forward biased, either during start−up (because of a large leakage inductance) or in normal operation, depicted by Figure 51. This condition sets the maximum voltage that can be reflected during t_F As a result, the flyback voltage which is reflected on the drain at the switch opening cannot be larger than the input voltage. When selecting components, you thus must adopt a turn ratio which adheres to the following equation:

$$N \cdot \left(V_{OUT} + V_F\right) < V_{IN,MIN} \quad \text{(eq. 6)}$$

2. In our case, since we operate from a 127 V dc rail while delivering 12 V, we can select a reflected voltage of 120 V dc maximum. Therefore, the turn ratio Np:Ns must be smaller than

$$\frac{V_{reflect}}{V_{OUT} + V_F} = \frac{120}{12 + 0.5} = 9.6 \text{ or } Np : Ns < 9.6$$

Here we choose N = 8 in this case. We will see later on how it affects the calculation.

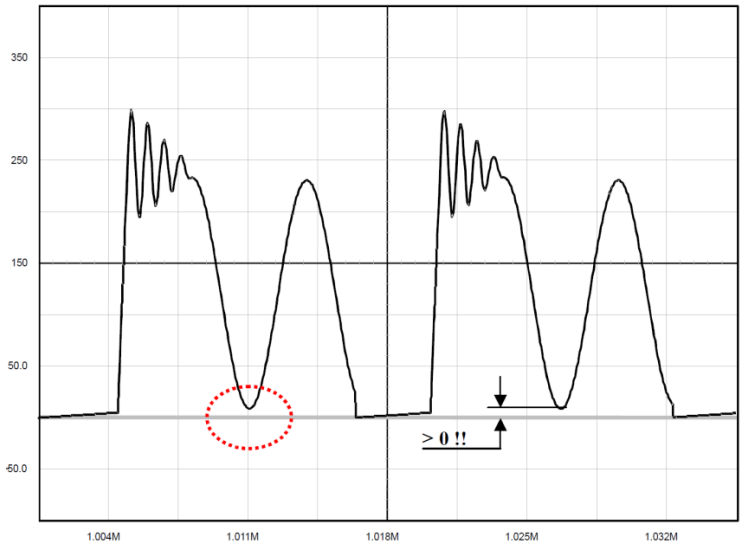


Figure 51. The Drain−Source Wave Shall Always be Positive

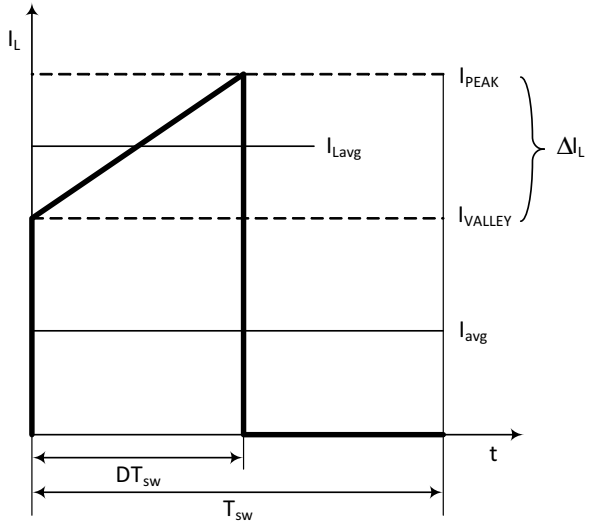


Figure 52. Primary Inductance Current Evolution in CCM

3. Lateral MOSFETs have a poorly doped body−diode which naturally limits their ability to sustain the avalanche. A traditional RCD clamping network shall thus be installed to protect the MOSFET. In some low power applications, a simple capacitor can also be used since

$$V_{DRAIN,MAX} = V_{IN} + N \cdot \left(V_{OUT} + V_F\right) + I_{PEAK} \cdot \sqrt{\frac{L_F}{C_{TOT}}} \quad \text{(eq. 7)}$$

where L_F is the leakage inductance, C_{TOT} the total capacitance at the drain node (which is increased by the capacitor you will wire between drain and source), N the N_P:N_S turn ratio, V_{OUT} the output voltage, V_F the secondary diode forward drop and finally, I_{PEAK} the maximum peak current. Worse case occurs when the SMPS is very close to regulation, e.g. the V_{OUT} target is almost reached and I_{PEAK} is still pushed to the maximum. For this

design, we have selected our maximum voltage around 650 V (at V_{IN} = 375 V dc). This voltage is given by the *RCD* clamp installed from the drain to the bulk voltage. We will see how to calculate it later on.

4. Calculate the maximum operating duty−cycle for this flyback converter operated in CCM:

$$D_{MAX} = \frac{N \cdot (V_{OUT} + V_F)}{N \cdot (V_{OUT} + V_F) + V_{IN,MIN}} = \frac{1}{1 + \frac{V_{IN,MIN}}{N \cdot (V_{OUT} + V_F)}} = 0.44 \quad \text{(eq. 8)}$$

5. To obtain the primary inductance, we have the choice between two equations:

$$L = \frac{(V_{IN} \cdot D)^2}{f_{SW} \cdot K \cdot P_{IN}} \quad \text{(eq. 9)}$$

where $$K = \frac{\Delta I_L}{I_{Lavg}} \quad \text{(eq. 10)}$$

and defines the amount of ripple we want in CCM, depicted by Figure 51.

- Small K: deep CCM, implying a large primary inductance, a low bandwidth and a large leakage inductance.
- Large K: approaching DCM where the conduction losses are worse, but smaller inductance, leading to a better leakage inductance.

From Equation 9, a *K* factor of 1 (50% ripple), gives an inductance of:

$$L = \frac{(127 \cdot 0.44)^2}{65\,k \cdot 1 \cdot 12.75} = 3.8\ mH \qquad \Delta I_L = \frac{V_{IN} \cdot D}{L \cdot f_{SW}} = \frac{127 \cdot 0.44}{3.8 \cdot 10^{-3} \cdot 65 \cdot 10^3} = 223\ mA \quad \text{(eq. 11)}$$

peak−to−peak

The peak current can be evaluated to be:

$$I_{PEAK} = \frac{I_{avg}}{D} + \frac{\Delta I_L}{2} = \frac{98 \cdot 10^{-3}}{0.44} + \frac{223 \cdot 10^{-3}}{2} = 335\ mA \quad \text{(eq. 12)}$$

On I_L, I_{Lavg} can also be calculated

$$I_{Lavg} = I_{PEAK} - \frac{\Delta I_L}{2} = 335 \cdot 10^{-3} - \frac{223 \cdot 10^{-3}}{2} = 223\ mA \quad \text{(eq. 13)}$$

6. Based on the above numbers, we can now evaluate the conduction losses:

$$I_{D,RMS} = \sqrt{D\left(I_{PEAK}^2 - I_{PEAK} \cdot \Delta I_L + \frac{\Delta I_L^2}{3}\right)} = \sqrt{0.44\left(0.335^2 - 0.335 \cdot 0.223 + \frac{0.223^2}{3}\right)} = 154\ mA \quad \text{(eq. 14)}$$

If we take the maximum $R_{DS(ON)}$ for a 125°C junction temperature, i.e. 10.1 Ω, then conduction losses worse case are:

$$P_{COND} = I_{D,RMS}^2 \cdot R_{DS(ON)} = (154 \cdot 10^{-3})^2 \cdot 13.6 = 323\ mW \quad \text{(eq. 15)}$$

7. Off−time and on−time switching losses can be estimated based on the following calculations:

$$P_{OFF} = \frac{I_{PEAK} \cdot (V_{BULK} + V_{CLAMP}) \cdot t_F}{2 \cdot T_{SW}} = \frac{0.335 \cdot (127 + 120 \cdot 2) \cdot 10 \cdot 10^{-9}}{2 \cdot 15.4 \cdot 10^{-6}} = 40\ mW \quad \text{(eq. 16)}$$

Where, assume the V_{CLAMP} is equal to 2 times of reflected voltage.

$$P_{ON} = \frac{I_{VALLEY} \cdot (V_{BULK} + N \cdot (V_{OUT} + V_F)) \cdot t_R}{6 \cdot T_{SW}} = \frac{0.112 \cdot (127 + 100) \cdot 20 \cdot 10^{-9}}{6 \cdot 15.4 \cdot 10^{-6}} = 5.5\ mW \quad \text{(eq. 17)}$$

It is noted that the overlap of voltage and current seen on MOSFET during turning on and off duration is dependent on the snubber and parasitic capacitance seen from drain pin. Therefore the t_F and t_R in Equations 16 and 17 have to be modified after measuring on the bench.

8. The theoretical total power is then

$$P_{MOSFET} = 323 + 40 + 5.5 = 368.5\ mW$$

9. If the NCP107xuz operates at DSS mode, then the losses caused by DSS mode should be counted as losses of this device on the following calculation:

$$P_{DSS} = I_{CC1} \cdot V_{IN,MAX} = 1.5 \cdot 10^{-3} \cdot 375 = 563\ mW \quad \text{(eq. 18)}$$

MOSFET Protection

As in any flyback design, it is important to limit the drain excursion to a safe value, e.g. below the MOSFET BV_{DSS} which is 700 V. Figure 53 **a−b−c** present possible implementations:

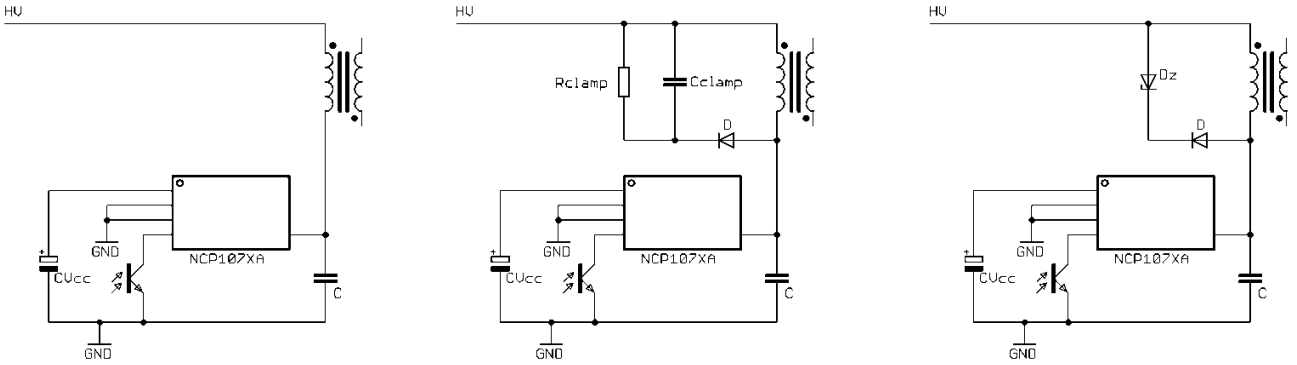


Figure 53. Different Options to Clamp the Leakage Spike

Figure 53a: the simple capacitor limits the voltage according to the lateral MOSFET body−diode shall never be forward biased, either during start−up (because of a large leakage inductance) or in normal operation as shown by Figure 51. This condition sets the maximum voltage that can be reflected during t_F. As a result, the flyback voltage which is reflected on the drain at the switch opening cannot be larger than the input voltage. When selecting components, you must adopt a turn ratio which adheres to the following Equation 6. This option is only valid for low power applications, e.g. below 5 W, otherwise chances exist to destroy the MOSFET. After evaluating the leakage inductance, you can compute C with (Equation 7). Typical values are between 100 pF and up to 470 pF. Large capacitors increase capacitive losses...

Figure 53b: the most standard circuitry is called the *RCD* network. You calculate R_{CLAMP} and C_{CLAMP} using the following formulae:

$$R_{CLAMP} = \frac{2 \cdot V_{CLAMP}\left(V_{CLAMP} + (V_{OUT} + V_F) \cdot N\right)}{L_{LEAK} \cdot I_{LEAK}^2 \cdot f_{SW}} \quad \text{(eq. 19)}$$

$$C_{CLAMP} = \frac{V_{CLAMP}}{V_{RIPPLE} \cdot f_{SW} \cdot R_{CLAMP}} \quad \text{(eq. 20)}$$

V_{CLAMP} is usually selected 50−80 V above the reflected value N x $(V_{OUT} + V_F)$. The diode needs to be a fast one and a MUR160 represents a good choice. One major drawback of the RCD network lies in its dependency upon the peak current. Worse case occurs when I_{PEAK} and V_{IN} are maximum and V_{OUT} is close to reach the steady−state value.

Figure 53c: this option is probably the most expensive of all three but it offers the best protection degree. If you need a very precise clamping level, you must implement a Zener diode or a TVS. There are little technology differences behind a standard Zener diode and a TVS. However, the die area is far bigger for a transient suppressor than that of Zener. A 5 W Zener diode like the 1N5388B will accept 180 W peak power if it lasts less than 8.3 ms. If the peak current in the worse case (e.g. when the PWM circuit maximum current limit works) multiplied by the nominal zener voltage exceeds these 180 W, then the diode will be destroyed when the supply experiences overloads. A transient suppressor like the P6KE200 still dissipates 5 W of continuous power but is able to accept surges up to 600 W @ 1 ms. Select the Zener or TVS clamping level between 40 to 80 volts above the reflected output voltage when the supply is heavily loaded.

As a good design practice, it is recommended to implement one of this protection to ensure a maximum drain pin voltage below 650 V (to have some margin between drain pin voltage and BV_{DSS}) during most stringent operating conditions (high V_{IN} and peak power condition).

Power Dissipation and Heatsinking

The NCP107xuz welcomes two dissipating terms, the DSS current−source (when active) and the MOSFET. Thus, $P_{TOT} = P_{DSS} + P_{MOSFET}$. It is mandatory to properly manage the heat generated by losses. If no precaution is taken, risks exist to trigger the internal thermal shutdown (TSD). To help dissipating the heat, the PCB designer must foresee large copper areas around the package. Take the PDIP−7 package as an example, when surrounded by a surface approximately 200 mm^2 of 35 μm copper, the maximum power the device can thus evacuate is:

$$P_{MAX} = \frac{T_{J(max)} - T_{AMB(max)}}{R_{\theta JA}} \qquad \text{(eq. 21)}$$

which gives around 1300 mW for an ambient of 50°C and a maximum junction of 150°C. If the surface is not large enough, the $R_{\theta JA}$ is growing and the maximum power the device can evacuate decreases. Figure 54 gives a possible layout to help drop the thermal resistance.

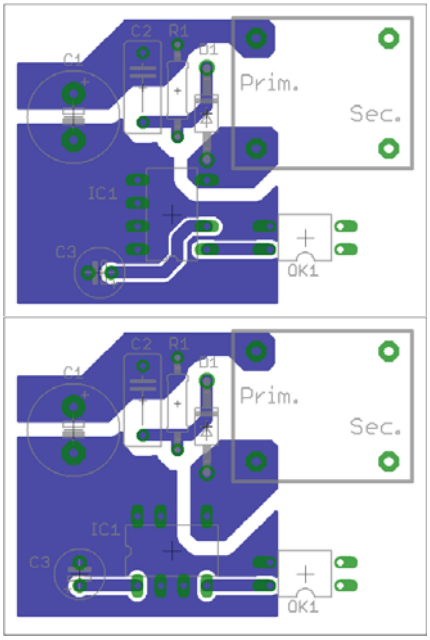


Figure 54. A Possible PCB Arrangement to Reduce the Thermal Resistance Junction−to−Ambient

Bill of Material:

C_1	Bulk capacitor, input dc voltage is connected to the capacitor
C_2, R_1, D_1	Clamping elements
C_3	V_{CC} capacitor
OK_1	Opto−coupler

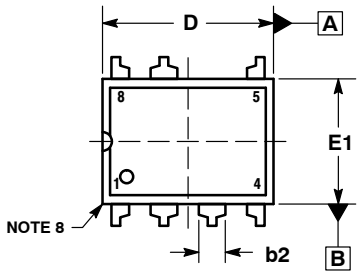
ORDERING INFORMATION

Device	Frequency [kHz]	$R_{DS(ON)}$ [Ω]	I_{PK} [mA]	2nd level OCP	Package Type	Shipping
NCP1075AAP065G	65	13.5	400	enabled	PDIP8 (Less pin#6)	50 Units / Rail
NCP1075AAP100G	100	13.5	400	enabled	PDIP8 (Less pin#6)	
NCP1075BAP065G	65	13.5	400	enabled	PDIP8 (Less pin#3)	
NCP1075BAP100G	100	13.5	400	enabled	PDIP8 (Less pin#3)	
NCP1075BAP130G	130	13.5	400	enabled	PDIP8 (Less pin#3)	
NCP1076AAP065G	65	4.8	650	enabled	PDIP8 (Less pin#6)	
NCP1076AAP100G	100	4.8	650	enabled	PDIP8 (Less pin#6)	
NCP1076BAP065G	65	4.8	650	enabled	PDIP8 (Less pin#3)	
NCP1076BAP100G	100	4.8	650	enabled	PDIP8 (Less pin#3)	
NCP1076BAP130G	130	4.8	650	enabled	PDIP8 (Less pin#3)	
NCP1077AAP065G	65	4.8	800	enabled	PDIP8 (Less pin#6)	
NCP1077AAP100G	100	4.8	800	enabled	PDIP8 (Less pin#6)	
NCP1077BAP065G	65	4.8	800	enabled	PDIP8 (Less pin#3)	
NCP1077BAP100G	100	4.8	800	enabled	PDIP8 (Less pin#3)	
NCP1077BAP130G	130	4.8	800	enabled	PDIP8 (Less pin#3)	
NCP1079AAP065G	65	2.9	1050	enabled	PDIP8 (Less pin#6)	
NCP1079AAP100G	100	2.9	1050	enabled	PDIP8 (Less pin#6)	
NCP1079BAP065G	65	2.9	1050	enabled	PDIP8 (Less pin#3)	
NCP1079BAP100G	100	2.9	1050	enabled	PDIP8 (Less pin#3)	
NCP1079BAP130G	130	2.9	1050	enabled	PDIP8 (Less pin#3)	
NCP1075ABP065G	65	13.5	400	disabled	PDIP8 (Less pin#6)	
NCP1075ABP100G	100	13.5	400	disabled	PDIP8 (Less pin#6)	
NCP1075BBP065G	65	13.5	400	disabled	PDIP8 (Less pin#3)	
NCP1075BBP100G	100	13.5	400	disabled	PDIP8 (Less pin#3)	
NCP1075BBP130G	130	13.5	400	disabled	PDIP8 (Less pin#3)	
NCP1076ABP065G	65	4.8	650	disabled	PDIP8 (Less pin#6)	
NCP1076ABP100G	100	4.8	650	disabled	PDIP8 (Less pin#6)	
NCP1076BBP065G	65	4.8	650	disabled	PDIP8 (Less pin#3)	
NCP1076BBP100G	100	4.8	650	disabled	PDIP8 (Less pin#3)	
NCP1076BBP130G	130	4.8	650	disabled	PDIP8 (Less pin#3)	
NCP1077ABP065G	65	4.8	800	disabled	PDIP8 (Less pin#6)	
NCP1077ABP100G	100	4.8	800	disabled	PDIP8 (Less pin#6)	
NCP1077BBP065G	65	4.8	800	disabled	PDIP8 (Less pin#3)	
NCP1077BBP100G	100	4.8	800	disabled	PDIP8 (Less pin#3)	
NCP1077BBP130G	130	4.8	800	disabled	PDIP8 (Less pin#3)	
NCP1079ABP065G	65	2.9	1050	disabled	PDIP8 (Less pin#6)	
NCP1079ABP100G	100	2.9	1050	disabled	PDIP8 (Less pin#6)	
NCP1079BBP065G	65	2.9	1050	disabled	PDIP8 (Less pin#3)	
NCP1079BBP100G	100	2.9	1050	disabled	PDIP8 (Less pin#3)	
NCP1079BBP130G	130	2.9	1050	disabled	PDIP8 (Less pin#3)	

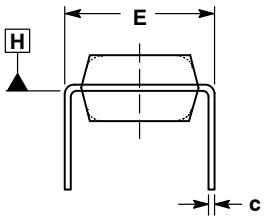
PDIP−7 (PDIP−8 LESS PIN 6)
CASE 626A
ISSUE C

DATE 22 APR 2015

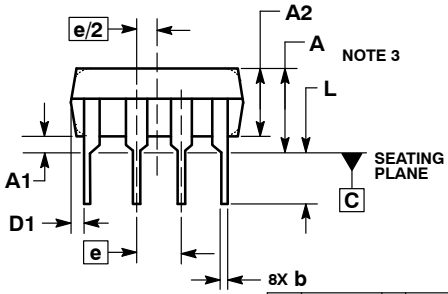
SCALE 1:1



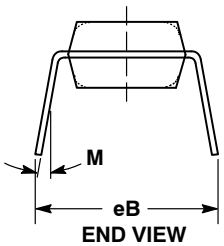
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW

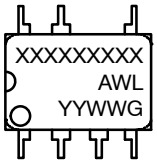


END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	**PDIP−7 (PDIP−8 LESS PIN 6)**		**PAGE 1 OF 1**

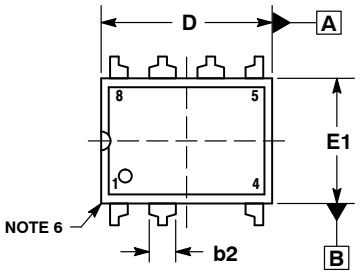
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

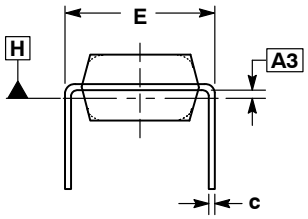
PDIP8 LESS PIN 3
CASE 626AS
ISSUE O

DATE 23 OCT 2015

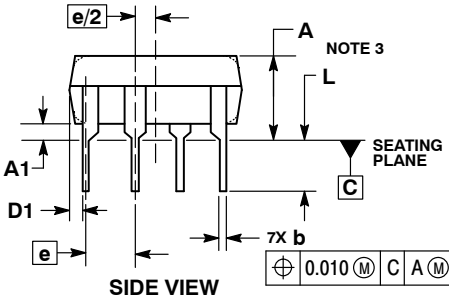
SCALE 1:1



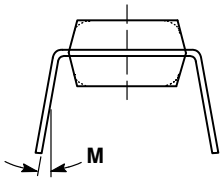
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW



END VIEW

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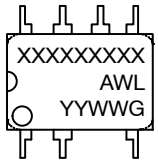
6. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.155	0.175	3.94	4.45
A1	0.020	0.040	0.51	1.02
A3	0.015 BSC		0.38 BSC	
b	0.015	0.020	0.38	0.50
b2	0.056	0.064	1.42	1.63
c	0.008	0.012	0.20	0.30
D	0.365	0.369	9.27	9.37
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.25
E1	0.244	0.260	6.20	6.60
e	0.100 BSC		2.54 BSC	
L	0.115	0.135	2.92	3.43
M	----	10°	---	10°

GENERIC MARKING DIAGRAM*



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DESCRIPTION:	PDIP8 LESS PIN 3	PAGE 1 OF 1