

# NCP130

## 300 mA, Very Low Dropout Bias Rail CMOS Voltage Regulator

The NCP130 is a 300 mA VLDO equipped with NMOS pass transistor and a separate bias supply voltage ( $V_{BIAS}$ ). The device provides very stable, accurate output voltage with low noise suitable for space constrained, noise sensitive applications. In order to optimize performance for battery operated portable applications, the NCP130 features low  $I_Q$  consumption. The XDFN6 1.2 mm x 1.2 mm package is optimized for use in space constrained applications.

### Features

- Input Voltage Range: 0.8 V to 5.5 V
- Bias Voltage Range: 2.4 V to 5.5 V
- Fixed Output Voltage Device
- Output Voltage Range: 0.8 V to 2.1 V
- $\pm 1.5\%$  Accuracy over Temperature, 0.5%  $V_{OUT}$  @ 25°C
- Ultra-Low Dropout: 150 mV Maximum at 300 mA
- Very Low Bias Input Current of Typ. 80  $\mu$ A
- Very Low Bias Input Current in Disable Mode: Typ. 0.5  $\mu$ A
- Logic Level Enable Input for ON/OFF Control
- Output Active Discharge Option Available
- Stable with a 1  $\mu$ F Ceramic Capacitor
- Available in XDFN6 – 1.2 mm x 1.2 mm x 0.37 mm Package
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- Battery-powered Equipment
- Smartphones, Tablets
- Cameras, DVRs, STB and Camcorders

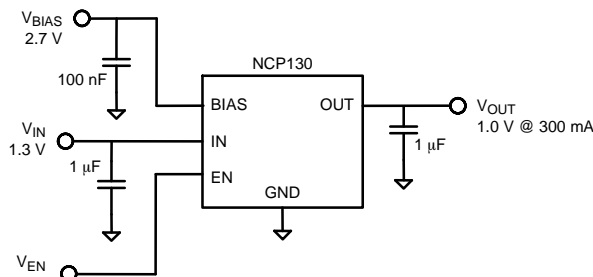


Figure 1. Typical Application Schematics



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### MARKING DIAGRAM

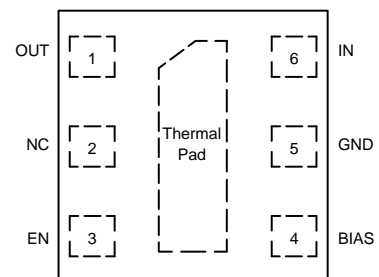


XDFN6  
CASE 711AT



XX = Specific Device Code  
M = Date Code

### PIN CONNECTIONS

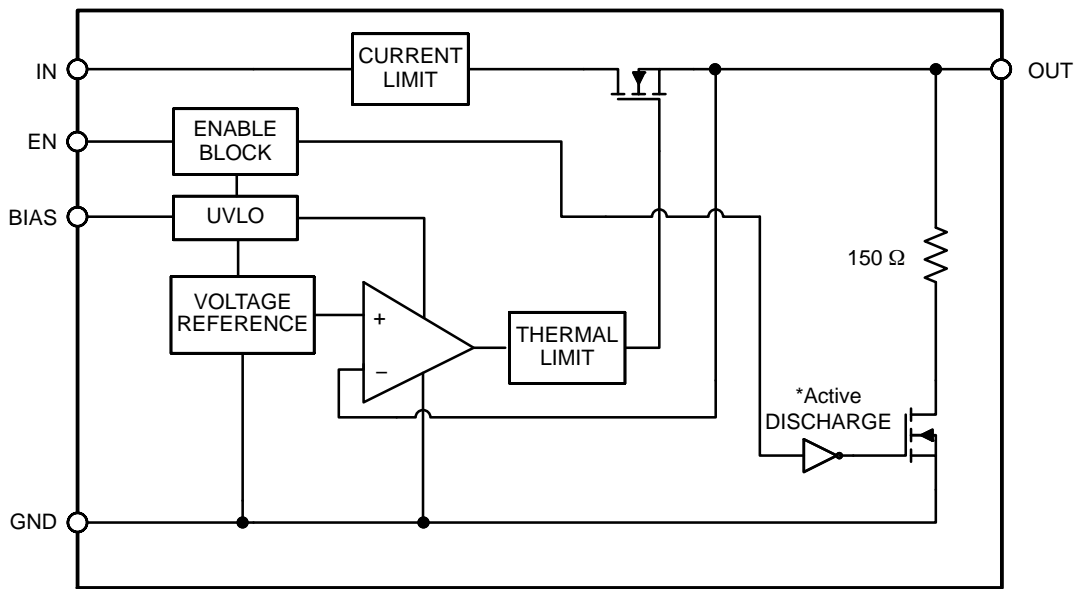


(Top View)

### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 8 of this data sheet.

# NCP130



\*Active output discharge function is present only in NCP130AMXyyyTCG devices.  
yyy denotes the particular output voltage option.

**Figure 2. Simplified Schematic Block Diagram**

## PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	OUT	Regulated Output Voltage pin
2	N/C	Not internally connected
3	EN	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode.
4	BIAS	Bias voltage supply for internal control circuits. This pin is monitored by internal Under-Voltage Lockout Circuit.
5	GND	Ground pin
6	IN	Input Voltage Supply pin
Pad		Should be soldered to the ground plane for increased thermal performance.

## ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	$V_{IN}$	-0.3 to 6	V
Output Voltage	$V_{OUT}$	-0.3 to $(V_{IN}+0.3) \leq 6$	V
Chip Enable and Bias Input	$V_{EN}, V_{BIAS}$	-0.3 to 6	V
Output Short Circuit Duration	$t_{SC}$	unlimited	s
Maximum Junction Temperature	$T_J$	150	°C
Storage Temperature	$T_{STG}$	-55 to 150	°C
ESD Capability, Human Body Model (Note 2)	$ESD_{HBM}$	2000	V
ESD Capability, Machine Model (Note 2)	$ESD_{MM}$	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection (except OUT pin) and is tested by the following methods:  
ESD Human Body Model tested per EIA/JESD22-A114  
ESD Machine Model tested per EIA/JESD22-A115  
Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

## THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, XDFN6 1.2 mm x 1.2 mm Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	170	°C/W

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## ELECTRICAL CHARACTERISTICS

−40°C ≤ T<sub>J</sub> ≤ 85°C; V<sub>BIAS</sub> = 2.7 V or (V<sub>OUT</sub> + 1.6 V), whichever is greater, V<sub>IN</sub> = V<sub>OUT(NOM)</sub> + 0.3 V, I<sub>OUT</sub> = 1 mA, V<sub>EN</sub> = 1 V, unless otherwise noted. C<sub>IN</sub> = 1 μF, C<sub>BIAS</sub> = 0.1 μF, C<sub>OUT</sub> = 1 μF (effective capacitance) (Note 3). Typical values are at T<sub>J</sub> = +25°C. Min/Max values are for −40°C ≤ T<sub>J</sub> ≤ 85°C unless otherwise noted. (Note 4)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Operating Input Voltage Range		V <sub>IN</sub>	V <sub>OUT</sub> +V <sub>DO</sub>		5.5	V
Operating Bias Voltage Range		V <sub>BIAS</sub>	(V <sub>OUT</sub> +1.35) ≥2.4		5.5	V
Undervoltage Lock-out	V <sub>BIAS</sub> Rising Hysteresis	UVLO		1.6 0.2		V
Output Voltage Accuracy	−40°C ≤ T <sub>J</sub> ≤ 85°C, V <sub>OUT(NOM)</sub> + 0.3 V ≤ V <sub>IN</sub> ≤ 5.0 V, 2.7 V or (V <sub>OUT(NOM)</sub> + 1.6 V), whichever is greater < V <sub>BIAS</sub> < 5.5 V, 1 mA < I <sub>OUT</sub> < 300 mA	V <sub>OUT</sub>	−1.5		+1.5	%
Output Voltage Accuracy		V <sub>OUT</sub>		±0.5		%
V <sub>IN</sub> Line Regulation	V <sub>OUT(NOM)</sub> + 0.3 V ≤ V <sub>IN</sub> ≤ 5.0 V	Line <sub>Reg</sub>		0.01		%/V
V <sub>BIAS</sub> Line Regulation	2.7 V or (V <sub>OUT(NOM)</sub> + 1.6 V), whichever is greater < V <sub>BIAS</sub> < 5.5 V	Line <sub>Reg</sub>		0.01		%/V
Load Regulation	I <sub>OUT</sub> = 1 mA to 300 mA	Load <sub>Reg</sub>		1.5		mV
V <sub>IN</sub> Dropout Voltage	I <sub>OUT</sub> = 300 mA (Note 5)	V <sub>DO</sub>		75	150	mV
V <sub>BIAS</sub> Dropout Voltage	I <sub>OUT</sub> = 300 mA, V <sub>IN</sub> = V <sub>BIAS</sub> (Note 5)	V <sub>DO</sub>		1.1	1.4	V
Output Current Limit	V <sub>OUT</sub> = 90% V <sub>OUT(NOM)</sub>	I <sub>CL</sub>	400	550	850	mA
Bias Pin Operating Current	V <sub>BIAS</sub> = 2.7 V	I <sub>BIAS</sub>		80	110	μA
Bias Pin Disable Current	V <sub>EN</sub> ≤ 0.4 V	I <sub>BIAS(DIS)</sub>		0.5	1	μA
V <sub>input</sub> Pin Disable Current	V <sub>EN</sub> ≤ 0.4 V	I <sub>VIN(DIS)</sub>		0.5	1	μA
EN Pin Threshold Voltage	EN Input Voltage "H"	V <sub>EN(H)</sub>	0.9			V
	EN Input Voltage "L"	V <sub>EN(L)</sub>			0.4	
EN Pull Down Current	V <sub>EN</sub> = 5.5 V	I <sub>EN</sub>		0.3	1.0	μA
Turn-On Time	C <sub>OUT</sub> = 1 μF, From assertion of V <sub>EN</sub> to V <sub>OUT</sub> = 98% V <sub>OUT(NOM)</sub> , V <sub>OUT(NOM)</sub> = 1.05 V	t <sub>ON</sub>		150		μs
Power Supply Rejection Ratio	V <sub>IN</sub> to V <sub>OUT</sub> , f = 1 kHz, I <sub>OUT</sub> = 300 mA, V <sub>IN</sub> ≥ V <sub>OUT</sub> + 0.5 V	PSRR(V <sub>IN</sub> )		65		dB
	V <sub>BIAS</sub> to V <sub>OUT</sub> , f = 1 kHz, I <sub>OUT</sub> = 300 mA, V <sub>IN</sub> ≥ V <sub>OUT</sub> + 0.5 V	PSRR(V <sub>BIAS</sub> )		80		
Output Noise Voltage	V <sub>IN</sub> = V <sub>OUT</sub> + 0.5 V, V <sub>OUT(NOM)</sub> = 1.05 V, f = 10 Hz to 100 kHz	V <sub>N</sub>		40		μV <sub>RMS</sub>
Thermal Shutdown Threshold	Temperature increasing			160		°C
	Temperature decreasing			140		
Output Discharge Pull-Down	V <sub>EN</sub> ≤ 0.4 V, V <sub>OUT</sub> = 0.5 V, NCP130A options only	R <sub>DISCH</sub>		150		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Effective capacitance, including the effect of DC bias, tolerance and temperature. See the Application Information section for more information.
- Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at T<sub>A</sub> = 25°C. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
- Dropout voltage is characterized when V<sub>OUT</sub> falls 3% below V<sub>OUT(NOM)</sub>.

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## APPLICATIONS INFORMATION

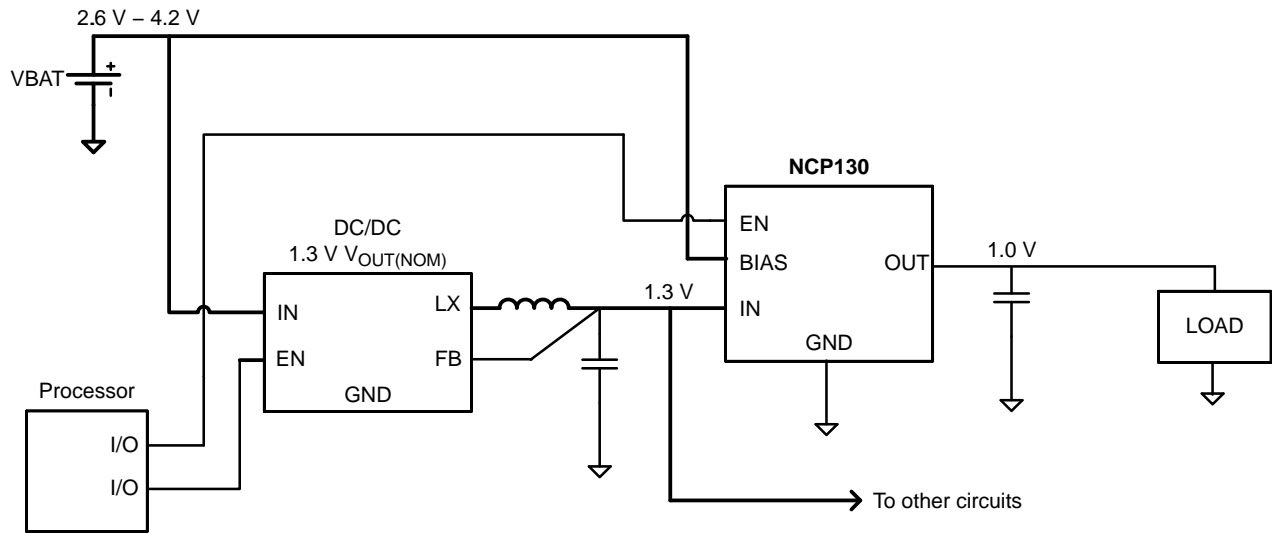


Figure 3. Typical Application: Low-Voltage Post-Regulator with ON/OFF functionality

TYPICAL CHARACTERISTICS

At  $T_J = +25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.3\text{ V}$ ,  $V_{BIAS} = 2.7\text{ V}$ ,  $V_{EN} = V_{BIAS}$ ,  $V_{OUT(NOM)} = 1.05\text{ V}$ ,  $I_{OUT} = 300\text{ mA}$ ,  $C_{IN} = 1\ \mu\text{F}$ ,  $C_{BIAS} = 0.1\ \mu\text{F}$ , and  $C_{OUT} = 1\ \mu\text{F}$  (effective capacitance), unless otherwise noted.

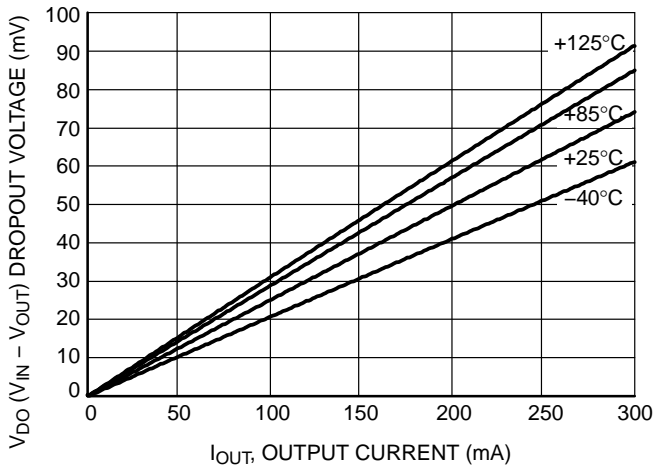


Figure 4.  $V_{IN}$  Dropout Voltage vs.  $I_{OUT}$  and Temperature  $T_J$

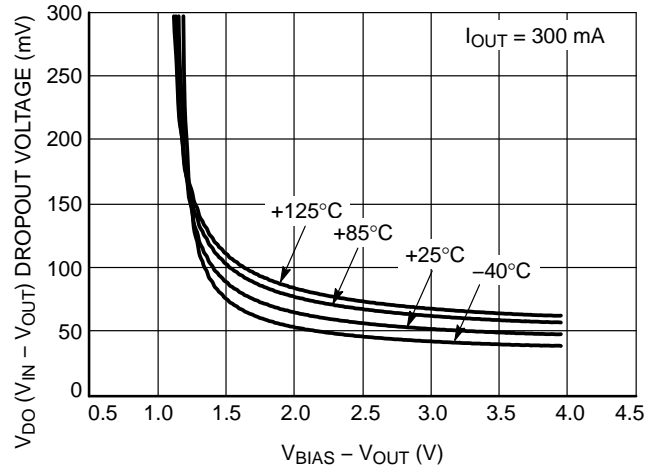


Figure 5.  $V_{IN}$  Dropout Voltage vs.  $(V_{BIAS} - V_{OUT})$  and Temperature  $T_J$

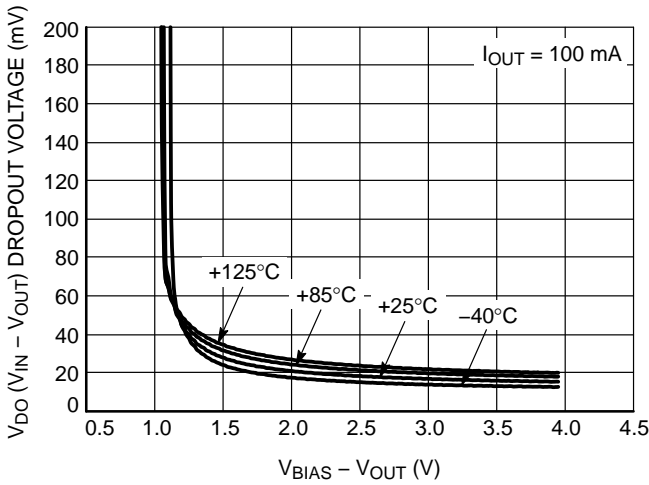


Figure 6.  $V_{IN}$  Dropout Voltage vs.  $(V_{BIAS} - V_{OUT})$  and Temperature  $T_J$

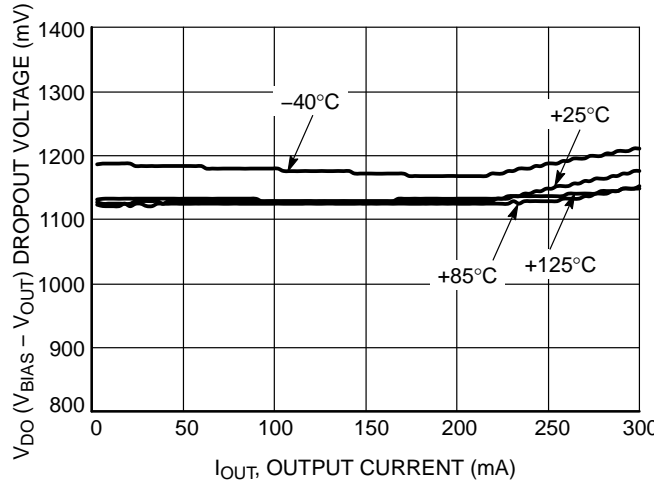


Figure 7.  $V_{BIAS}$  Dropout Voltage vs.  $I_{OUT}$  and Temperature  $T_J$

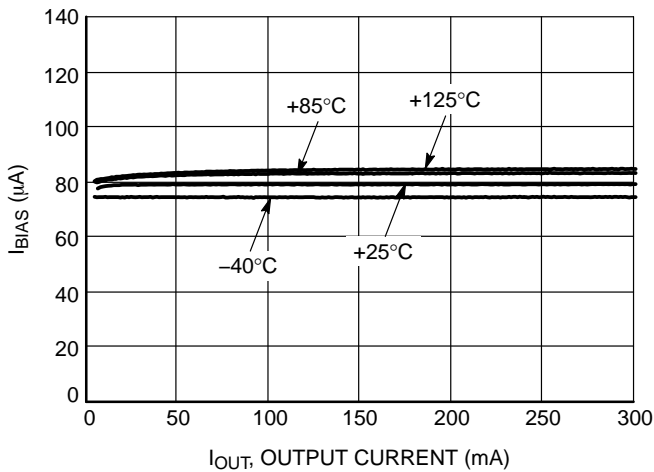


Figure 8. BIAS Pin Current vs.  $I_{OUT}$  and Temperature  $T_J$

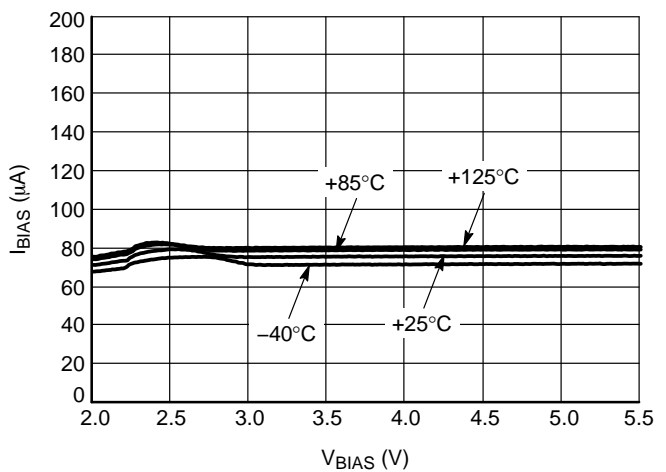


Figure 9. BIAS Pin Current vs.  $V_{BIAS}$  and Temperature  $T_J$

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## TYPICAL CHARACTERISTICS

At  $T_J = +25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.3\text{ V}$ ,  $V_{BIAS} = 2.7\text{ V}$ ,  $V_{EN} = V_{BIAS}$ ,  $V_{OUT(NOM)} = 1.05\text{ V}$ ,  $I_{OUT} = 300\text{ mA}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{BIAS} = 0.1\text{ }\mu\text{F}$ , and  $C_{OUT} = 1\text{ }\mu\text{F}$  (effective capacitance), unless otherwise noted.

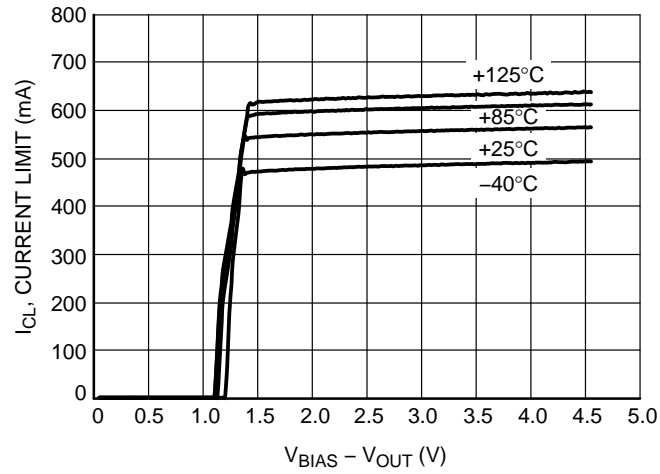


Figure 10. Current Limit vs.  $(V_{BIAS} - V_{OUT})$

## APPLICATIONS INFORMATION

The NCP130 dual-rail very low dropout voltage regulator is using NMOS pass transistor for output voltage regulation from  $V_{IN}$  voltage. All the low current internal control circuitry is powered from the  $V_{BIAS}$  voltage.

The use of an NMOS pass transistor offers several advantages in applications. Unlike a PMOS topology devices, the output capacitor has reduced impact on loop stability.  $V_{IN}$  to  $V_{OUT}$  operating voltage difference can be very low compared with standard PMOS regulators in very low  $V_{IN}$  applications.

The NCP130 offers smooth monotonic start-up. The controlled voltage rising limits the inrush current.

The Enable (EN) input is equipped with internal hysteresis.

NCP130 is a Fixed Voltage linear regulator.

### Dropout Voltage

Because of two power supply inputs  $V_{IN}$  and  $V_{BIAS}$  and one  $V_{OUT}$  regulator output, there are two Dropout voltages specified.

The first, the  $V_{IN}$  Dropout voltage is the voltage difference ( $V_{IN} - V_{OUT}$ ) when  $V_{OUT}$  starts to decrease by percents specified in the Electrical Characteristics table.  $V_{BIAS}$  is high enough, specific value is published in the Electrical Characteristics table.

The second,  $V_{BIAS}$  dropout voltage is the voltage difference ( $V_{BIAS} - V_{OUT}$ ) when  $V_{IN}$  and  $V_{BIAS}$  pins are joined together and  $V_{OUT}$  starts to decrease.

### Input and Output Capacitors

The device is designed to be stable for ceramic output capacitors with Effective capacitance in the range from 1  $\mu\text{F}$  to 10  $\mu\text{F}$ . The device is also stable with multiple capacitors in parallel, having the total effective capacitance in the specified range.

In applications where no low input supplies impedance available (PCB inductance in  $V_{IN}$  and/or  $V_{BIAS}$  inputs as example), the recommended  $C_{IN} = 1 \mu\text{F}$  and  $C_{BIAS} = 0.1 \mu\text{F}$  or greater. Ceramic capacitors are recommended. For the best performance all the capacitors should be connected to the NCP130 respective pins directly in the device PCB copper layer, not through vias having not negligible impedance.

When using small ceramic capacitor, their capacitance is not constant but varies with applied DC biasing voltage, temperature and tolerance. The effective capacitance can be much lower than their nominal capacitance value, most importantly in negative temperatures and higher LDO output voltages. That is why the recommended Output capacitor capacitance value is specified as Effective value in the specific application conditions.

### Enable Operation

The enable pin will turn the regulator on or off. The threshold limits are covered in the electrical characteristics table in this data sheet. If the enable function is not to be used then the pin should be connected to  $V_{IN}$  or  $V_{BIAS}$ .

### Current Limitation

The internal Current Limitation circuitry allows the device to supply the full nominal current and surges but protects the device against Current Overload or Short.

### Thermal Protection

Internal thermal shutdown (TSD) circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When TSD activated, the regulator output turns off. When cooling down under the low temperature threshold, device output is activated again. This TSD feature is provided to prevent failures from accidental overheating.

# NCP130

## ORDERING INFORMATION

Device	Nominal Output Voltage	Marking	Marking Rotation	Option	Package	Shipping†
NCP130AMX080TCG	0.80 V	Q	180°	Output Active Discharge	XDFN6 (Pb-Free)	3000 / Tape & Reel
NCP130AMX090TCG	0.90 V	EA	No rotation			
NCP130AMX100TCG	1.00 V	EC	No rotation			
NCP130AMX105TCG	1.05 V	R	180°			
NCP130AMX110TCG	1.10 V	T	180°			
NCP130AMX115TCG	1.15 V	V	180°			
NCP130AMX120TCG	1.20 V	Y	180°			
NCP130AMX150TCG	1.50 V	2	180°			
NCP130AMX170TCG	1.70 V	ED	No rotation			
NCP130AMX180TCG	1.80 V	3	180°			
NCP130AMX210TCG	2.10 V	4	180°			
NCP130BMX080TCG	0.80 V	Q	270°	Non-Active Discharge		
NCP130BMX090TCG	0.90 V	HA	No rotation			
NCP130BMX100TCG	1.00 V	HC	No rotation			
NCP130BMX105TCG	1.05 V	R	270°			
NCP130BMX110TCG	1.10 V	T	270°			
NCP130BMX115TCG	1.15 V	V	270°			
NCP130BMX120TCG	1.20 V	Y	270°			
NCP130BMX150TCG	1.50 V	2	270°			
NCP130BMX170TCG	1.70 V	HD	No rotation			
NCP130BMX180TCG	1.80 V	3	270°			
NCP130BMX210TCG	2.10 V	4	270°			

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

To order other package and voltage variants, please contact your ON sales representative



# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

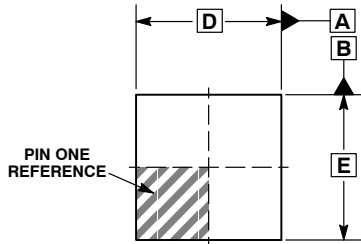
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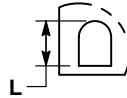
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**XDFN6 1.20x1.20, 0.40P**  
CASE 711AT  
ISSUE C

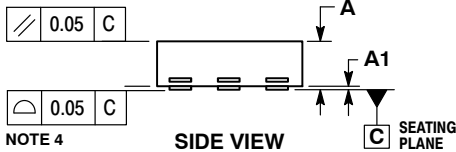
DATE 04 DEC 2015



TOP VIEW

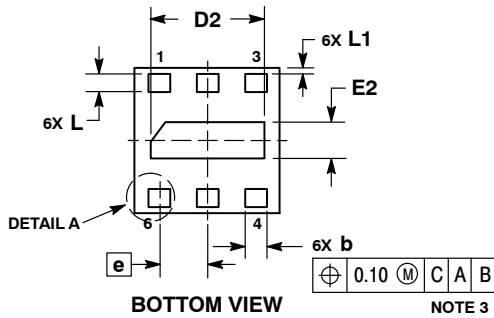


DETAIL A  
OPTIONAL  
CONSTRUCTION



SIDE VIEW

NOTE 4



BOTTOM VIEW

NOTE 3

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO THE PLATED TERMINALS.
4. COPLANARITY APPLIES TO THE PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN	TYP	MAX
A	0.30	0.37	0.45
A1	0.00	0.03	0.05
b	0.13	0.18	0.23
D	1.15	1.20	1.25
D2	0.84	0.94	1.04
E	1.15	1.20	1.25
E2	0.20	0.30	0.40
e	0.40 BSC		
L	0.15	0.20	0.25
L1	0.00	0.05	0.10

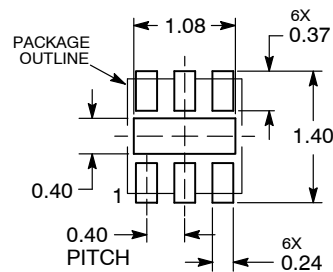
**GENERIC MARKING DIAGRAM\***



XX = Specific Device Code  
M = Date Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

**RECOMMENDED MOUNTING FOOTPRINT\***



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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<b>DESCRIPTION:</b>	<b>XDFN6, 1.20 X 1.20, 0.40P</b>	<b>PAGE 1 OF 1</b>

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