NCP1532GEVB

NCP1532 Dual Output Step-down Converter Evaluation Board User's Manual

2.25 MHz High−efficiency, Out of Phase Operation, Low Quiescent Current, Source up to 1.6 A Evaluation Board

ON Semiconductor®

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EVAL BOARD USER'S MANUAL

OVERVIEW

The NCP1532 dual step down DCDC converter is a monolithic integrated circuit dedicated to supply core and I/O voltages of new multimedia design in portable applications powered from 1−cell Li−ion or 3 cell Alkaline / NiCd / NiMH batteries.

Both channels are externally adjustable from 0.9 V to 3.3 V and can source totally up to 1.6 A, 1.0 A maximum per channel. Converters are running at 2.25 MHz switching frequency which reduces component size by allowing the use of small inductor (down to 1 μH) and capacitors and operates 180° out of phase to reduce large amount of current demand on the battery. Automatic switching PWM/PFM mode and synchronous rectification offer improved system efficiency. The device can also operate into fixed frequency PWM mode for low noise applications where low ripple and good load transients are required.

Additional features include integrated soft−start, cycle−by−cycle current limit and thermal shutdown protection. The device can also be synchronized to an external clock signal in the range of 2.25 MHz.

The NCP1532 is available in a space saving, ultra low profile 3x3 x 0.55 mm 10 pin _DFN package.

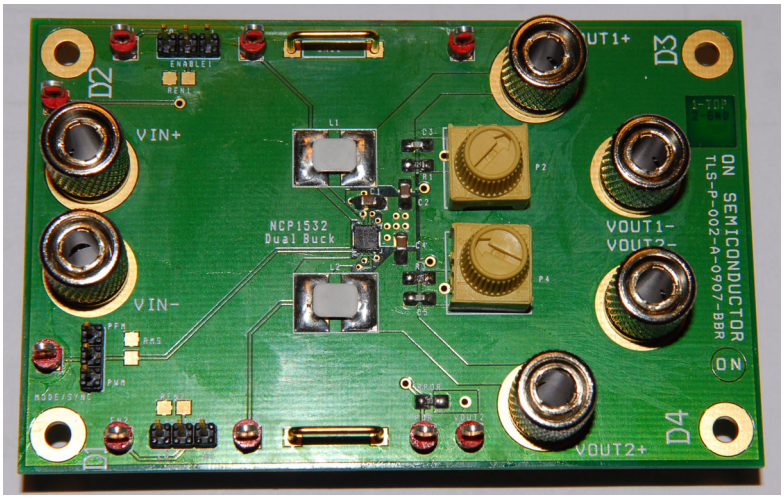

Figure 1. Board Picture

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Minimum Voltage All Pins	V_{min}	−0.3	V
Maximum Voltage All Pins (Note 1)	V_{max}	7.0	V
Maximum Voltage EN1, EN2, MODE	V_{max}	VIN + 0.3	V
Thermal Resistance Junction to Air (UDFN10 Package) Thermal Resistance Using Recommended Board Layout (Note 8)	$R_{\theta JA}$	200 40	°C/W
Operating Ambient Temperature Range (Notes 6 and 7)	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−55 to 150	°C
Junction Operating Temperature (Notes 6 and 7)	T_J	−40 to 150	°C
Latch−up current maximum rating Ta = 85°C (Note 4) other pins	Lu	±100	mA
ESD Withstand Voltage (Note 3) Human Body Model Machine Model	V_{esd}	 2.0 200	 kV V
Moisture Sensitivity Level (Note 5)	MSL	1	per IPC

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T_A = 25°C
2. According JEDEC standard JESD22−A108B
3. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) per JEDEC standard: JESD22−A114
   Machine Model (MM) per JEDEC standard: JESD22−A115
4. Latchup current maximum rating per JEDEC standard: JESD78.
5. JEDEC Standard: J−STD−020A.
6. In applications with high power dissipation (low V_{IN}, high I_{OUT}), special care must be paid to thermal dissipation issues. Board design considerations − thermal dissipation vias, traces or planes and PCB material − can significantly improve junction to air thermal resistance $R_{\theta JA}$ (for more information, see design and layout consideration section). Environmental conditions such as ambient temperature Ta brings thermal limitation on maximum power dissipation allowed.
   The following formula gives calculation of maximum ambient temperature allowed by the application: $T_{A(max)} = T_{J(max)} - (R_{\theta JA} \times Pd)$
   Where
   T_J is the junction temperature,
   Pd is the maximum power dissipated by the device (worst case of the application), and $R_{\theta JA}$ is the junction−to−ambient thermal resistance.
7. To prevent permanent thermal damages, this device include a thermal shutdown which engages at 180°C (typical).
8. Board recommended UDFN10 layout is described in Layout Considerations section.

ELECTRICAL CHARACTERISTICS

For Electrical Characteristic, please report to our NCP1532 datasheet available on our website.

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Table 1. BOARD CONNECTIONS

Symbol	Switch Descriptions
INPUT POWER	
VIN+	This is the positive connection for power supply.
VIN−	This is the return connection for the power supply.
GND1, GND2	Ground clip.
SETUP	
ENABLE1	To enable the buck converter 1, connect a shorting jumper between ENABLE−1 and ENABLE1−2. To disable the buck converter 1, connect a shorting jumper between ENABLE1−3 and ENABLE1−2. Do not let this pin floating.
ENABLE2	To enable the buck converter 2, connect a shorting jumper between ENABLE2−1 and ENABLE2−2. To disable the buck converter 2, connect a shorting jumper between ENABLE2−3 and ENABLE2−2. Do not let this pin floating.
MODE/SYNC	To run the regulator in automatic switching PFM/PWM, use a jumper to connect the MODE/SYNC−2 to the ground (PFM). To run the converter in PWM mode only, use a jumper to connect the MODE/SYNC−2 to the high level (PWM). Always connect this selector to a mode. Following rule is being used: “0”: Eco mode, automatic switching PFM/PWM. “1”: Low noise, forced PWM mode. “CLK”: External synchronization, forced PWM mode, 0° in phase.
OUTPUT POWER	
VOUT1+	This is the positive connection of the output voltage for the buck 1.
VOUT1−	This is the return connection of the output voltage for the buck 1.
VOUT2+	This is the positive connection of the output voltage for the buck 2.
VOUT2−	This is the return connection of the output voltage for the buck 2.
TEST POINT	
TPVIN	This is the test point of the input voltage.
TPEN1	This is the test point of the enable pin for the buck 1.
TPEN2	This is the test point of the enable pin for the buck 2.
TPSW1	This is the test point of the inductor voltage for the buck 1.
TPSW2	This is the test point of the inductor voltage for the buck 2.
TPVOUT1	This is the test point of the output voltage for the buck 1.
TPVOUT2	This is the test point of the output voltage for the buck 2.
TPMODE/SYNC	This is the test point of the mode selection.
TPPOR	This is the test point of the Power On Reset. This is an open drain output. This output is shutting down when each output voltages are less than 90% of their nominal values and goes high after 120 ms when active outputs are within regulation.

BOARD SCHEMATIC

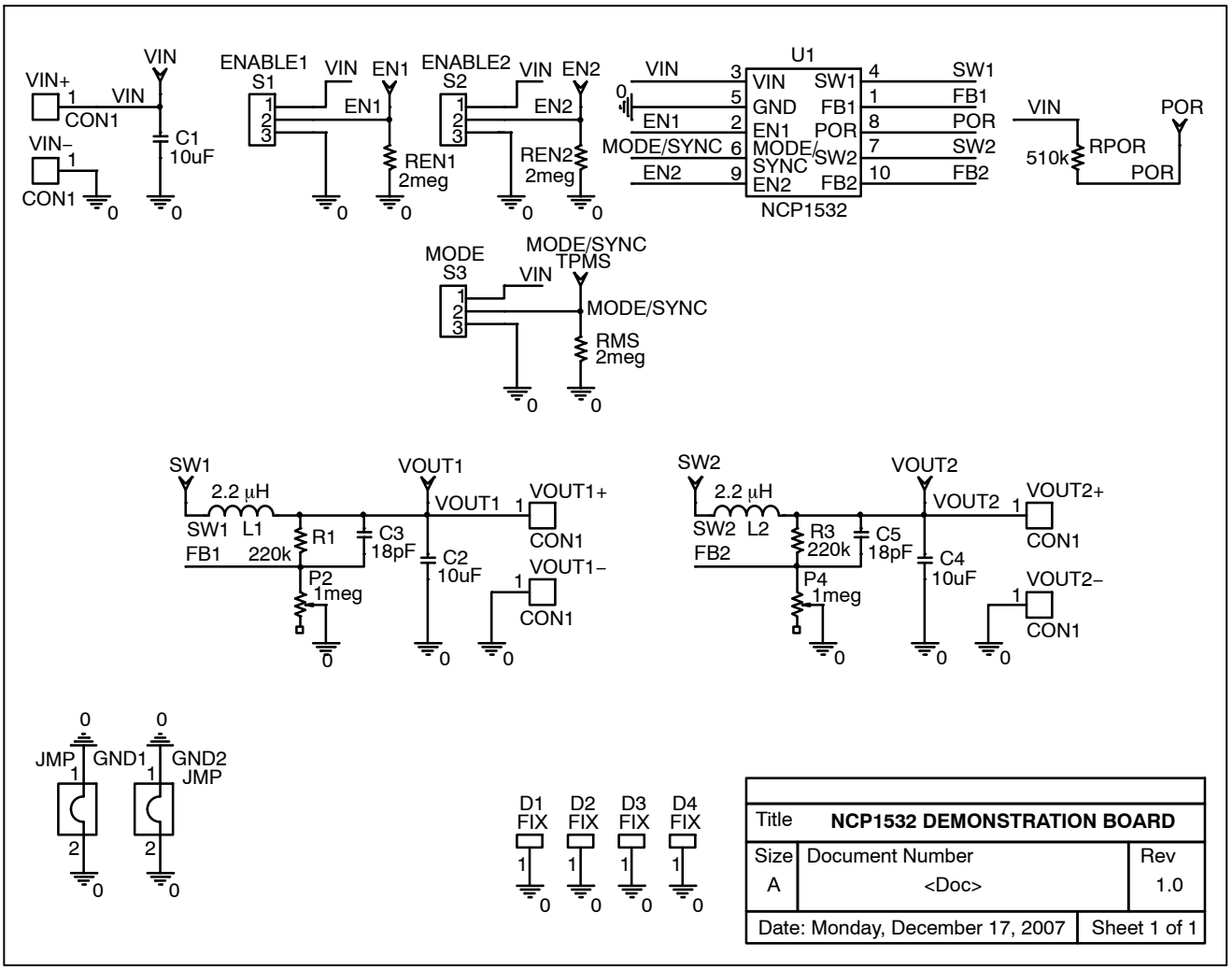


Figure 2. Board Schematic

Test Procedure

Equipment needed

- Power Supply
- Digital Volt Meter
- Digital Amp Meter

Test

1. Jumpers ENABLE1 and ENABLE2 should be closed to GND (Low).
2. Connect the MODE jumper to PFM (GND).
3. Set the power supply to 3.6 V and the current limit of at least 1.5 A.
4. Connect Vin+ to power supply and Vin− to ground. The DC current measurement on Vin+ line should be around 0.3 μA.
5. Switch the ENABLE1 connector to High (Power).
6. Modify P2 potentiometer to get Vout1 to 1.2 V. Output voltage value is defined by: Vout = 0.6 x (1 + R1/R2). Verify that Vout2 = 0 V.
7. The DC current measurement on Vin+ line should be around 45 μA. The part operates in PFM mode for Vout1:

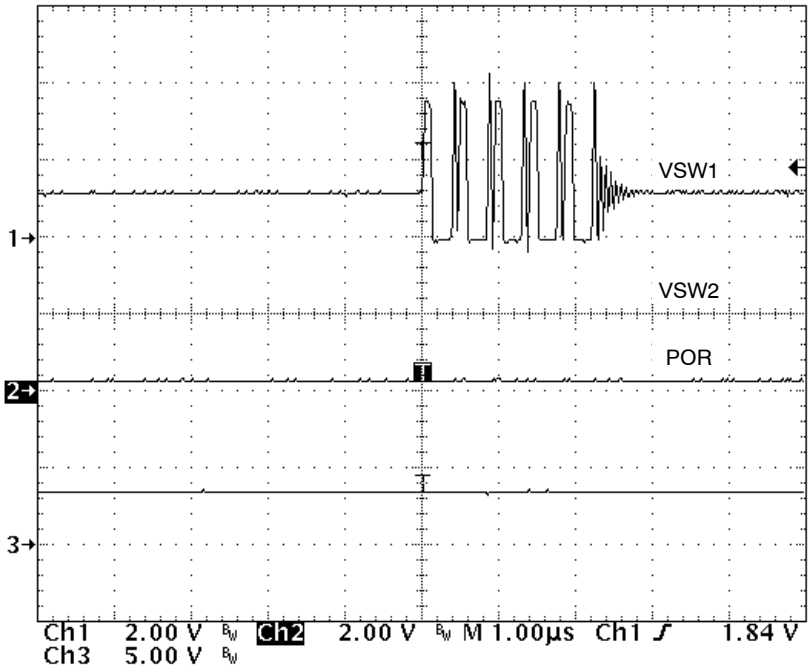


Figure 3. VSW1 and VSW2 in PFM mode (B1 On & B2 Off)

8. The POR is “on” (“1” logic level).
9. Switch the ENABLE2 connector to High (Power).
10. Modify P4 potentiometer to get Vout1 to 1.2 V. Output voltage value is defined by: Vout = 0.6 x (1 + R3/R4).
11. The DC current measurement on Vin+ line should be around 60 μA. The part operates in PFM mode for Vout1 & Vout2:

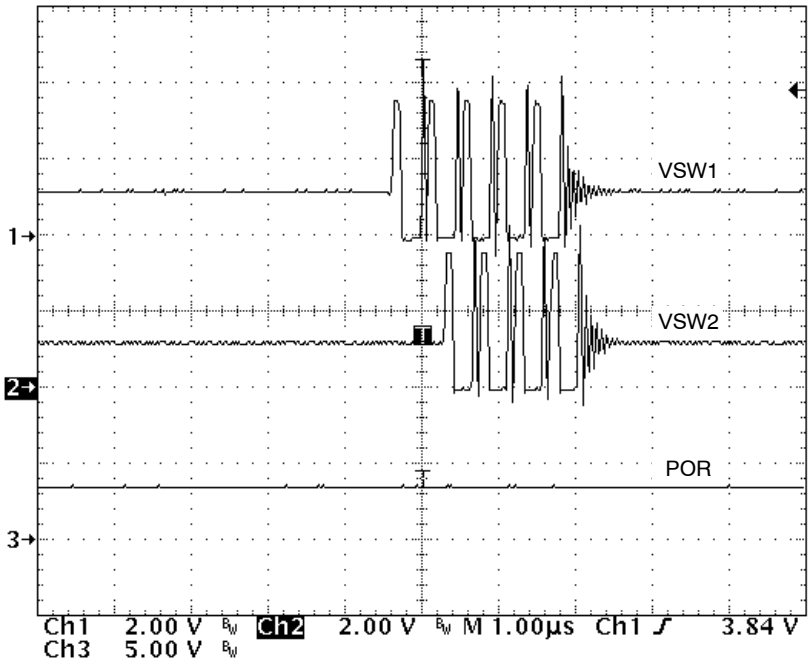


Figure 4. VSW1 and VSW2 in PFM mode (B1 & B2 On)

12. The POR is “on” (“1” logic level).
13. Connect the MODE jumper to PWM (Power).
14. The DC current measurement on Vin+ line should be around **6.3** mA. The part operates in PWM mode for Vout1 & Vout2:

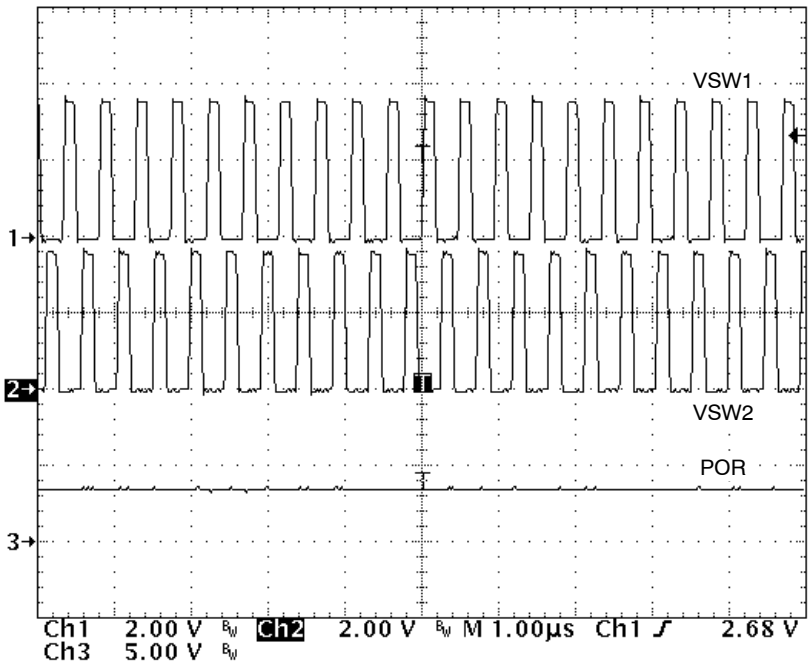


Figure 5. VSW1 and VSW2 in PWM mode (B1 & B2 On)

15. Switch the ENABLE1 connector to Low (GND).
16. The DC current measurement on Vin+ line should be around 3.3 mA. The part operates in PWM mode for Vout1 & Vout2:

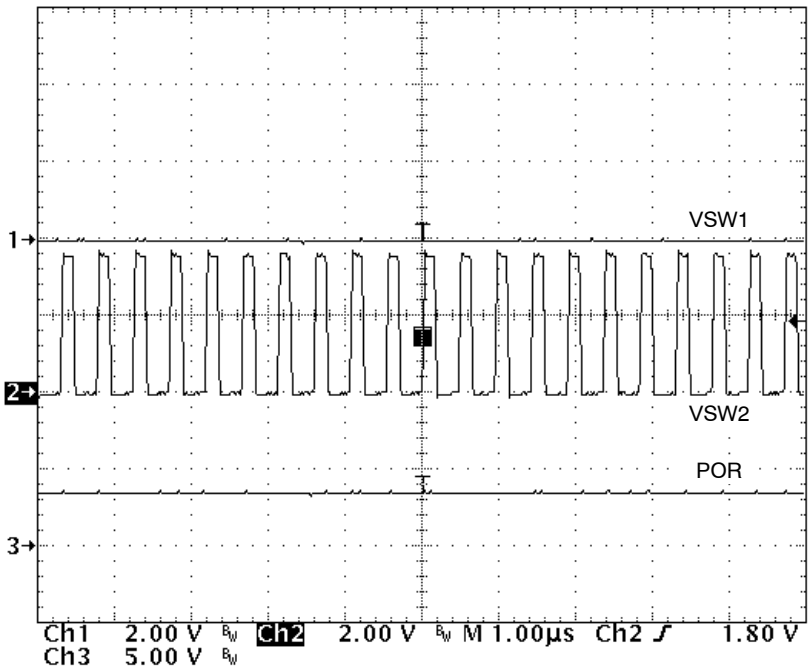


Figure 6. VSW1 and VSW2 in PWM mode (B1 Off & B2 On)

17. Switch the ENABLE2 connector to Low (GND). The DC current measurement on Vp line should be around 7.3 μA.
18. Connect the MODE jumper to PFM (GND). The DC current measurement on Vp line should be back around 0.3 μA.

COMPONENTS SELECTION

Input Capacitor Selection

In PWM operating mode, the input current is pulsating with large switching noise. Using an input bypass capacitor can reduce the peak current transients drawn from the input supply source, thereby reducing switching noise significantly. The capacitance needed for the input bypass capacitor depends on the source impedance of the input supply.

The maximum RMS current occurs at 50% duty cycle with maximum output current, which is IO, max/2.

For NCP1532, a low profile ceramic capacitor of 10 μF should be used for most of the cases. For effective bypass results, the input capacitor should be placed as close as possible to the VIN Pin

Table 2. List of Input Capacitor

Murata	GRM21BR60J106KE19	10 μF
	GRM219R60J106KE19	
Taiyo Yuden	JMK107BJ106MA	10 μF
TDK	C2012X5R0J106KT	10 μF

Output L−C Filter Design Considerations

The NCP1532 is built in 2.25 MHz frequency and uses current mode architecture. The correct selection of the output filter ensures good stability and fast transient response.

Due to the nature of the buck converter, the output L−C filter must be selected to work with internal compensation. For NCP1532, the internal compensation is internally fixed and it is optimized for an output filter of L = 2.2 μH and C_{OUT} = 10 μF.

The corner frequency is given by:

$$f_c = \frac{1}{2\pi\sqrt{L \cdot C_{OUT}}} = \frac{1}{2\pi\sqrt{2.2\ \mu H \cdot 10\ \mu F}} = 34\ kHz \quad \text{(eq. 1)}$$

The device operates with inductance value of 2.2 μH. If the corner frequency is moved, it is recommended to check the loop stability depending of the accepted output ripple voltage and the required output current. Take care to check the loop stability. The phase margin is usually higher than 45°.

Table 3. L−C Filter Example

Inductance (L)	Output capacitor (Cout)
1.0 μH	22 μF
2.2 μH	10 μF
4.7 μH	4.7 μF

Inductor Selection

The inductor parameters directly related to device performances are saturation current and DC resistance and inductance value. The inductor ripple current (ΔI_L) decreases with higher inductance:

$$\Delta I_L = \frac{V_{OUT}}{L \cdot f_{sw}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad \text{(eq. 2)}$$

ΔI_L = Peak to peak inductor ripple current

L = Inductor value

f_{sw} = Switching frequency

The saturation current of the inductor should be rated higher than the maximum load current plus half the ripple current:

$$I_{L(max)} = I_{O(max)} + \frac{\Delta I_L}{2} \quad \text{(eq. 3)}$$

$I_{L(max)}$ = Maximum inductor current

$I_{O(max)}$ = Maximum Output current

The inductor's resistance will factor into the overall efficiency of the converter. For best performances, the DC resistance should be less than 0.3 Ω for good efficiency.

Table 4. List of Inductors

FDK	MIPW3226 series
TDK	VLF3010AT series
	TFC252005 series
Taiyo Yuden	LQ CBL2012
Coil craft	DO1605−T series
	LPO3008

Output Capacitor Selection

Selecting the proper output capacitor is based on the desired output ripple voltage. Ceramic capacitors with low ESR values will have the lowest output ripple voltage and are strongly recommended. The output capacitor requires either an X7R or X5R dielectric.

The output ripple voltage in PWM mode is given by:

$$\Delta V_{OUT} = \Delta I_L \cdot \left(\frac{1}{4 \cdot f_{sw} \cdot C_{OUT}} + ESR\right) \quad \text{(eq. 4)}$$

Table 5. List of Output Capacitors

Murata	GRM188R60J475KE	4.7 μF
	GRM21BR71C475KA	
	GRM188R60OJ106ME	10 μF
Taiyo Yuden	JMK212BY475MG	4.7 μF
	JMK212BJ106MG	10 μF
TDK	C2012X5R0J475KT	4.7 μF
	C1608X5R0J475KT	
	C2012X5R0J106KT	10 μF

Feed−Forward Capacitor Selection

The feed−forward capacitor sets the feedback loop response and is critical to obtain good loop stability. Given that the compensation is internally fixed, an 18 pF or higher ceramic capacitor is needed. Choose a small ceramic capacitor X7R or X5R or COG dielectric.

Table 6. BILL OF MATERIALS

Designator	Qty.	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number
U1	1	IC, Converter, DC/DC	NA	NA	UDFN−10	ON Semiconductor	NCP1532
C1, C2, C4	3	Ceramic capacitor	10 μF, 10 V, X5R	10%	0805	TDK	C2012X5R1A106
C3, C5	2	Ceramic capacitor	18 pF, 50 V, COG	5%	0603	TDK	C1608C0G1H180
R1, R3	2	SMD Resistor	220 k	1%	0603	std	std
RPOR	1	SMD Resistor	510 k	1%	0604	std	std
P2, P4	2	Potentiometer	1 meg	10%		Vishay Spectrol	63M−T607−105
L1, L2	2	Inductor	2,2 μH	20%	1605	Coilcraft	DO1605T−222MLB
VIN, VOUT	6	Connector	NA	NA	NA	Emerson Network Power Connectivity Solutions	111−2223−001
ENABLE1, ENABLE2, MODE	3	3 Pin Jumper Header	NA	NA	2,54 mm	TYCO/AMP Molex / Waldom	5−826629−0 90120−0160
GND1, GND2	2	Jumper for GND	NA	NA	10,16 mm	Harwin Molex / Waldom	D3082−01 90120−0160
EN, SW, MODE/SYNC, POR, VIN, VOUT	9	Test point type 3	NA	NA	ϕ 1,60 mm	Keystone	5010
PCB	1	87 mm x 57 mm x 1.0 mm 4 Layers	NA	NA	NA	Any	TLS−P−002−A−0907−BBR

NOTE: RMS, REN1, REN2: not connected

PCB LAYOUT GUIDELINES

Electrical Layout Considerations

Implementing a high frequency DC−DC converter requires respect of some rules to get a powerful portable application. Good layout is key to prevent switching regulators to generate noise to application and to themselves.

Electrical layout guide lines are:

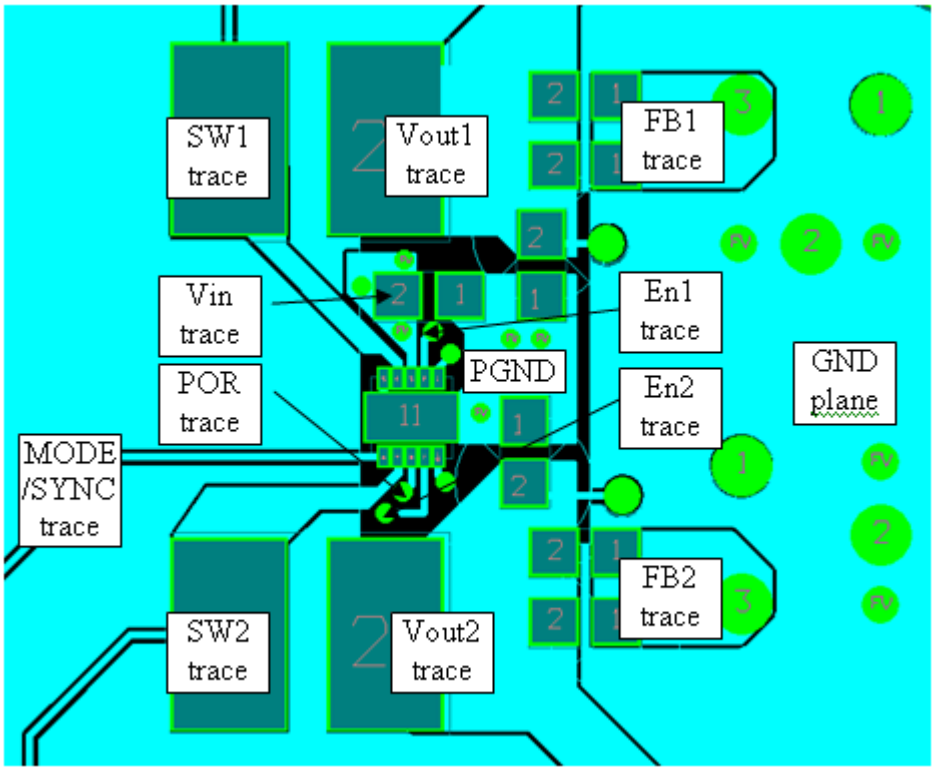
- Use short and large traces when large amount of current is flowing.
- Keep the same ground reference for input and output capacitors to minimize the loop formed by high current path from the battery to the ground plane.
- Isolate feedback pin from the switching pin and the current loop to protect against any external parasitic signal coupling. Add a feed−forward capacitor between VOUT and FB which adds a zero to the loop and participates to the good loop stability. A 18 pF capacitor is recommended to meet compensation requirements. A four layer PCB with a ground plane and a power plane will help NCP1532 noise immunity and loop stability.

Thermal Layout Considerations

High power dissipation in small package leads to thermal consideration such as:

- Enlarge VIN trace and added several vias connected to power plane.
- Connect GND pin to top plane.
- Join top, bottom and each ground plane together using several free vias in order to increase radiator size.

For high ambient temperature and high power dissipation requirements, refer to Notes 7, 8, and 9 to prevent any thermal issue.



PCB LAYOUT

Board Reference: TLS−P−003−A−0907−BBR

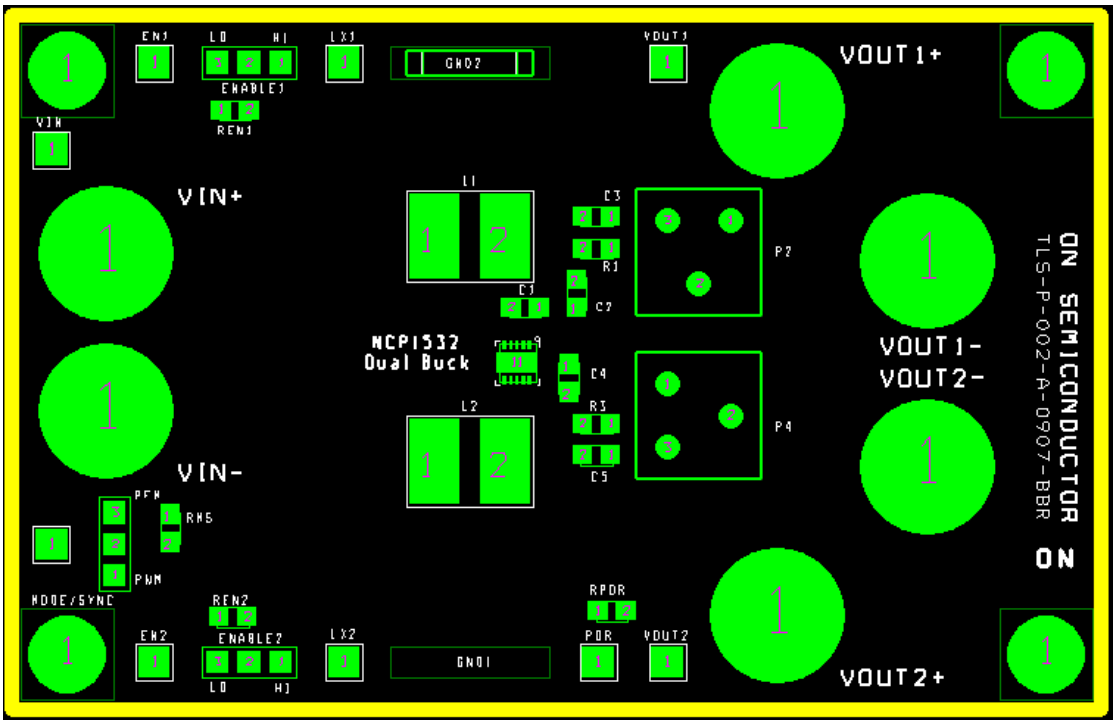


Figure 7. Assembly Layer

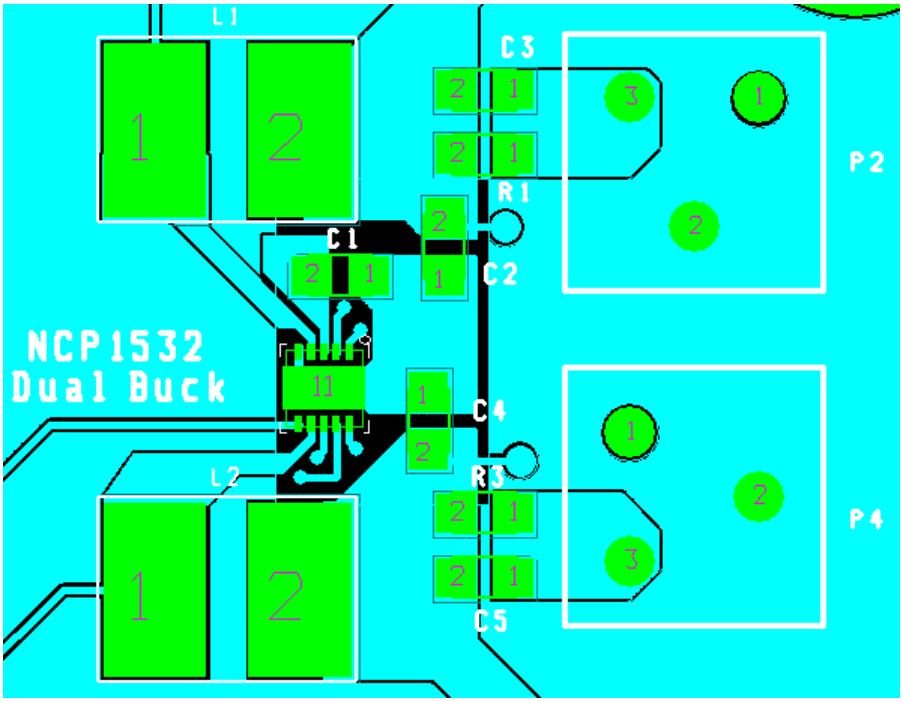


Figure 8. Part Layout

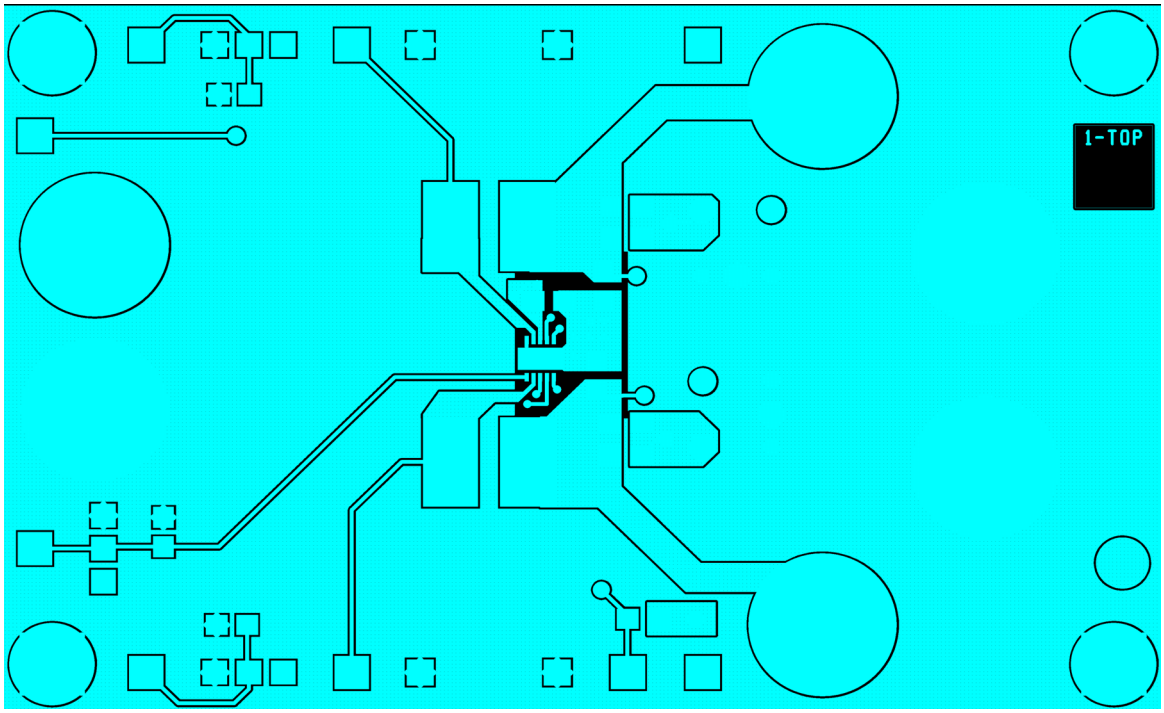


Figure 9. Top Layer Routing

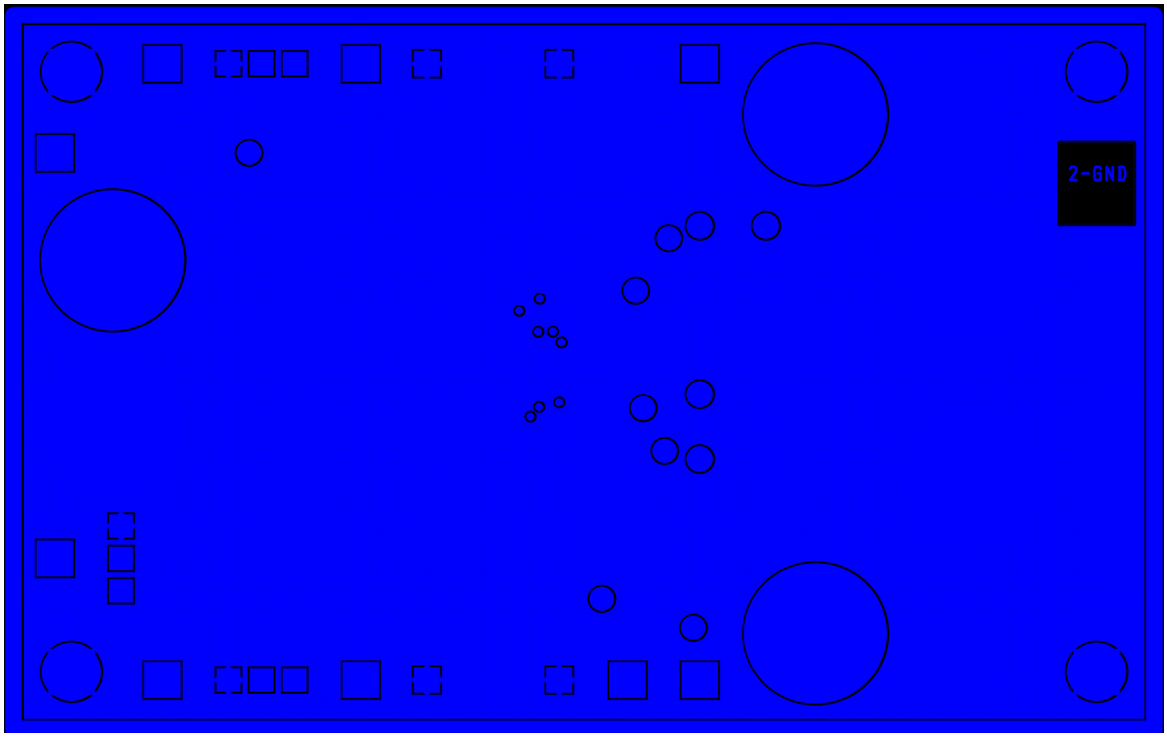


Figure 10. Ground Layer Routing

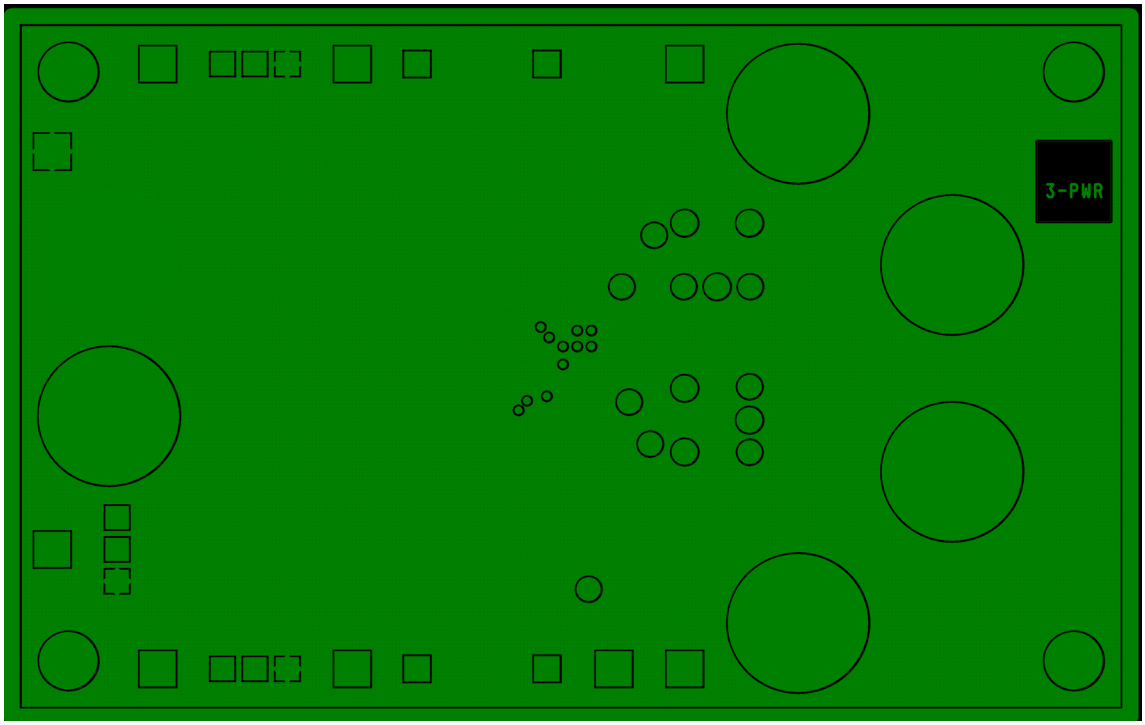


Figure 11. Power Layer Routing

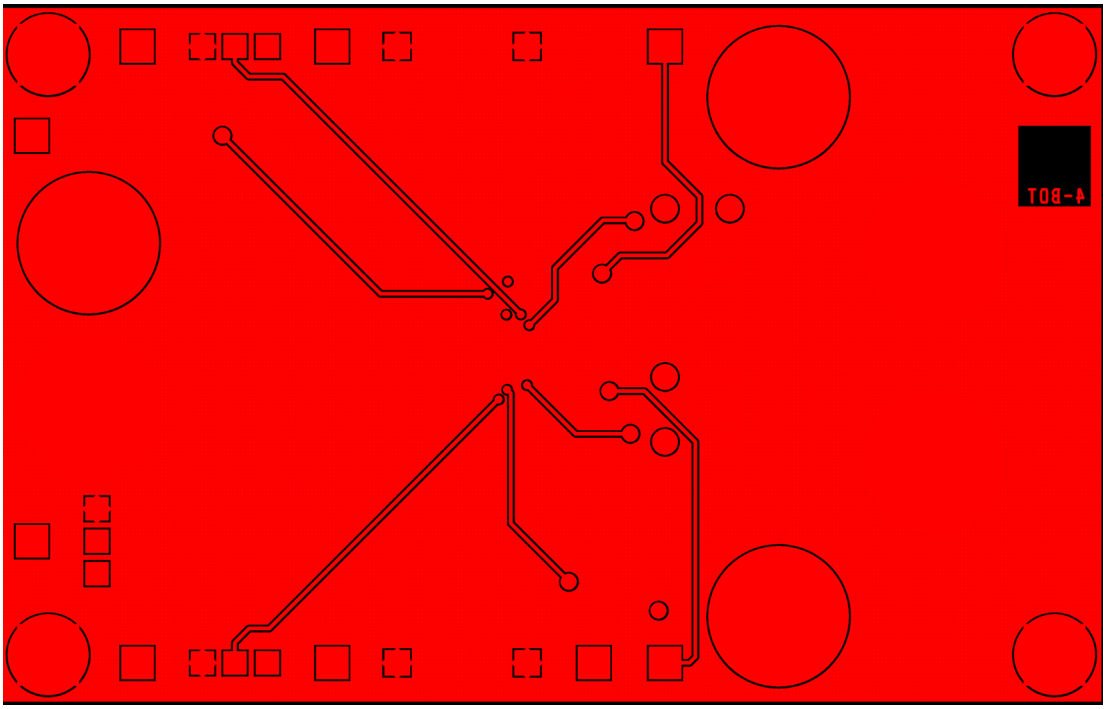


Figure 12. Bottom Layer Routing