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NCP1622GEVB

160-W, Wide Mains, PFC Stage Driven by the NCP1622 Evaluation Board User's Manual.

Rev1.0 February 20th 2017

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EVAL BOARD USER'S MANUAL

Introduction

Housed in a TSOP6 package, the NCP1622 is designed to drive PFC boost stages in so-called Valley Synchronized Frequency Fold-back (VSFF). In this mode, the circuit classically operates in Critical conduction Mode (CrM) when VCTRL pin voltage exceeds a product version programmable voltage level. When VCTRL pin voltage is below this programmable level, the NCP1622 linearly decays the frequency down to about 20 kHz, when the load current is nearly zero. VSFF maximizes the efficiency throughout the load range. Incorporating protection features for rugged operation, it is furthermore ideal in systems where cost-effectiveness, reliability, low stand-by power and high-efficiency are the key requirements. Extremely slim, the NCP1622 evaluation board is designed to be less than 13 mm high. This low-profile PFC Stage is intended to deliver 160 W under a 390-V output voltage from a wide mains input. This is a PFC boost converter as used in flat TVs, high power LED street light power supplies, and all-in-one computer supplies. The evaluation board embeds the NCP1622 AEA-version which is powered by an external V_{CC}. With the help of an external dc source, apply a V_{CC} voltage that exceeds the NCP1622-AEA start-up level (18.2 V max) to ensure the circuit starts operating. The V_{CC} operating range is from 9.5 V up to 30 V.

Table 1 ELECTRICAL SPECIFICATIONS

Description	Value	Units
Input Voltage Range	90-265	V rms
Line Frequency Range	45 to 66	Hz
Maximum Output Power	160	W
Minimum Output Load Current(s)	0	A
Number of Outputs	1	
Nominal Output Voltage	390	V
Maximum Startup Time	< 3	s
No-Load Power (115 V rms)	< 250	mW
Target Efficiency at Full Load (115 V rms)	95	%
Load conditions for efficiency measurements (10%, 20%,..)	10-100	%
Minimum efficiency at 20% load, 115 V rms	93	%
Minimum PF over the line range at full load	95	%
Hold-up time (the output voltage remaining above 300 V)	> 10	ms
Peak to peak low frequency output ripple	< 8	%

Differences between the NCP1622 and NCP1602

The NCP1622 is a spin-off of the NCP1602 and the attached table summarizes all the differences between the two products. The evaluation board of the two products is the same, except for the name printed on it and from the fact that NCP1602 evaluation board has by default the power MOSFET drain voltage used for the ZCD detection as the NCP1622 has by default the auxiliary voltage used for ZCD detection.

	NCP1602			NCP1622		
2-Level Boost Follower	YES			NOT AVAILABLE		
LLINE flag stuck at zero	YES (only when aux winding is used for ZCD)			FIXED		
	min	typ	max	min	typ	max
ICC,start Over consumption	-	-	480µA	-	-	70µA
[*J*] option $t_{ON,max,LL}$	NA	NA	NA	26µs	30µs	34µs
[*K*] option $t_{ON,max,LL}$	NA	NA	NA	26µs	30µs	34µs
[*L*] option $t_{ON,max,LL}$	NA	NA	NA	26µs	30µs	34µs
V_{UVPH}	555mV	612mV	670mV	477mV	530mV	583mV
V_{HL}	1718mV	1801mV	1882mV	1605mV	1690mV	1774mV
V_{LL}	1310mV	1392mV	1474mV	1406mV	1480mV	1554mV

Table 2: Differences between the NCP1622 and NCP1602

THE BOARD

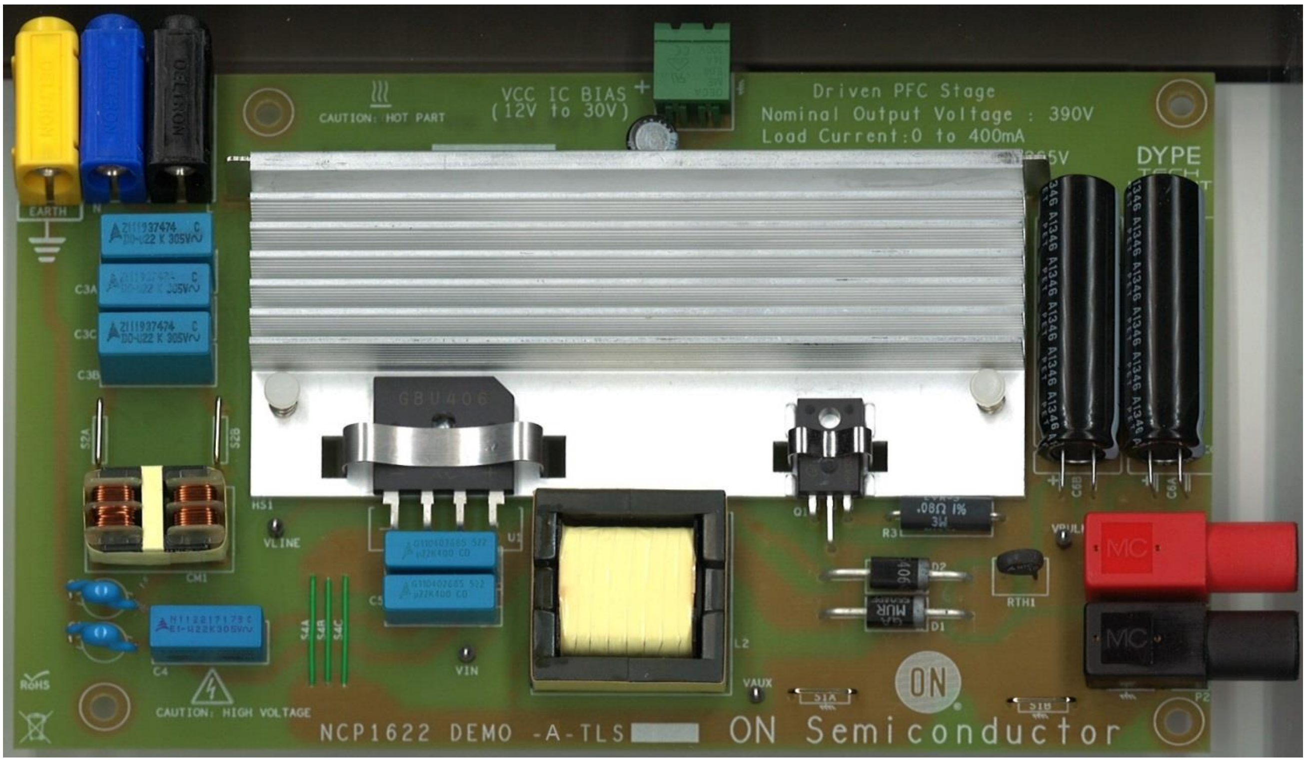


Figure 1. NCP1622 slim board (height < 13mm)

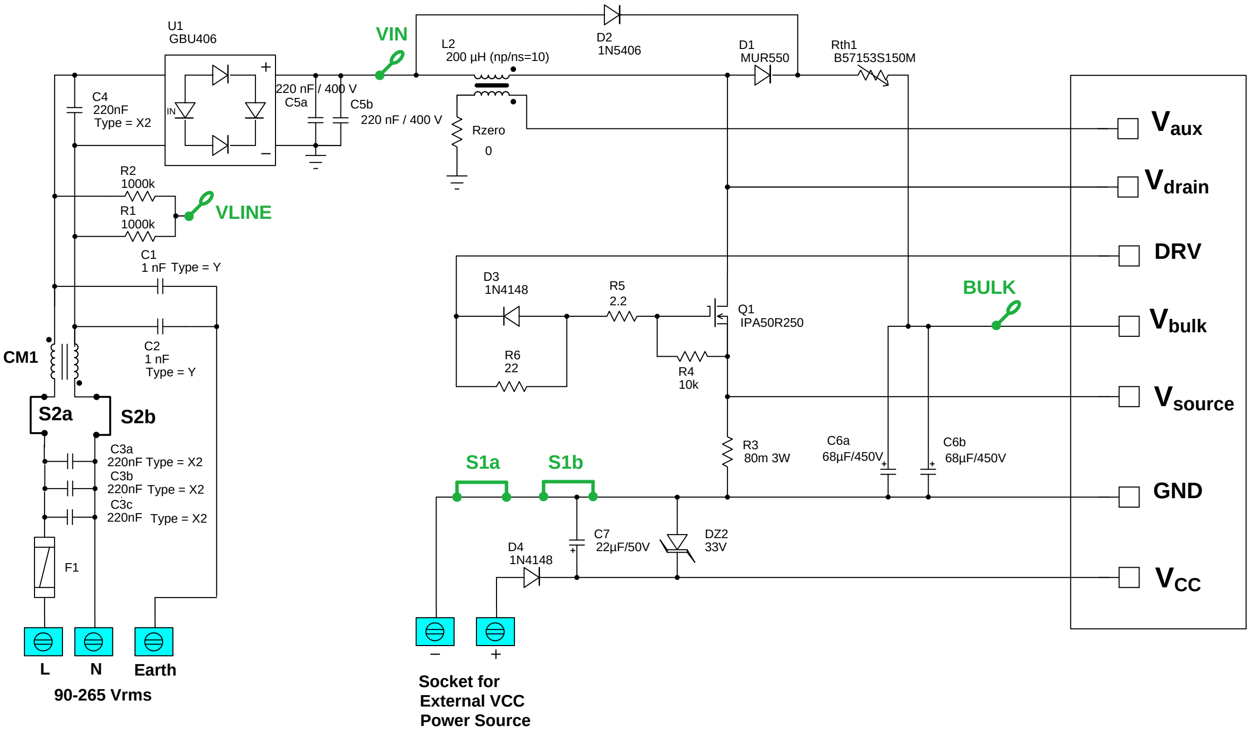


Figure 2 – NCP1622 application schematic – Power section

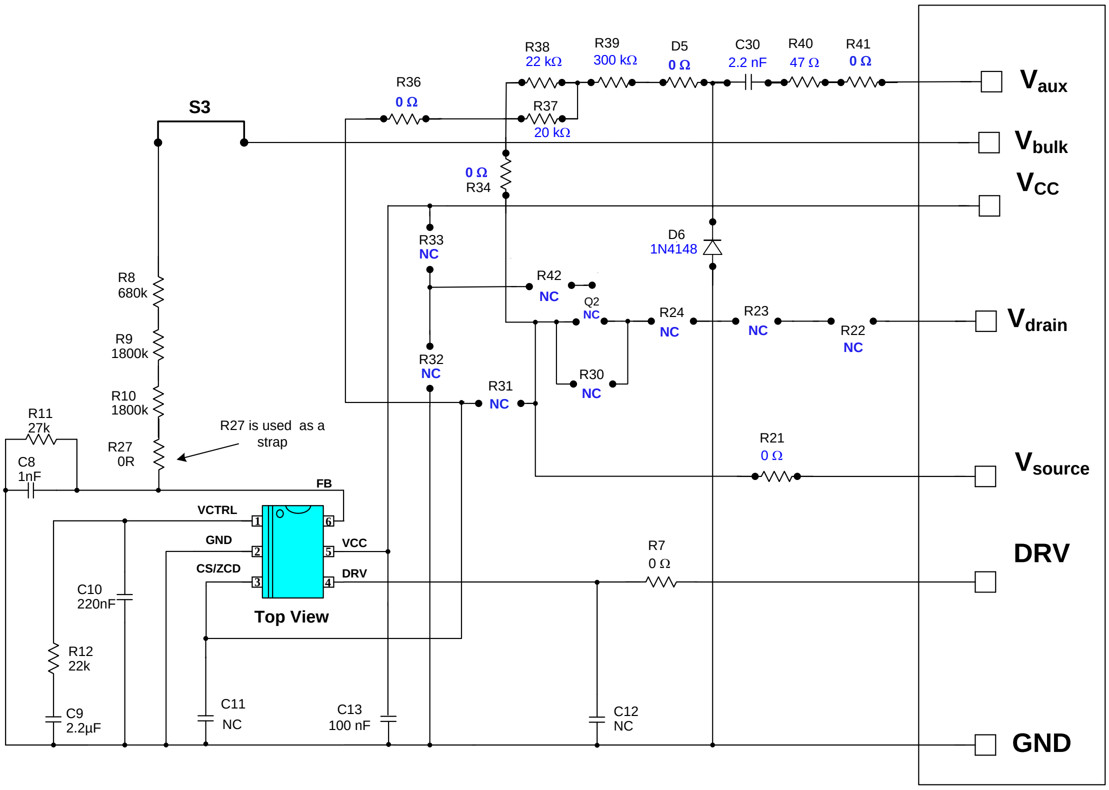


Figure 3 – NCP1622 application schematic: control section (NC means Not Connected)

VSFF Operation

The NCP1622 operates in so called Valley Synchronized Frequency Fold-back (VSFF) where the circuit works in Critical conduction Mode (CrM) when the load current is medium to high (V_{CTRL} pin voltage medium or high). The load current is correlated with the V_{CTRL} pin voltage (see Figure 8). $V_{CTRL} = 4.5$ V corresponds to the maximum current capability which in our case is not reached because we limit the application to 160 W and $V_{CTRL} = 0.5$V corresponds to zero load current. When VCTRL pin voltage (V_{CTRL}) is lower than a preset level, the switching frequency linearly decays to about 20 kHz. VSFF maximizes the efficiency at both nominal and light loads. In particular, stand-by losses are minimized. When VCTRL pin voltage (V_{CTRL}) exceeds $V_{CTRL,DT}$ voltage ($V_{CTRL,DT} = 1.553$ V for the AEA option) , the circuit operates in CrM (typical CrM waveforms are depicted in Figure 4) . If V_{CTRL} is below $V_{CTRL,DT}$, the circuit forces a delay (or dead-time) before re-starting a DRV cycle which is proportional to the difference between $V_{CTRL,DT}$ reference and V_{CTRL} voltage. This mode is called discontinuous conduction mode (DCM) or Frequency Foldback and the main waveforms are depicted in Figure 5. This delay is maximum when V_{CTRL} reached is 0.5-V minimum value. When the 0.5-V V_{CTRL} minimum value is reached, the circuit works in a so-called Static OVP mode (for no SKIP mode options like AEA option used on this board), by skipping cycles based on the difference voltage between V_{CTRL} and 0.5-V. This static OVP mode offers a very low output ripple voltage, unlike the classical SKIP mode of other options. The added dead time starts at the end of the boost inductor demagnetization cycle and ends at the on-time start which is synchronized with the boost inductor zero crossing (valley turn on) event.

In all cases, the circuit turns on in a drain-source voltage valley:

- Classical valley turn on in CrM operation
- At the first valley following the completion of the dead-time generated by the VSFF function to reduce the frequency.

One can also note that the switching frequency being less when the load current is low, the frequency is particularly low at light load, high line. On the other hand, CrM operation being more likely to occur at heavy load, low line.

Refer to the data sheet for a detailed explanation of the VSFF operation and of its implementation in the NCP1622 [2].

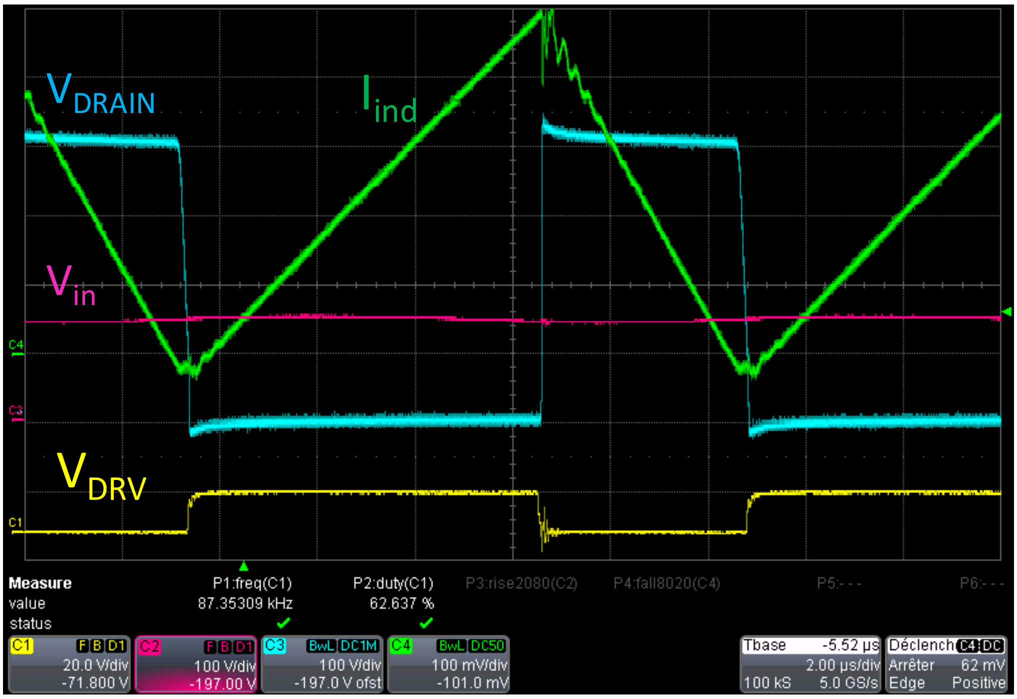


Figure 4. Typical waveforms in CrM @ V_{mains} = 110 V rms, F_{mains} = 60 Hz, I_{load} = 400 mA

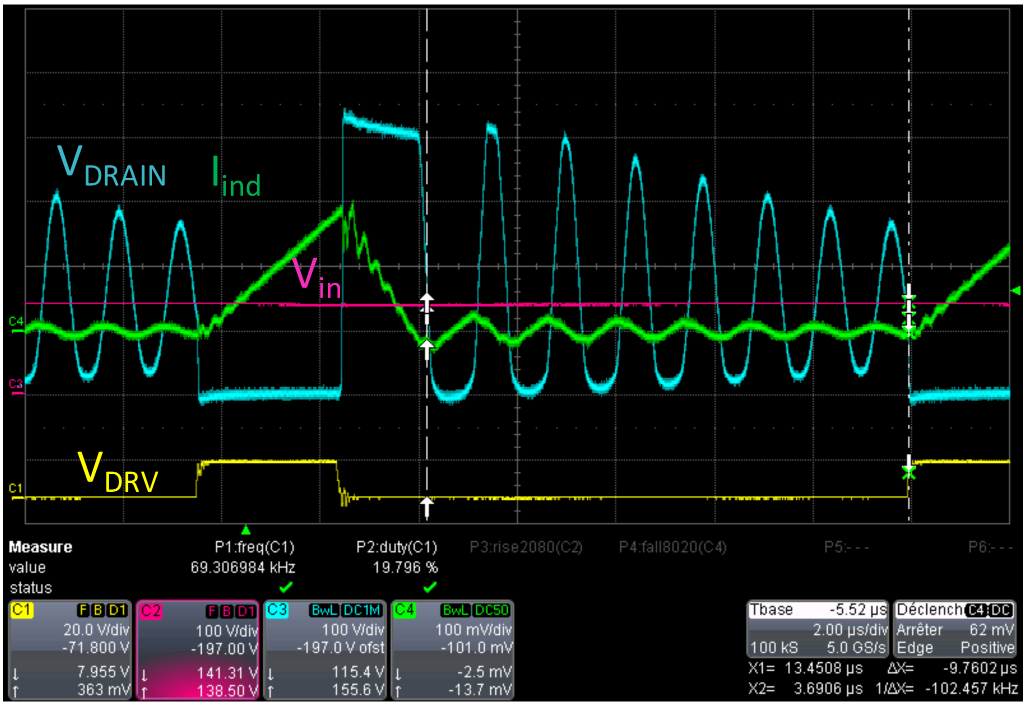


Figure 5. Typical waveforms in DCM @ V_{mains} = 110 V rms, F_{mains} = 60 Hz, I_{load} = 50 mA

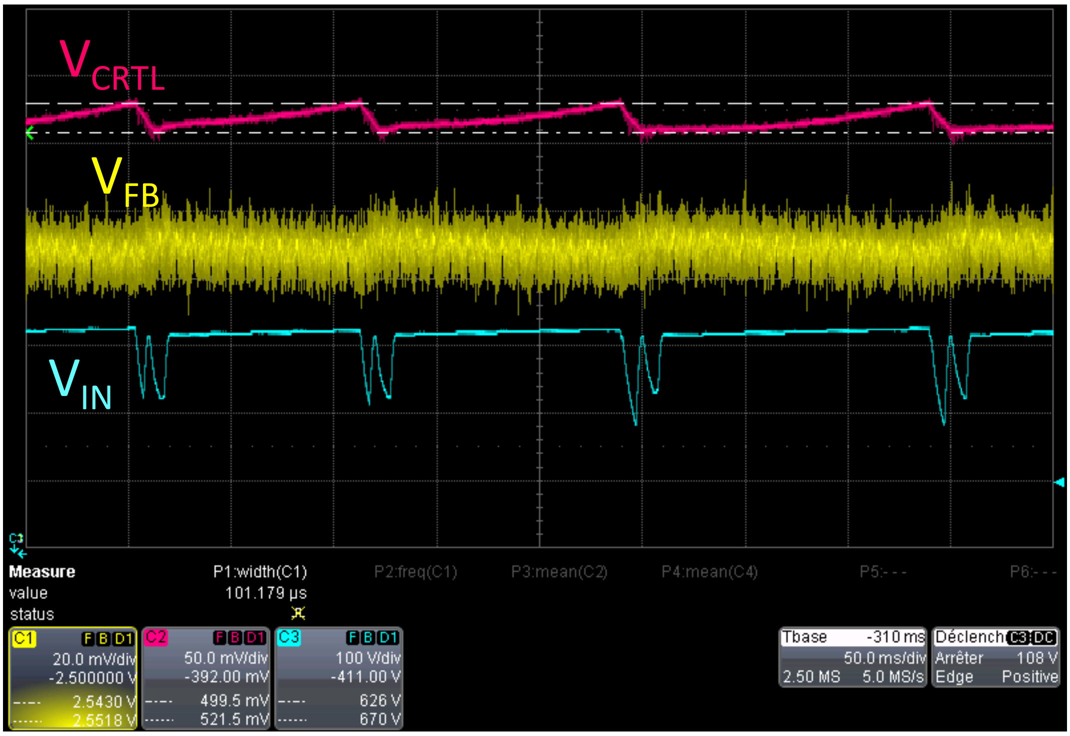
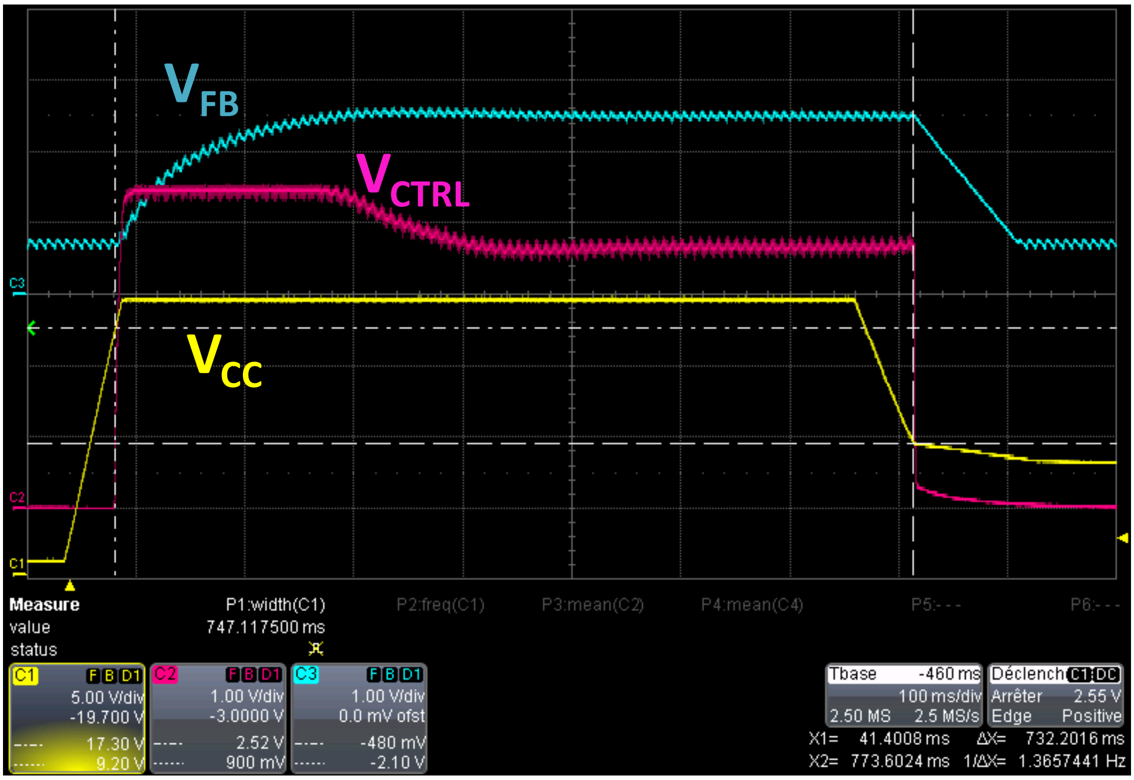


Figure 6. No-load waveforms for option AEA (skip mode disabled) featuring static OVP @V_{mains}=230 V rms



Measure P1:width(C1) P2:freq(C1) P3:mean(C2) P4:mean(C4) P5:- - - P6:- - -
value 747.117500 ms
status

C1 F B D1 5.00 V/div -19.700 V 17.30 V 9.20 V
C2 F B D1 1.00 V/div -3.0000 V 2.52 V 900 mV
C3 F B D1 1.00 V/div 0.0 mV ofst -480 mV -2.10 V

Tbase -460 ms 100 ms/div 2.50 MS 2.5 MS/s
Déclench C1 DC Arrêter 2.55 V Edge Positive
X1= 41.4008 ms ΔX= 732.2016 ms
X2= 773.6024 ms 1/ΔX= 1.3657441 Hz

Figure 7. Startup and stop sequence @ I_{load}=400 mA ; V_{mains}=90 V rms; V_{cc} OFF=>ON=>OFF

V_{mains} (V rms)	@I_{load} = 400 mA	@I_{load} = 300 mA	@I_{load} = 100 mA	@I_{load} = 50 mA	@I_{load} = 0 mA
90	3.77	3.01	1.38	0.96	0.490
110	2.55	2.13	1.02	0.75	0.490
230	1.77	1.42	0.79	0.63	0.490
265	1.35	1.10	0.67	0.57	0.490

Figure 8. V_{CTRL} voltage versus I_{load} & V_{mains}

POWER FACTOR AND EFFICIENCY

The NCP1622 evaluation board embeds a NTC to limit the in-rush current that takes place when the PFC stage is plugged in. The NTC is placed in series with the boost diode. This location is rather optimum in term of efficiency since it is in the in-rush current path at a place where the rms current is less compared to the input side. However, this component still consumes some power. That is why the efficiency is given with a shorted NTC to approximately improve the power efficiency value by 1 percent.

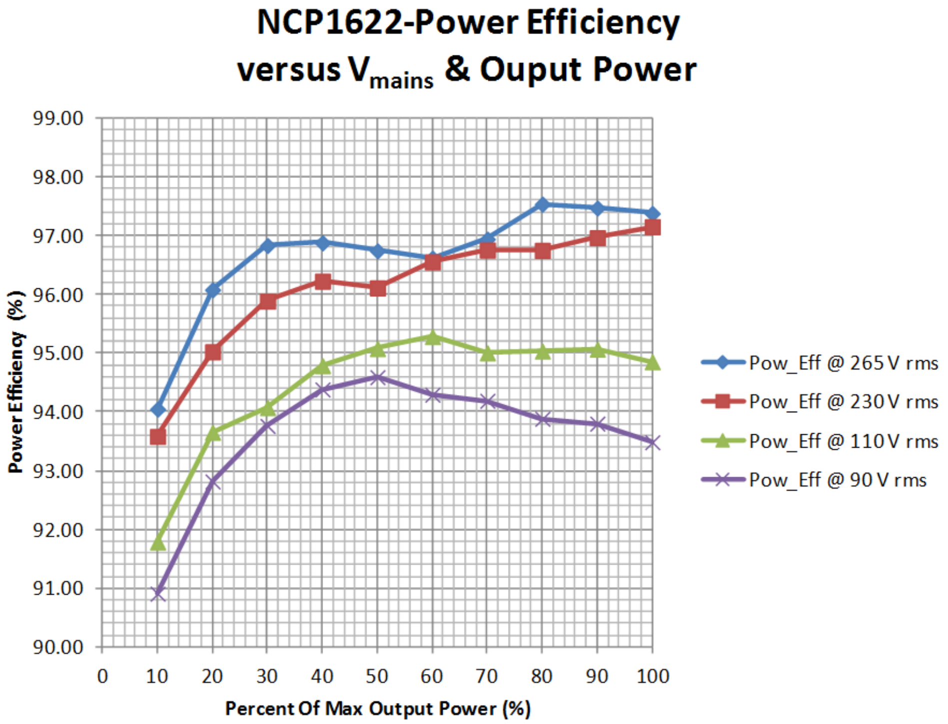


Figure 9 . Evaluation board power efficiency versus output power (NTC is shorted)
100% ouput power corresponds to 160 W

Figure 9 displays the efficiency versus load at different line levels. When considering efficiency versus load, we generaly think of the traditional bell-shaped curves:

- At low line, the efficiency peaks somewhere at a medium load and declines at full load as a result of the conduction losses and at light load due to the switching losses.
- At high line, the conduction losses being less critical, efficiency is maximal at or near the maximum load point and decays when the power demand diminishes because the increasing impact of the switching losses.

Curves of Figure 9 meet this behavior in the right-hand side where our demo-board resembles a traditional CrM PFC stage. In the left-hand side, the efficiency normally drops because of the switching losses until an inflection point where it rises up again as a result of the VSFF operation. As previously stated, VSFF makes the switching frequency decay linearly as a function of V_{CTRL} voltage (load current) when it goes below a preset level.

PF and THD performance have been measured using a CHROMA 66202 Digital Power Meter.

Figure 10 and Figure 11 show that VSFF exhibits very similar PF ratios compared to those obtained with CrM traditional operation. VSFF improves the THD performance at light load. We can see on Figure 11 a 5% decrease of THD value when switching from CrM mode to DCM mode. This behavior is due to the fact that in CrM, close to mains voltage zero crossing, there is a zone of zero mains current which leads to a slight mains current distortion (higher THD). When entering DCM, as a dead time is added, the inductor peak current gets higher and the zero mains current region becomes narrower, leading to a 5% decrease of the THD value.

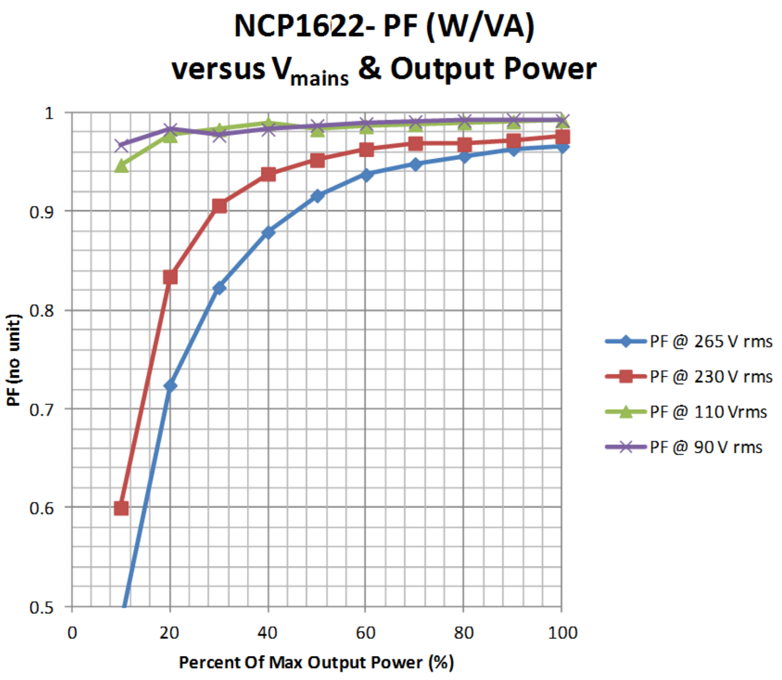


Figure 10. Evaluation board PF versus output power - 100% output power corresponds to 160 W

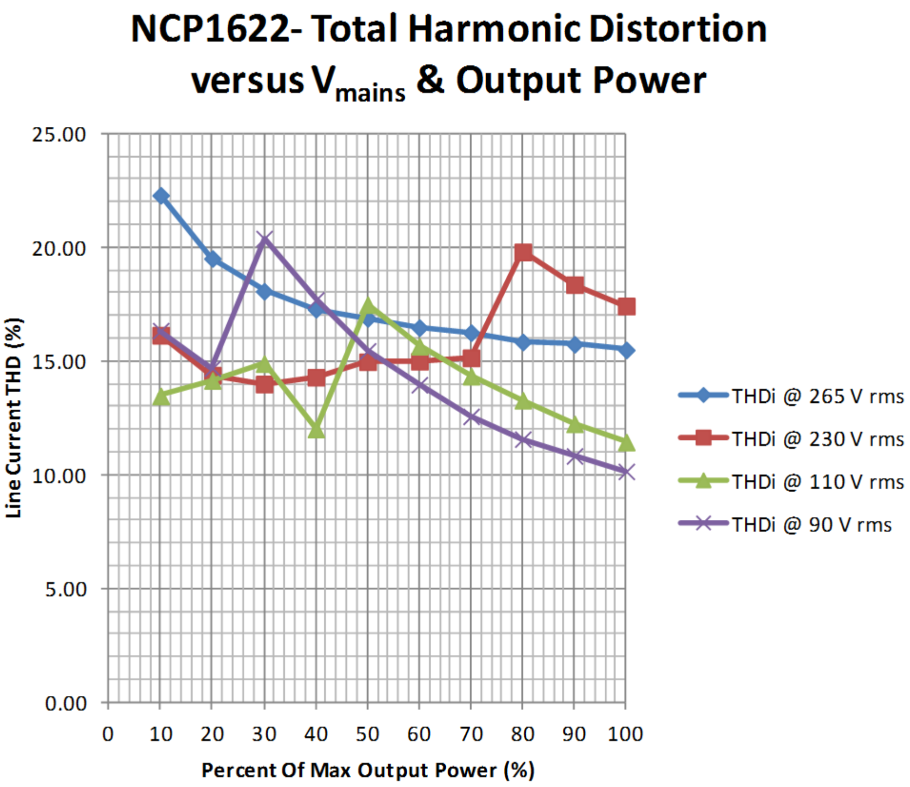


Figure 11. Evaluation board THD versus output power - 100% output power corresponds to 160 W

PROTECTION OF THE PFC STAGES

The NCP1622 protection features allows to design very rugged PFC stages

Brown-out

Brown out detection is disabled in product option AEA which is used in this Evaluation Board. If brown-is needed, check which option is needed using the product datasheet [2] and use the application note [1] for operating details .

Over−Current Protection (OCP)

The NCP1622 is designed to monitor the current flowing through the power switch. A current sense resistor (R3 of Figure 2) is inserted between the MOSFET source and ground to generate a positive voltage proportional to the MOSFET current (VCSZCD). When VCSZCD exceeds a 500-mV internal reference, the circuit forces the driver low. A 400-ns blanking time prevents the OCP comparator from tripping because of the switching spikes that occur when the MOSFET turns on. In our application, the theoretical maximal inductor current is

$$I_{ind,\max} = \left(\frac{500\text{ mV}}{80\text{ m}\Omega}\right) \approx 6.25\text{ A} \qquad (1)$$

Figure 12 shows the inductor current when clamped. The over-current situation was obtained @ V_{mains}= 90 V rms with a 427-mA load. A 20-V VCC power source was applied to the board.

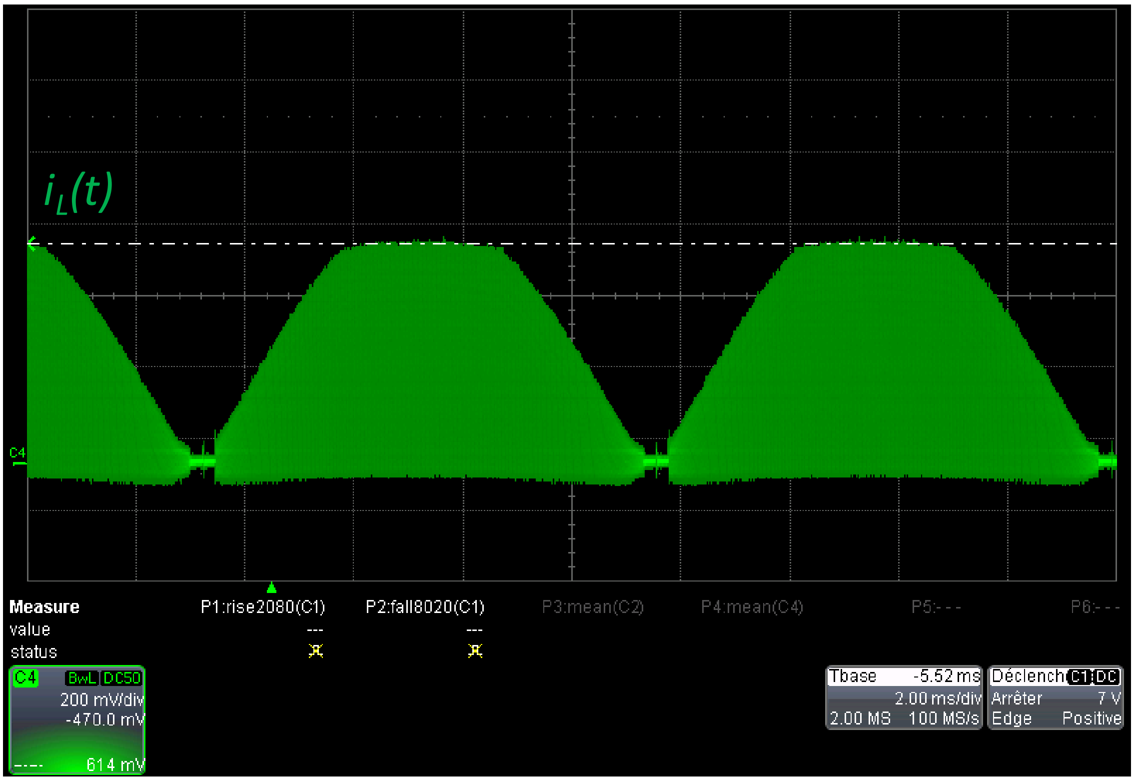
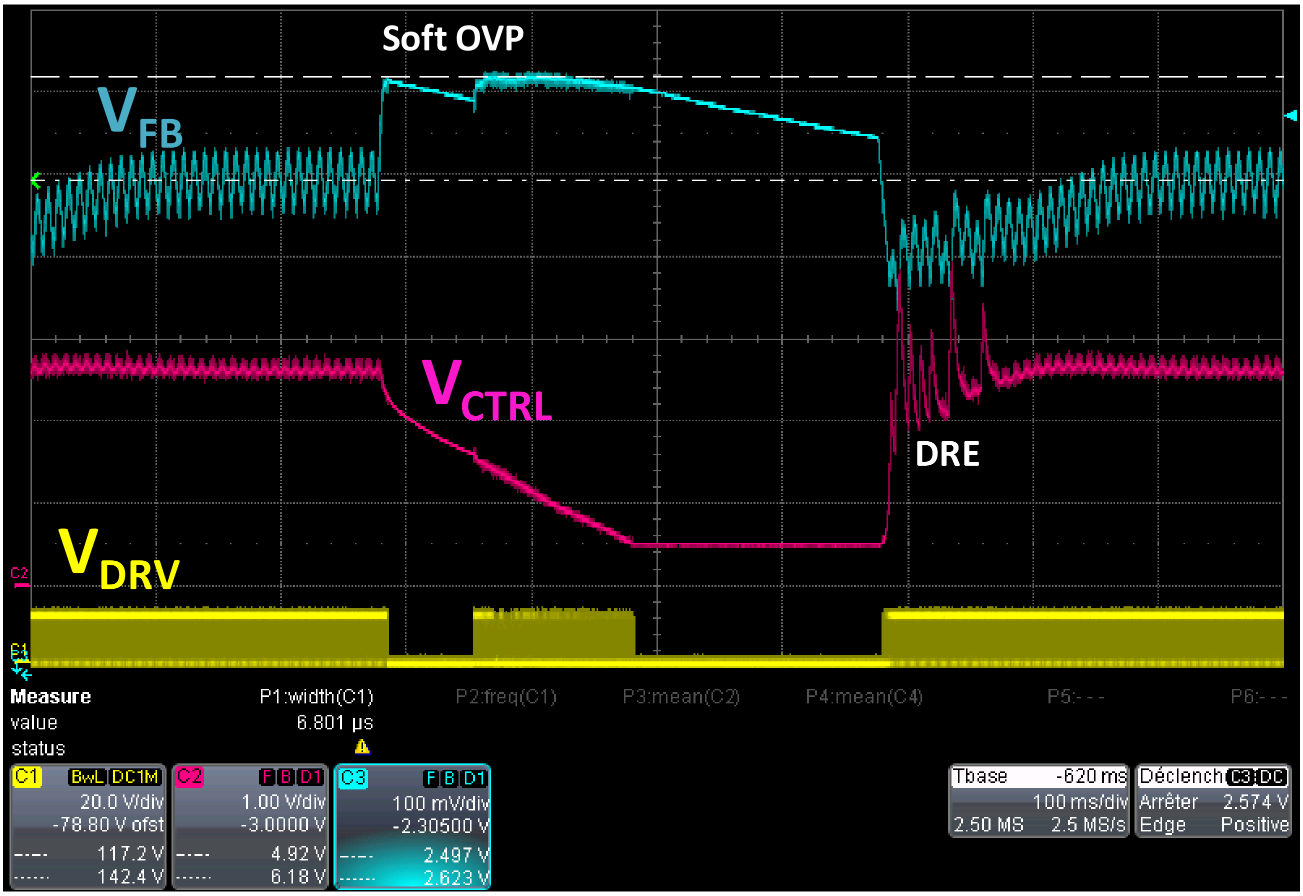


Figure 12. Inductor current showing OCP limitation @ V_{mains} = 90 V rms ; F_{mains} = 60 Hz ; I_{load} = 427 mA

DYNAMIC PERFORMANCE

The NCP1622 features the **dynamic response enhancer** (DRE) that increases the loop gain by an order of magnitude when the output voltage goes below 95.5% of its nominal level. This function dramatically reduces undershoots in case of an abrupt increase of the load demand. As an example, Figure 13 illustrates a load step from 400 mA to 0 mA and 0 mA to 400 mA (2-A/µs slope) @ 110 V rms input voltage. One can note that as a result of the DRE function, the control signal (VCTRL) steeply rises multiple times when the FB voltage goes below 0.955*2.5V = 2.487 V



Measure P1:width(C1) P2:freq(C1) P3:mean(C2) P4:mean(C4) P5:- - - P6:- - -
value 6.801 µs
status ⚠

C1 BwL DC1M 20.0 V/div -78.80 V ofst ---- 117.2 V ...... 142.4 V
C2 F B D1 1.00 V/div -3.0000 V ---- 4.92 V ...... 6.18 V
C3 F B D1 100 mV/div -2.30500 V ---- 2.497 V ...... 2.623 V
Tbase -620 ms 100 ms/div 2.50 MS 2.5 MS/s
Déclench C3 DC Arrêter 2.574 V Edge Positive

Figure 13. Load current transient featuring Soft OVP and DRE @ I_{load}=400mA / zero mA ;Vcc=20V, V_{mains}=110V_{rms}

BEHAVIOR UNDER FAILURE SITUATIONS

Elements of the PFC stage can be accidently shorted, badly soldered or damaged as a result of manufacturing incidents, of an excessive operating stress or of other troubles. In particular, adjacent pins of controllers can be shorted, a pin, grounded or badly connected. It is often required that such open/short situations do not cause fire, smoke nor loud noise. The NCP1622 integrates functions that help meet this requirement, for instance, in case of an improper pin connection (including GND) or of a short of the boost or bypass diode.

As an example, we will illustrate here the circuit operation when the PFC bypass diode is shorted. When the PFC stage is plugged in, a large in-rush current takes place that charges the bulk capacitor to the line peak voltage. Traditionally, a bypass diode (D_2 in the application schematic of Figure 2) is placed between the input and output high-voltage rails to divert this inrush current from the inductor and boost diode. When it is shorted, the bulk voltage being equal to the input voltage, the inductor slightly demagnetizes owing to the boost diode voltage drop. As this voltage is small, the demagnetization can be extremely long. This is generally far insufficient to prevent a cycle-by-cycle cumulative rise of the inductor current and an unsafe heating of the inductor, the MOSFET and the boost diode. As the internal NCP1622 watchdog may kick in during this long demagnetization period, continuous conduction mode (CCM) can occur for a few cycles. The NCP1622 incorporates a second over-current comparator that trips whenever the MOSFET current happens to exceed 150% of its maximum level. Such an event can happen when a) the watchdog restarts a cycle as explained before b) if the current slope is so sharp that the main over-current comparator cannot prevent the current from exceeding this second level as the result of the inductor saturation for instance. In this case, the circuit detects an “overstress” situation and disables the driver for an 800-µs delay. This long delay leads to a very low duty-ratio operation to dramatically limit the risk of overheating. Figure 14 illustrates the operation while the bypass diode and the NTC are both shorted @ V_{mains}=110 V with a 400-mA load current, the NCP1622 being supplied by a 20-V external power source. When the bypass diode is shorted, the demagnetization of the inductor takes too much time and the 200-µs Watchdog timer helps to start a new on-time, during which the OCP limit is reached. Because the previous demag was not reached and OCP is triggered, a 800-µs timer is used before allowing to start a new on-time. This helps limit the current resulting from the shorting of the bypass diode and the very low duty-ratio prevents the application from heating up.

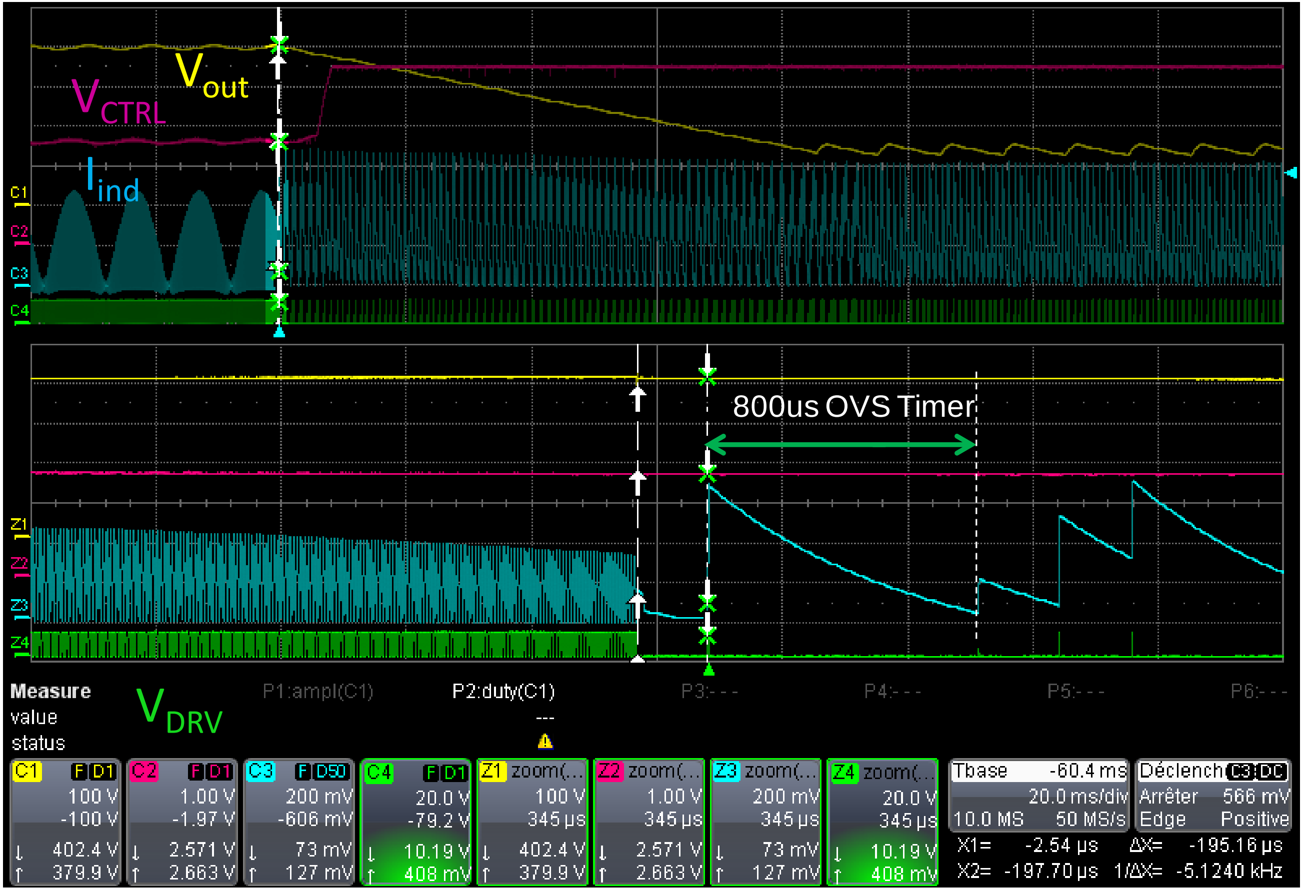
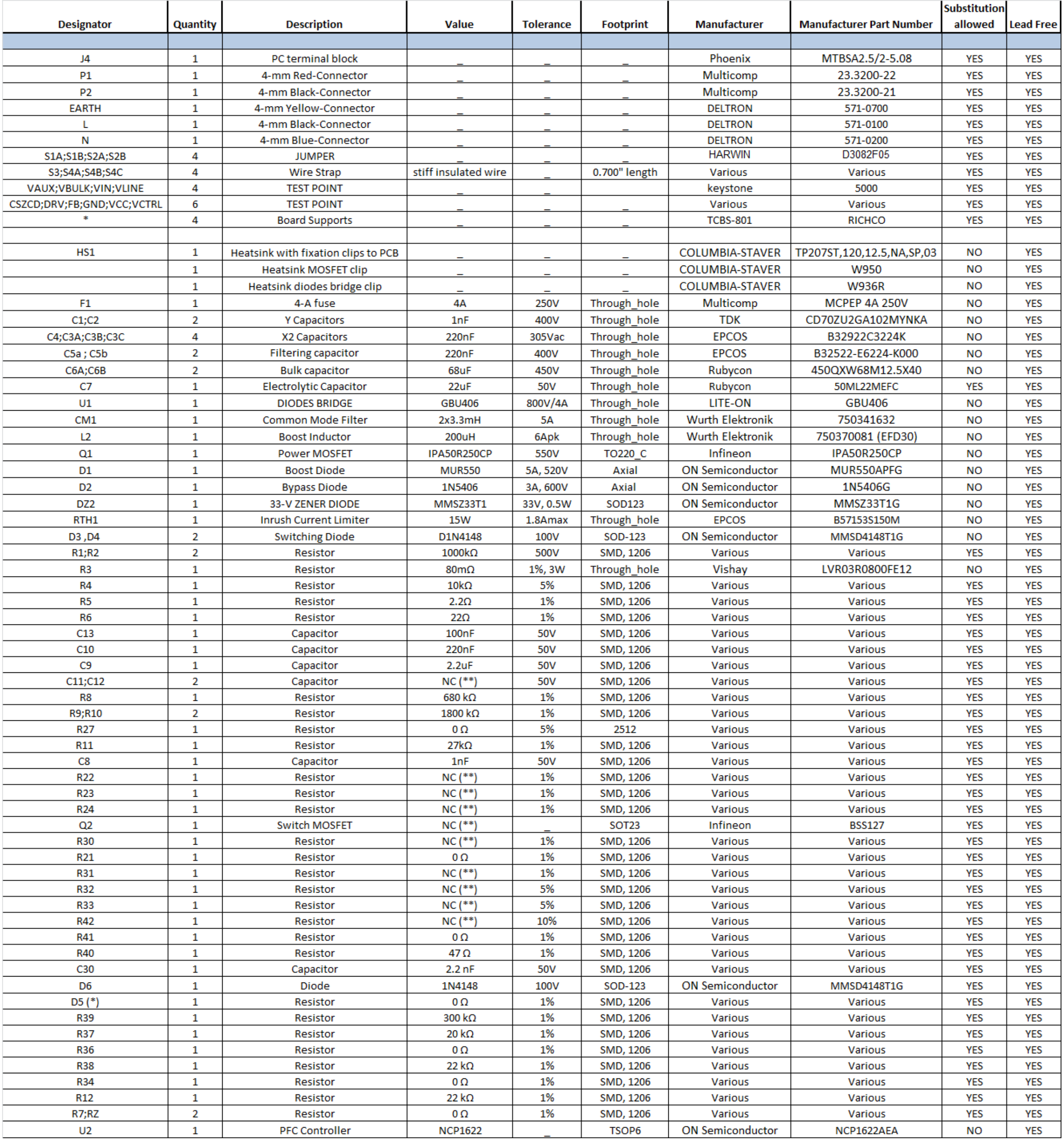


Figure 14. From steady state the bypass diode is shorted @V_{mains}=110V_{rms}, F_{mains}=60Hz, I_{load}=400mA , NTC shorted

Please note that we do not guarantee that the a NCP1622-driven PFC stage necessarily passes all the safety tests and in particular the boost diode short one since the performance can vary with respect to the application or conditions. The reported tests are intended to illustrate the typical behavior of the part in one particular application, highlighting the protections helping pass the safety tests. The reported tests were made at 25 °C ambient temperature.

BILL OF MATERIALS (Used by default on the EVB)



Designator	Quantity	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number	Substitution allowed	Lead Free
J4	1	PC terminal block	_	_	_	Phoenix	MTBSA2.5/2-5.08	YES	YES
P1	1	4-mm Red-Connector	_	_	_	Multicomp	23.3200-22	YES	YES
P2	1	4-mm Black-Connector	_	_	_	Multicomp	23.3200-21	YES	YES
EARTH	1	4-mm Yellow-Connector	_	_	_	DELTRON	571-0700	YES	YES
L	1	4-mm Black-Connector	_	_	_	DELTRON	571-0100	YES	YES
N	1	4-mm Blue-Connector	_	_	_	DELTRON	571-0200	YES	YES
S1A;S1B;S2A;S2B	4	JUMPER	_	_	_	HARWIN	D3082F05	YES	YES
S3;S4A;S4B;S4C	4	Wire Strap	stiff insulated wire	_	0.700" length	Various	Various	YES	YES
VAUX;VBULK;VIN;VLINE	4	TEST POINT	_	_		keystone	5000	YES	YES
CSZCD;DRV;FB;GND;VCC;VCTRL	6	TEST POINT	_	_	_	Various	Various	YES	YES
*	4	Board Supports	_	_	_	TCBS-801	RICHCO	YES	YES
HS1	1	Heatsink with fixation clips to PCB	_	_	_	COLUMBIA-STAVER	TP207ST,120,12.5,NA,SP,03	NO	YES
	1	Heatsink MOSFET clip	_	_	_	COLUMBIA-STAVER	W950	NO	YES
	1	Heatsink diodes bridge clip	_	_	_	COLUMBIA-STAVER	W936R	NO	YES
F1	1	4-A fuse	4A	250V	Through_hole	Multicomp	MCPEP 4A 250V	NO	YES
C1;C2	2	Y Capacitors	1nF	400V	Through_hole	TDK	CD70ZU2GA102MYNKA	NO	YES
C4;C3A;C3B;C3C	4	X2 Capacitors	220nF	305Vac	Through_hole	EPCOS	B32922C3224K	NO	YES
C5a ; C5b	2	Filtering capacitor	220nF	400V	Through_hole	EPCOS	B32522-E6224-K000	NO	YES
C6A;C6B	2	Bulk capacitor	68uF	450V	Through_hole	Rubycon	450QXW68M12.5X40	NO	YES
C7	1	Electrolytic Capacitor	22uF	50V	Through_hole	Rubycon	50ML22MEFC	YES	YES
U1	1	DIODES BRIDGE	GBU406	800V/4A	Through_hole	LITE-ON	GBU406	NO	YES
CM1	1	Common Mode Filter	2x3.3mH	5A	Through_hole	Wurth Elektronik	750341632	NO	YES
L2	1	Boost Inductor	200uH	6Apk	Through_hole	Wurth Elektronik	750370081 (EFD30)	NO	YES
Q1	1	Power MOSFET	IPA50R250CP	550V	TO220_C	Infineon	IPA50R250CP	NO	YES
D1	1	Boost Diode	MUR550	5A, 520V	Axial	ON Semiconductor	MUR550APFG	NO	YES
D2	1	Bypass Diode	1N5406	3A, 600V	Axial	ON Semiconductor	1N5406G	NO	YES
DZ2	1	33-V ZENER DIODE	MMSZ33T1	33V, 0.5W	SOD123	ON Semiconductor	MMSZ33T1G	NO	YES
RTH1	1	Inrush Current Limiter	15W	1.8Amax	Through_hole	EPCOS	B57153S150M	NO	YES
D3 ,D4	2	Switching Diode	D1N4148	100V	SOD-123	ON Semiconductor	MMSD4148T1G	NO	YES
R1;R2	2	Resistor	1000kΩ	500V	SMD, 1206	Various	Various	YES	YES
R3	1	Resistor	80mΩ	1%, 3W	Through_hole	Vishay	LVR03R0800FE12	NO	YES
R4	1	Resistor	10kΩ	5%	SMD, 1206	Various	Various	YES	YES
R5	1	Resistor	2.2Ω	1%	SMD, 1206	Various	Various	YES	YES
R6	1	Resistor	22Ω	1%	SMD, 1206	Various	Various	YES	YES
C13	1	Capacitor	100nF	50V	SMD, 1206	Various	Various	YES	YES
C10	1	Capacitor	220nF	50V	SMD, 1206	Various	Various	YES	YES
C9	1	Capacitor	2.2uF	50V	SMD, 1206	Various	Various	YES	YES
C11;C12	2	Capacitor	NC (**)	50V	SMD, 1206	Various	Various	YES	YES
R8	1	Resistor	680 kΩ	1%	SMD, 1206	Various	Various	YES	YES
R9;R10	2	Resistor	1800 kΩ	1%	SMD, 1206	Various	Various	YES	YES
R27	1	Resistor	0 Ω	5%	2512	Various	Various	YES	YES
R11	1	Resistor	27kΩ	1%	SMD, 1206	Various	Various	YES	YES
C8	1	Capacitor	1nF	50V	SMD, 1206	Various	Various	YES	YES
R22	1	Resistor	NC (**)	1%	SMD, 1206	Various	Various	YES	YES
R23	1	Resistor	NC (**)	1%	SMD, 1206	Various	Various	YES	YES
R24	1	Resistor	NC (**)	1%	SMD, 1206	Various	Various	YES	YES
Q2	1	Switch MOSFET	NC (**)	_	SOT23	Infineon	BSS127	YES	YES
R30	1	Resistor	NC (**)	1%	SMD, 1206	Various	Various	YES	YES
R21	1	Resistor	0 Ω	1%	SMD, 1206	Various	Various	YES	YES
R31	1	Resistor	NC (**)	1%	SMD, 1206	Various	Various	YES	YES
R32	1	Resistor	NC (**)	5%	SMD, 1206	Various	Various	YES	YES
R33	1	Resistor	NC (**)	5%	SMD, 1206	Various	Various	YES	YES
R42	1	Resistor	NC (**)	10%	SMD, 1206	Various	Various	YES	YES
R41	1	Resistor	0 Ω	1%	SMD, 1206	Various	Various	YES	YES
R40	1	Resistor	47 Ω	1%	SMD, 1206	Various	Various	YES	YES
C30	1	Capacitor	2.2 nF	50V	SMD, 1206	Various	Various	YES	YES
D6	1	Diode	1N4148	100V	SOD-123	ON Semiconductor	MMSD4148T1G	YES	YES
D5 (*)	1	Resistor	0 Ω	1%	SMD, 1206	Various	Various	YES	YES
R39	1	Resistor	300 kΩ	1%	SMD, 1206	Various	Various	YES	YES
R37	1	Resistor	20 kΩ	1%	SMD, 1206	Various	Various	YES	YES
R36	1	Resistor	0 Ω	1%	SMD, 1206	Various	Various	YES	YES
R38	1	Resistor	22 kΩ	1%	SMD, 1206	Various	Various	YES	YES
R34	1	Resistor	0 Ω	1%	SMD, 1206	Various	Various	YES	YES
R12	1	Resistor	22 kΩ	1%	SMD, 1206	Various	Various	YES	YES
R7;RZ	2	Resistor	0 Ω	1%	SMD, 1206	Various	Various	YES	YES
U2	1	PFC Controller	NCP1622	_	TSOP6	ON Semiconductor	NCP1622AEA	NO	YES

Table 3. NCP1622 GEVB Bill of Materials (ZCD detection using V_{aux})

REFERENCES

[1] “5 Key Steps to Designing a Compact, High-Efficiency PFC Stage Using The NCP1602”, Application noteAND9218/D, http://www.onsemi.com/pub_link/Collateral/AND9218-D.PDF

[2] NCP1622 Data Sheet, http://www.onsemi.com/xxxxx

[3] NCP1622 Evaluation Board documents http://www.onsemi.com/xxxxx

ANNEX

Schematic & BOM for modifying the evaluation board in order to use the Power MOSFET Drain voltage instead of the Auxiliary voltage for CS/ZCD pin

While this evaluation board uses the auxiliary voltage for ZCD detection, it is also possible to use the power MOSFET drain voltage to do the ZCD detection. It is possible to configure this same evaluation board for using the power MOSFET drain voltage to feed the CS/ZCD pin for ZCD detection .The power section of the schematic does not change and it is only the control schematic which changes. The components on the path between the auxiliary voltage and CS/ZCD pin must be removed and new components placed between the power MOSFET drain voltage (Vdrain) and CS/ZCD pin. The details of this modification are entirely described by the schematic of Figure 15 and, the bill of materials of Table 4. Application note AND9218/D [1] gives the design procedure and equations.

Using the schematic using power MOSFET drain voltage has pros and cons.

Power MOSFET Drain for ZCD Detection (Alternative BOM)	**Auxiliary Voltage for ZCD Detection (EVB default BOM)**
Pros: • A simple boost inductor can be used (not necessary to use a transformer) • Brown-out detection is possible when using brown-out activated product option	**Pros:** • R_{38} and R_{39} value can be small and sensitivity to noise and parasitic capacitances is reduced • Consumes no power during standby even if R_{38} and R_{39} value are small
Cons: • R_{22},R_{23} and R_{24} must not be too high because pin CSZCD is very sensitive to parasitic • Standby power (when there is no switching activity) is consumed by R_{22},R_{23} and R_{24}	**Cons:** • Brown-out detection is not possible when using brown-out activated product option • The simple inductor becomes a transformer to which an auxiliary winding is added

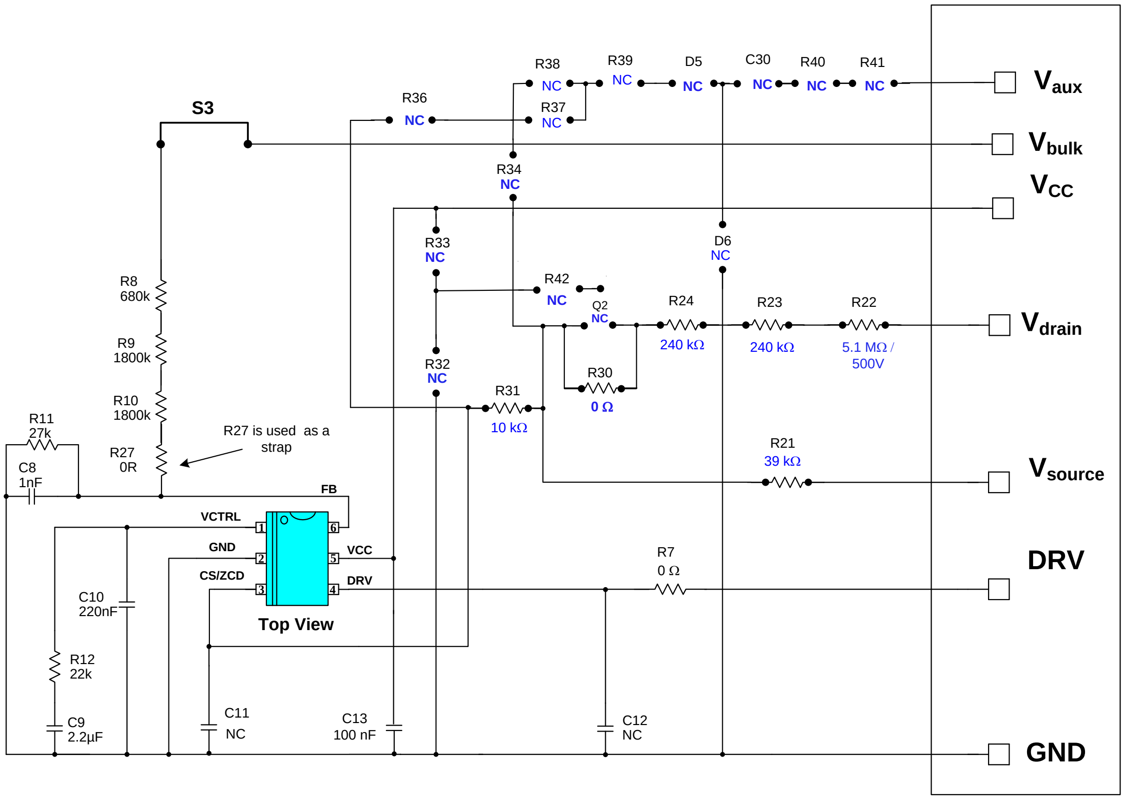


Figure 15. NCP1622 application Schematic − Control Section for ZCD Detection Using power MOSFET drain voltage (V_{drain})