1.5 A, Step-Up/Down/ Inverting Switching Regulators

NCP3063, NCP3063B, NCV3063

The NCP3063 Series is a higher frequency upgrade to the popular MC34063A and MC33063A monolithic DC−DC converters. These devices consist of an internal temperature compensated reference, comparator, a controlled duty cycle oscillator with an active current limit circuit, a driver and a high current output switch. This series was specifically designed to be incorporated in Step−Down, Step−Up and Voltage−Inverting applications with a minimum number of external components.

Features

- Operation to 40 V Input
- Low Standby Current
- Output Switch Current to 1.5 A
- Output Voltage Adjustable
- Frequency Operation of 150 kHz
- Precision 1.5% Reference
- New Features: Internal Thermal Shutdown with Hysteresis
  Cycle−by−Cycle Current Limiting
- Pb−Free Packages are Available

Applications

- Step−Down, Step−Up and Inverting supply applications
- High Power LED Lighting
- Battery Chargers

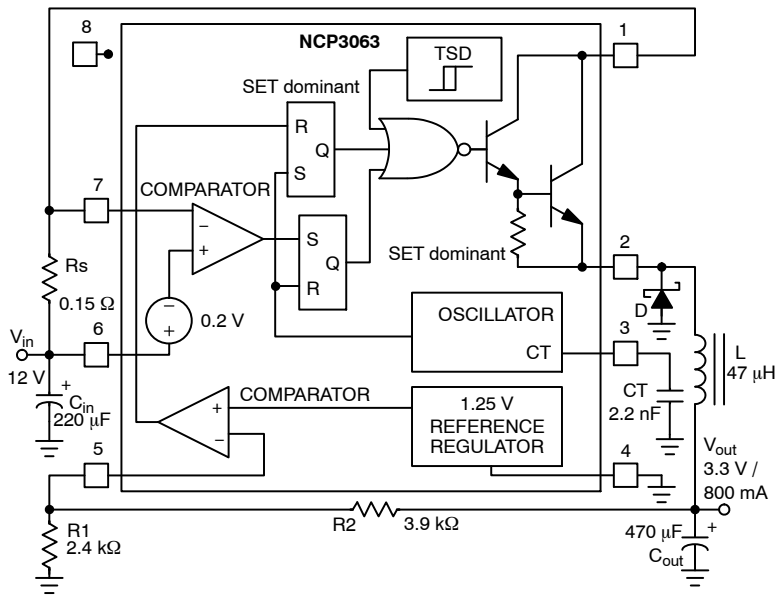
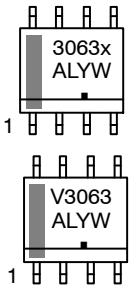
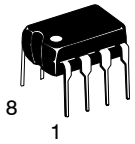


Figure 1. Typical Buck Application Circuit

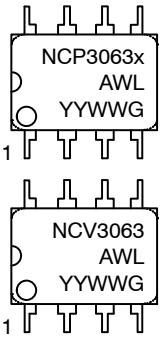
MARKING DIAGRAMS

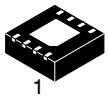
SOIC−8
D SUFFIX
CASE 751



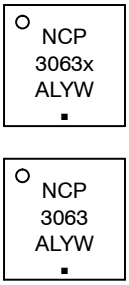


PDIP−8
P, P1 SUFFIX
CASE 626





DFN−8
CASE 488AF



NCP3063x	=	Specific Device Code x = B
A	=	Assembly Location
L, WL	=	Wafer Lot
Y, YY	=	Year
W, WW	=	Work Week
▪	=	Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 16 of this data sheet.

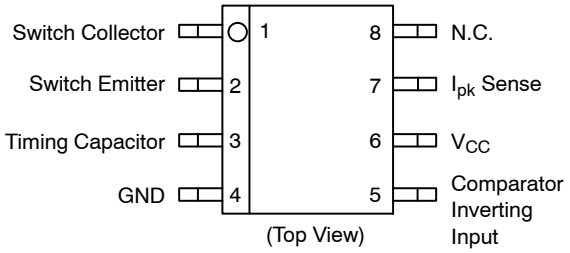
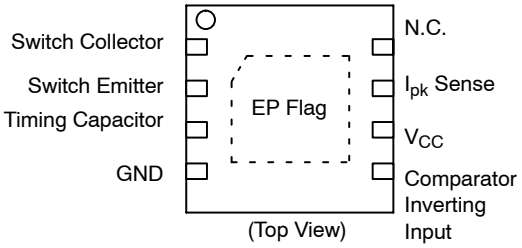


Figure 2. Pin Connections



NOTE: EP Flag must be tied to GND Pin 4 on PCB

Figure 3. Pin Connections

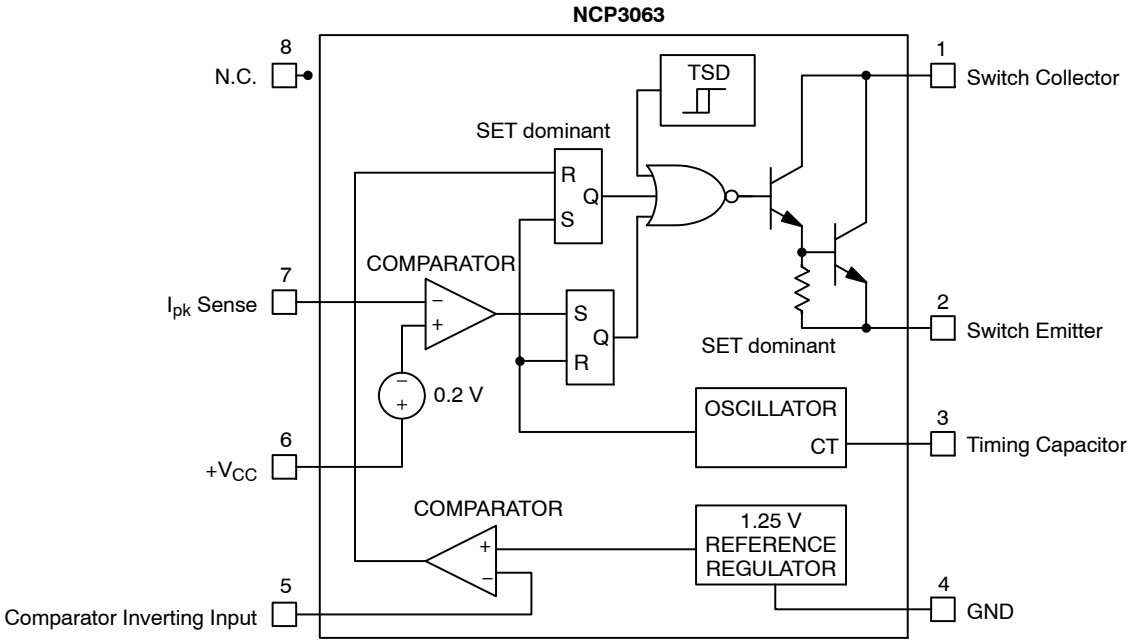


Figure 4. Block Diagram

PIN DESCRIPTION

Pin No.	Pin Name	Description
1	Switch Collector	Internal Darlington switch collector
2	Switch Emitter	Internal Darlington switch emitter
3	Timing Capacitor Oscillator Input	Timing Capacitor
4	GND	Ground pin for all internal circuits
5	Comparator Inverting Input	Inverting input pin of internal comparator
6	V_{CC}	Voltage Supply
7	I_{pk} Sense	Peak Current Sense Input to monitor the voltage drop across an external resistor to limit the peak current through the circuit
8	N.C.	Pin Not Connected
Exposed Pad	Exposed Pad	The exposed pad beneath the package must be connected to GND (Pin 4). Additionally, using proper layout techniques, the exposed pad can greatly enhance the power dissipation capabilities of the NCP3063.

MAXIMUM RATINGS (measured vs. Pin 4, unless otherwise noted)

Rating	Symbol	Value	Unit
V_{CC} pin 6	V_{CC}	0 to +40	V
Comparator Inverting Input pin 5	V_{CII}	−0.2 to + V_{CC}	V
Darlington Switch Collector pin 1	V_{SWC}	0 to +40	V
Darlington Switch Emitter pin 2 (transistor OFF)	V_{SWE}	−0.6 to + V_{CC}	V
Darlington Switch Collector to Emitter pin 1−2	V_{SWCE}	0 to +40	V
Darlington Switch Current	I_{SW}	1.5	A
I_{pk} Sense Pin 7	V_{IPK}	−0.2 to V_{CC} + 0.2	V
Timing Capacitor Pin 3	V_{TCAP}	−0.2 to +1.4	V

POWER DISSIPATION AND THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
PDIP−8 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	 100	°C/W
SOIC−8 Thermal Resistance, Junction−to−Air Thermal Resistance, Junction−to−Case	$R_{\theta JA}$ $R_{\theta JC}$	 180 45	°C/W
DFN−8 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	 80	°C/W
Storage Temperature Range	T_{STG}	−65 to +150	°C
Maximum Junction Temperature	$T_{J\ MAX}$	+150	°C
Operating Junction Temperature Range (Note 3) NCP3063 NCP3063B, NCV3063	T_J	 0 to +70 −40 to +125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Pin 1−8: Human Body Model 2000 V per AEC Q100−002; 003 or JESD22/A114; A115
   Machine Model Method 200 V
2. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.
3. The relation between junction temperature, ambient temperature and Total Power dissipated in IC is $T_J = T_A + R_\theta \bullet P_D$
4. The pins which are not defined may not be loaded by external signals

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_J = T_{low} to T_{high} [Note 5], unless otherwise specified)

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
OSCILLATOR						
f_{OSC}	Frequency	(V_{Pin} 5 = 0 V, CT = 2.2 nF, T_J = 25°C)	110	150	190	kHz
I_{DISCHG} / I_{CHG}	Discharge to Charge Current Ratio	(Pin 7 to V_{CC}, T_J = 25°C)	5.5	6.0	6.5	–
I_{DISCHG}	Capacitor Discharging Current	(Pin 7 to V_{CC}, T_J = 25°C)		1650		μA
I_{CHG}	Capacitor Charging Current	(Pin 7 to V_{CC}, T_J = 25°C)		275		μA
$V_{IPK(Sense)}$	Current Limit Sense Voltage	(T_J = 25°C) (Note 6)	165	200	235	mV
OUTPUT SWITCH (Note 7)						
$V_{SWCE(DROP)}$	Darlington Switch Collector to Emitter Voltage Drop	(I_{SW} = 1.0 A, Pin 2 to GND, T_J = 25°C) (Note 7)		1.0	1.3	V
$I_{C(OFF)}$	Collector Off−State Current	(V_{CE} = 40 V)		0.01	100	μA
COMPARATOR						
V_{TH}	Threshold Voltage	T_J = 25°C		1.250		V
		NCP3063	−1.5		+1.5	%
		NCP3063B, NCV3063	−2		+2	%
REG_{LiNE}	Threshold Voltage Line Regulation	(V_{CC} = 5.0 V to 40 V)	−6.0	2.0	6.0	mV
$I_{CII\ in}$	Input Bias Current	(V_{in} = V_{th})	−1000	−100	1000	nA
TOTAL DEVICE						
I_{CC}	Supply Current	(V_{CC} = 5.0 V to 40 V, CT = 2.2 nF, Pin 7 = V_{CC}, V_{Pin} 5 > V_{th}, Pin 2 = GND, remaining pins open)			7.0	mA
	Thermal Shutdown Threshold			160		°C
	Hysteresis			10		°C

5. NCP3063: T_{low} = 0°C, T_{high} = +70°C;
   NCP3063B, NCV3063: T_{low} = −40°C, T_{high} = +125°C
6. The $V_{IPK(Sense)}$ Current Limit Sense Voltage is specified at static conditions. In dynamic operation the sensed current turn−off value depends on comparator response time and di/dt current slope. See the Operating Description section for details.
7. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.
8. NCV prefix is for automotive and other applications requiring site and change control.

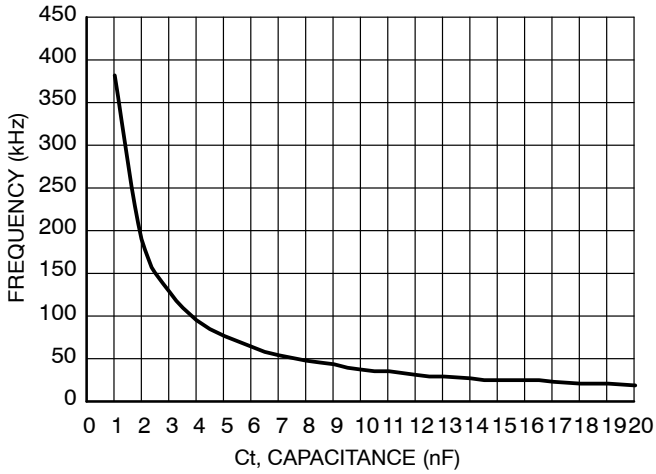


Figure 5. Oscillator Frequency vs. Oscillator Timing Capacitor

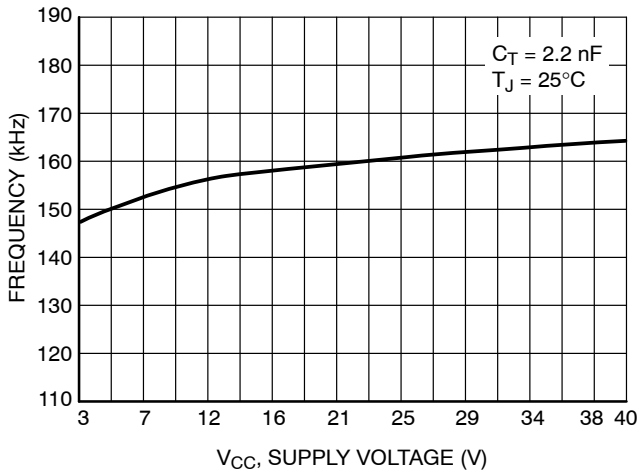


Figure 6. Oscillator Frequency vs. Supply Voltage

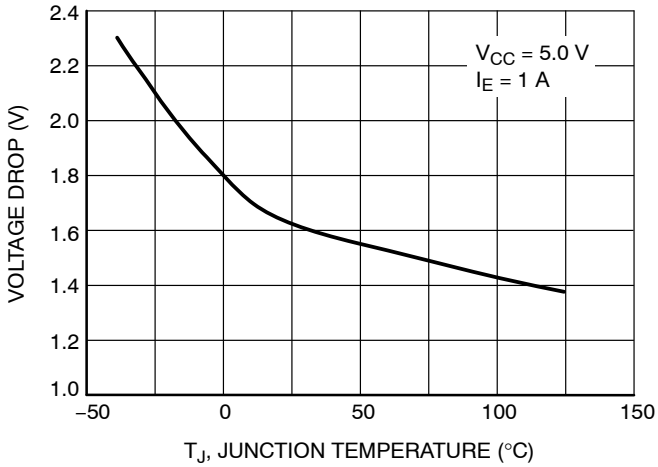


Figure 7. Emitter Follower Configuration Output Darlington Switch Voltage Drop vs. Temperature

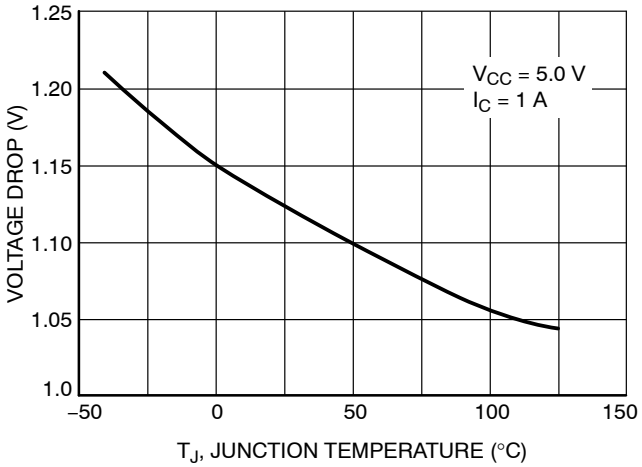


Figure 8. Common Emitter Configuration Output Darlington Switch Voltage Drop vs. Temperature

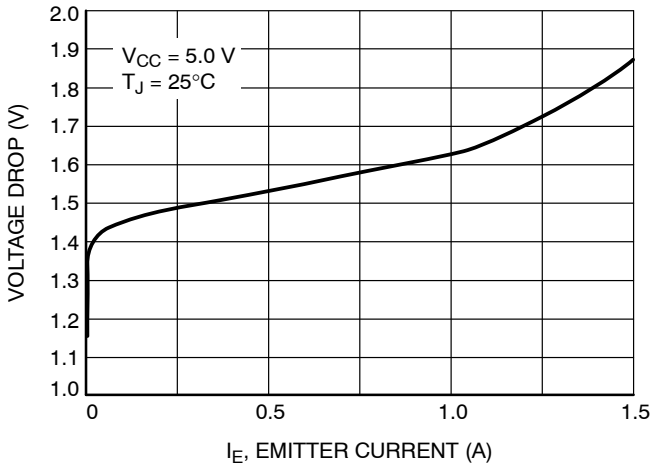


Figure 9. Emitter Follower Configuration Output Darlington Switch Voltage Drop vs. Emitter Current

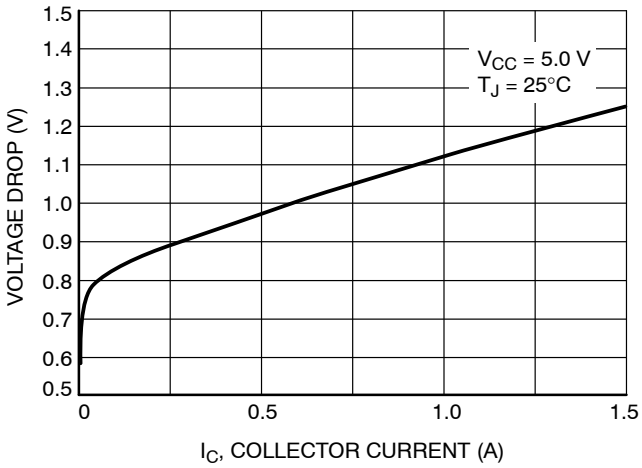


Figure 10. Common Emitter Configuration Output Darlington Switch Voltage Drop vs. Collector Current

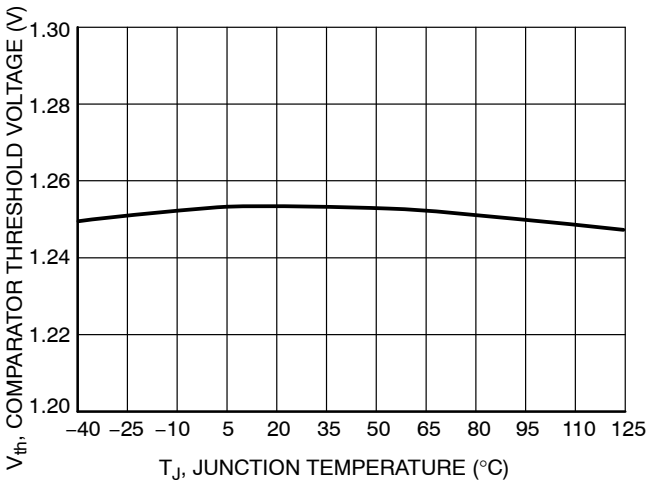


Figure 11. Comparator Threshold Voltage vs. Temperature

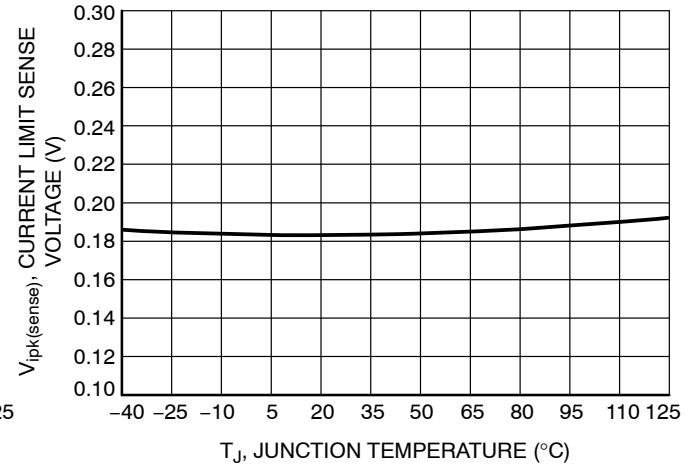


Figure 12. Current Limit Sense Voltage vs. Temperature

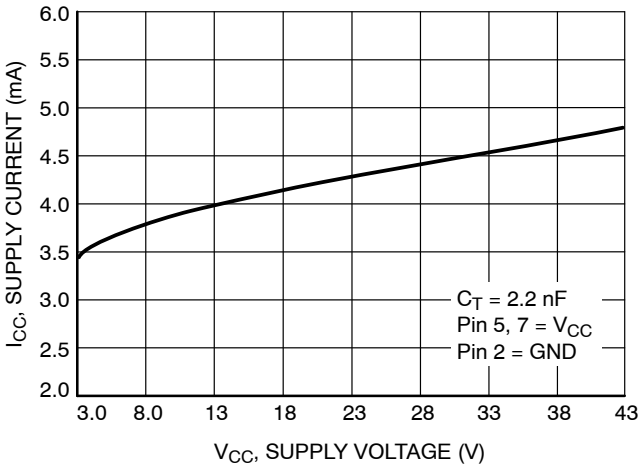


Figure 13. Standby Supply Current vs. Supply Voltage

INTRODUCTION

The NCP3063 is a monolithic power switching regulator optimized for dc to dc converter applications. The combination of its features enables the system designer to directly implement step−up, step−down, and voltage−inverting converters with a minimum number of external components. Potential applications include cost sensitive consumer products as well as equipment for industrial markets. A representative block diagram is shown in Figure 4.

Operating Description

The NCP3063 is a hysteretic, dc−dc converter that uses a gated oscillator to regulate output voltage. In general, this mode of operation is somewhat analogous to a capacitor charge pump and does not require dominant pole loop compensation for converter stability. The Typical Operating Waveforms are shown in Figure 14. The output voltage waveform shown is for a step−down converter with the ripple and phasing exaggerated for clarity. During initial converter startup, the feedback comparator senses that the output voltage level is below nominal. This causes the output switch to turn on and off at a frequency and duty cycle controlled by the oscillator, thus pumping up the output filter capacitor. When the output voltage level reaches nominal, the output switch next cycle turning on is inhibited. The feedback comparator will enable the switching immediately when the load current causes the output voltage to fall below nominal. Under these conditions, output switch conduction can be enabled for a partial oscillator cycle, a partial cycle plus a complete cycle, multiple cycles, or a partial cycle plus multiple cycles. (See AN920/D for more information).

Oscillator

The oscillator frequency and off−time of the output switch are programmed by the value selected for timing capacitor C_T. Capacitor C_T is charged and discharged by a 1 to 6 ratio internal current source and sink, generating a positive going sawtooth waveform at Pin 3. This ratio sets the maximum $t_{ON}/(t_{ON} + t_{OFF})$ of the switching converter as 6/(6 + 1) or 0.857 (typical) The oscillator peak and valley voltage difference is 500 mV typically. To calculate the C_T capacitor value for required oscillator frequency, use the equations found in Figure 15. An Excel based design tool can be found at www.onsemi.com on the NCP3063 product page.

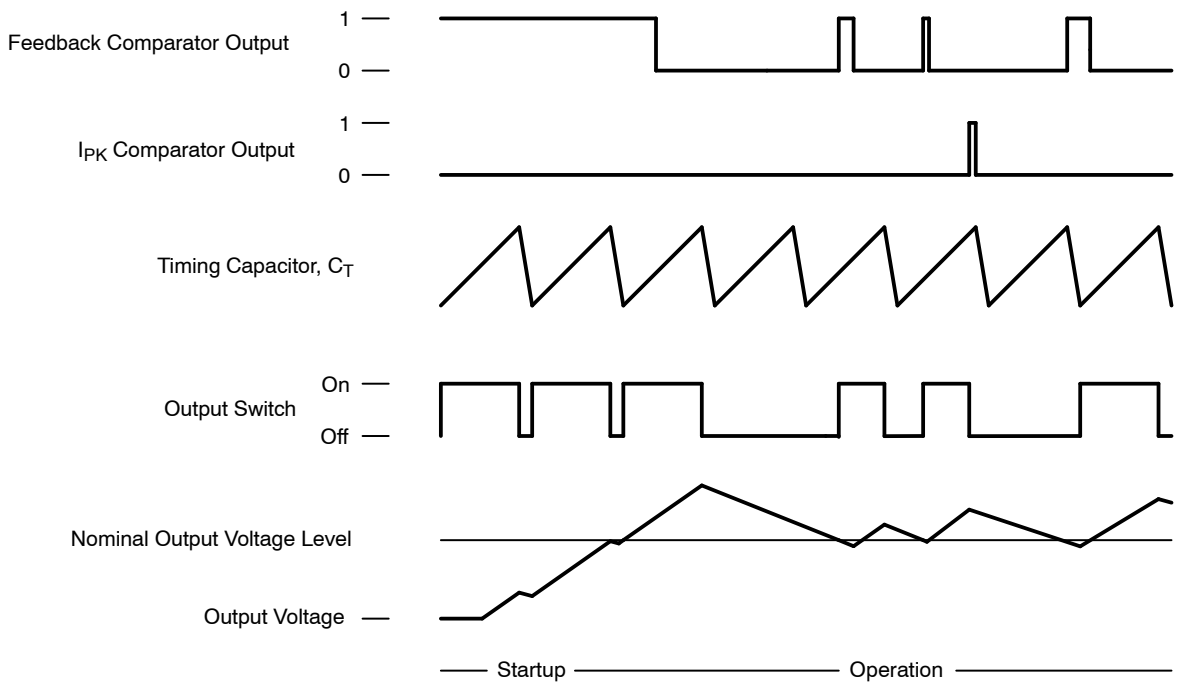
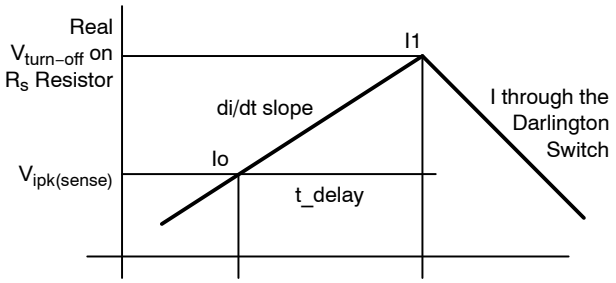


Figure 14. Typical Operating Waveforms

Peak Current Sense Comparator

With a voltage ripple gated converter operating under normal conditions, output switch conduction is initiated by the Voltage Feedback comparator and terminated by the oscillator. Abnormal operating conditions occur when the converter output is overloaded or when feedback voltage sensing is lost. Under these conditions, the I_{pk} Current Sense comparator will protect the Darlington output Switch. The switch current is converted to a voltage by inserting a fractional ohm resistor, R_{SC}, in series with V_{CC} and the Darlington output switch. The voltage drop across R_{SC} is monitored by the Current Sense comparator. If the voltage drop exceeds 200 mV with respect to V_{CC}, the comparator will set the latch and terminate output switch conduction on a cycle−by−cycle basis. **This Comparator/Latch configuration ensures that the Output Switch has only a single on−time during a given oscillator cycle.**



The $V_{IPK(Sense)}$ Current Limit Sense Voltage threshold is specified at static conditions. In dynamic operation the sensed current turn−off value depends on comparator response time and di/dt current slope.

Real $V_{turn-off}$ on R_{sc} resistor

$$V_{turn\_off} = V_{ipk(sense)} + Rs \cdot (t\_delay \cdot di/dt)$$

Typical I_{pk} comparator response time t_delay is 350 ns. The di/dt current slope is growing with voltage difference on the inductor pins and with decreasing inductor value.

It is recommended to check the real max peak current in the application at worst conditions to be sure that the max peak current will never get over the 1.5 A Darlington Switch Current max rating.

Thermal Shutdown

Internal thermal shutdown circuitry is provided to protect the IC in the event that the maximum junction temperature is exceeded. When activated, typically at 160°C, the Output Switch is disabled. The temperature sensing circuit is designed with 10°C hysteresis. The Switch is enabled again when the chip temperature decreases to at least 150°C threshold. **This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a replacement for proper heatsinking.**

Output Switch

The output switch is designed in a Darlington configuration. This allows the application designer to operate at all conditions at high switching speed and low voltage drop. The Darlington Output Switch is designed to switch a maximum of 40 V collector to emitter voltage and current up to 1.5 A.

APPLICATIONS

Figures 16 through 24 show the simplicity and flexibility of the NCP3063. Three main converter topologies are demonstrated with actual test data shown below each of the circuit diagrams.

Figure 15 gives the relevant design equations for the key parameters. Additionally, a complete application design aid for the NCP3063 can be found at www.onsemi.com.

Figures 25 through 31 show typical NCP3063 applications with external transistors. This solution helps to increase output current and helps with efficiency still keeping low cost bill of materials. Typical schematics of boost configuration with NMOS transistor, buck configuration with PMOS transistor and buck configuration with LOW $V_{CE(sat)}$ PNP are shown.

Another advantage of using the external transistor is higher operating frequency which can go up to 250 kHz. Smaller size of the output components such as inductor and capacitor can be used then.

(See Notes 9, 10, 11)	Step−Down	Step−Up	Voltage−Inverting
$\frac{t_{on}}{t_{off}}$	$\frac{V_{out} + V_F}{V_{in} - V_{SWCE} - V_{out}}$	$\frac{V_{out} + V_F - V_{in}}{V_{in} - V_{SWCE}}$	$\frac{\lvert V_{out}\rvert + V_F}{V_{in} - V_{SWCE}}$
t_{on}	$\frac{\frac{t_{on}}{t_{off}}}{f\left(\frac{t_{on}}{t_{off}} + 1\right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f\left(\frac{t_{on}}{t_{off}} + 1\right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f\left(\frac{t_{on}}{t_{off}} + 1\right)}$
C_T	$C_T = \frac{381.6 \cdot 10^{-6}}{f_{osc}} - 343 \cdot 10^{-12}$		
$I_{L(avg)}$	I_{out}	$I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$	$I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$
$I_{pk\ (Switch)}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$
R_{SC}	$\frac{0.20}{I_{pk\ (Switch)}}$	$\frac{0.20}{I_{pk\ (Switch)}}$	$\frac{0.20}{I_{pk\ (Switch)}}$
L	$\left(\frac{V_{in} - V_{SWCE} - V_{out}}{\Delta I_L}\right) t_{on}$	$\left(\frac{V_{in} - V_{SWCE}}{\Delta I_L}\right) t_{on}$	$\left(\frac{V_{in} - V_{SWCE}}{\Delta I_L}\right) t_{on}$
$V_{ripple(pp)}$	$\Delta I_L \sqrt{\left(\frac{1}{8 f C_O}\right)^2 + (ESR)^2}$	$\approx \frac{t_{on}\, I_{out}}{C_O} + \Delta I_L \cdot ESR$	$\approx \frac{t_{on}\, I_{out}}{C_O} + \Delta I_L \cdot ESR$
V_{out}	$V_{TH}\left(\frac{R_2}{R_1} + 1\right)$	$V_{TH}\left(\frac{R_2}{R_1} + 1\right)$	$V_{TH}\left(\frac{R_2}{R_1} + 1\right)$

9. V_{SWCE} − Darlington Switch Collector to Emitter Voltage Drop, refer to Figures 7, 8, 9 and 10.
10. V_F − Output rectifier forward voltage drop. Typical value for 1N5819 Schottky barrier rectifier is 0.4 V.
11. The calculated t_{on}/t_{off} must not exceed the minimum guaranteed oscillator charge to discharge ratio.

The Following Converter Characteristics Must Be Chosen:

V_{in} − Nominal operating input voltage.

V_{out} − Desired output voltage.

I_{out} − Desired output current.

ΔI_L − Desired peak−to−peak inductor ripple current. For maximum output current it is suggested that ΔI_L be chosen to be less than 10% of the average inductor current $I_{L(avg)}$. This will help prevent $I_{pk\ (Switch)}$ from reaching the current limit threshold set by R_{SC}. If the design goal is to use a minimum inductance value, let $\Delta I_L = 2(I_{L(avg)})$. This will proportionally reduce converter output current capability.

f − Maximum output switch frequency.

$V_{ripple(pp)}$ − Desired peak−to−peak output ripple voltage. For best performance the ripple voltage should be kept to a low value since it will directly affect line and load regulation. Capacitor C_O should be a low equivalent series resistance (ESR) electrolytic designed for switching regulator applications.

Figure 15. Design Equations

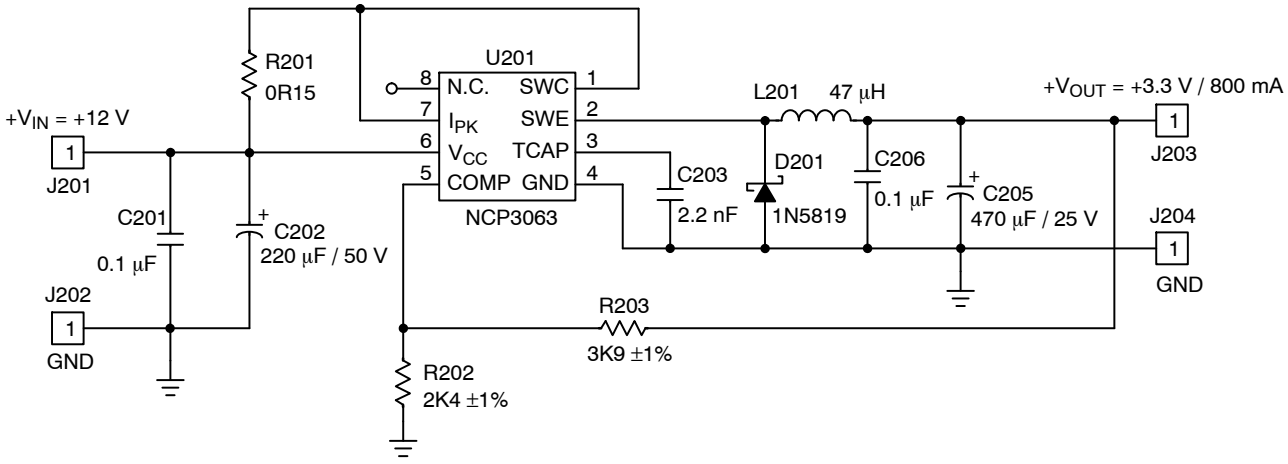


Figure 16. Typical Buck Application Schematic

Value of Components

Name	Value
L201	47 µH, I_{sat} > 1.5 A
D201	1 A, 40 V Schottky Rectifier
C202	220 µF, 50 V, Low ESR
C205	470 µF, 25 V, Low ESR
C203	2.2 nF Ceramic Capacitor

Name	Value
R201	150 mΩ, 0.5 W
R202	2.40 kΩ
R203	3.90 kΩ
C201	100 nF Ceramic Capacitor
C202	100 nF Ceramic Capacitor

Test Results

Test	Condition	Results
Line Regulation	V_{in} = 9 V to 12 V, I_o = 800 mA	8 mV
Load Regulation	V_{in} = 12 V, I_o = 80 mA to 800 mA	9 mV
Output Ripple	V_{in} = 12 V, I_o = 40 mA to 800 mA	≤ 85 mV_{pp}
Efficiency	V_{in} = 12 V, I_o = 400 mA to 800 mA	> 73%
Short Circuit Current	V_{in} = 12 V, R_{load} = 0.15 Ω	1.25 A

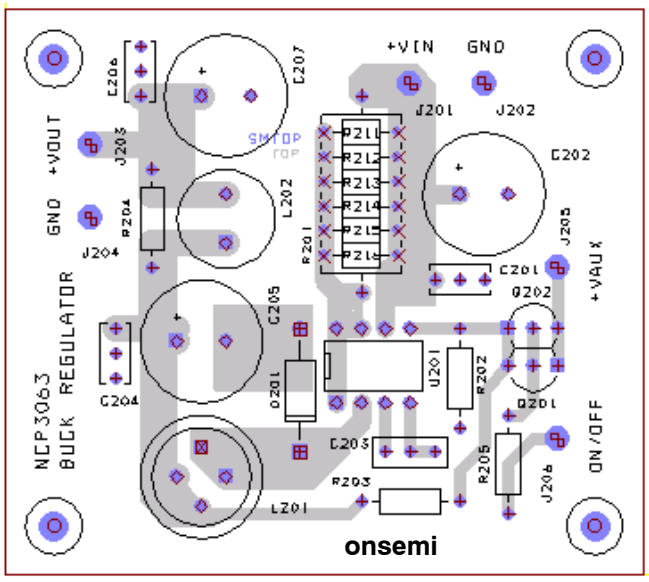


Figure 17. Buck Demoboard Layout

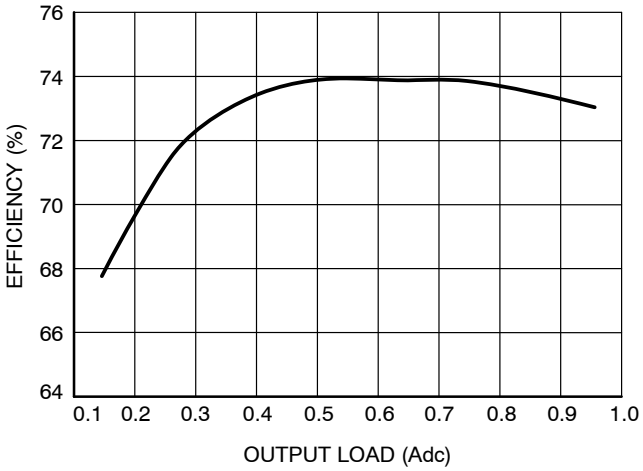


Figure 18. Efficiency vs. Output Current for the Buck Demo Board at V_{in} = 12 V, V_{out} = 3.3 V, T_A = 25°C

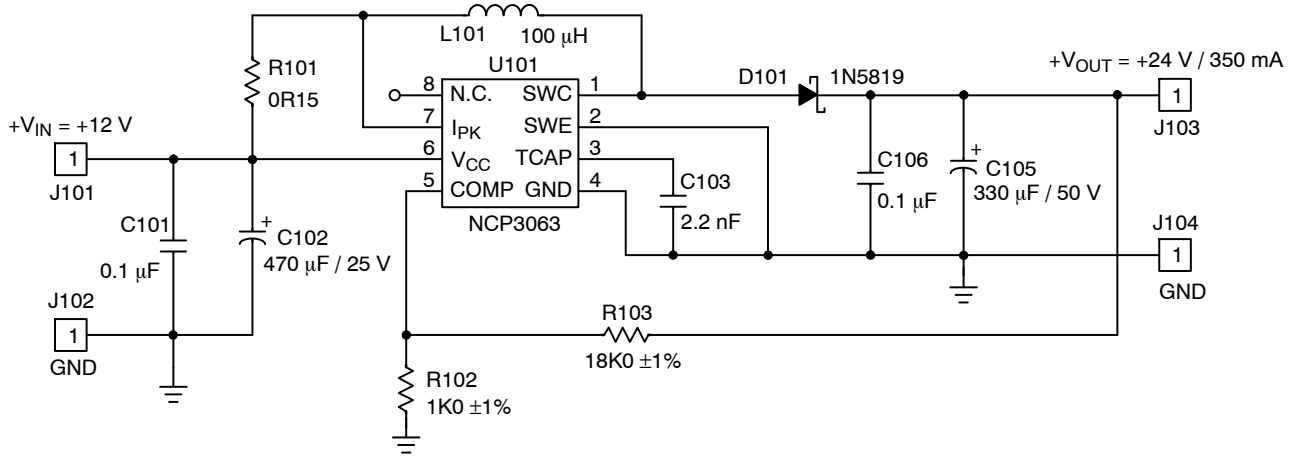


Figure 19. Typical Boost Application Schematic

Value of Components

Name	Value
L101	100 μH, I_{sat} > 1.5 A
D101	1 A, 40 V Schottky Rectifier
C102	470 μF, 25 V, Low ESR
C105	330 μF, 50 V, Low ESR
C103	2.2 nF Ceramic Capacitor

Name	Value
R101	150 mΩ, 0.5 W
R102	1.00 kΩ
R103	18.00 kΩ
C101	100 nF Ceramic Capacitor
C106	100 nF Ceramic Capacitor

Test Results

Test	Condition	Results
Line Regulation	V_{in} = 9 V to 15 V, I_o = 250 mA	2 mV
Load Regulation	V_{in} = 12 V, I_o = 30 mA to 350 mA	5 mV
Output Ripple	V_{in} = 12 V, I_o = 10 mA to 350 mA	≤ 350 mV_{pp}
Efficiency	V_{in} = 12 V, I_o = 50 mA to 350 mA	> 85.5%

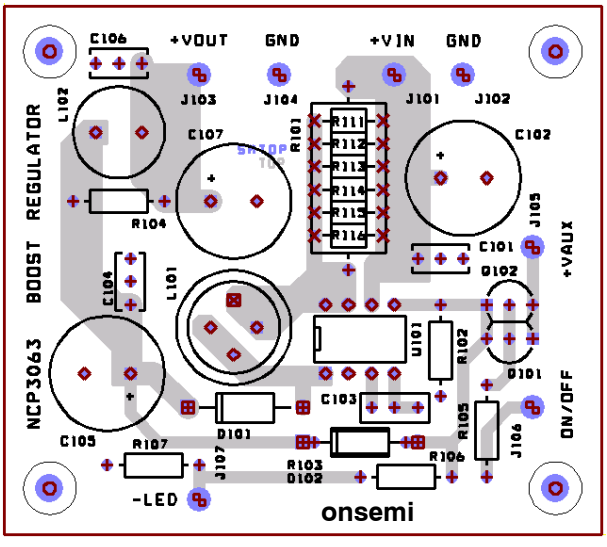


Figure 20. Boost Demoboard Layout

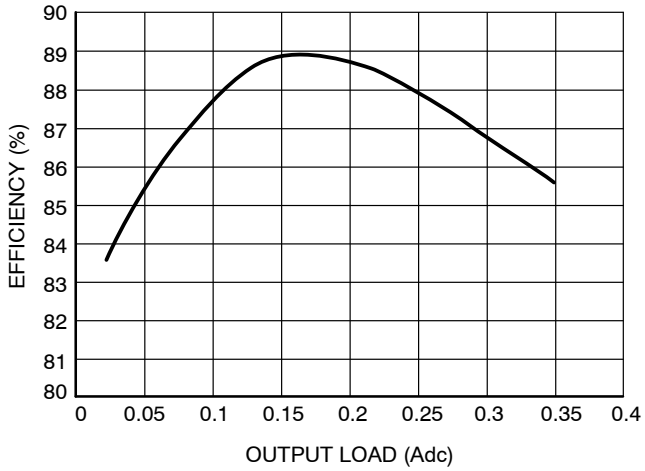


Figure 21. Efficiency vs. Output Current for the Boost Demo Board at V_{in} = 12 V, V_{out} = 24 V, T_A = 25°C

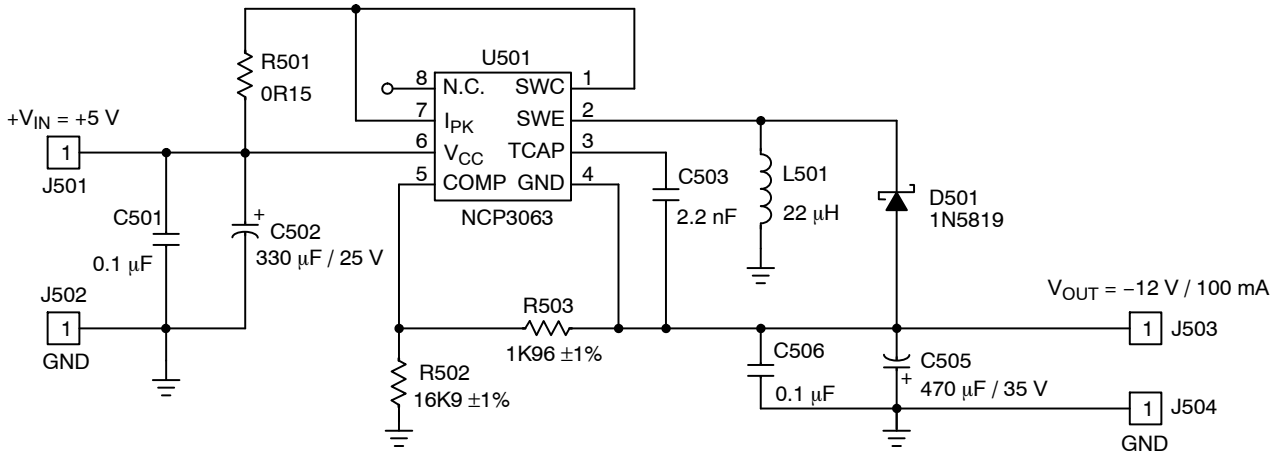


Figure 22. Typical Voltage Inverting Application Schematic

Value of Components

Name	Value
L501	22 μH, I_{sat} > 1.5 A
D501	1 A, 40 V Schottky Rectifier
C502	330 μF, 25 V, Low ESR
C505	470 μF, 35 V, Low ESR
C503	2.2 nF Ceramic Capacitor

Name	Value
R501	150 mΩ, 0.5 W
R502	16.9 kΩ
R503	1.96 kΩ
C501	100 nF Ceramic Capacitor
C506	100 nF Ceramic Capacitor

Test Results

Test	Condition	Results
Line Regulation	V_{in} = 4.5 V to 6 V, I_o = 50 mA	1.5 mV
Load Regulation	V_{in} = 5 V, I_o = 10 mA to 100 mA	1.6 mV
Output Ripple	V_{in} = 5 V, I_o = 0 mA to 100 mA	≤ 300 mV_{pp}
Efficiency	V_{in} = 5 V, I_o = 100 mA	49.8%
Short Circuit Current	V_{in} = 5 V, R_{load} = 0.15 Ω	0.885 A

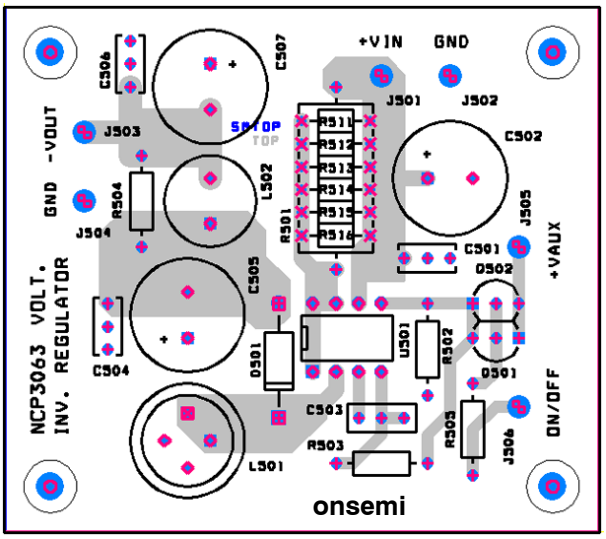


Figure 23. Voltage Inverting Demoboard Layout

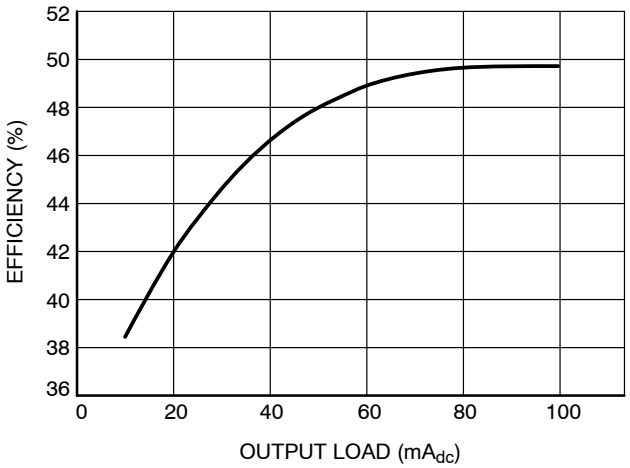


Figure 24. Efficiency vs. Output Current for the Voltage Inverting Demo Board at V_{in} = +5 V, V_{out} = −12 V, T_A = 25°C

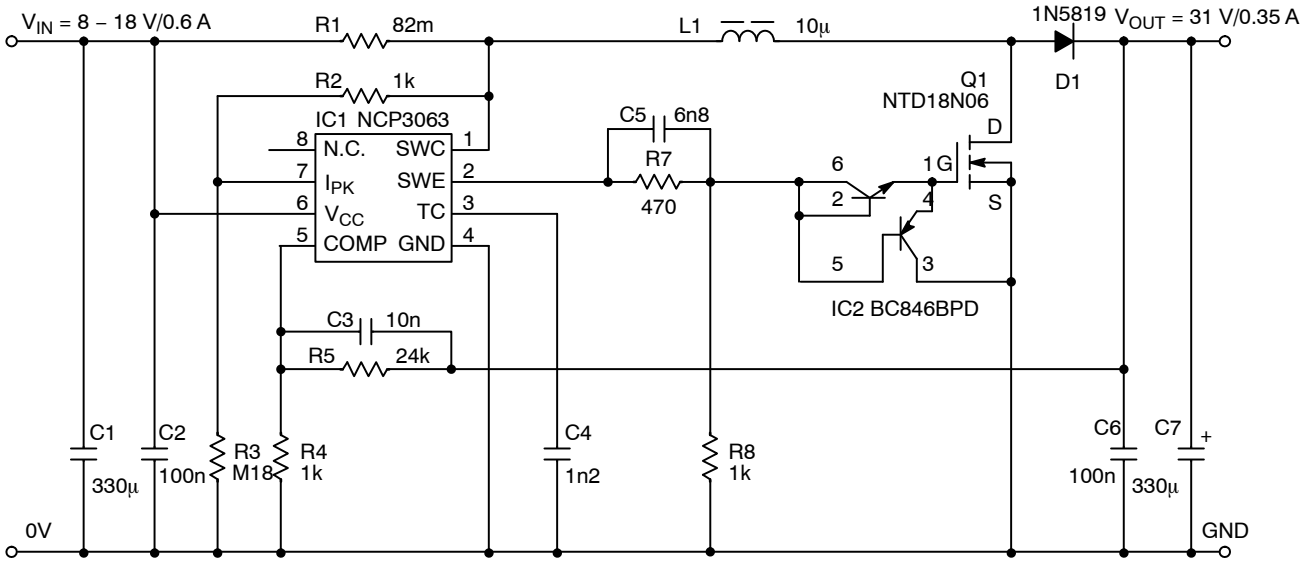


Figure 25. Typical Boost Application Schematic with External NMOS Transistor

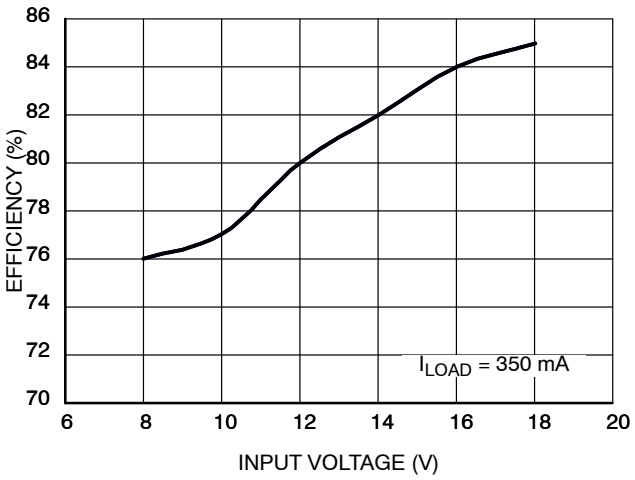


Figure 26. Typical Efficiency for Application Shown in Figure 25.

External transistor is recommended in applications where wide input voltage ranges and higher power is required. The suitable schematic with an additional NMOS transistor and its driving circuit is shown in the Figure 25. The driving circuit is controlled from SWE Pin of the NCP3063 through frequency compensated resistor divider R7/R8. The driver IC2 is **onsemi** low cost dual NPN/PNP transistor BC846BPD. Its NPN transistor is connected as a super diode for charging the gate capacitance. The PNP transistor works as an emitter follower for discharging the gate capacitor. This configuration assures sharp driving edge between 50 – 100 ns as well as it limits power consumption of R7/R8 divider down to 50 mW. The output current limit is balanced by resistor R3. The fast switching with low $R_{DS(on)}$ NMOS transistor will achieve efficiencies up to 85% in automotive applications.

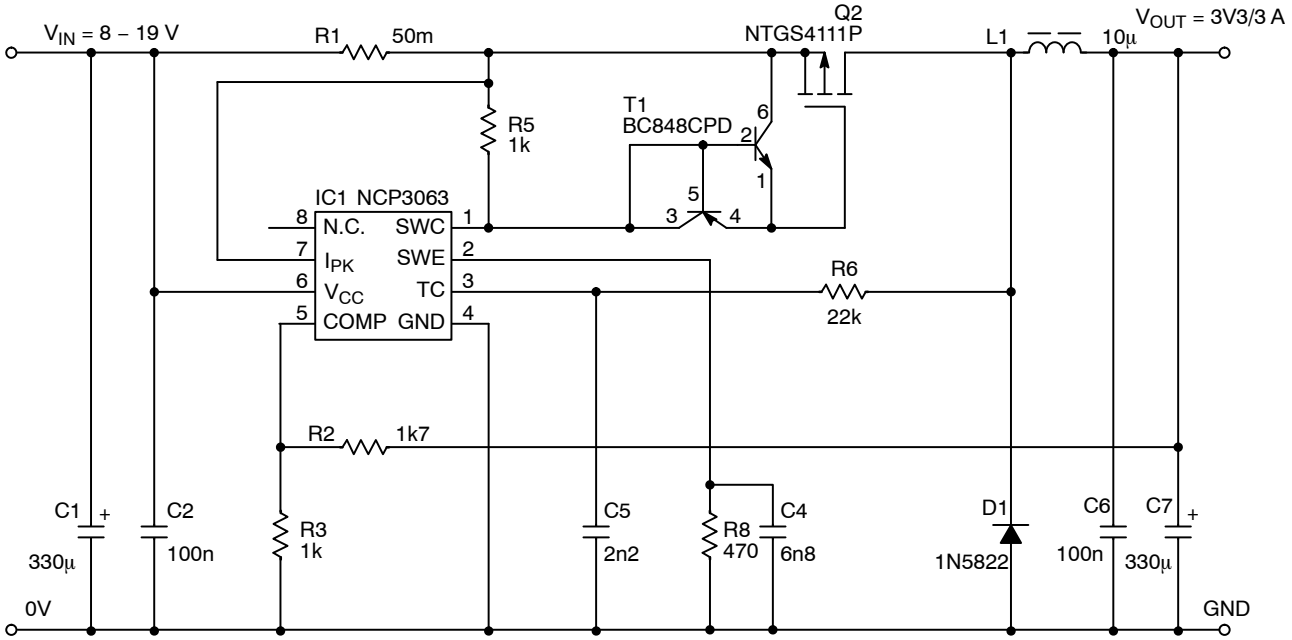


Figure 27. Typical Buck Application Schematic with External PMOS Transistor

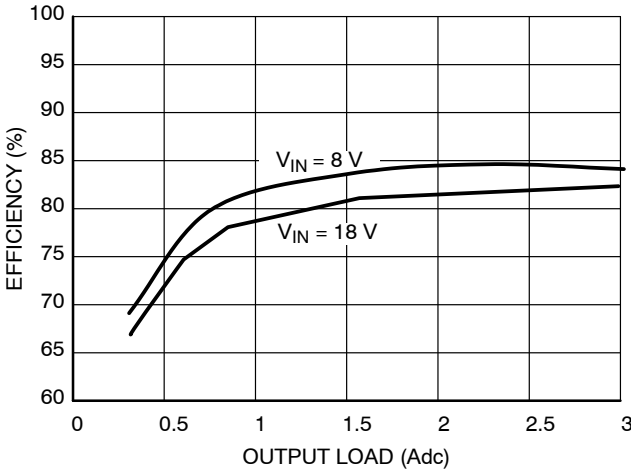


Figure 28. NCP3063 Efficiency vs. Output Current for Buck External PMOS at V_{out} = 3.3 V, f = 220 kHz, T_A = 25°C

Figure 27 shows typical buck configuration with external PMOS transistor. The principle of driving the Q2 gate is the same as shown in Figure 27.

Resistor R6 connected between TC and SWE pin provides a pulsed feedback voltage. It is recommended to use this pulsed feedback approach on applications with a wide input voltage range, applications with the input voltage over +12 V or applications with tighter specifications on output ripple. The suitable value of resistor R6 is between 10k – 68k. The pulse feedback approach increases the operating frequency by about 20%. It also creates more regular switching waveforms with constant operating frequency which results in lower output ripple voltage and improved efficiency.

The pulse feedback resistor value has to be selected so that the capacitor charge and discharge currents as listed in the electrical characteristic table, are not exceeded. Improper selection will lead to errors in the oscillator operation. The maximum voltage at the TC Pin cannot exceed 1.4 V when implementing pulse feedback.

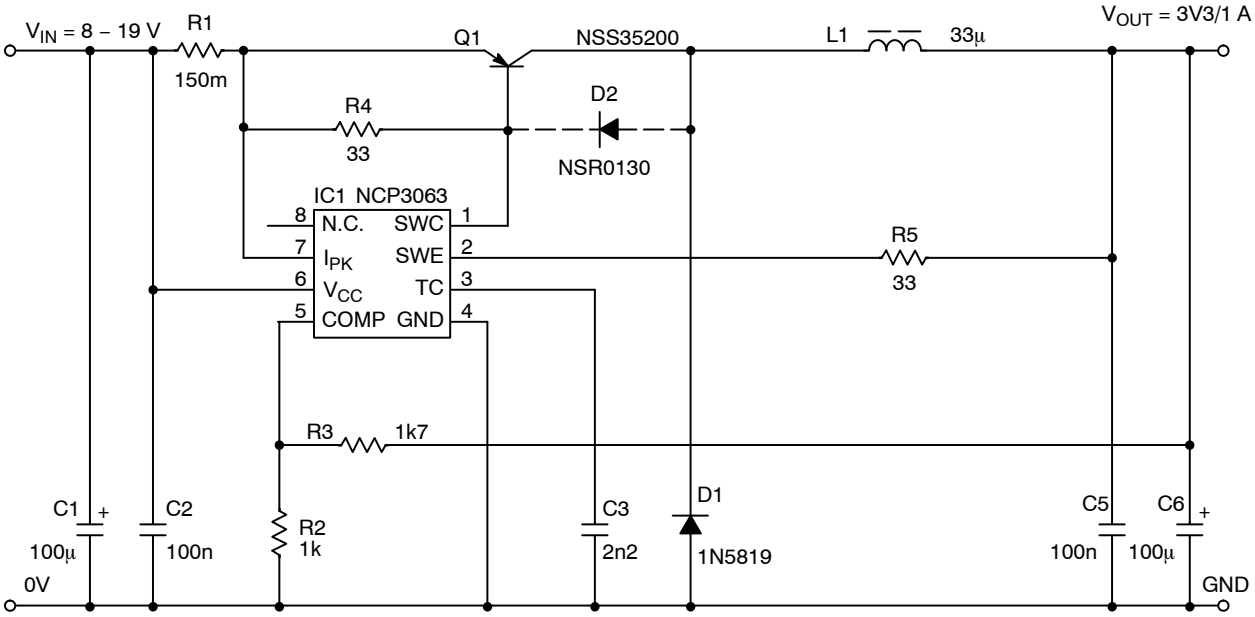


Figure 29. Typical Buck Application Schematic with External Low V_{CE}(sat) PNP Transistor

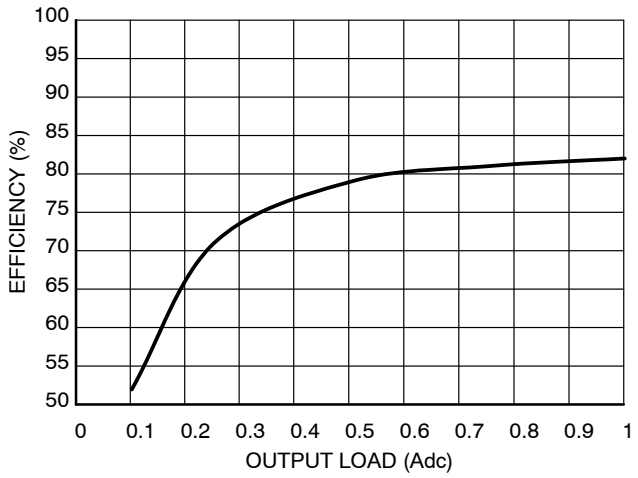


Figure 30. NCP3063 Efficiency vs. Output Current for External Low $V_{CE(sat)}$ at V_{in} = +5 V, f = 160 kHz, T_A = 25°C

Typical application of the buck converter with external bipolar transistor is shown in the Figure 29. It is an ideal solution for configurations where the input and output voltage difference is small and high efficiency is required. NSS35200, the low $V_{CE(sat)}$ transistor from **onsemi** will be ideal for applications with 1 A output current, the input voltages up to 15 V and operating frequency 100 – 150 kHz. The switching speed could be improved by using desaturation diode D2.

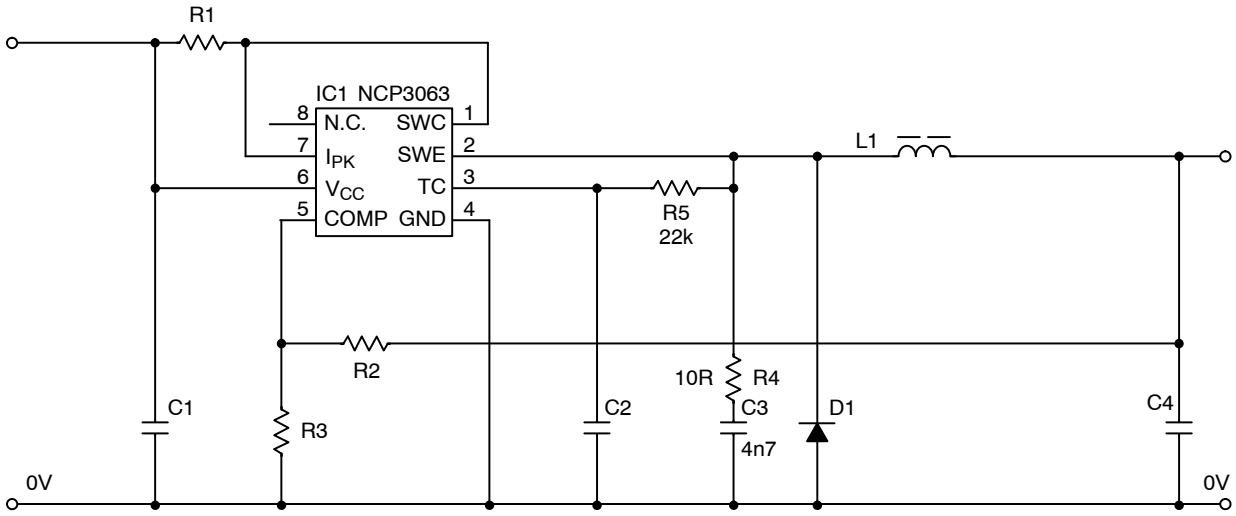


Figure 31. Typical Schematic of Buck Converter with RC Snubber and Pulse Feedback

In some cases where there are oscillations on the output due to the input/output combination, output load variations or PCB layout a snubber circuit on the SWE Pin will help minimize the oscillation. Typical usage is shown in the Figure 31. C3 values can be selected between 2.2 nF and 6.8 nF and R4 can be from 10 Ω to 22 Ω.

ORDERING INFORMATION

Device	Package	Shipping†
NCP3063PG	PDIP−8 (Pb−Free)	50 Units / Rail
NCP3063BPG	PDIP−8 (Pb−Free)	50 Units / Rail
NCP3063BMNTXG	DFN−8 (Pb−Free)	4000 / Tape & Reel
NCP3063DR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP3063BDR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP3063MNTXG	DFN−8 (Pb−Free)	4000 / Tape & Reel
NCV3063PG	PDIP−8 (Pb−Free)	50 Units / Rail
NCV3063DR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCV3063MNTXG	DFN−8 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

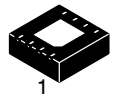
NCV prefix is for automotive and other applications requiring site and change control.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

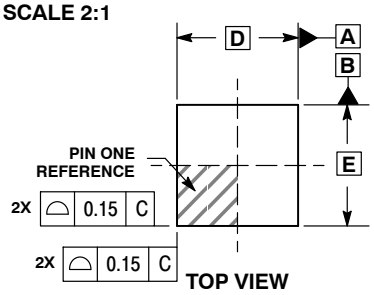
ON Semiconductor®

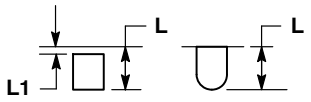
DFN8, 4x4
CASE 488AF−01
ISSUE C

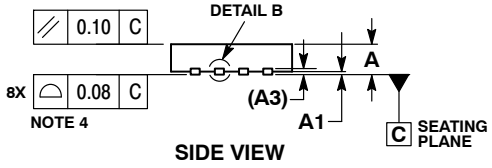
DATE 15 JAN 2009

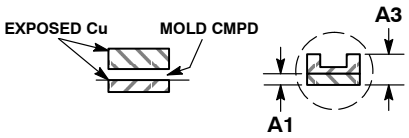


SCALE 2:1



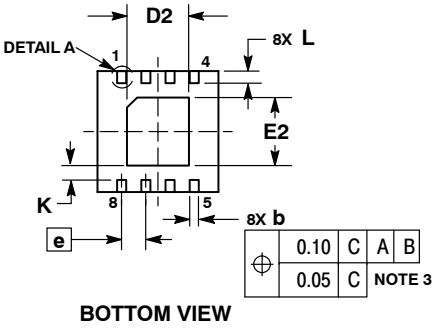




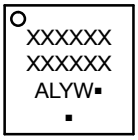


NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DETAILS A AND B SHOW OPTIONAL CONSTRUCTIONS FOR TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	4.00 BSC	
D2	1.91	2.21
E	4.00 BSC	
E2	2.09	2.39
e	0.80 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15



GENERIC MARKING DIAGRAM*

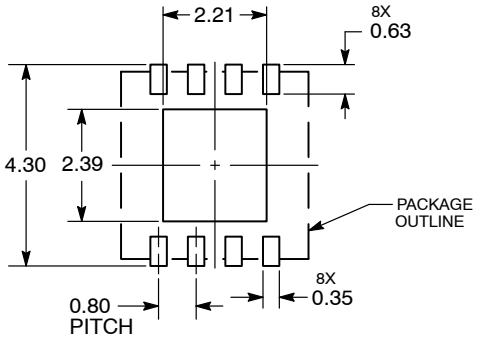


XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON15232D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	DFN8, 4X4, 0.8P	PAGE 1 OF 1

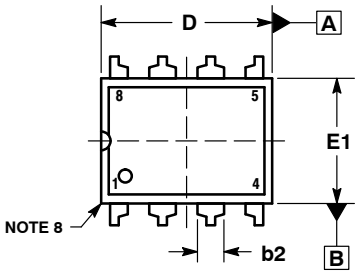
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

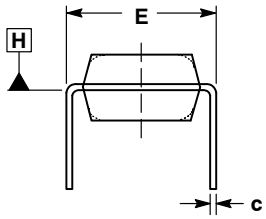
SCALE 1:1

PDIP–8
CASE 626–05
ISSUE P

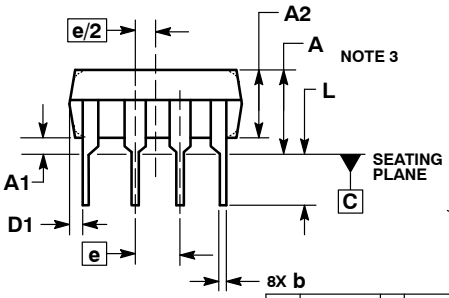
DATE 22 APR 2015



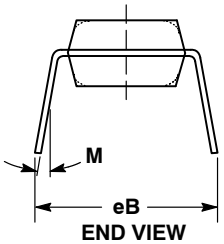
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW



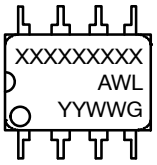
END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC – IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	98ASB42420B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	PDIP–8	PAGE 1 OF 1

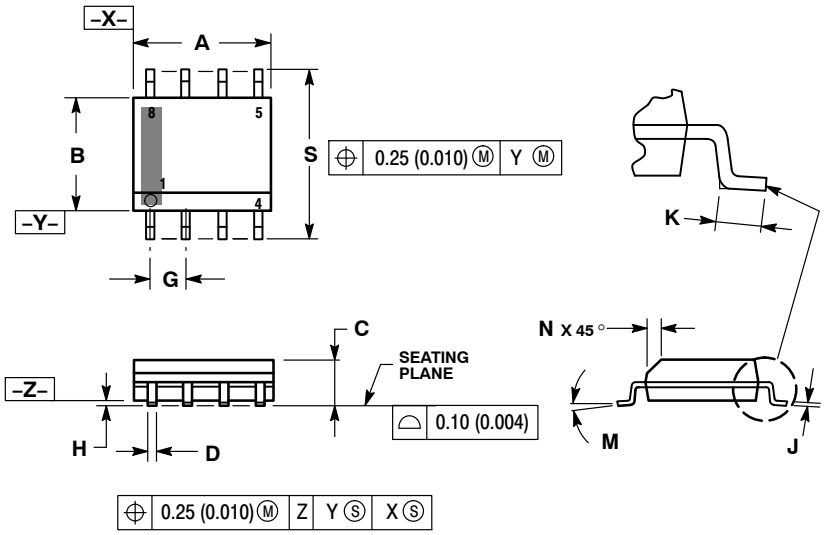
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

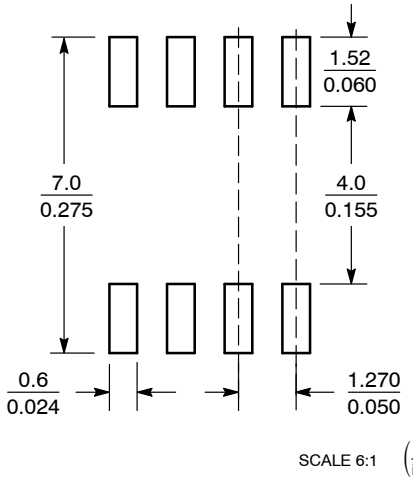
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

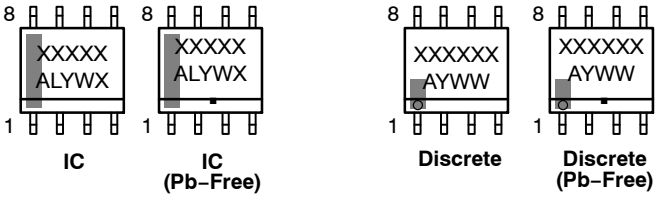
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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