NCP336, NCP337

Controlled Load Switch with Auto-Discharge Path, 3 A

Description

The NCP336 and NCP337 are very low Ron MOSFET controlled by external logic pin, allowing optimization of battery life, and portable device autonomy.

Indeed, thanks to a current consumption optimization with PMOS structure, leakage currents are eliminated by isolating connected IC on the battery when not used.

Output discharge path is also embedded to eliminate residual voltages on the output rail for the NCP337 part only.

Proposed in a wide input voltage range from 1.2 V to 5.5 V, in a small 1 x 1.5 mm WLCSP6, pitch 0.5 mm.

Features

- 1.2 V – 5.5 V Operating Range
- 21 mΩ P MOSFET at 4.5 V
- DC Current up to 3 A
- Output Auto−Discharge
- Active High EN Pin
- WLCSP6 1 x 1.5 mm
- This Device is Pb−Free, Halogen Free/BFR Free and is RoHS Compliant

Applications

- Mobile Phones
- Tablets
- Digital Cameras
- GPS
- Portable Devices

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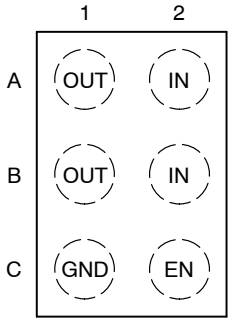
WLCSP6
FC SUFFIX
CASE 567FH

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

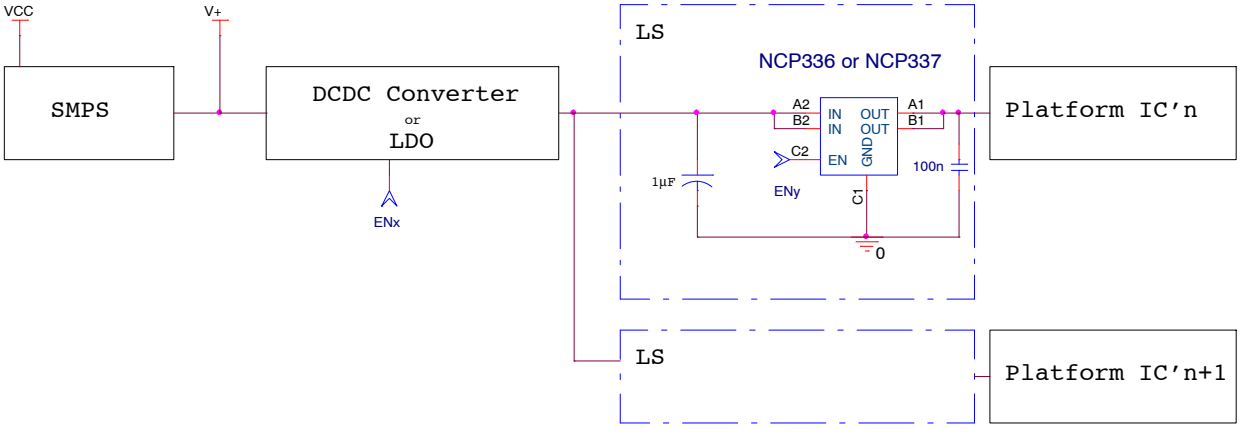


Figure 1. Typical Application Circuit

Table 1. PIN FUNCTION DESCRIPTION

Pin Name	Pin Number	Type	Description
IN	A2, B2	POWER	Load−switch input voltage; connect a 1 μF or greater ceramic capacitor from IN to GND as close as possible to the IC.
GND	C1	POWER	Ground connection.
EN	C2	INPUT	Enable input, logic high turns on power switch.
OUT	A1, B1	OUTPUT	Load−switch output; connect a 1 μF ceramic capacitor from OUT to GND as close as possible to the IC is recommended.

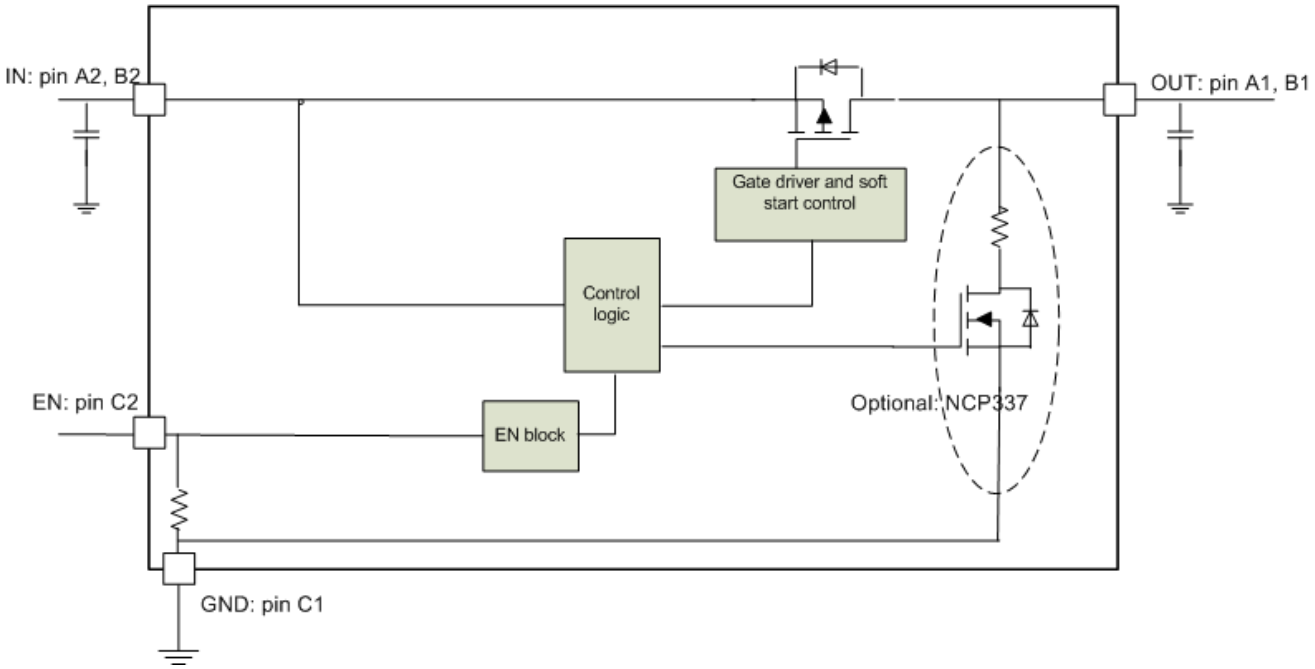


Figure 2. Block Diagram

Table 2. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IN, OUT, EN, Pins: (Note 1)	V_{EN}, V_{IN}, V_{OUT}	−0.3 to + 7.0	V
From IN to OUT Pins: Input/Output (Note 1)	V_{IN}, V_{OUT}	0 to + 7.0	V
Maximum Junction Temperature	T_J	−40 to + 125	°C
Storage Temperature Range	T_{STG}	−40 to + 150	°C
Moisture Sensitivity (Note 2)	MSL	Level 1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. OPERATING CONDITIONS

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IN}	Operational Power Supply			1.2		5.5	V
V_{EN}	Enable Voltage			0		5.5	
T_A	Ambient Temperature Range			−40	25	+85	°C
T_J	Junction Temperature Range			−40	25	+125	°C
C_{IN}	Decoupling input capacitor			1			μF
C_{OUT}	Decoupling output capacitor			1			μF
$R_{\theta JA}$	Thermal Resistance Junction to Air	WLCSP package (Note 3)			100		°C/W
I_{OUT}	Maximum DC current					3	A
P_D	Power Dissipation Rating (Note 4)	$T_A \le 25°C$	WLCSP package		0.66		W
		$T_A = 85°C$	WLCSP package		0.26		W

1. According to JEDEC standard JESD22−A108.
2. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020.
3. The $R_{\theta JA}$ is dependent of the PCB heat dissipation and thermal via.
4. The maximum power dissipation ($_{PD}$) is given by the following formula:

$$P_D = \frac{T_{JMAX} - T_A}{R_{\theta JA}}$$

Table 4. ELECTRICAL CHARACTERISTIC Min & Max Limits apply for T_A between −40°C to +85°C for V_{IN} between 1.2 V to 5.5 V (Unless otherwise noted). Typical values are referenced to T_A = +25°C and V_{IN} = 5 V (Unless otherwise noted).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
POWER SWITCH							
R_{DSON}	Static drain−source on−state resistance	Vin = 5.5 V	I = 1 A (Note 5)		20	22	mΩ
		Vin = 4.5 V	I = 500 mA (Note 5)		21	25	
		Vin = 3.3 V	I = 500 mA (Note 5)		23	28	
		Vin = 2.5 V	I = 500 mA (Note 5)		28	35	
		Vin = 1.8 V	I = 250 mA (Note 5)		40	45	
		Vin = 1.2 V	T_A = 25°C, I = 200 mA		95	120	
Rdis	Output discharge path	EN = low			70	90	Ω
V_{IH}	High−level input voltage			0.9			V
V_{IL}	Low−level input voltage					0.5	
R_{pd}	EN pull down resistor				5		MΩ
QUIESCENT CURRENT							
Istd	Standby current	Vin = 4.2 V	EN = low, No load			1	μA
Iq	Quiescent current	Vin = 4.2 V	EN = high, No load			1	μA
TIMINGS							
T_{EN}	Enable time	Vin = 3.6 V (Note 6)	R_L = 25 Ω, Cout = 1 μF		323		μs
T_R	Output rise time		R_L = 25 Ω, Cout = 1 μF		810		
T_{ON}	ON time (T_{EN} + T_R)		R_L = 25 Ω, Cout = 1 μF		1130		
T_F	Output fall time		NCP337. R_L = 25 Ω, Cout = 1 μF		42		

5. Guaranteed by design and characterization
6. Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the OUT pin with respect to the ground

TIMINGS

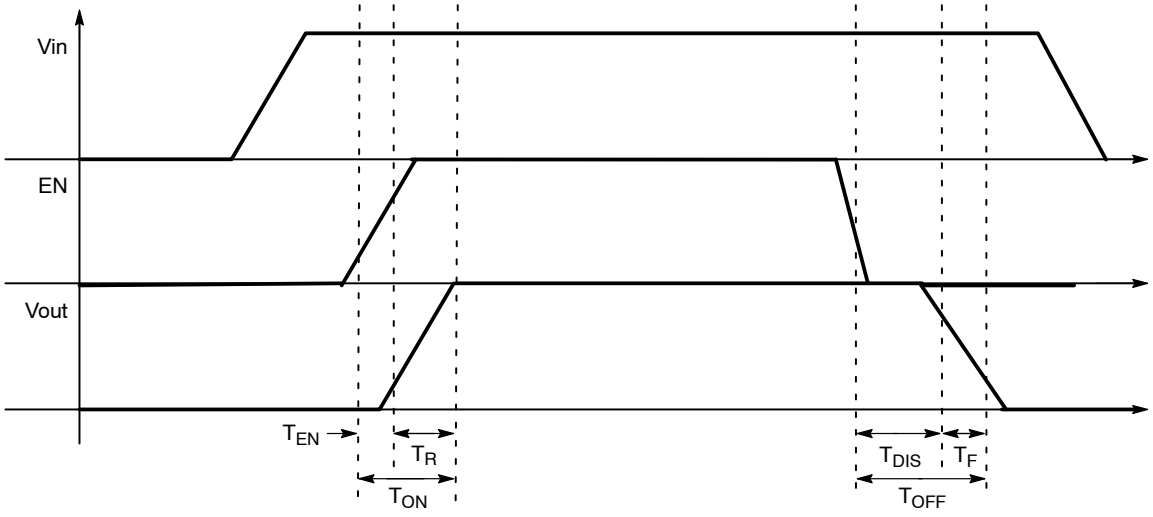


Figure 3. Enable, Rise and Fall Time

TYPICAL CHARACTERISTICS

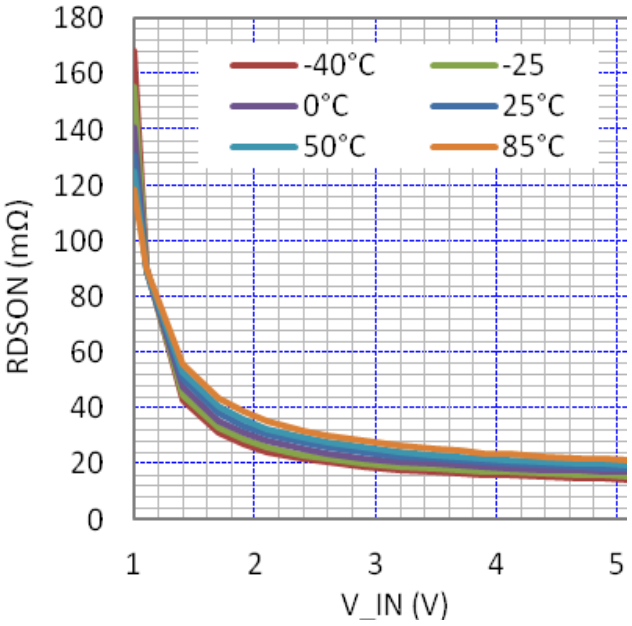


Figure 4. Rdson (mΩ) vs. Vin (V)

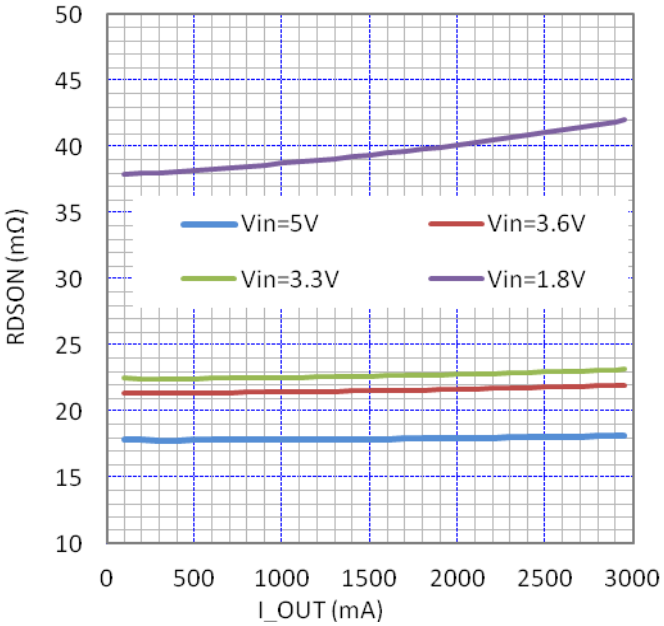


Figure 5. Rdson (mΩ) vs. Iload (A)

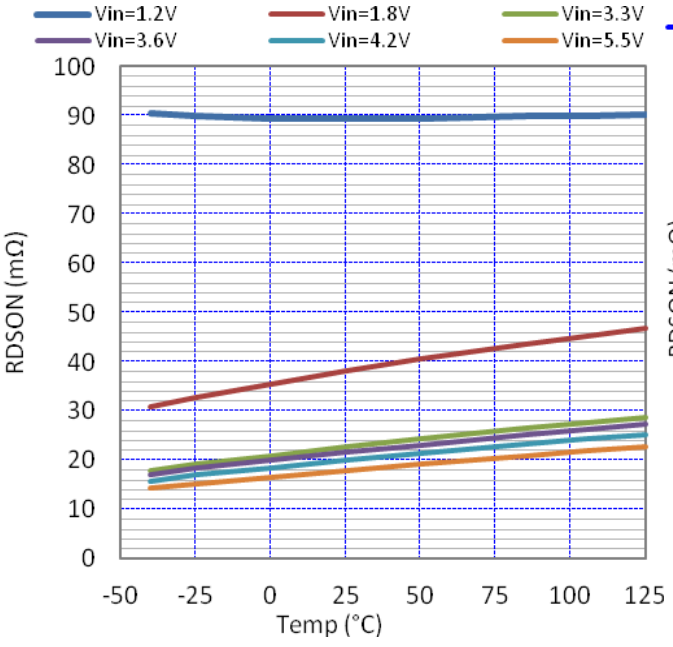


Figure 6. Rdson (mΩ) vs. Temperature (°C) at 100 mA

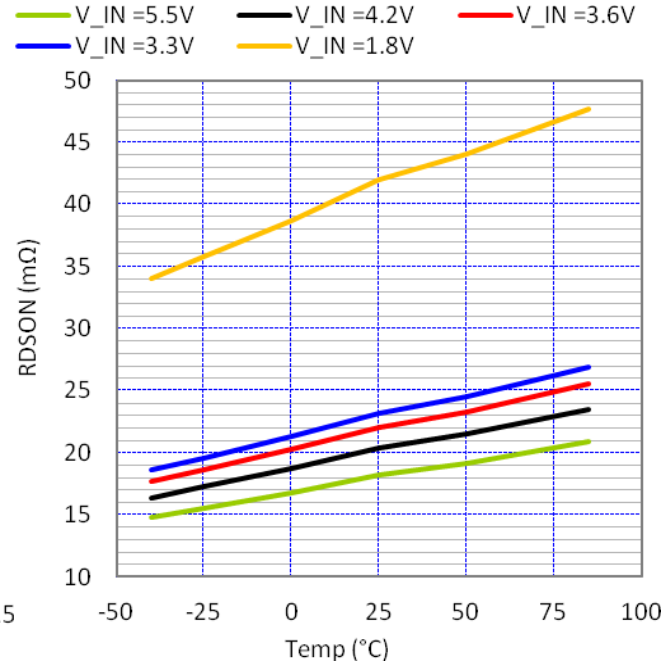


Figure 7. Rdson (mΩ) vs. Temperature (°C) at 3 A

TYPICAL CHARACTERISTICS

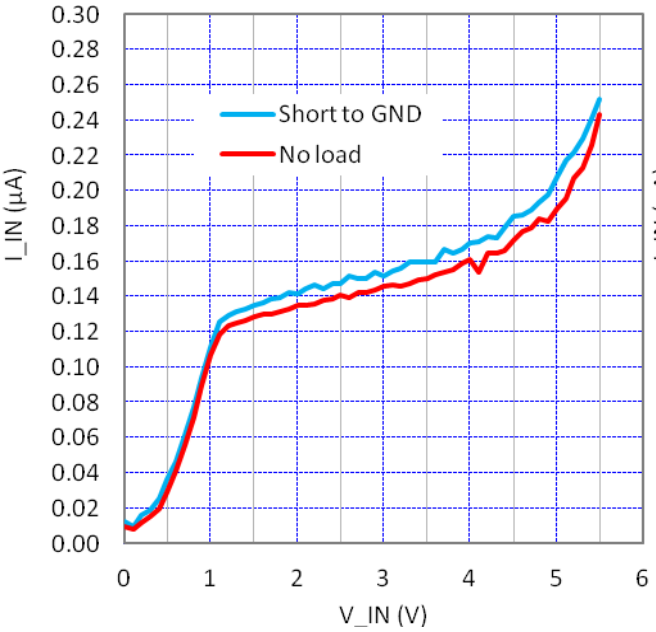


Figure 8. Standby (µA) and Leakage Current (µA) vs. Vin (V)

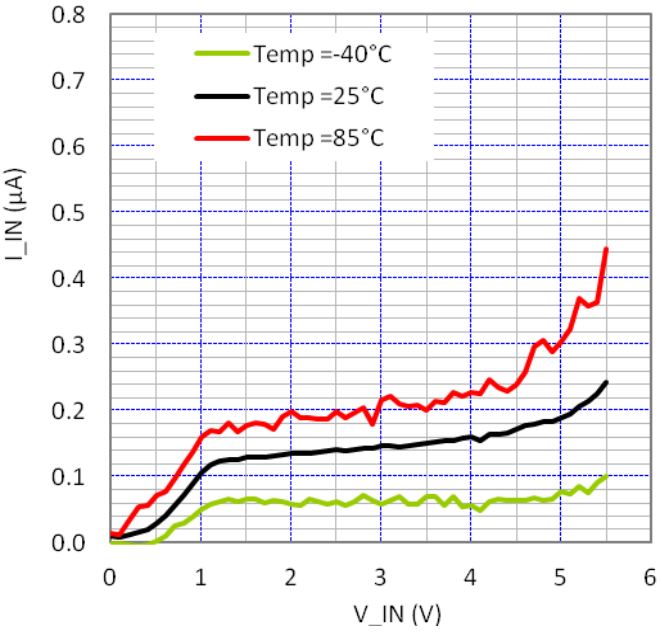


Figure 9. Standby Current (µA) vs. Temperature (°C)

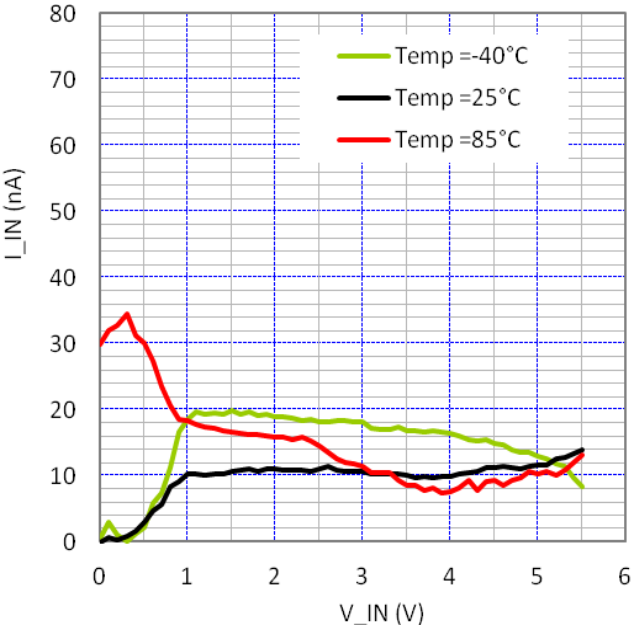


Figure 10. Leakage Current (µA) vs. Temperature (°C)

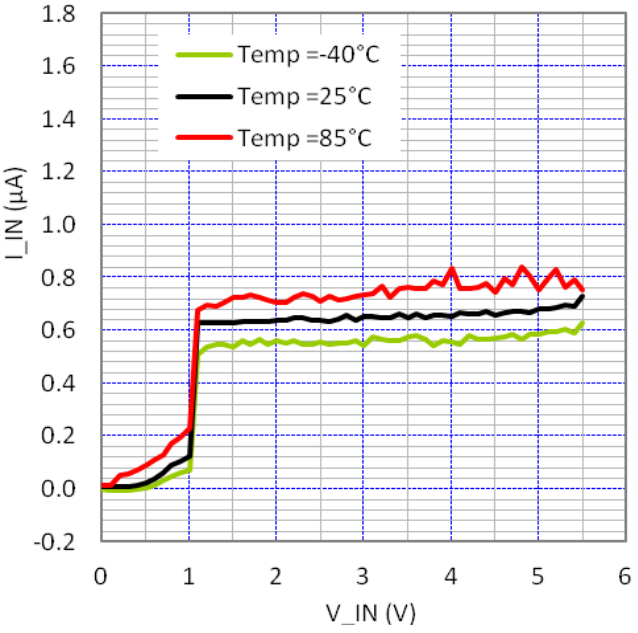


Figure 11. Quiescent Current (µA) vs. Temperature (°C)

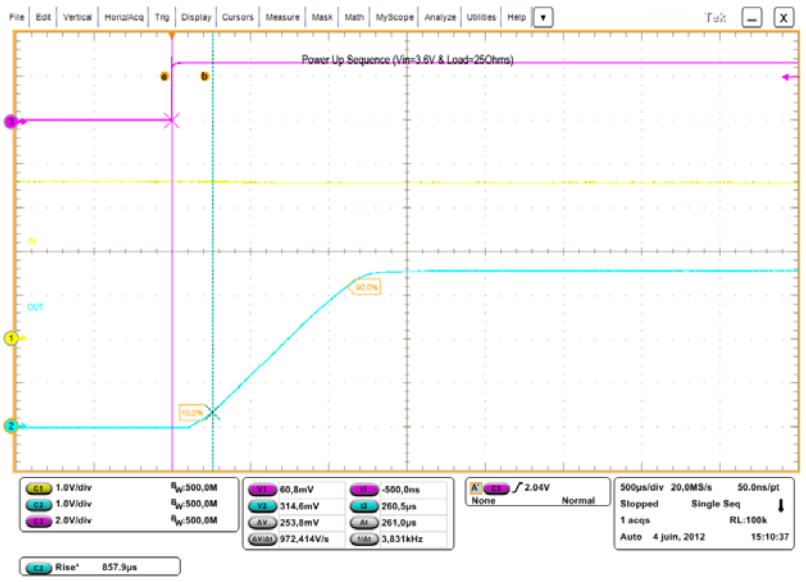


Figure 12. Enable Time and Rise Time

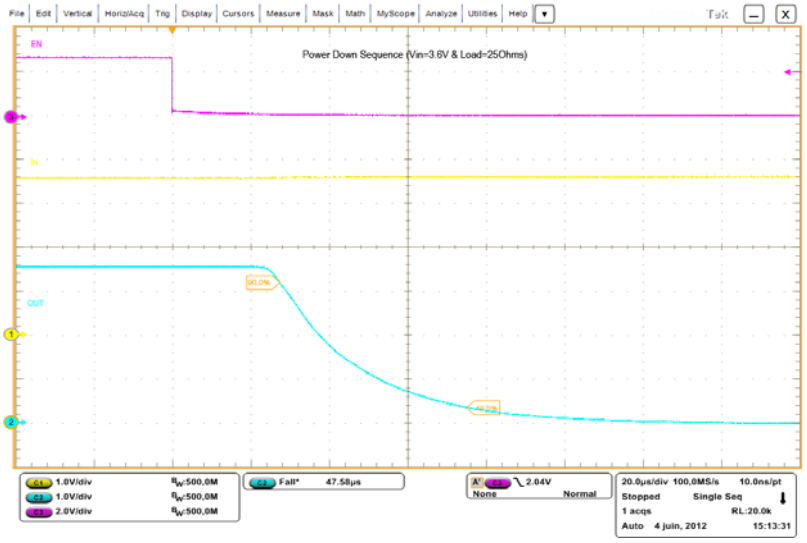


Figure 13. Disable Time and Fall Time

FUNCTIONAL DESCRIPTION

Overview

The NCP337 is a high side P channel MOSFET power distribution switch designed to isolate ICs connected on the battery in order to save energy. The part can be turned on, with a wide range of battery from 1.2 V to 5.5 V.

Enable Input

Enable pin is an active high. The path is opened when EN pin is tied low (disable), forcing P MOS switch off.

The IN/OUT path is activated with a minimum of Vin of 1.2 V and EN forced to high level.

Auto Discharge

NMOS FET is placed between the output pin and GND, in order to discharge the application capacitor connected on OUT pin.

The auto−discharge is activated when EN pin is set to low level (disable state).

The discharge path (Pull down NMOS) stays activated as long as EN pin is set at low level and Vin > 1.2 V.

In order to limit the current across the internal discharge Nmosfet, the typical value is set at 70 Ω.

Cin and Cout Capacitors

IN and OUT, 1 µF, at least, capacitors must be placed as close as possible the part to for stability improvement.

APPLICATION INFORMATION

Power Dissipation

Main contributor in term of junction temperature is the power dissipation of the power MOSFET. Assuming this, the power dissipation and the junction temperature in normal mode can be calculated with the following equations:

- $P_D = R_{DS(on)} \times (I_{OUT})^2$
  P_D = Power dissipation (W)
  $R_{DS(on)}$ = Power MOSFET on resistance (Ω)
  I_{OUT} = Output current (A)
- $T_J = P_D \times R_{\theta JA} + T_A$
  T_J = Junction temperature (°C)
  $R_{\theta JA}$ = Package thermal resistance (°C/W)
  T_A = Ambient temperature (°C)

PCB Recommendations

The NCP337 integrates an up to 3 A rated PMOS FET, and the PCB design rules must be respected to properly evacuate the heat out of the silicon. By increasing PCB area, especially around IN and OUT pins, the $R_{\theta JA}$ of the package can be decreased, allowing higher power dissipation.

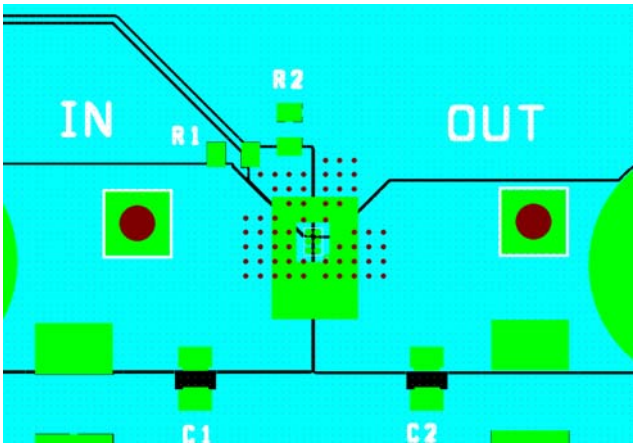


Figure 14. Routing Example: 2 oz, 4 layers with vias across 2 internal inners.

Example of application definition.

$$T_J - T_A = R_{\theta JA} \times P_D = R_{\theta JA} \times R_{DS(on)} \times I^2$$

T_J: junction temperature.
T_A: ambient temperature.
R_θ = Thermal resistance between IC and air, through PCB.
$R_{DS(on)}$: intrinsic resistance of the IC Mosfet.
I: load DC current.

Taking into account of R_θ obtain with:

- 1 oz, 2 layers: 100°C/W.

At 3 A, 25°C ambient temperature, $R_{DS(on)}$ 20 mΩ @ Vin 5 V, the junction temperature will be:

$$T_J = T_A + R_\theta \times P_D = 25 + (0.024 \times 3^2) \times 100 = 43°C$$

Taking into account of R_θ obtain with:

- 2 oz, 4 layers: 60°C/W.

At 3 A, 65°C ambient temperature, $R_{DS(on)}$ 24 mΩ @ Vin 5 V, the junction temperature will be:

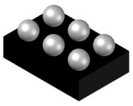
$$T_J = T_A + R_\theta \times P_D = 65 + (0.024 \times 3^2) \times 60 = 78°C$$

ORDERING INFORMATION

Device	Marking	Option	Package	Shipping†
NCP337FCT2G	AC	Auto discharge	WLCSP 1 x 1.5 mm	3000 Tape / Reel
NCP336FCT2G	AF	Without Autodischarge	WLCSP 1 x 1.5 mm	3000 Tape / Reel

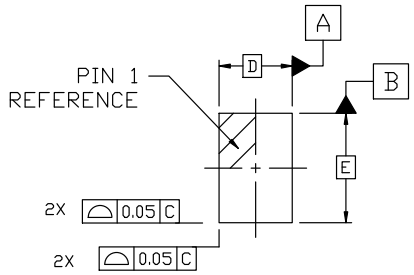
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

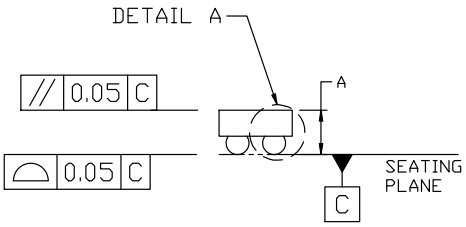


WLCSP6 1.0x1.5x0.609
CASE 567FH
ISSUE A

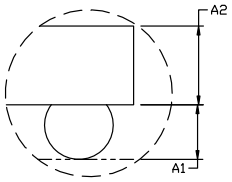
DATE 21 JUN 2022



TOP VIEW



SIDE VIEW

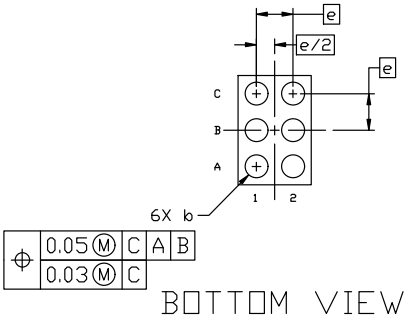


DETAIL A
SCALE 1:3

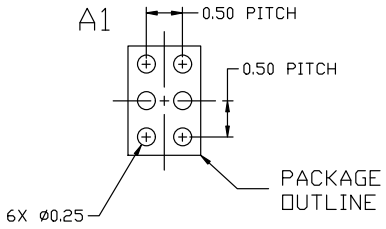
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.554	0.609	0.664
A1	0.219	0.249	0.279
A2	0.335	0.360	0.385
b	0.282	0.312	0.342
D	1.00 BSC		
E	1.50 BSC		
e	0.50 BSC		



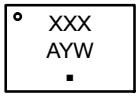
BOTTOM VIEW



RECOMMENDED
MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON79918E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	WLCSP6 1.0x1.5x0.609	PAGE 1 OF 1