NCP81172

2-Phase Synchronous Buck Controller with Integrated Gate Drivers and PWM VID Interface

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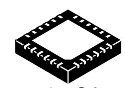
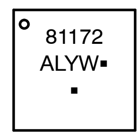
The NCP81172, a general−purpose two−phase synchronous buck controller, integrates gate drivers and PWM VID interface in a QFN−24 package and provides a compact−footprint power management solution for new generation computing processors. It receives power save command (PSI) from processors and operates in 1−phase diode emulation mode to obtain high efficiency in light−load condition. Operating in high switching frequency up to 800 kHz allows employing small size inductor and capacitors. The part is able to support all−ceramic−capacitor applications.



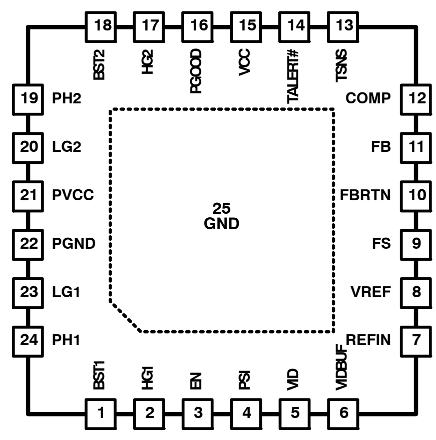
QFN24
CASE 485L

MARKING DIAGRAM



81172	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PINOUT



(Top View)

Features

- 4.5 V to 24 V Input Voltage Range
- Output Voltage up to 2.0 V with PWM VID Interface
- Differential Output Voltage Sense
- Integrated Gate Drivers
- 200 kHz ~ 800 kHz Switching Frequency
- Power Saving Interface (PSI)
- Power Good Output
- Programmable Over Current Protection
- Over Voltage Protection
- Under Voltage Protection
- Temperature Sense and Alert Output
- Thermal Shutdown Protection
- QFN−24, 4 x 4 mm, 0.5 mm Pitch Package
- This is a Pb−Free Device

Typical Applications

- GPU and CPU Power
- Graphics Card Applications
- Desktop and Notebook Applications

ORDERING INFORMATION

Device	Package	Shipping†
NCP81172MNTXG	QFN24 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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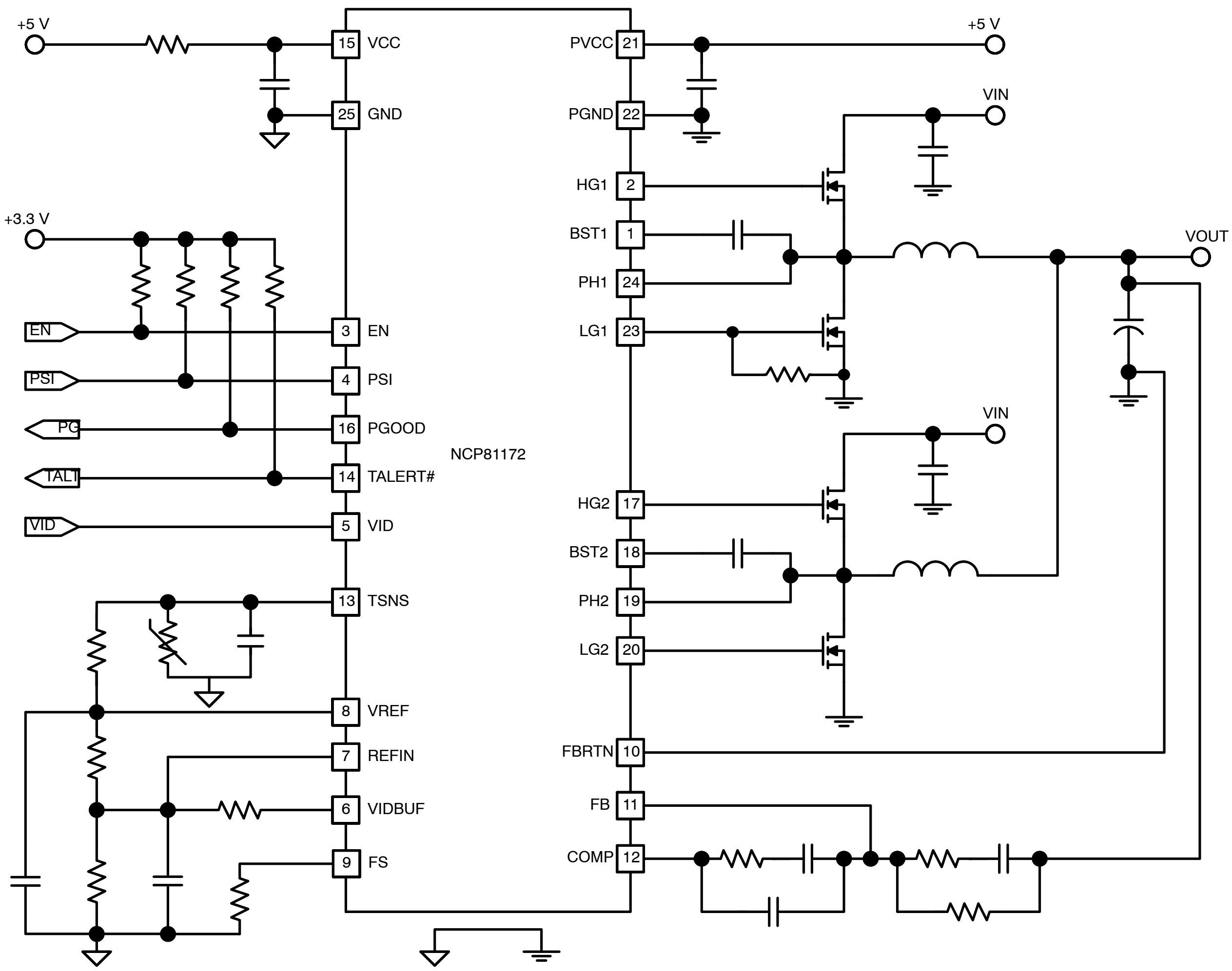

Figure 1. Typical Application Circuit with PWM−VID Interface

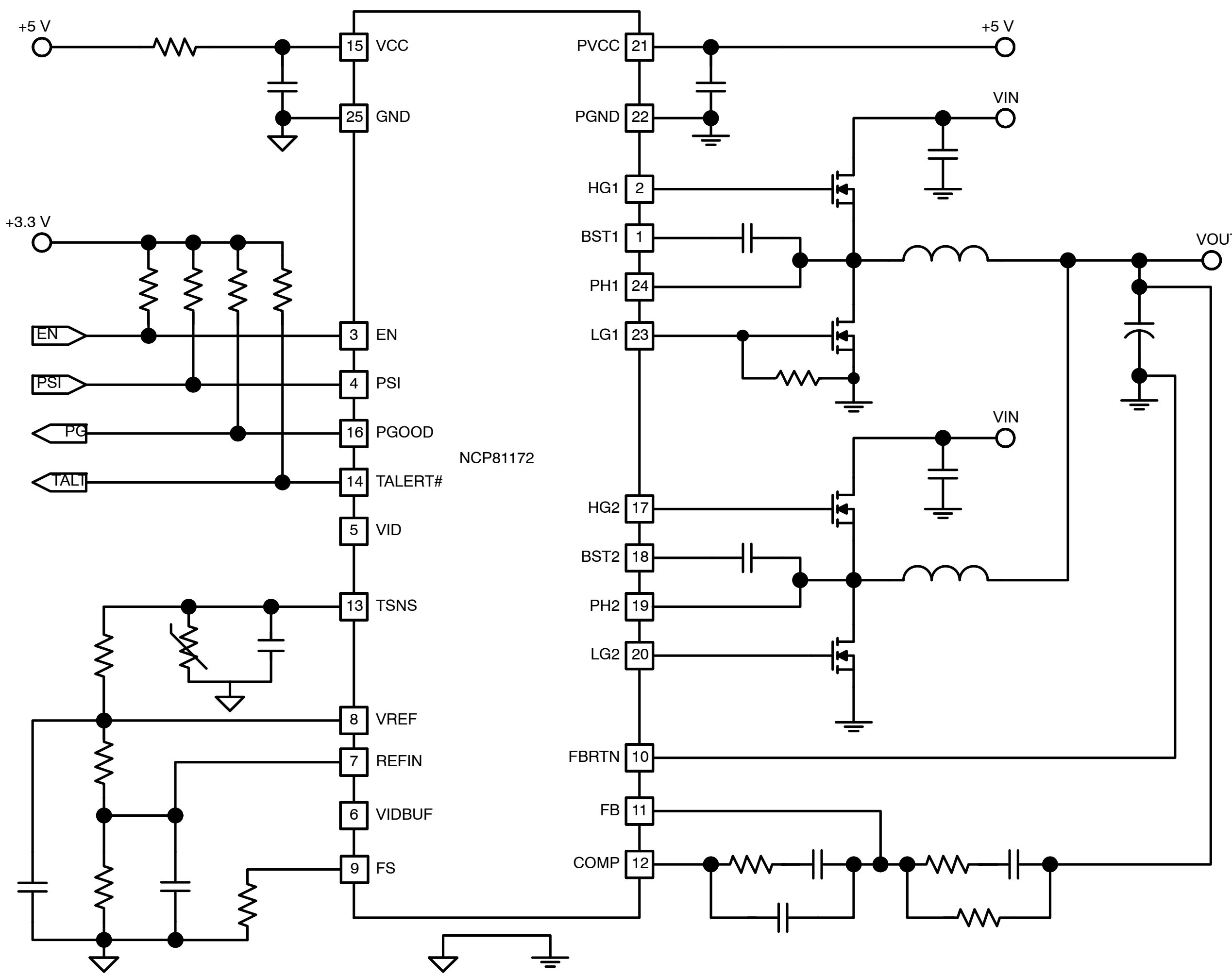

Figure 2. Typical Application Circuit without PWM−VID Interface

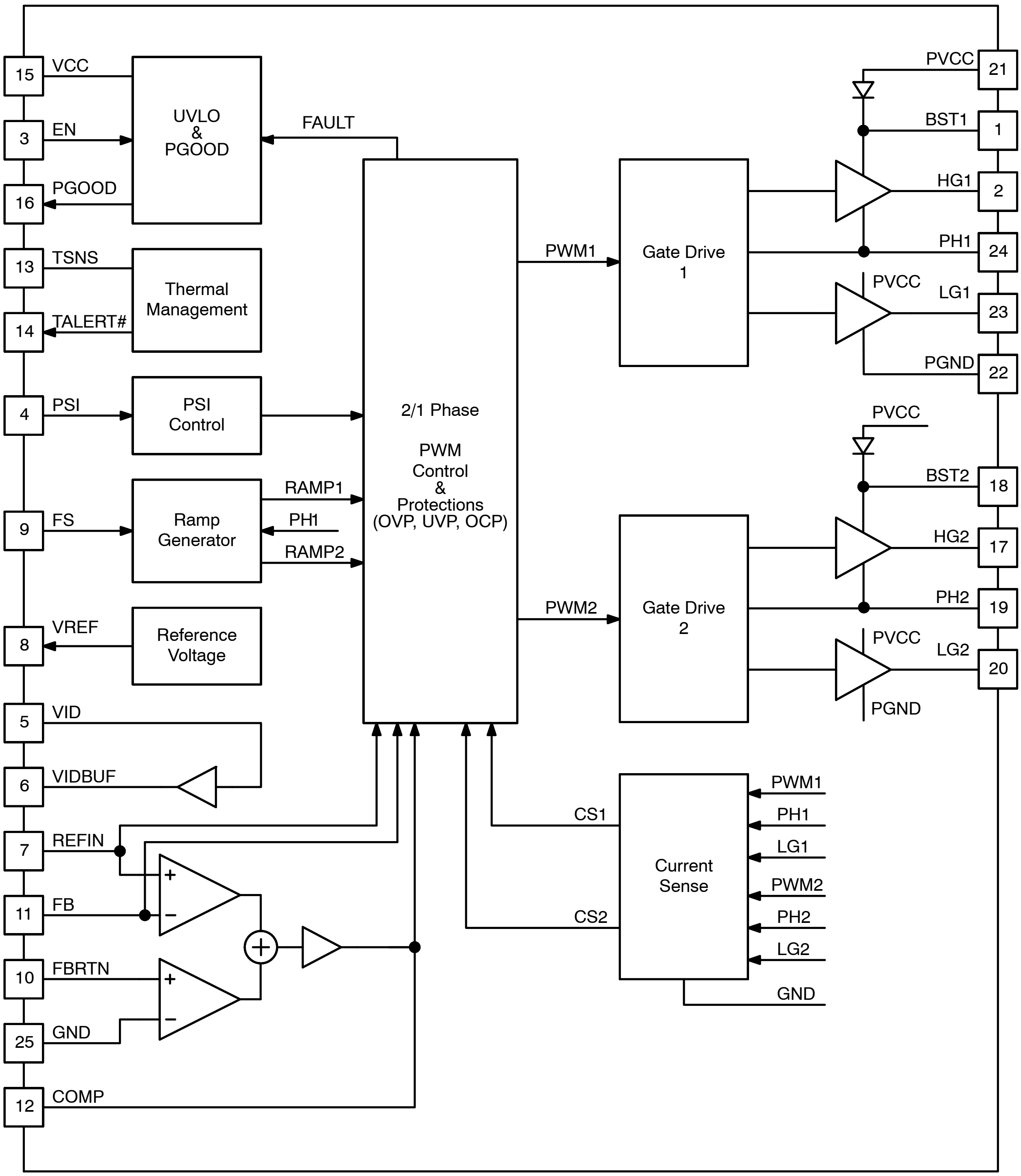

Figure 3. Functional Block Diagram

PIN DESCRIPTION

Pin	Name	Type	Description
1	BST1	Analog Power	Bootstrap 1. Provides bootstrap voltage for the high−side gate drive of phase 1. A 0.1 μF ~ 1 μF ceramic capacitor is required from this pin to PH1 (pin 24).
2	HG1	Analog Output	High−Side Gate 1. Directly connected with the gate of the high−side power MOSFET of phase 1.
3	EN	Logic Input	Enable. Logic high enables the device and logic low makes the device in standby mode.
4	PSI	Logic Input	Power Saving Interface. Logic high enables 2 phase CCM operation, mid level enables 1−phase CCM operation, and logic low enables 1−phase CCM/DCM operation.
5	VID	Logic Input	Voltage ID. Voltage ID input from processor.
6	VIDBUF	Analog Output	Voltage ID Buffer. VID PWM pulse output from an internal buffer.
7	REFIN	Analog Input	Reference Input. Reference voltage input for output voltage regulation. The pin is connected to a non−inverting input of internal error amplifier.
8	VREF	Analog Output	Output Reference Voltage. Precise 2 V reference voltage output. A 10 nF ceramic capacitor is required from this pin to GND.
9	FS	Analog Input	Frequency Selection. A resistor from this pin to ground programs switching frequency.
10	FBRTN	Analog Input	Voltage Feedback Return Input. An inverting input of internal error amplifier.
11	FB	Analog Input	Feedback. An inverting input of internal error amplifier.
12	COMP	Analog Output	Compensation. Output pin of error amplifier.
13	TSNS	Analog Input	Temperature Sensing. Temperature sensing input.
14	TALERT#	Logic Output	Thermal Alert. Open drain output and active low indicates over temperature.
15	VCC	Analog Power	Voltage Supply of Controller. Power supply input pin of control circuits. A 1 μF or larger ceramic capacitor bypasses this input to GND. This capacitor should be placed as close as possible to this pin.
16	PGOOD	Logic Output	Power GOOD. Open−drain output. Provides a logic high valid power good output signal, indicating the regulator’s output is in regulation window.
17	HG2	Analog Output	High−Side Gate 2. Connected with the gate of the high−side power MOSFET in phase 2.
18	BST2	Analog Power	Bootstrap 2. Provides bootstrap voltage for the high−side gate drive of phase 2. A 0.1 μF ~ 1 μF ceramic capacitor is required from this pin to PH2 (pin 19).
19	PH2	Analog Input	Phase Node 2. Connected to interconnection between high−side MOSFET and low−side MOSFET in phase 2.
20	LG2	Analog Output	Low−Side Gate 2. Connected with the gate of the low−side power MOSFET in phase 2.
21	PVCC	Analog Power	Voltage Supply of Gate Drivers. Power supply input pin of internal gate drivers. A 4.7 μF or larger ceramic capacitor bypasses this input to ground. This capacitor should be placed as close as possible to this pin.
22	PGND	Analog Ground	Power Ground. Power ground of internal gate drivers. Must be connected to the system ground.
23	LG1	Analog Output	Low−Side Gate 1. Connected with the gate of the low−side power MOSFET in phase 1. A resistor may be applied between this pin and GND to program OCP threshold.
24	PH1	Analog Input	Phase Node 1. Connected to interconnection between high−side MOSFET and low−side MOSFET in phase 1.
25	THERM/GND	Analog Ground	Thermal Pad and Analog Ground. Ground of internal control circuits. Must be connected to the system ground.

MAXIMUM RATINGS

Rating	Symbol	Value		Unit
		MIN	MAX	
PH to PGND	V_{PH}	−2 −8 (<100 ns)	30	V
Gate Driver Supply Voltage PVCC to GND	V_{PVCC}	−0.3	6.5	V
Supply Voltage VCC to GND	V_{VCC}	−0.3	6.5	V
BST to PGND	V_{BST_PGND}	−0.3	35	V
BST to PH	V_{BST_PH}	−0.3	6.5	V
HG to PH	V_{HG}	−0.3 −2 (<200 ns)	BST+0.3	V
LG to GND	V_{LG}	−0.3 −2 (<200 ns)	PVCC+0.3	V
PGND to GND	V_{PGND}	−0.3	0.3	V
FBRTN to GND	V_{FBRTN}	−0.3	0.3	V
Other Pins to GND		−0.3	VCC+0.3	V
Human Body Model (HBM) ESD Rating Are (Note 1)	ESD HBM		2000	V
Machine Model (MM) ESD Rating Are (Note 1)	ESD MM		200	V
Latch up Current: (Note 2) All pins, except digital pins Digital pins	I_{LU}	 −100 −10	 100 10	mA
Operating Junction Temperature Range (Note 4)	T_J	−40	125	°C
Operating Ambient Temperature Range	T_A	−40	100	°C
Storage Temperature Range	T_{STG}	−40	150	°C
Thermal Resistance Junction to Top Case (Note 5)	$R_{\Psi JC}$	6.0		°C/W
Thermal Resistance Junction to Board (Note 5)	$R_{\Psi JB}$	7.5		°C/W
Thermal Resistance Junction to Ambient (Note 4)	$R_{\theta JA}$	50		°C/W
Power Dissipation (Note 6)	P_D	2.0		W
Moisture Sensitivity Level (Note 7)	MSL	1		–

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device is ESD sensitive. Handling precautions are needed to avoid damage or performance degradation.
2. Latch up Current per JEDEC standard: JESD78 class II.
3. The thermal shutdown set to 150°C (typical) avoids potential irreversible damage on the device due to power dissipation.
4. EDEC standard JESD 51−7 (1S2P Direct−Attach Method) with 0 LFM.
5. JEDEC standard JESD 51−7 (1S2P Direct−Attach Method) with 0 LFM. For checking junction temperature using external measurement.
6. The maximum power dissipation (PD) is dependent on input voltage, maximum output current and external components selected. T ambient = 25°C, Tjunc_max = 125°C, PD = (Tjunc_max−T_amb)/Theta JA
7. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12 V, V_{VCC} = V_{PVCC} = 5 V, V_{REFIN} = 1.0 V, V_{PSI} = 3.3 V, typical values are referenced to T_J = 25°C, Min and Max values are referenced to T_J from −40°C to 100°C. unless other noted)

Characteristics	Test Conditions	Symbol	Min	Typ	Max	Unit
SUPPLY VOLTAGE						
VIN Supply Voltage Range	(Note 8)	V_{IN}	4.5	12	24	V
VCC Supply Voltage Range	(Note 8)	V_{CC}	4.5	5	5.5	V

8. Guaranteed by design, not tested in production.

ELECTRICAL CHARACTERISTICS (continued)
(V_{IN} = 12 V, V_{VCC} = V_{PVCC} = 5 V, V_{REFIN} = 1.0 V, V_{PSI} = 3.3 V, typical values are referenced to T_J = 25°C, Min and Max values are referenced to T_J from −40°C to 100°C. unless other noted)

Characteristics	Test Conditions	Symbol	Min	Typ	Max	Unit
SUPPLY VOLTAGE						
PVCC Supply Voltage Range	(Note 8)	V_{PCC}	4.5	5	5.5	V
VCC Under−Voltage (UVLO) Threshold	VCC falling	V_{CCUV-}	4.0	4.05	4.2	V
VCC OK Threshold	VCC rising	V_{CCOK}	4.2	4.25	4.4	V
SUPPLY CURRENT						
VCC Quiescent Current	EN high, no switching, PS0 EN high, no switching, PS1/PS2	I_{CC}	– –	9 9	15 15	mA mA
VCC Shutdown Current	EN low	I_{sdCC}	–	30	50	μA
PVCC Quiescent Supply Current	EN high, no switching, PS0 EN high, no switching, PS1/PS2	I_{PCC}	– –	0.35 0.35	0.6 0.6	mA mA
PVCC Shutdown Current	EN low	I_{sdPCC}	–	–	2.0	μA
SWITCHING FREQUENCY SETTING						
PS0 Switching Frequency Range	(Note 8)	F_{SW}	200		800	kHz
FS Voltage	RFS = 39.2 kΩ	V_{FS}		2.0		V
VOLTAGE REFERENCE						
VREF Reference Voltage	I_{REF} = 1 mA	V_{VREF}	1.98	2.0	2.02	V
PWM MODULATION						
Minimum On Time	(Note 8)	T_{on_min}		50		ns
Minimum Off Time	(Note 8)	T_{off_min}		250		ns
Maximum Duty Cycle	(Note 8)	D_{max}	–	100	–	%
VOLTAGE ERROR AMPLIFIER						
Open−Loop DC Gain	(Note 8)	$GAIN_{EA}$		80		dB
Unity Gain Bandwidth	(Note 8)	GBW_{EA}		20		MHz
Slew Rate	(Note 8)	SR_{COMP}		20		V/μs
COMP Voltage Swing	I_{COMP}(source) = 2 mA	$V_{maxCOMP}$	3.2	3.4	–	V
	I_{COMP}(sink) = 2 mA	$V_{minCOMP}$	–	1.05	1.15	V
FB, REFIN Bias Current	V_{FB} = V_{REFIN} = 1.0 V	I_{FB}	−400		400	nA
Input Offset Voltage	V_{osEA} = V_{REFIN} − V_{FB} (Note 8)	V_{osEA}	−4		4	mV
REFIN Discharge Switch ON−Resistance	I_{REFIN} (sink) = 2 mA			6.25		Ω
CURRENT−SENSE AMPLIFIER						
Closed−Loop DC Gain		$GAIN_{CA}$		−5.5		V/V
−3dB Gain Bandwidth	(Note 8)	BW_{CA}		10		MHz
Input Offset Voltage	V_{osCS} = V_{PH} − V_{PGND} (Note 8)	V_{osCS}	−500	–	500	uV
ENABLE						
EN High Threshold		V_{highEN}	1.6	–	–	V
EN Low Threshold		V_{lowEN}	–	–	0.8	V
EN Input Bias Current	External 1k pull−up to 3.3 V	I_{biasEN}	–	–	1.0	μA

8. Guaranteed by design, not tested in production.

ELECTRICAL CHARACTERISTICS (continued)
(V_{IN} = 12 V, V_{VCC} = V_{PVCC} = 5 V, V_{REFIN} = 1.0 V, V_{PSI} = 3.3 V, typical values are referenced to T_J = 25°C, Min and Max values are referenced to T_J from −40°C to 100°C. unless other noted)

Characteristics	Test Conditions		Symbol	Min	Typ	Max	Unit
POWER SAVE INPUT							
PSI High Threshold	Rising		$V_{highPSI}$		2.4	2.55	V
	Falling			2.05	2.2		
PSI Low Threshold	Rising		V_{lowPSI}		0.8	0.95	V
	Falling			0.5	0.6		
PSI Input Bias Current			$I_{biasPSI}$	–	–	1.0	μA
SOFT START AND PGOOD							
Vout Startup Delay	Measured from EN to Vout Start up from 0 V				1.15		ms
Cout Startup Slew Rate					3.0		V/ms
PGOOD Startup Delay	Measured from EN to PGOOD assertion					2.0	ms
PGOOD Shutdown Delay	Measured from EN to PGOOD de−assertion				125		ns
PGOOD Low Voltage	I_{PGOOD}= 4 mA (sink)		V_{lPGOOD}	–	–	0.3	V
PGOOD Leakage Current	PGOOD = 5 V		$I_{lkgPGOOD}$	–	–	1.0	μA
PROTECTION							
Current Limit Threshold	Measured from PGND to Phx (R_{ILMT}(1%) is connected from LG1 to GND)	R_{ILMT} is open	V_{OCTH}	110	122	134	mV
		R_{ILMT} = 6.98 kΩ		72	82	92	
		R_{ILMT} = 21.0 kΩ		89	100	111	
		R_{ILMT} = 35.7 kΩ		146	163	180	
		R_{ILMT} = 49.9 kΩ		OCP is disabled			–
Fast Under Voltage Protection (FUVP) Threshold	Voltage from FB to GND			0.15	0.2	0.25	V
Faster Under Voltage Protection (FUVP) Delay	(Note 8)				2.0		μs
Slow Under Voltage Protection (SUVP) Threshold	Voltage from COMP to GND				3.0		V
Slow Under Voltage Protection (SUVP) Delay	(Note 8)				50		us
Over Voltage Protection (OVP) Threshold	Voltage from FB to GND			1.85	2.0	2.15	V
Over Voltage Protection (OVP) Delay	(Note 8)				2.0		μs
Over Temperature Protection (OTP) Threshold	(Note 8)		T_{sd}	140	150		°C
Recovery Temperature Threshold	(Note 8)		T_{rec}		125		°C
Over Temperature Protection (OTP) Delay	(Note 8)				125		ns
OUTPUT DISCHARGE							
Output Discharge Resistance per Phase	Measured from PHx to PGND when EN is low (Note 8)		$R_{dischrg}$		2		kΩ

8. Guaranteed by design, not tested in production.

ELECTRICAL CHARACTERISTICS (continued)
(V_{IN} = 12 V, V_{VCC} = V_{PVCC} = 5 V, V_{REFIN} = 1.0 V, V_{PSI} = 3.3 V, typical values are referenced to T_J = 25°C, Min and Max values are referenced to T_J from −40°C to 100°C. unless other noted)

Characteristics	Test Conditions	Symbol	Min	Typ	Max	Unit
TSENSE and ALERT						
TALERT# Assert Threshold	Measured at TSNS (Temperature Rising)	$V_{lowTSNS}$	0.99	1.00	1.01	V
TALERT# De−Assert Threshold	Measured at TSNS (Temperature Falling)	$V_{highTSNS}$	–	1.05	–	V
TALERT# Low Voltage	I_{ALERT}= 4 mA (sink)	$V_{lowALERT}$	–	–	0.3	V
TALERT# Leakage Current	TALERT# = 5 V	$I_{lkgALERT}$	–	–	1.0	μA
PWM−VID BUFFER						
VID Input Threshold				1.4		V
Buffer Output Rise Time		T_r		3		ns
Buffer Output Fall Time		T_f		3		ns
Rising and Falling Edge Delay	$\Delta T = \lvert T_r - T_f \rvert$ (Note 8)	ΔT			0.5	ns
Propagation Delay	$T_{pd} = T_{pHL} = T_{pLH}$	T_{pd}		8		ns
Propagation Delay Error	$\Delta T_{pd} = T_{pHL} - T_{pLH}$ (Note 8)	ΔT_{pd}			0.5	ns
INTERNAL HIGH−SIDE GATE DRIVE						
Pull−High Drive ON Resistance	$V_{BST} - V_{PH}$ = 5 V, I_{HG} = 2 mA (source)	R_{DRV_HH}	–	1.5	–	Ω
Pull−Low Drive ON Resistance	$V_{BST} - V_{PH}$ = 5 V, I_{HG} = 2 mA (sink)	R_{DRV_HL}	–	1.0	–	Ω
HG Propagation Delay Time	From LG off to HG on	T_{pdHG}		16		ns
INTERNAL LOW−SIDE GATE DRIVE						
Pull−High Drive ON Resistance	$V_{PVCC} - V_{PGND}$ = 5 V, I_{LG} = 2 mA (source)	R_{DRV_LH}	–	1.0	–	Ω
Pull−Low Drive ON Resistance	$V_{PVCC} - V_{PGND}$ = 5 V, I_{LG} = 2 mA (sink)	R_{DRV_LL}	–	0.5	–	Ω
LG Propagation Delay Time	From HG off to LG on	T_{pdLG}		10		ns
BOOTSTRAP						
On Resistance of Rectifier Switch	V_{PVCC} = 5 V, Id = 2 mA, T_A = 25°C	R_{BST}	5.0	14	20	Ω
Rectifier Switch Leakage Current	V_{PVCC} = 5 V, EN = 0 V	I_{lkgBST}	–	–	3	μA

8. Guaranteed by design, not tested in production.

DETAILED DESCRIPTION

General

The NCP81172, a 2−phase synchronous buck controller, integrates gate drivers and PWM VID interface in a QFN−24 package and provides a compact−footprint power management solution for new generation computing processors. It receives power save input (PSI) from processors and operates in 1−phase diode emulation mode to obtain high efficiency in light−load condition. Operating in high switching frequency up to 800 kHz allows employing small size inductor and capacitors. Introduction of multi−phase current−mode RPM control results in fast transient response and good dynamic current balance. It is able to support all−ceramic−capacitor applications.

Operation Modes

The NCP81172 has three power operation modes responding to PSI levels as shown in Table 1. The operation mode can be changed on the fly. In 1−phase operation, no switching in phase 2.

Table 1. POWER SAVING INTERFACE (PSI) CONFIGURATION

PSI Level	Power Mode	Phase Configuration
High (PSI ≥ 2.4 V)	PS0	2−Phase, FCCM
Intermediate (0.8 V < PSI < 2.4 V)	PS1	1−Phase, FCCM
Low (PSI ≤ 0.8 V)	PS2	1−Phase, Auto CCM/DCM

The NCP81172 is also able to support pure single−phase applications without a need to stuff components for phase 2. In this configuration, the four pins including BST2, HG2, LG2, and PH2 can be float, but make sure the voltage at PSI pin is never in high level.

Remote Voltage Sense

A high performance and high input impedance differential error amplifier, as shown in Figure 4, provides an accurate sense for the output voltage of the regulator. The output voltage and FBRTN inputs should be connected to the regulator’s output voltage sense points via a Kelvin−sense pair. The output voltage sense signal goes through a compensation network and into the inverting input (FB pin) of the error amplifier. The non−inverting input of the error amplifier is connected to the reference input (REFIN pin).

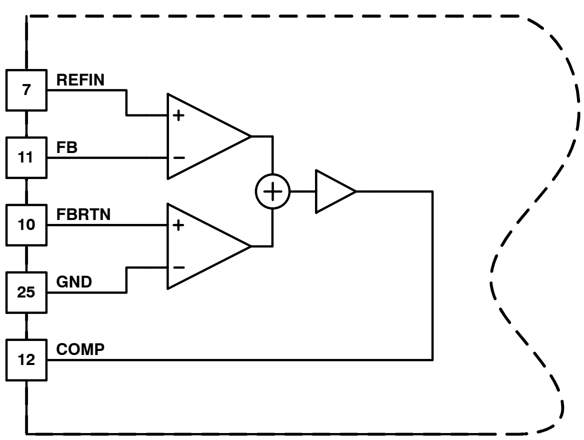

Figure 4. Differential Error Amplifier

Switching Frequency

Switching frequency is programmed by a resistor RFS applied from the FS pin to ground. The typical frequency range is from 200 kHz to 800 kHz. The FS pin provides approximately 2 V out and the source current is mirrored into the internal ramp generator. The switching frequency in 2−phase operation (PS0 mode) can be estimated by

$$F_{SW(kHz)} = 6603 \cdot R_{FS(k\Omega)}{}^{-0.766} \qquad \text{(eq. 1)}$$

To reduce output ripple in 1−phase operation, the switching frequency in PS1 and PS2 modes is set to be higher than PS0 mode, which can be estimated by

$$F_{SW(kHz)} = 5226 \cdot R_{FS(k\Omega)}{}^{-0.665} \qquad \text{(eq. 2)}$$

Figure 5 shows a measurement based on a typical application under condition of V_{in} = 20 V, V_{out} = 0.9 V, I_{out} = 10 A for PS1 mode operation and I_{out} = 20 A for PS0 mode operation. It can be also found that the higher $R_{DS(on)}$ of the low−side MOSFETs the smaller frequency difference between PS0 and PS1 mode.

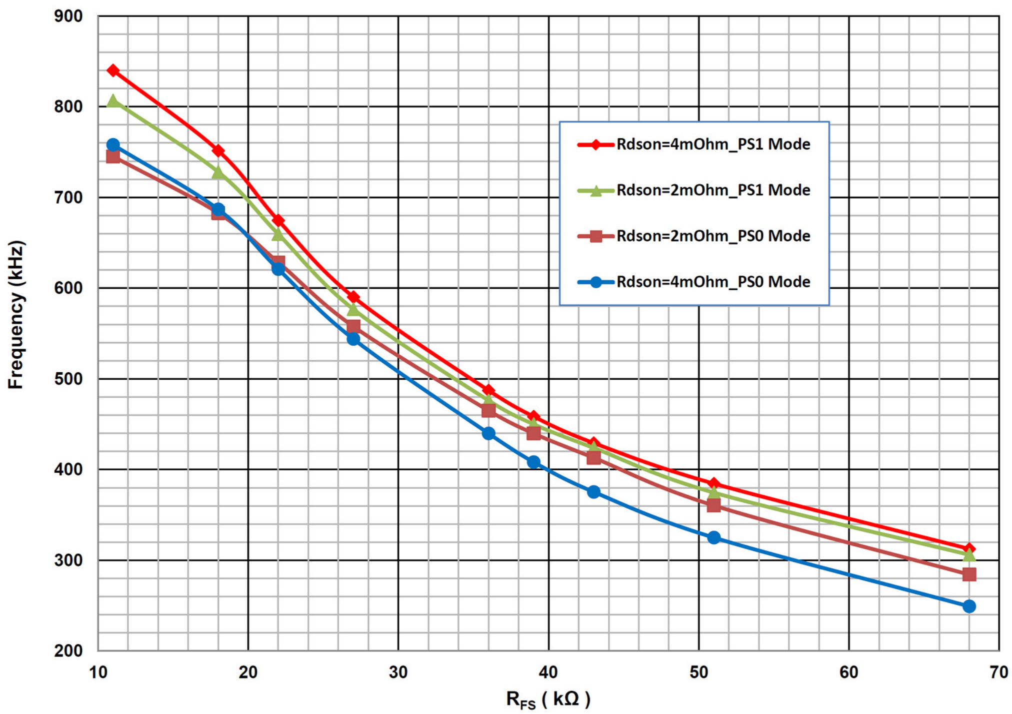

Figure 5. Switching Frequency Programmed by Resistor RFS at FS Pin

Soft Start

The NCP81172 has a soft start function. The output starts to ramp up following a system reset period after the device is enabled. The device is able to start up smoothly under an output pre−biased condition without discharging the output before ramping up.

REFIN Discharge

An internal switch in REFIN pin starts to short REFIN to GND just after EN is pulled high and it turns off just before the beginning of the soft start. The typical on resistance of the switch is 6.25 Ω.

Output Discharge in Shut Down

The NCP81172 has an output discharge function when the device is in shutdown mode. The resistors (2 kΩ per phase) from PH node to PGND in both phases are active to discharge the output capacitors.

Temperature Sense and Thermal Alert

The NCP81172 provides external temperature sense and thermal alert in the normal operation mode, and disables the function in the standby mode. The temperature sense and thermal alert circuit diagram is shown in . An external voltage divider, consisting of a NTC thermistor R_NTC and a resistor R_TSNS, is employed to sense temperature and program alert level. Usually the thermistor is placed close to a hot spot like a power MOSFET. The NCP81172 monitors the voltage at TSNS pin and compares the voltage to an internal 1 V threshold by an internal comparator. Once the TSNS voltage drops below 1 V, the comparator turns on an open−drain switch at TALERT# pin and thus indicates a high temperature alert. The thermal alert can be de−asserted when TSNS voltage raises back to be higher than 1.05V. In an exemplary application where a 100 kΩ (B = 4250 at 25°C) NTC thermistor is applied together with a 5.62 kΩ resistor, an low−valid thermal alert signal is asserted when the temperature of the NTC thermistor reaches 100°C and de−asserted when the temperature drops down to 97°C.

Thermal Shutdown

The NCP81172 has a thermal shutdown protection to protect the device from overheating when the die temperature exceeds 150°C. Once the thermal protection is triggered, the fault state can be ended by re−applying VCC and/or EN if the temperature drops down below 125°C.

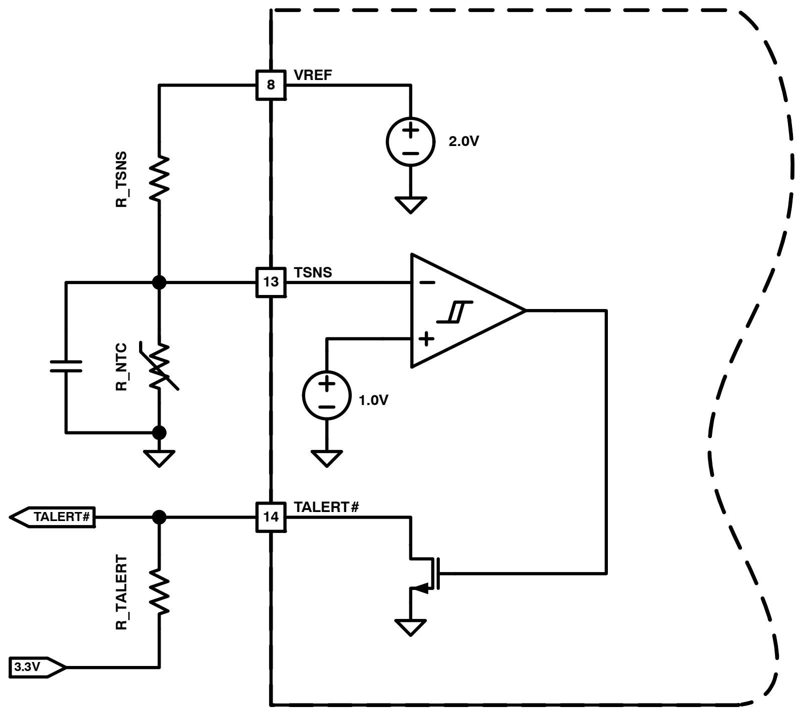

Figure 6. Temperature Sense and Thermal Alert Circuit Diagram

Over Current Protection

The NCP81172 protects converters from over current. The current through each phase is monitored by voltage sensing from phase node PHx to power ground PGND. The sense signal is compared to an internal voltage threshold. Once over load happens, the inductor current is limited to an average current per phase, which can be estimated by

$$I_{LMT(phase)} = \frac{V_{thOC}}{R_{DS(phase)}} \qquad \text{(eq. 3)}$$

where $R_{DS(phase)}$ is a total on conduction resistance of low−side MOSFETs per phase. Normally, a continuous over load event leads to a voltage drop in the output voltage and possible to eventually trip under voltage protection.

The over−current threshold can be externally programmed by adding a 1% tolerance resistor between LG1 pin and GND. The selectable thresholds can be found in the electrical table. Please note the maximum RC time constant formed by the resistor and the total input capacitance of the low−side MOSFETs should be smaller than 300 μs in order to make sure the detection voltage settles well.

Under Voltage Protection

There are two under voltage protections implemented in the NCP81172, which are fast under voltage protection and slow under voltage protection.

Fast under voltage protection (FUVP) protects converters in case of an extreme short circuit in output by monitoring FB voltage. Once FB voltage drops below 0.2 V for more than 2 μs, the NCP81172 latches off, both the high−side MOSFETs and the low-side MOSFETs in all phases are turned off. The fault remains set until the system has either VCC or EN toggled state. The FUVP function is disabled in soft start.

Slow under voltage protection (SUVP) of the NCP81172 is based on voltage detection at COMP pin. In normal operation, COMP level is below 2.5 V. When the output voltage drops below REFIN voltage for long time and COMP rises to be over 3 V, an internal UV fault timer will be triggered. If the fault still exists after 50 μs, the NCP81172 latches off, both the high-side MOSFETs and the low−side MOSFETs in all phases are turned off. The fault remains set until the system has either VCC or EN toggled state.

Over Voltage Protection

Over voltage protection of the NCP81172 is based on voltage detection at FB pin. Once FB voltage is over 2 V for more than 2 μs, all the high−side MOSFETs are turned off and all the low−side MOSFETs are latched on. The NCP81172 latches off until the system has either VCC or EN has toggled state.

LAYOUT GUIDELINES

Electrical Layout Considerations

Good electrical layout is a key to make sure proper operation, high efficiency, and noise reduction.

- Power Paths: Use wide and short traces for power paths to reduce parasitic inductance and high−frequency loop area. It is also good for efficiency improvement.
- Power Supply Decoupling: The power MOSFET bridges should be well decoupled by input capacitors and input loop area should be as small as possible to reduce parasitic inductance, input voltage spike, and noise emission. Place decoupling caps as close as possible to the controller VCC and VCCP pins.
- Output Decoupling: The output capacitors should be as close as possible to the load like a GPU. If the load is distributed, the capacitors should also be distributed and generally placed in greater proportion where the load is more dynamic.
- Switching Nodes: Switching nodes between HS and LS MOSFETs should be copper pours to carry high current and dissipate heat, but compact because they are also noise sources.
- Gate Drive: All the gate drive traces such as HGx, LGx, PHx, and BSTx should be short, straight as possible, and not too thin. The bootstrap cap and an option resistor need to be very close and directly connected between BSTx pin and PHx pin.
- Ground: It would be good to have separated ground planes for PGND and GND and connect the two planes at one point. PGND plane is an isolation plane between noisy power traces and all the sensitive control circuits. Directly connect the exposed pad (GND pin) to GND ground plane through vias. The analog control circuits should be surrounded by GND ground plane. GND ground plane is connected to PGND plane by single joint with low impedance.
- Voltage Sense: Use Kelvin sense pair and arrange a “quiet” path for the differential output voltage sense.
- Current Sense: The NCP81172 senses phase currents by monitoring voltages from phase nodes PHx to the common ground PGND pin. PGND ground plane should be well underneath PHx trances. To get better current balance between the two phases, try to make a layout as symmetrical as possible and balance the current flow in PGND plane for the two phases.
- Temperature Sense: A NTC thermistor is placed close to a hot spot like a power MOSFET, and a filter capacitor is placed close to TSNS pin of the controller. To avoid the traces from/to the NTC thermistor to cross over other sensitive control circuits.
- Compensation Network: The compensation network should be close to the controller. Keep FB trace short to minimize their capacitance to GND.
- PWM VID Circuit: The PWM VID is a high slew−rate digital signal from GPU to the controller. The trace routing of it should be done to avoid noise coupling from the switching node and to avoid coupling to other sensitive analog circuit as well. The RC network of the PWM VID circuit needs to be close to the controller. A 10 nF ceramic cap is connected from VREF pin to GND plane, and another small ceramic cap is connected from REFIN pin to GND plane.

Thermal Layout Considerations

Good thermal layout helps high power dissipation from a small−form factor VR with reduced temperature rise.

- The exposed pads of the controller and power MOSFETs must be well soldered on the board.
- A four or more layers PCB board with solid ground planes is preferred for better heat dissipation.
- More vias are welcome to be underneath the exposed pads and surrounding the power devices to connect the inner ground layers to reduce thermal resistances.
- Use large area copper pour to help thermal conduction and radiation.
- Try distributing multiple heat sources to reduce temperature rise in hot spots.