

# ON Semiconductor

## Is Now

# onsemi™

To learn more about onsemi™, please visit our website at  
[www.onsemi.com](http://www.onsemi.com)

---

**onsemi** and **onsemi** and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi** product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner. Other names and brands may be claimed as the property of others.

# Hot Swap Smart Fuse

## NCP81292

The NCP81292 is a 50 A, electronically re-settable, in-line fuses for use in 12 V, high current applications such as servers, storage and base stations. The NCP81292 offers a very low 0.65 mΩ integrated MOSFET to reduce solution size and minimize power loss. It also integrates a highly accurate current sensor for monitoring and overload protection.

### Power Features

- Co-packaged Power Switch, Hotswap Controller and Current Sense
- Up to 50 A Continuous, 80 A Peak Output Current
- Vin Range: 4.5 V to 18 V
- 0.65 mΩ, no R<sub>SENSE</sub> Required

### Control Features

- Enable Input
- Optional Enable-controlled Output Pulldown when Disabled
- Programmable Soft-Start
- Programmable, Multi-level Current Limit

### Reporting Features

- Accurate Analog Load Current Monitor
- Programmable Over Current Alert Output
- Analog Temperature Output
- Status Fault OK Output

### Other Features

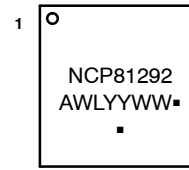
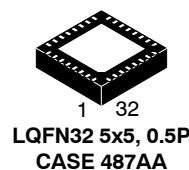
- 5 mm x 5 mm QFN32 Package
- Operating Temperature: -40°C to 125°C
- Can be Paralleled for Higher Current Applications
- Built-in Insertion Delay for Hotswap Applications
- Auto-Retry Mode for Following Protection Features
  - ◆ Current-limit after Delay
  - ◆ Fast Short-circuit Protection
  - ◆ Over-Temperature Shutdown
  - ◆ Excessive Soft-start Duration
- Internal Switch Fault Diagnostics
- Low-power Auxiliary Output Voltage



ON Semiconductor®

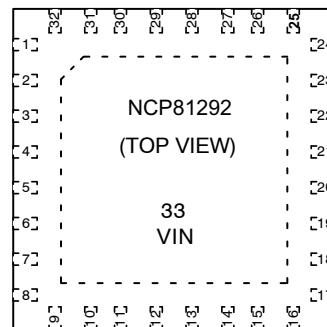
[www.onsemi.com](http://www.onsemi.com)

### MARKING DIAGRAM



NCP81292 = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
▪ = Pb-Free Package  
(may or may not be present)  
(Note: Microdot may be in either location)

### PINOUT

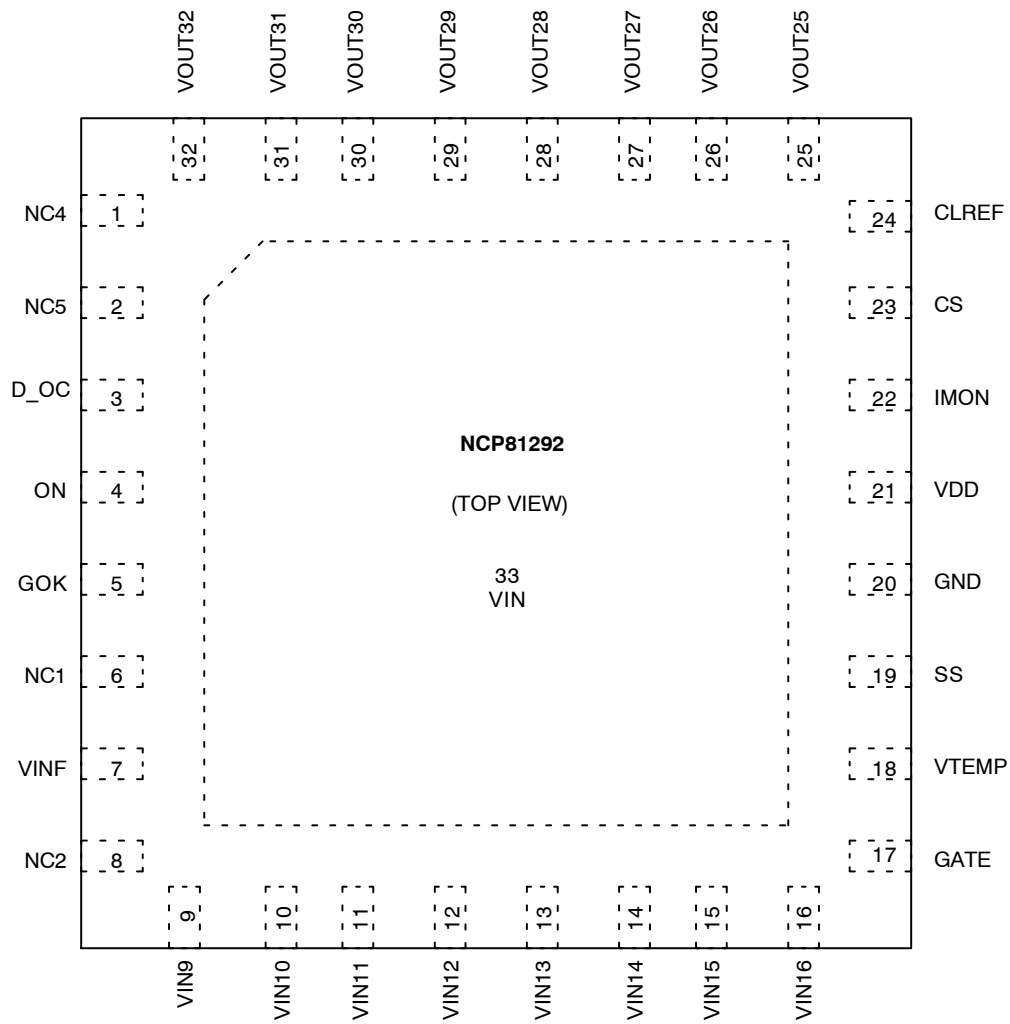


For more details see Figure 1.

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# NCP81292



**Figure 1. Pin Configuration**

**Table 1. DEVICE ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
NCP81292MNTXG	QFN32	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NCP81292

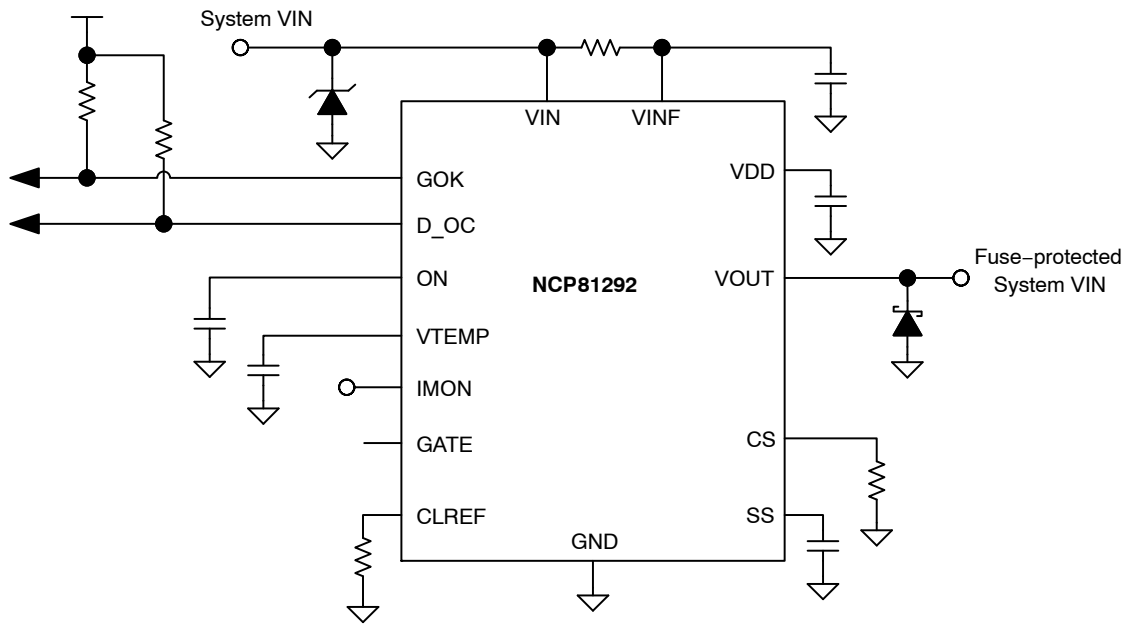


Figure 2. Typical Application

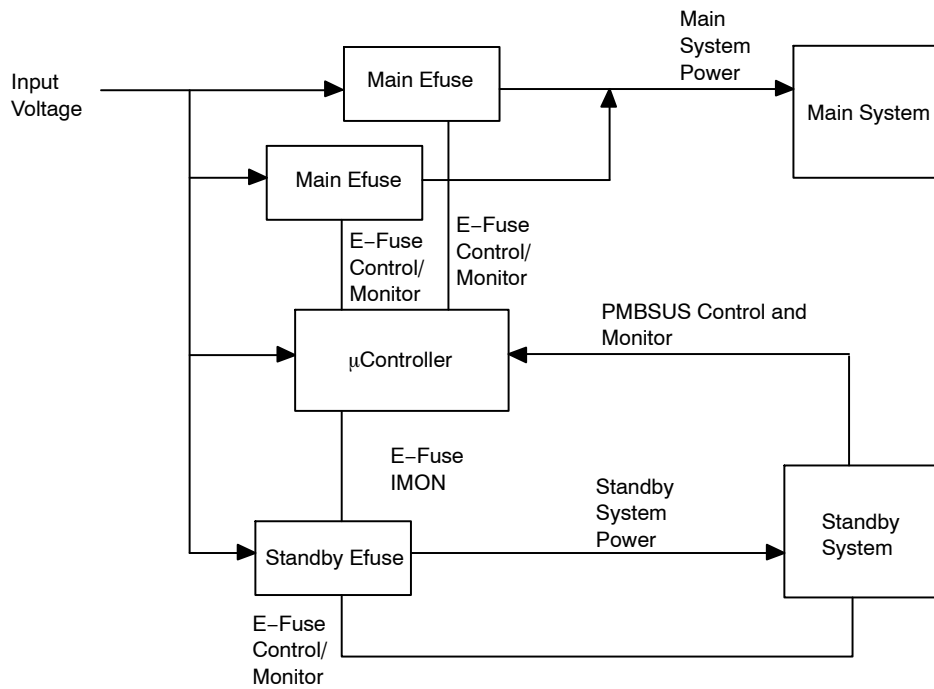
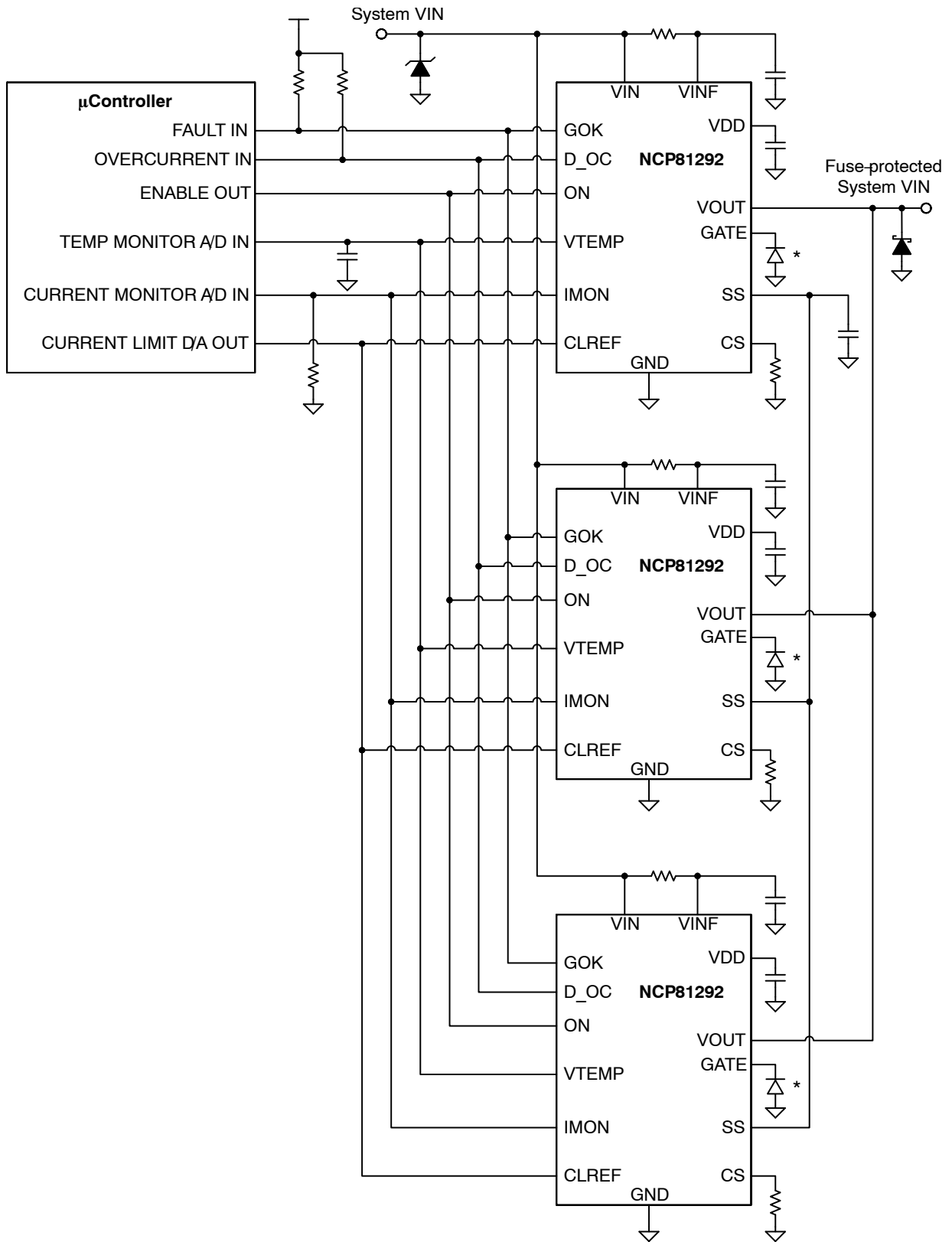


Figure 3. Typical Application Diagram

# NCP81292



**Figure 4. Application Schematic – Parallel Fuse Operation with Controller**

\*For parallel NCP81292 applications, a BAS16, or equivalent, diode is recommended at each GATE pin to limit the negative voltage/current during output fault conditions. Due to reverse leakage potential, a schottky diode should not be used.

# NCP81292

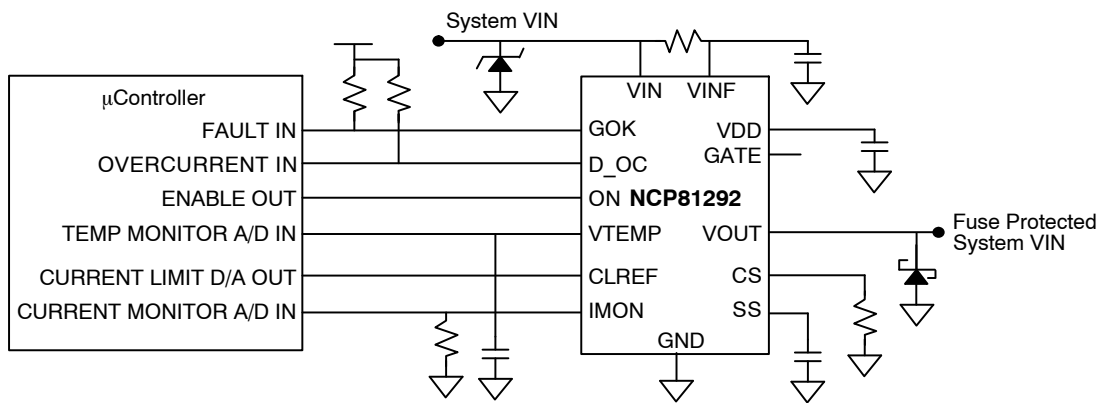


Figure 5. Application Schematic - Single EFuse with Controller

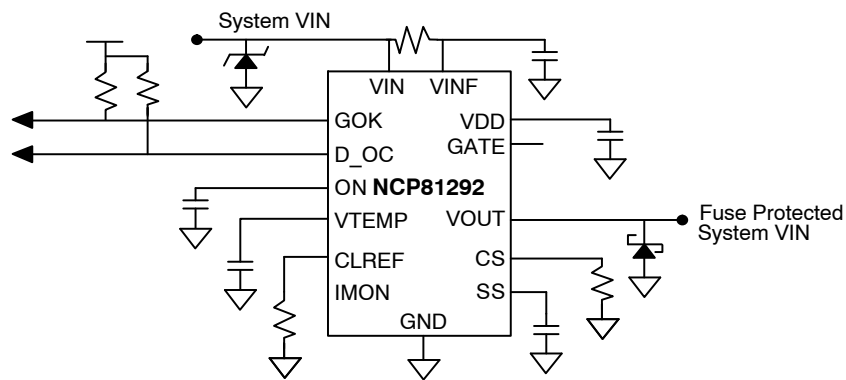
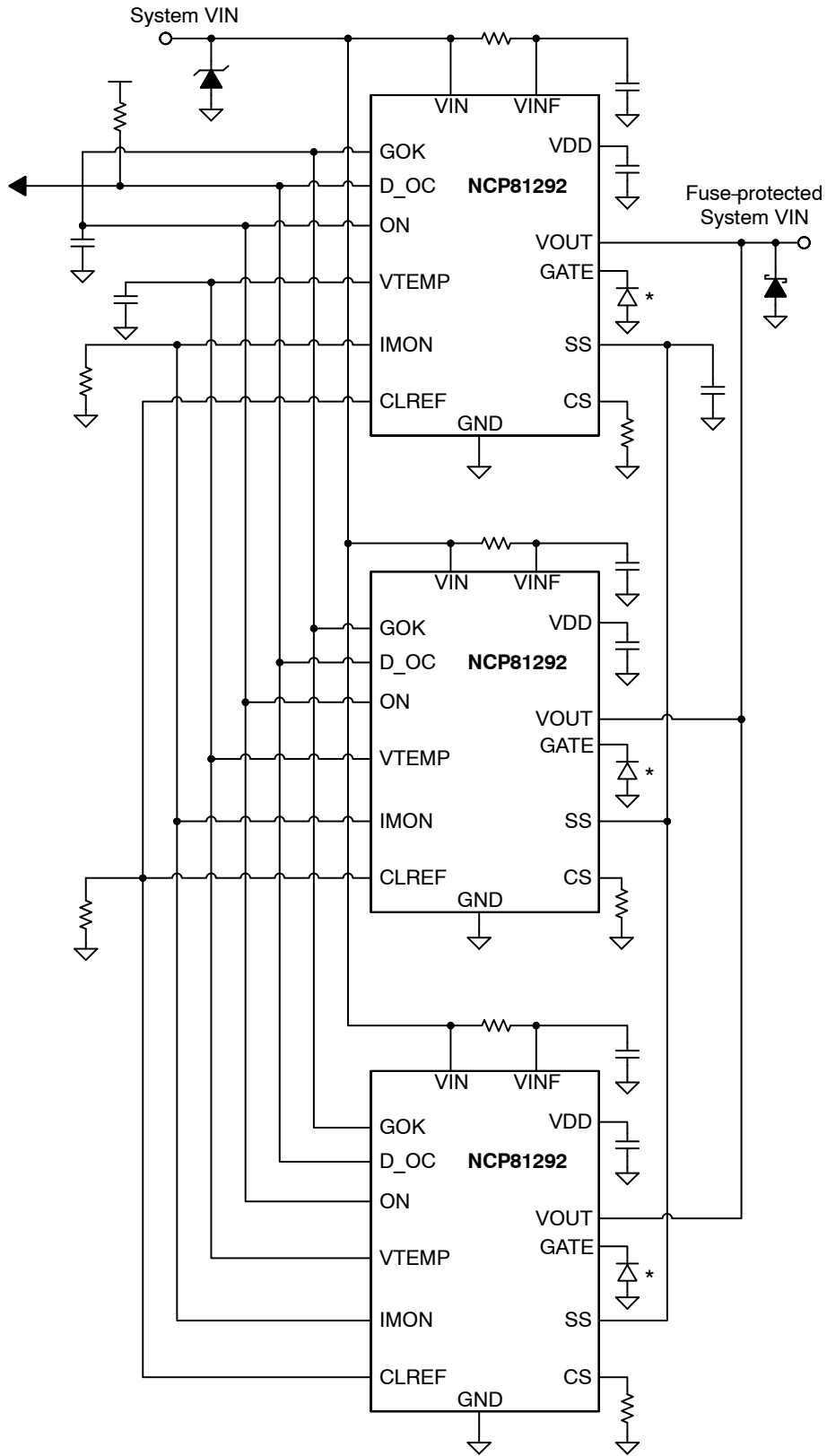


Figure 6. Application Schematic - Stand-alone Single EFuse

# NCP81292



**Figure 7. Application Schematic – Stand-alone Parallel EFuse**

\*For parallel NCP81292 applications, a BAS16, or equivalent, diode is recommended at each GATE pin to limit the negative voltage/current during output fault conditions. Due to reverse leakage potential, schottky diodes should not be used.

# NCP81292

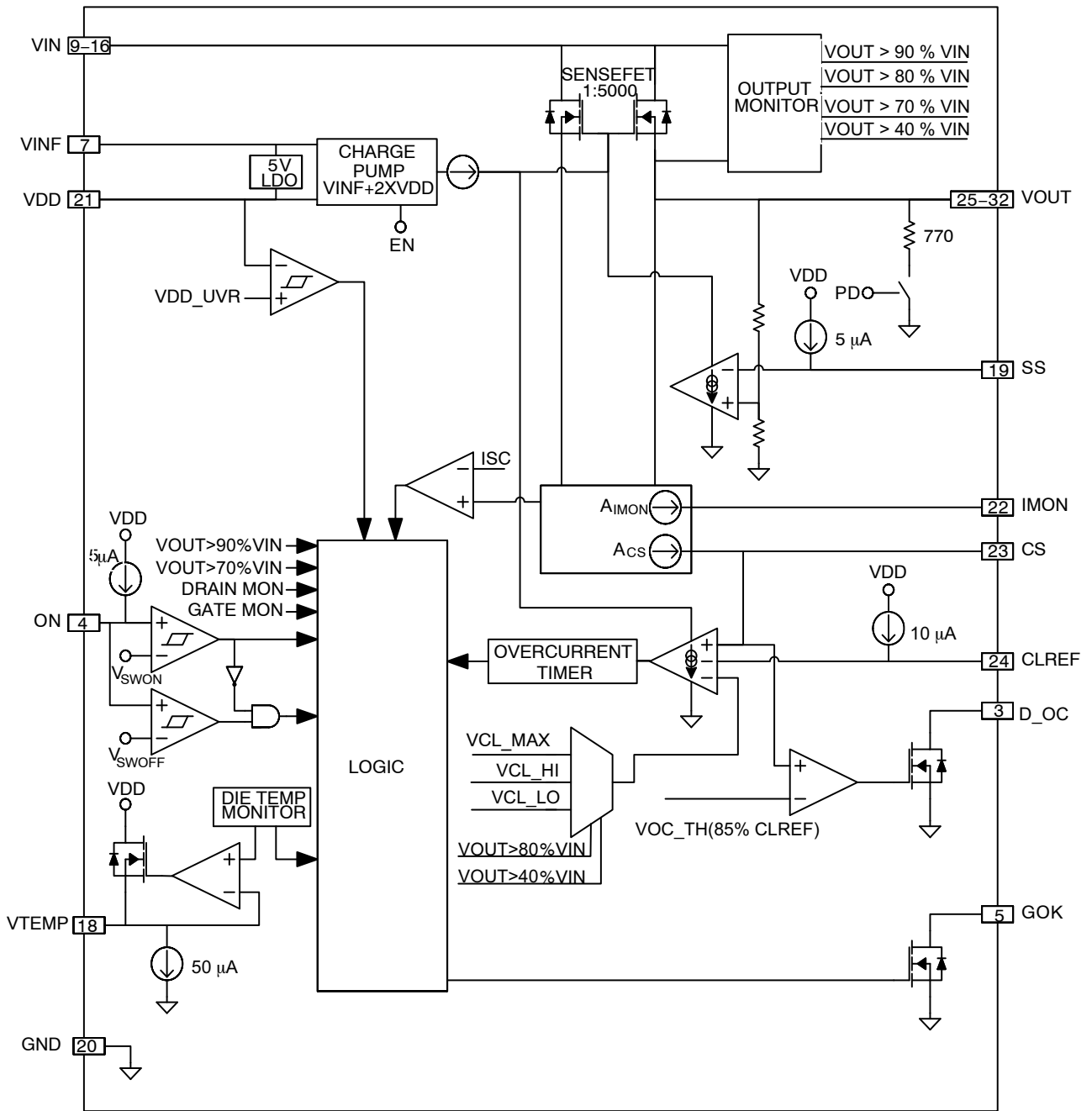


Figure 8. Block Diagram



# NCP81292

**Table 2. PIN DESCRIPTION**

Pin No.	Symbol	Description
1	NC4	No electrical connection internally. May connect to any potential
2	NC5	No electrical connection internally. May connect to any potential
3	D_OC	Overcurrent indicator output (open drain). Low indicates the NCP81292 is limiting current. The D_OC output does not report current limiting during soft-start.
4	ON	Enable input and output pulldown resistance control.
5	GOK	OK status indicator output (open drain). Low indicates that the NCP81292 was turned off by a fault.
6	NC1	Test pin. Do not connect to this pin. Leave floating
7	VINF	Control circuit power supply input. Connect to VIN pins through an RC filter. (1 $\Omega$ / 0.1 $\mu$ F)
8	NC2	Internal FET sense pin. Do not connect to this pin. Leave floating
9	VIN09	Input of high current output switch
10	VIN10	Input of high current output switch
11	VIN11	Input of high current output switch
12	VIN12	Input of high current output switch
13	VIN13	Input of high current output switch
14	VIN14	Input of high current output switch
15	VIN15	Input of high current output switch
16	VIN16	Input of high current output switch
17	GATE	Internal FET gate pin. Connect to the cathode of an anode grounded diode such as BAS16P2T5G. A 4.7 nF ceramic capacitor is reserved between this pin and GND for NCP81292 to mitigate the oscillation risk when small amount of output capacitance (< 100 $\mu$ F) or long input/output cable (large $L_{IN}$ / $L_{OUT}$ ) happens.
18	VTEMP	Analog temperature monitor output.
19	SS	Soft Start time programming pin. Connect a capacitor to this pin to set the softstart time.
20	GND	Ground
21	VDD	Linear regulator output
22	IMON	Analog current monitor output
23	CS	Current sense feedback output (current). Scaling the voltage developed at this pin with a resistor to ground makes this also an input for several current limiting functions and overcurrent indicator D_OC.
24	CLREF	Current limit setpoint input for normal operation (after soft-start).
25	VOUT25	Output of high current output switch
26	VOUT26	Output of high current output switch
27	VOUT27	Output of high current output switch
28	VOUT28	Output of high current output switch
29	VOUT29	Output of high current output switch
30	VOUT30	Output of high current output switch
31	VOUT31	Output of high current output switch
32	VOUT32	Output of high current output switch
33	VIN33	Input of high current output switch

# NCP81292

**Table 3. MAXIMUM RATINGS**

Rating		Symbol	Min	Max	Unit
Input Voltage Range (VINx, VINf pins)	VOUT Enabled	VIN, VINf	-0.3	20	V
	VOUT Disabled (Note 2)		-0.3	30	V
Output Voltage Range (VOUTx pins)		VOUT	-0.3 -1 (<500 ms)	20	V
VDD Pin Voltage Range		VDD	-0.3	6	V
GATE Pin Voltage Range		VGATE	-0.3, -0.8 (<1 ms)	30	V
		VGATE-VOUT	-20	20	V
All Other Pins (Note 3)			-0.3	VDD + 0.3	V
Operating Junction Temperature Range		TJ	-40	150	°C
Storage Temperature Range		TSTG	-55	150	°C
Lead Soldering Temperature, Reflow, Pb-Free (Note 4)		TSLD		260	°C
Electrostatic Discharge, Human Body Model (per EIA/JESD22-A114)		ESDHBM		3.0	kV
Electrostatic Discharge, Charged Device Model (per EIA/JESD22-A115)		ESDCDM		2.0	kV
Maximum Latch-Up Current Limit (per JESD78)		ILU		100	mA
Moisture Sensitivity Level		MSL		3	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. All signals referenced to GND unless noted otherwise.
2. Vout disable is the state of output OFF when internal FET has turned off by disable ON or FAULTs protection.
3. Pin ratings referenced to VDD apply with VDD at any voltage within the VDD Pin Voltage Range.
4. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

**Table 4. THERMAL CHARACTERISTICS**

Rating	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient (Note 5)	RθJA	30	°C/W
Thermal Resistance, Junction-to-Top-Case	RθJCT	50	°C/W
Thermal Resistance, Junction-to-Bottom-Case	RθJCB	1.5	°C/W
Thermal Resistance, Junction-to-Board (Note 6)	RθJB	1.5	°C/W
Thermal Resistance, Junction-to-Case (Note 7)	RθJC	1.5	°C/W

5. RθJA is obtained by simulating the device mounted on a 500 mm<sup>2</sup>, 1-oz Cu pad on a 80 mm x 80 mm, 1.6 mm thick 8-layer FR4 board.
6. RθJB value based on hottest board temperature within 1 mm of the package.
7. RθJC ≈ RθJCT // RθJCB (Two-Resistor Compact Thermal Model, JESD15-3).

**Table 5. RECOMMENDED OPERATING RANGES**

Parameter (Note 1)	Symbol	Min	Max	Unit
VIN, VINf Pin Voltage Range		4.5	18	V
Maximum Continuous Output Current	I <sub>AVE</sub>		50	A
Peak Output Current	I <sub>PEAK</sub>		80	A
VDD Output Load Capacitance Range	C <sub>VDD</sub>	2.2	10	μF
VTEMP Output Load Capacitance Range	C <sub>VTEMP</sub>	0.1		μF
Softstart Duration	T <sub>SS</sub>	10	100	ms
CS Load Resistance Range	R <sub>CS</sub>	1.8	4	kΩ
CLREF Voltage Range	V <sub>CLREF</sub>	0.2	1.55	V
Operating Junction Temperature	T <sub>J(OP)</sub>	-40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# NCP81292

**Table 6. ELECTRICAL CHARACTERISTICS** ( $V_{INx} = V_{INF} = 12.0\text{ V}$ ,  $V_{ON} = 3.3\text{ V}$ ,  $C_{VINx} = 0.1\ \mu\text{F}$ ,  $C_{VDD} = 4.7\ \mu\text{F}$ ,  $C_{VTEMP} = 0.1\ \mu\text{F}$ ,  $R_{VTEMP} = 1\ \text{k}\Omega$ ,  $C_{SS} = 100\ \text{nF}$  (unless specified otherwise) Min/Max values are valid for the temperature range  $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$  unless noted otherwise, and are guaranteed by design and characterization through statistical correlation.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
-----------	--------	-----------------	-----	-----	-----	-------

## VINF INPUT

Quiescent Current		$V_{ON} > 1.4\text{ V}$ , no load		3.23	5.0	mA
		$V_{ON} > 1.4\text{ V}$ , fault			5.0	mA
		$V_{ON} < 0.8\text{ V}$		2.38	4.0	mA
		$V_{ON} < 0.8\text{ V}$ , $V_{INF} = 16\text{ V}$			4.0	mA

## VDD REGULATOR

VDD Output Voltage	$V_{DD\_NL}$	$I_{VDD} = 0\text{ mA}$ , $V_{INF} = 6\text{ V}$	4.7	5.09	5.3	V
VDD Load Capability	$I_{DDLOAD}$	$V_{INF} = 5.5\text{ V}$			30	mA
VDD Current Limit	$I_{DD\_CL}$	$V_{INF} = 12\text{ V}$ and $V_{INF} = 6\text{ V}$	50	70		mA
VDD Dropout Voltage		$I_{VDD} = 25\text{ mA}$ , $V_{INF} = 4.5\text{ V}$		85	200	mV
UVLO threshold – rising	$V_{DD\_UVR}$		4.1	4.3	4.5	V
UVLO threshold – falling	$V_{DD\_UVF}$		3.8	4.0	4.2	V

## ON INPUT

Bias Current	$I_{ON}$	From pin into a 0 V or 1.5 V source	4.0	5.0	6.0	$\mu\text{A}$
Switch ON Threshold	$V_{SWON}$		1.33	1.4	1.47	V
Switch OFF/ Pulldown Upper Threshold	$V_{SWOFF}$		1.13	1.2	1.27	V
Pulldown Lower Threshold	$V_{PDOFF}$			0.8		V
Switch ON Delay Timer	$t_{ON}$	From ON transitioning above $V_{SWON}$ to SS start	0.6	1.0	2.5	ms
Switch OFF Delay Time (Note 8)	$t_{OFF}$	From ON transitioning below $V_{SWOFF}$ to GATE pulldown		1.7		$\mu\text{s}$
ON Current Source Clamp Voltage	$V_{ON\_CLMP}$	Max pullup voltage of current source	2.8	3.0		V
Load Pulldown Delay Timer	$t_{PD\_DEL}$	From ON transitioning into the range between $V_{SWOFF}$ and $V_{PDOFF}$		2.0		ms
Output Pulldown Resistance	$R_{PD}$	$V_{OUT} = 12\text{ V}$ , PD mode = 1		0.77		$\text{k}\Omega$

## SS PIN

Bias Current	$I_{SS}$	From pin into a 0 V or 1 V source	4.62	5.15	5.62	$\mu\text{A}$
Gain to VOUT	$A_{VSS}$		9.6	10	10.4	V/V
SS Pulldown Voltage	$V_{OL\_SS}$	0.1 mA into pin during ON delay		22		mV

## GOK OUTPUT

Output Low Voltage	$V_{OL\_GOK}$	$I_{GOK} = 1\text{ mA}$			0.1	V
Off-state Leakage Current	$I_{LK\_GOK}$	$V_{GOK} = 5\text{ V}$			1.0	$\mu\text{A}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Guaranteed by design or characterization data. Not tested in production.

# NCP81292

**Table 6. ELECTRICAL CHARACTERISTICS** (VINx = VINf = 12.0 V, VON = 3.3 V, CVINF = 0.1 μF, CVDD = 4.7 μF, CVTEMP = 0.1 μF, RVTEMP = 1 kΩ, CSS = 100 nF (unless specified otherwise) Min/Max values are valid for the temperature range -40°C ≤ TJ ≤ 125°C unless noted otherwise, and are guaranteed by design and characterization through statistical correlation.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units	
<b>IMON/CS OUTPUT</b>							
IMON or CS Current (single EFuse) Based on 10 μA/A	I <sub>IMON/ICS</sub>	T <sub>J</sub> = 0 to 125°C	IOUT = 5 A (Note 8)		50		μA
			IOUT = 10 A (Note 8)		100		μA
			IOUT = 25 A (Note 8)		250		μA
			IOUT = 50 A (Note 8)		500		μA
Accuracy (single EFuse)		T <sub>A</sub> = 25°C	IOUT = 8 A	-3		3	%
			IOUT > 8 A (Note 8)	-3		3	%
		T <sub>A</sub> = 0 to 85°C	IOUT ≥ 8 A (Note 8)	-5		5	%
IMON or CS Current Source Clamp Voltage	V <sub>IM_CLMP</sub> / V <sub>CS_CLMP</sub>	Max pullup voltage of current source	2.8	3.0		V	

### CURRENT LIMIT & CLREF PIN

Current Limit Voltage	V <sub>CL_TH</sub>	If V <sub>CS</sub> > V <sub>CL_TH</sub> current limiting regulation occurs via gate	95	98	101	%V <sub>CLREF</sub>
Current Limit Enact Offset Voltage	V <sub>ENACT</sub>	0.2 V < V <sub>CLREF</sub> < 1.55 V	-70	-24	12	mV
Current Limit Clamp Voltage	V <sub>CL_LO</sub>	V <sub>OUT</sub> < 40% VIN, V <sub>CLREF</sub> > 0.165 V	135	152	165	mV
	V <sub>CL_HI</sub>	40% VIN < V <sub>OUT</sub> < 80% VIN V <sub>CLREF</sub> > 0.55 V	480	504	520	mV
Max Current Limit Reference Voltage	V <sub>CL_MX</sub>	V <sub>OUT</sub> > 80% VIN, V <sub>CLREF</sub> > 1.65 V	1.55	1.6	1.65	V
Response Time (Note 8)	t <sub>CL_REG</sub>	V <sub>CS</sub> > V <sub>CLREF</sub> current limiting time		200		μs
CLREF Bias Current	I <sub>CL</sub>	From pin into a 1.2 V source	9.6	10	10.4	μA
CLREF Current Source Clamp Voltage	V <sub>CL_CLMP</sub>	Max pullup voltage of current source	2.8	3.0		V
FET Turn-off Timer	t <sub>CL_LA</sub>	Delay between current limit detection and FET turn-off (GOK = 0)		250		μs

### D\_OC OUTPUT

Overcurrent Threshold	V <sub>OC_TH</sub>	If V <sub>CS</sub> > V <sub>OC_TH</sub> , the D_OC pin pulls low	82	85	89	%V <sub>CLREF</sub>
Output Low Voltage	V <sub>OL_DOC</sub>	I <sub>DOC</sub> = 1 mA			0.1	V
Off-state Leakage Current	I <sub>LK_DOC</sub>	V <sub>DOC</sub> = 5 V			1.0	μA
De-bounce Time (Note 8)		V <sub>CS</sub> < limit until D_OC rising		3.0		μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Guaranteed by design or characterization data. Not tested in production.

# NCP81292

**Table 6. ELECTRICAL CHARACTERISTICS** ( $V_{INx} = V_{INF} = 12.0\text{ V}$ ,  $V_{ON} = 3.3\text{ V}$ ,  $C_{VINx} = 0.1\text{ }\mu\text{F}$ ,  $C_{VDD} = 4.7\text{ }\mu\text{F}$ ,  $C_{VTEMP} = 0.1\text{ }\mu\text{F}$ ,  $R_{VTEMP} = 1\text{ k}\Omega$ ,  $C_{SS} = 100\text{ nF}$  (unless specified otherwise) Min/Max values are valid for the temperature range  $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$  unless noted otherwise, and are guaranteed by design and characterization through statistical correlation.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
<b>SHORT CIRCUIT PROTECTION</b>						
Current Threshold (Note 8)	$I_{SC}$			100		A
Response Time (Note 8)	$t_{SC}$	From $I_{OUT} > I_{LIMSC}$ until gate pulldown		500		ns
<b>VTEMP OUTPUT</b>						
Bias Voltage	$V_{VTEMP25}$	At $25^{\circ}\text{C}$		450		mV
Gain (Note 8)	$A_{VTEMP}$	$0^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$		10		mV/ $^{\circ}\text{C}$
Load Capability (Note 8)	$R_{VTEMP}$	At $25^{\circ}\text{C}$		1		k $\Omega$
Pulldown Current	$I_{VTEMP}$	At $25^{\circ}\text{C}$		50		$\mu\text{A}$
<b>THERMAL SHUTDOWN</b>						
Temperature Shutdown (Note 8)	$T_{TSD}$	GOK pulls down		140		$^{\circ}\text{C}$
<b>OUTPUT SWITCH (FET)</b>						
On Resistance	$R_{DSon}$	$T_J = 25^{\circ}\text{C}$ , $I_{OUT} = 8\text{ A}$		0.65	1.0	m $\Omega$
Off-state leakage current	$I_{DSoff}$	$V_{IN} = 16\text{ V}$ , $V_{ON} < 1.2\text{ V}$ , $T_J = 25^{\circ}\text{C}$			1.0	$\mu\text{A}$
<b>FAULT detection</b>						
$V_{DS}$ Short Threshold	$V_{DS\_TH}$	Startup postponed if $V_{OUT} > V_{DS\_TH}$ at $V_{ON} > V_{SWON}$ transition		88.8		%VIN
$V_{DS}$ Short OK Threshold	$V_{DS\_OK}$	Startup resumed if $V_{OUT} < V_{DS\_OK}$ anytime after postponed		68.6		%VIN
$V_{GD}$ Short Threshold	$V_{DG\_TH}$	Startup postponed if $V_G > V_{DG\_TH}$ at $V_{ON} > V_{SWON}$ transition		3.1		V
$V_{GD}$ Short OK Threshold	$V_{DG\_OK}$	Startup resumed if $V_G < V_{DG\_OK}$ anytime after postponed		3.0		V
$V_G$ Low Threshold	$V_{G\_TH}$	Latch/Restart if $V_{GD} < V_{G\_TH}$ after $t_{SSF\_END}$ or $t_{GATE\_FLT}$		5.4		V
$V_{OUT}$ Low Threshold	$V_{OUTL\_TH}$	Latch/Restart if $V_{OUT} < V_{OUTL\_TH}$ after $t_{SSF\_END}$		90		%VIN
Gate Fault Timer (Note 8)	$t_{GATE\_FLT}$	Time from $V_{GD} < V_{G\_TH}$ transition after $t_{SSF\_END}$ completed		200		ms
Startup Timer Failsafe (Note 8)	$t_{SSF\_END}$	Time from $V_{ON} > V_{SWON}$ transition, Max programmable softstart time		200		ms
<b>AUTO-RETRY</b>						
Auto-Retry Delay	$t_{DLY\_RETRY}$	Delay from power-down to retry of startup		1000		ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Guaranteed by design or characterization data. Not tested in production.

# NCP81292

## TYPICAL CHARACTERISTICS

Test Conditions:  $V_{in} = 12\text{ V}$ ,  $R_{cs} = 2\text{ k}\Omega$ ,  $C_{ss} = 200\text{ nF}$ ,  $R_{CLREF} = 121\text{ k}\Omega$ ,  $R_{IMON} = 2\text{ k}\Omega$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

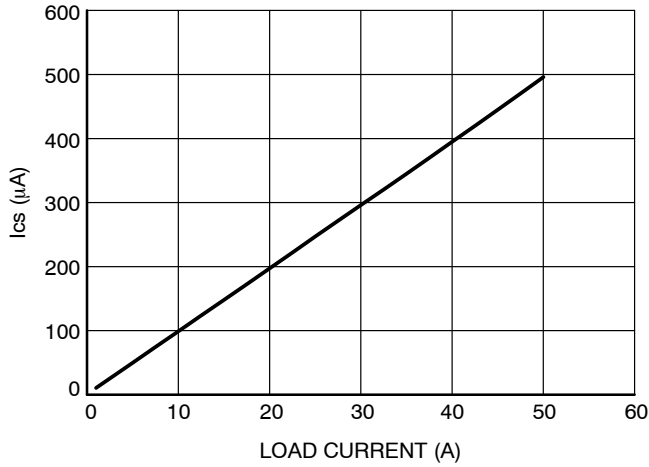


Figure 9. Ics vs. Load Current

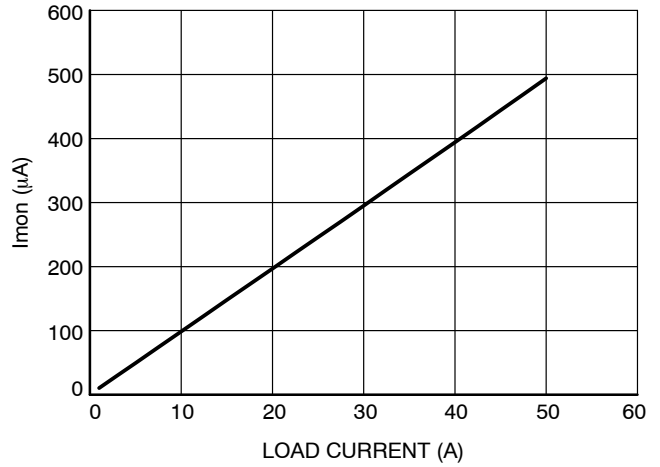


Figure 10. Imon vs. Load Current

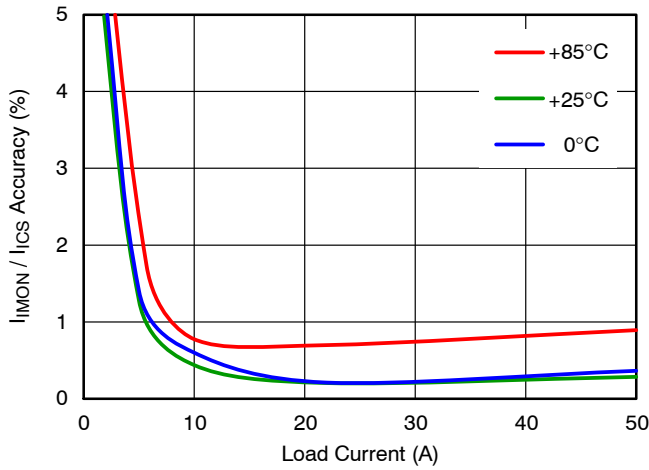


Figure 11.  $I_{IMON} / I_{CS}$  Accuracy vs. Load Current

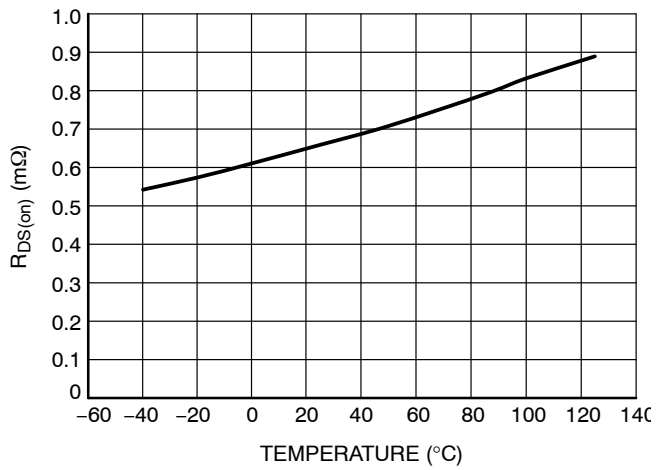


Figure 12. Output Switch  $R_{DS(on)}$  @ 22 A vs. Temperature

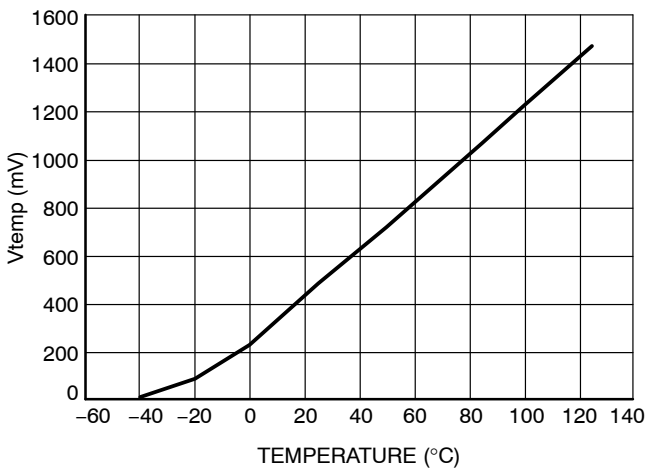


Figure 13. Vtemp vs. Temperature (no load)

TYPICAL CHARACTERISTICS

Test Conditions:  $V_{in} = 12\text{ V}$ ,  $R_{cs} = 2\text{ k}\Omega$ ,  $C_{ss} = 200\text{ nF}$ ,  $R_{CLREF} = 121\text{ k}\Omega$ ,  $R_{IMON} = 2\text{ k}\Omega$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

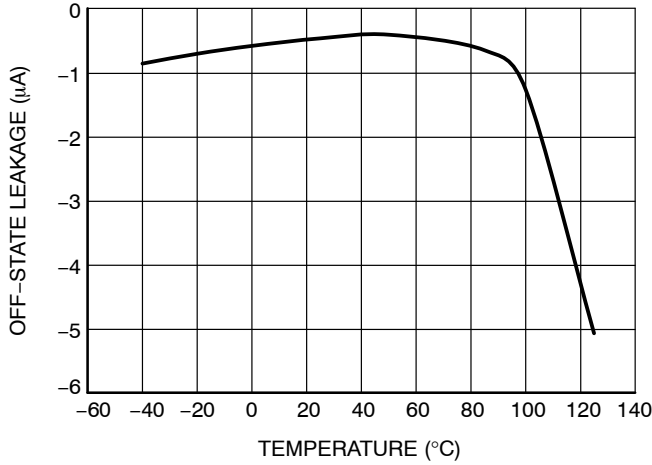


Figure 14. Output Switch Off-state Leakage vs. Temperature

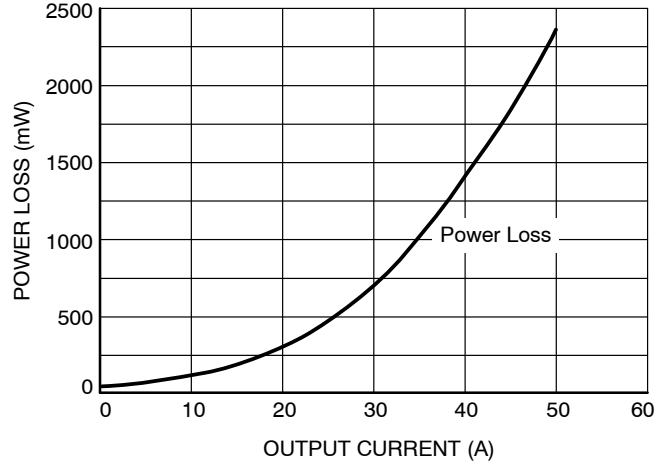


Figure 15. Power Loss vs. Load Current

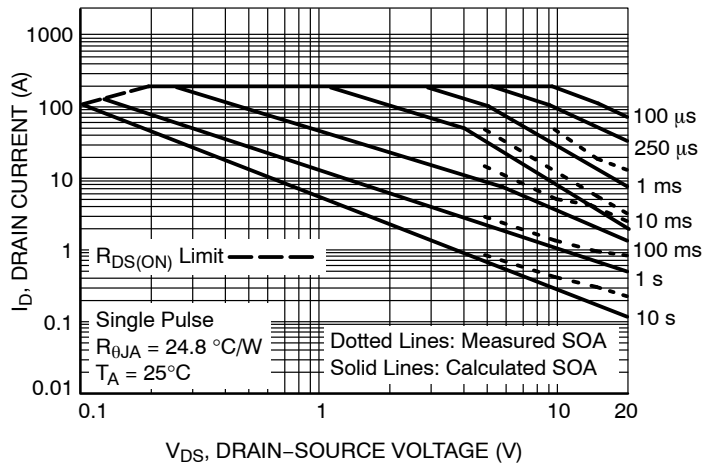


Figure 16. Internal FET's Safe Operating Area (SOA)

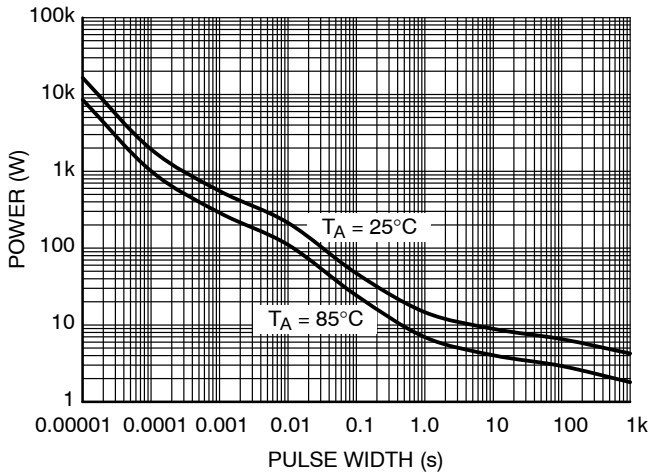


Figure 17. Single Pulse Power Rating (10  $\mu\text{s}$  - 1000 s, Junction-to-Ambient, Note 4)

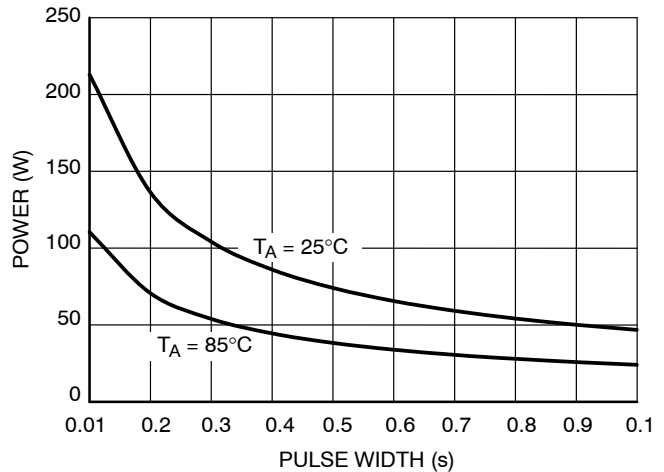


Figure 18. Single Pulse Power Rating (10 ms - 100 ms, Junction-to-Ambient, Note 4)

TYPICAL CHARACTERISTICS

Test Conditions:  $V_{in} = 12\text{ V}$ ,  $R_{cs} = 2\text{ k}\Omega$ ,  $C_{ss} = 200\text{ nF}$ ,  $R_{CLREF} = 121\text{ k}\Omega$ ,  $R_{IMON} = 2\text{ k}\Omega$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

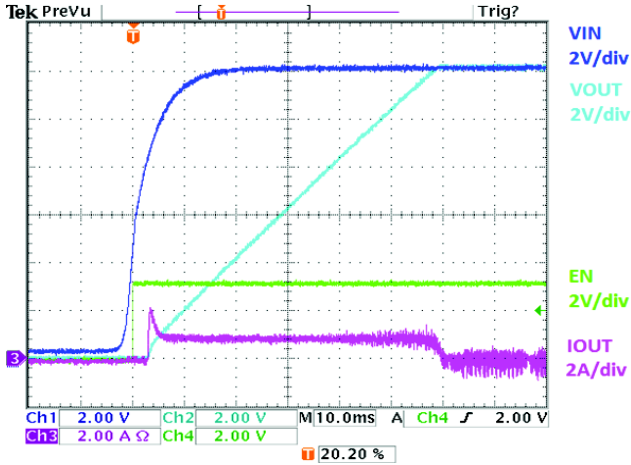


Figure 19. Start Up by VIN (Iout = 0 A)

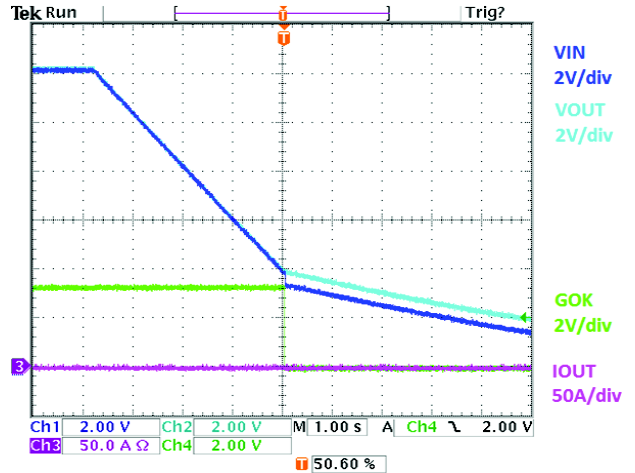


Figure 20. Shut Down by VIN (Iout = 0 A)

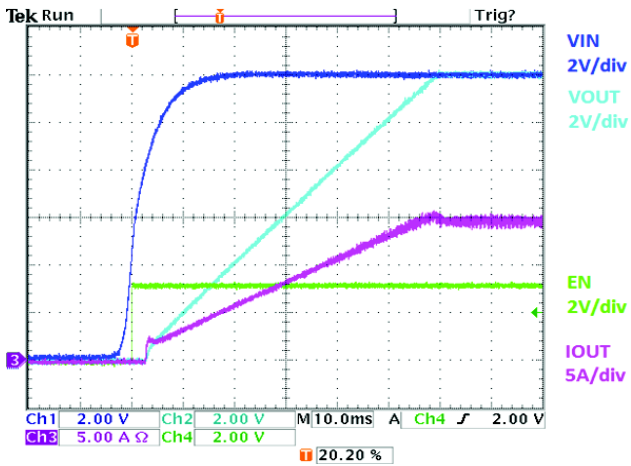


Figure 21. Start Up by VIN (Iout = 15 A)

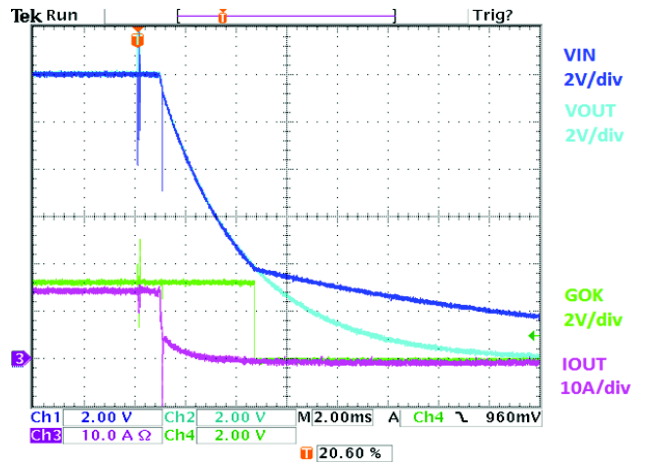


Figure 22. Shut Down by VIN (Iout = 15 A)

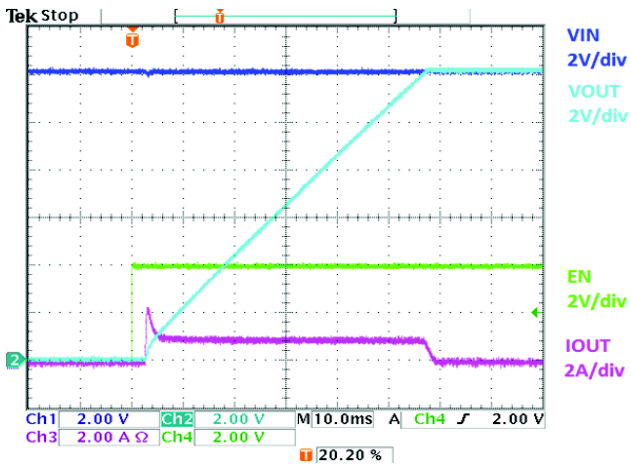


Figure 23. Start Up by EN (Iout = 0 A)

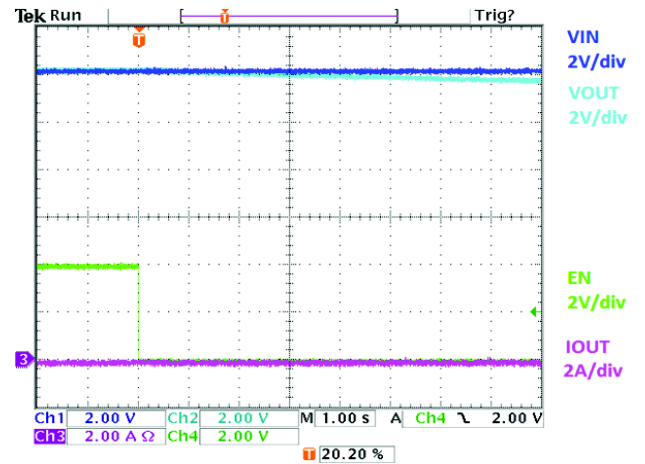


Figure 24. Shut Down by EN (Iout = 0 A)



# NCP81292

## TYPICAL CHARACTERISTICS

Test Conditions:  $V_{in} = 12\text{ V}$ ,  $R_{cs} = 2\text{ k}\Omega$ ,  $C_{ss} = 200\text{ nF}$ ,  $R_{CLREF} = 121\text{ k}\Omega$ ,  $R_{IMON} = 2\text{ k}\Omega$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

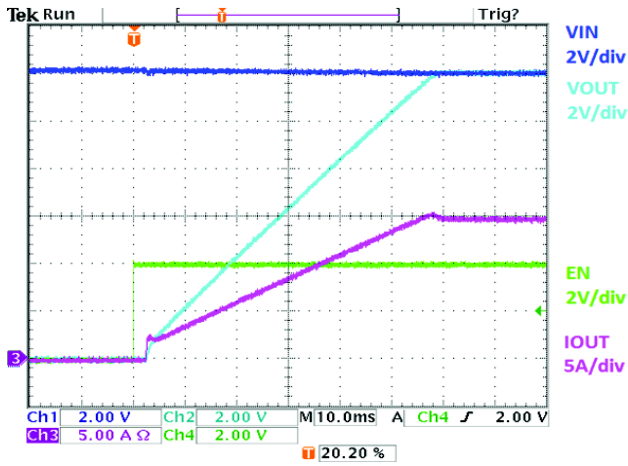


Figure 25. Start Up by EN (Iout = 15 A)

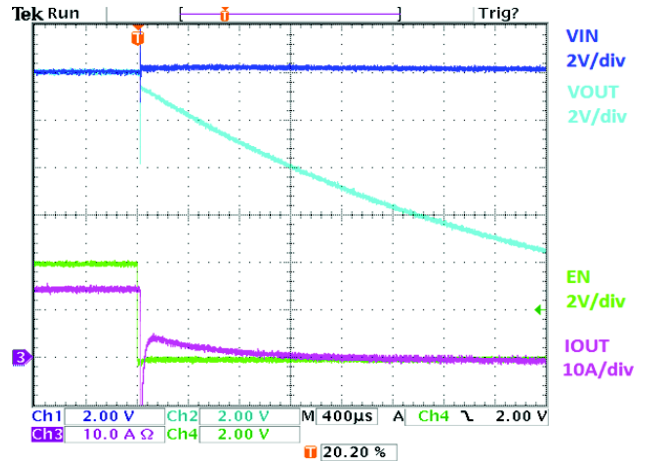


Figure 26. Shut Down by EN (Iout = 15 A)

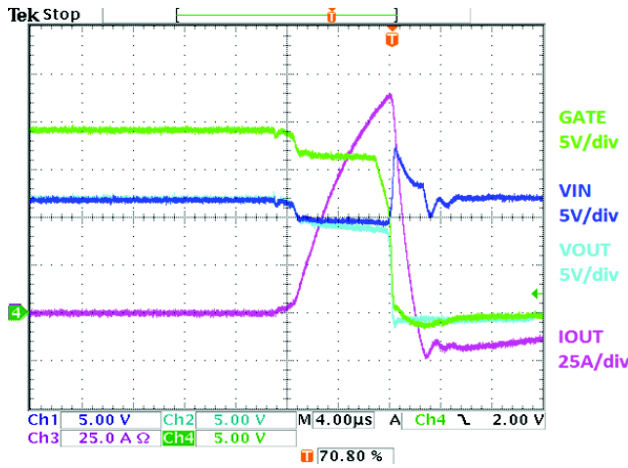


Figure 27. Short Circuit during Normal Operation (Iout = 0 A)

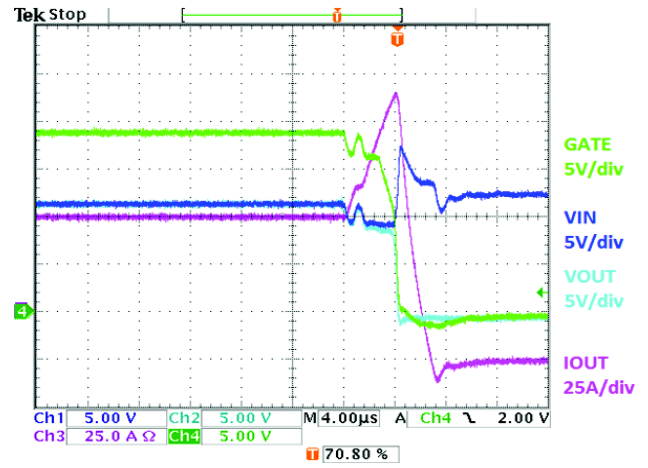


Figure 28. Short Circuit during Normal Operation (Iout = 50 A)

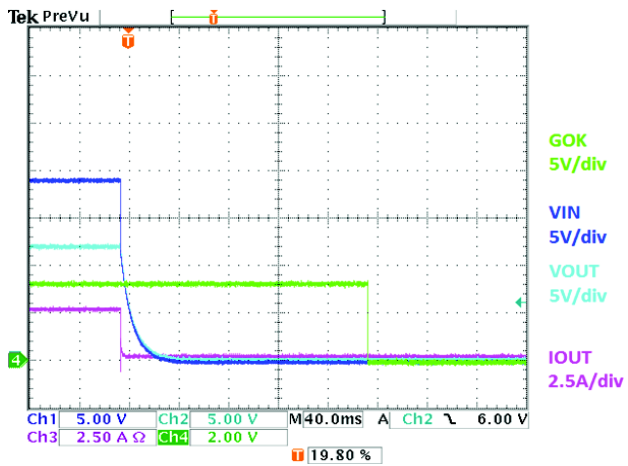


Figure 29. Short FET's Gate During Normal Operation (Iout = 2.5 A)

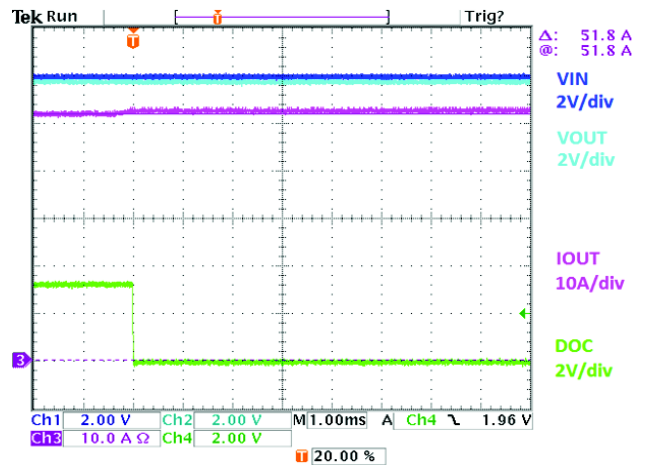


Figure 30. DOC Index for Current Limit during Normal Operation (Iout = 51.8 A)

# NCP81292

## TYPICAL CHARACTERISTICS

Test Conditions:  $V_{in} = 12\text{ V}$ ,  $R_{cs} = 2\text{ k}\Omega$ ,  $C_{ss} = 200\text{ nF}$ ,  $R_{CLREF} = 121\text{ k}\Omega$ ,  $R_{IMON} = 2\text{ k}\Omega$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

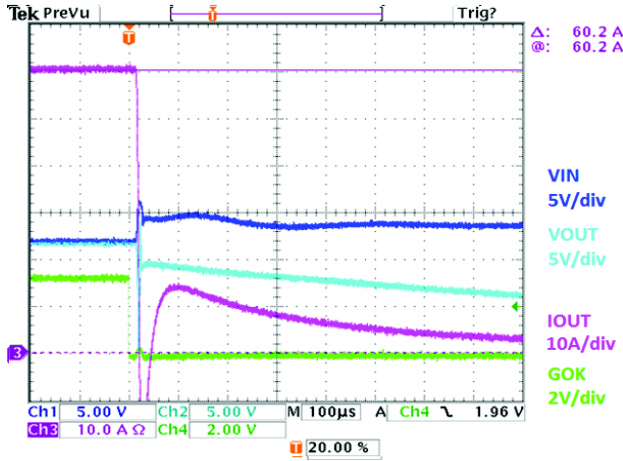


Figure 31. OCP during Normal Operation( $I_{out}=60.2\text{A}$ )

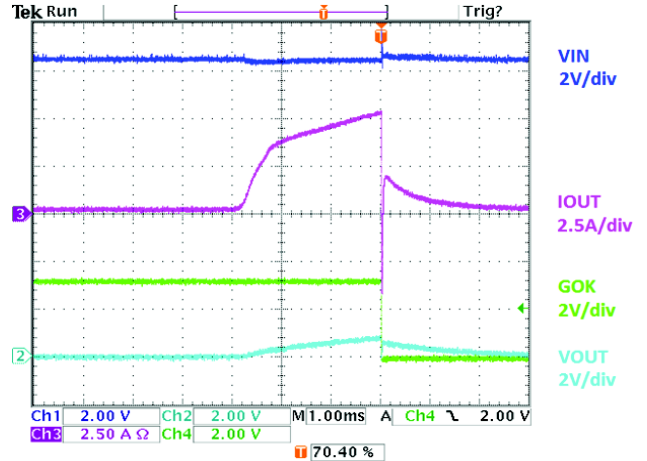


Figure 32. OCP during Power Up by Enable

**General Information**

The NCP81292 is an N-channel MOSFET co-packaged with a smart hotswap controller. It is suited for high-side current limiting and fusing in hot-swap applications. It can be used either alone, or in a parallel configuration for higher current applications.

**VDD Output (Auxiliary Regulated Supply)**

An internal linear regulator draws current from the VIN pin to produce and regulate voltage at the VDD pin. This auxiliary output supply is current-limited to I<sub>DD\_CL</sub>. A ceramic capacitor in the range of 2.2 μF to 10 μF must be placed between the VDD and GND pins, as close to the NCP81292 as possible. The voltage difference between VIN and VIN pin voltage should be within 0.4 V for better CS/IMON performance. Small time constant R/C filter such as 1 Ω/0.1 μF on the VIN pin is recommended.

**ON Input (Device Enable)**

When the ON pin voltage (V<sub>ON</sub>) is higher than V<sub>SWON</sub>, and no undervoltage (UVLO) or output switch faults are present, the output switch turns on. When V<sub>ON</sub> is lower than V<sub>SWOFF</sub>, the output switch is off. If V<sub>ON</sub> is between V<sub>PDOFF</sub> and V<sub>SWOFF</sub> for longer than t<sub>PD\_DEL</sub>, the output switches off, and a pull-down resistance to ground, of R<sub>PD</sub>, is applied to VOUT. In other words, there is behavior as follows:

- When V<sub>ON</sub> < 0.8 V, FET turns off.
- When 0.8 V < V<sub>ON</sub> < 1.2 V, VOUT will discharge with ~ 15 mA.
- When V<sub>ON</sub> > 1.2 V, FET turns on.

For standalone applications, the ON pin sources current I<sub>ON</sub>, which can be used to delay output switch turn-on for some time after the appearance of input voltage by connecting a capacitor from the ON pin to ground.

A bi-level control signal driving to ground can be biased up with a resistive divider to produce ON input levels between V<sub>PDOFF</sub> < V<sub>ON</sub> < V<sub>SWON</sub> and V<sub>ON</sub> > V<sub>SWON</sub> in order to always apply the output pull-down when the output switch is off.

**SS Output (Soft-Start)**

When the output switch first turns on, it does so in a controlled manner. The output voltage (VOUT) follows the voltage at the SS pin, produced by current I<sub>SS</sub> into a capacitor from SS to ground. The duration of soft-start can be programmed by selection of the capacitor value. In parallel fuse applications, the SS pins of all fuses should be shorted together to one shared SS capacitor. Internal soft-start load balancing circuitry will ensure the soft-start current is shared between paralleled devices, so as not to stress one device more than another or hit a soft start-current limit.

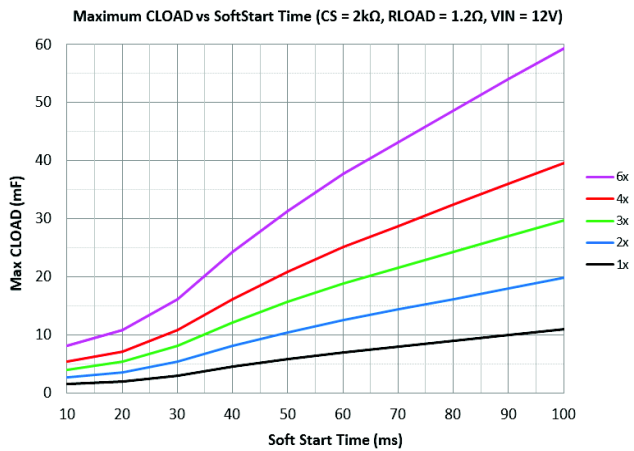
The soft-start capacitor value can be calculated by:

$C_{SS} = (t_{SS} * I_{SS} * AV_{SS})/VIN$  (where t<sub>SS</sub> is the target soft-start time). The recommended range of t<sub>SS</sub> is 10 – 100 ms.

The typical C<sub>SS</sub> values for different t<sub>SS</sub> are listed below:

t <sub>SS</sub> (ms)	C <sub>SS</sub> (nF)	t <sub>SS</sub> (ms)	C <sub>SS</sub> (nF)
10	47	60	270
20	82	70	330
30	120	80	330
40	180	90	470
50	220	100	470

The maximum load capacitor value NCP81292 can power up depends on the device soft-start time. When V<sub>IN</sub> = 12 V, R<sub>CS</sub> = 2 kΩ, R<sub>LOAD</sub> = 2.4 Ω, their relationship for different paralleled operations are shown as below chart (above line device shuts down safely due to protection, below line device powers up successfully without trigger protection):



**GOK Output (Gate OK)**

The GOK pin is an open-drain output that is pulled low to report the fault under the following conditions:

- V<sub>DD</sub> voltage is below UVLO voltage at any time.
- V<sub>ON</sub> disabled and V<sub>DS\_OK</sub> is false (indicates a short from VIN to VOUT).
- V<sub>ON</sub> disabled and V<sub>DG\_OK</sub> is false (indicates a short from GATE to VIN).
- V<sub>ON</sub> enabled and V<sub>SS\_OK</sub> is false at t<sub>SSF\_END</sub> (indicates VOUT < 90% after soft-start completes).
- V<sub>ON</sub> enabled and V<sub>G</sub> is below V<sub>G\_TH</sub> at t<sub>SSF\_END</sub> (indicates leakage on GATE in startup).
- V<sub>ON</sub> enabled and V<sub>G</sub> is below V<sub>G\_TH</sub> after t<sub>GATE\_FLT</sub> (indicates leakage on GATE during normal operation).
- V<sub>ON</sub> enabled and a current-limiting condition lasts longer than t<sub>OC\_LA</sub>
- V<sub>ON</sub> enabled and device temperature is above T<sub>TSD</sub> (indicates an over-temperature is detected).

Usually GOK can't be used as power good to indicate the output voltage is in the normal range.

**IMON Output (Current Monitor)**

The IMON pin sources a current that is  $A_{IMON}$  (10  $\mu$ A/A) times the VOUT output current. A resistor connected from the IMON pin to ground can be used to monitor current information as a voltage up to  $V_{IM\_CLMP}$ . A capacitor of any value in parallel with the IMON resistor can be used to low-pass filter the IMON signal without affecting any internal operation of the device.

**CLREF Pin (Current Limit and Over-Current Reference)**

The CLREF pin voltage determines the current-limit regulation point and over-current indication point via its interaction with the CS pin voltage. The CLREF voltage can be applied by an external source, such as a hot-swap controller or D-to-A converter, or developed across a programming resistor to ground by the CLREF bias current,  $I_{CL}$ . The recommended range of CLREF voltage is 0.2 – 1.55 V.

**CS Input/Output (Current Set)**

The CS pin is both an input and an output. The CS pin sources a current that is  $A_{CS}$  (10  $\mu$ A/A) times the VOUT current. This produces a voltage on the CS pin that is the product of the CS pin current and an external CS pin resistance to ground.

The voltage generated on  $V_{CS}$  determines the D\_OC over-current indicator trip point and the current-limit regulation point, via its interaction with the voltage on CLREF pin.

When the voltage on the CS pin is higher than  $V_{OC\_TH}$ , D\_OC is pulled low. If the CS pin voltage drops below  $V_{OC\_TH}$ , the D\_OC pin is released to and gets pulled high by the external pullup resistor. D\_OC transitions based on the following formula:

$$I_{OUT} = \frac{V_{OC\_TH} + V_{ENACT}}{R_{CS} \cdot 10 \mu} \quad (\text{eq. 1})$$

The  $V_{OC\_TH}$  trip point is based on a percentage of  $V_{CLREF}$  (86%).

During normal operation ( $V_{ON} > V_{SWON}$  for longer than  $t_{SS\_END}$ ), if the voltage on the CS pin is above  $V_{CL\_TH}$  ( $V_{CL\_TH}$  is clamped at  $V_{CL\_MX}$  if  $V_{CL\_TH} > V_{CL\_MX}$ ), then the gate voltage of the FET is modulated to limit current into the output based on the following formula:

$$I_{OUT} = \frac{V_{CL\_TH} + V_{ENACT}}{R_{CS} \cdot 10 \mu} \quad (\text{eq. 2})$$

The  $V_{CL\_TH}$  regulation point is equal to  $V_{CLREF}$ .

During startup ( $V_{ON} > V_{SWON}$  for less than  $t_{SS\_END}$ ), the current limit reference voltage is clamped according to the following:

- When  $V_{OUT} < 40\%$  of  $V_{IN}$ ,  $V_{CL\_TH} = V_{CL\_LO}$  or  $V_{CLREF}$  (whichever is lower).
- When  $V_{OUT}$  is between 40% and 80% of  $V_{IN}$ ,  $V_{CL\_TH} = V_{CL\_HI}$  or  $V_{CLREF}$  (whichever is lower).
- When  $V_{OUT}$  exceeds 80% of  $V_{IN}$ ,  $V_{CL\_TH} = V_{CL\_MX}$  or  $V_{CLREF}$  (whichever is lower).

During soft-start, current is actively limited to  $V_{CL\_TH}$  for up to  $t_{CL\_REG}$  before the device shuts off and automatically restarts. Once  $t_{SS\_END}$  elapses, current exceeding the limit established by  $V_{CLREF}$  for  $> t_{CL\_LA}$  results in device shutdown and automatic restart.

The CS pin must have no capacitive loading other than parasitic device/board capacitance to function correctly. The recommended range of  $R_{CS}$  is 1.8 – 4 k $\Omega$ .

**CS AMP**

NCP81292 uses an auto-zero Op-Amp to sense current in FET with high-accuracy. The internal IMON and CS current source follow below relationship:

$$I_{OUT} = \frac{I_{CS}}{10 \mu} \quad (\text{eq. 3})$$

and

$$I_{OUT} = \frac{I_{MON}}{10 \mu} \quad (\text{eq. 4})$$

**D\_OC Output (Over-current Indicator)**

The D\_OC pin is an open-drain output that indicates when an over-current condition exists after soft-start is complete. When the voltage on the CS pin is higher than  $V_{OC\_TH}$ , D\_OC is pulled low. If output current drops below  $V_{OC\_TH}$ , the D\_OC pin is released and gets pulled high by an external pullup resistor.

**VTEMP Output (Temperature Indicator)**

VTEMP is a voltage output proportional to device temperature, with an offset voltage. The VTEMP output can source much more current than it can sink, so that if multiple VTEMP outputs are connected together, the voltage of all VTEMP outputs will be driven to the voltage produced by the hottest NCP81292. A 100 nF capacitor or greater must be connected from the VTEMP pin to ground.

## Auto-Retry Restart

Under certain fault conditions, the FET is turned off and another soft-start procedure takes place. Between the fault and the new soft-start, there is a delay of  $t_{DLY\_RETRY}$ . The protection features that use this hiccup mode restart are:

- Over-Current
- Short-Circuit Detection
- Over-Temperature
- Excessive Soft-Start Duration
- Gate Leakage

## Protection Features

For the following protection features, the FET turns off and initiates a restart, unless noted otherwise.

### Excessive Current Limiting

If a current limiting condition exists anytime for a continuous duration  $> t_{CL\_LA}$ , then the FET restarts.

### Excessive Soft-Start Duration

During soft-start, current is actively limited to  $V_{CL\_TH}$  for up to  $t_{CL\_REG}$  before the device shuts off and automatically restarts. Once  $t_{SS\_END}$  elapses, current exceeding the limit established by  $V_{CLREF}$  for  $> t_{CL\_LA}$  results in device shutdown and automatic restart.

### Short Circuit Detection

If switch current exceeds  $I_{SC}$ , the device reacts within  $t_{SC}$ , and the FET restarts. The short-circuit current monitor is independent of CS, CLREF, IMON and current limit setting (cannot be changed externally).

### Over-Temperature Shutdown

If the FET controller temperature  $> T_{TSD}$ , then the FET restarts.

## FET Fault Detection

The device contains various FET monitoring circuits:

- VIN to VOUT short: If the device is disabled and  $V_{OUT} > V_{DS\_TH}$  then GOK is pulled low and the device is prevented from powering up. The device is allowed to power up once  $V_{OUT} < V_{DS\_OK}$ .
- GATE to VIN short: If the device is disabled and  $GATE (Pin 8) > V_{DG\_TH}$ , then GOK is pulled low and device is prevented from powering up. The device is allowed to power up once  $GATE < V_{DG\_OK}$ .
- GATE leakage – startup.  
If  $(GATE - V_{INF}) < V_{G\_TH}$  at  $t_{SS\_END}$ , then GOK is pulled low and FET restarts.
- GATE leakage – normal operation.  
If  $(GATE - V_{INF}) < V_{G\_TH}$  for  $t_{GATE\_FLT}$  time after the soft-start timer completes, then GOK is pulled low and device restarts.

## FET SOA Limits

In-built timed current limits and fault-monitoring circuits ensure the co-packaged FET is always kept within SOA limits.

The NCP81292 is rated for 50 A continuous current. For repetitive pulsed loads up to 80 A with a period less than 200 ms, 50 A RMS is supported.

## Multiple Fuse Power Up

When multiple NPC81292 are paralleled together as shown in Figure 4, they will turn on together. Keeping the current through each switch within 1 A (typical) helps to prevent overstress on each switching during soft-start.

For stand-alone parallel applications, the ON and GOK pins should be connected as shown in Figure 7 to synchronize hiccup timing and prevent cascading faults.

When using system  $\mu$ Controller for parallel applications (Figure 4), the  $\mu$ Controller should be provisioned such that ON is not asserted until GOK is released to high state.