Operational Amplifier, Low Power, 1.2 MHz, 42 μA

NCS20081/2/4, NCV20081/2/4

The NCS20081/2/4 is a family of single, dual and quad Operational Amplifiers (Op Amps) with 1.2 MHz of Gain−Bandwidth Product (GBWP) While consuming only 42 μA of Quiescent current per opamp. The NCS2008x has Input Offset Voltage of 4 mV and operates from 1.8 V to 5.5 V supply voltage over a wide temperature range (−40°C to +125°C). The Rail−to−Rail In/Out operation allows the use of the entire supply voltage range while taking advantage of the 1.2 MHz GBWP. Thus, this family offers superior performance over many industry standard parts. These devices are AEC−Q100 qualified which is denoted by the NCV prefix.

NCS2008x's low current consumption and low supply voltage performance in space saving packages, makes them ideal for sensor signal conditioning and low voltage current sensing applications in Automotive, Consumer and Industrial markets.

Features

- Wide Bandwidth: 1.2 MHz
- Low Supply Current/ Channel: 42 μA typ (V_S = 1.8 V)
- Low Input Offset Voltage: 4 mV max
- Wide Supply Range: 1.8 V to 5.5 V
- Wide Temperature Range: −40°C to +125°C
- Rail−to−Rail Input and Output
- Unity Gain Stable
- Available in Single, Dual and Quad Packages
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

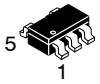
Applications

- Automotive
- Battery Powered/ Portable
- Sensor Signal Conditioning
- Low Voltage Current Sensing
- Filter Circuits
- Unity Gain Buffer

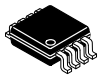
ON Semiconductor®

www.onsemi.com

SC70−5
CASE 419A

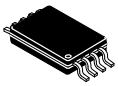


TSOP−5/SOT23−5
CASE 483

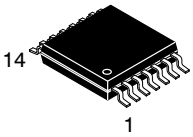


Micro8/MSOP8
CASE 846A

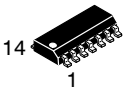
SOIC−8
CASE 751



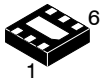
TSSOP−8
CASE 948S



TSSOP−14
CASE 948G



SOIC−14
CASE 751A



UDFN6
CASE 517AP

DEVICE MARKING INFORMATION

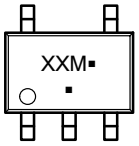
See general marking information in the device marking section on page 2 of this data sheet.

ORDERING INFORMATION

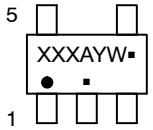
See detailed ordering and shipping information on page 3 of this data sheet.

MARKING DIAGRAMS

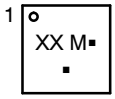
Single Channel Configuration
NCS20081, NCV20081



SC70−5
CASE 419A

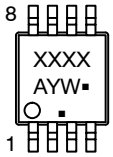


TSOP−5/SOT23−5
CASE 483

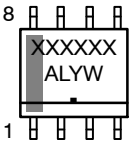


UDFN6
CASE 517AP

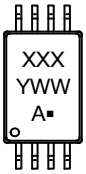
Dual Channel Configuration
NCS20082, NCV20082



Micro8™/MSOP8
CASE 846A

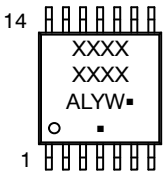


SOIC−8
CASE 751

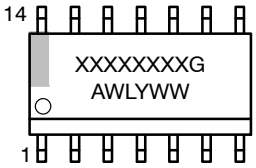


TSSOP−8
CASE 948S

Quad Channel Configuration
NCS20084, NCV20084



TSSOP−14
CASE 948G

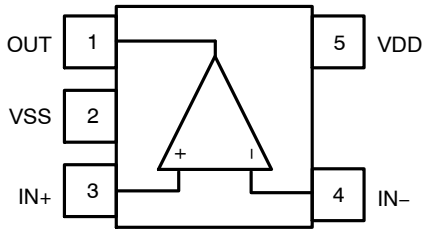


SOIC−14
CASE 751A

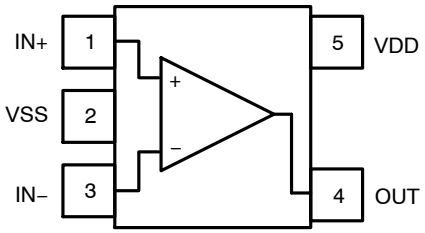
XXXXX = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package

(Note: Microdot may be in either location)

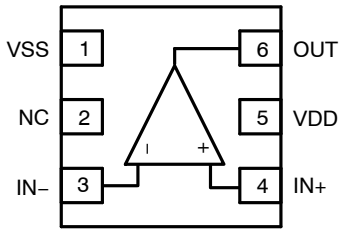
Single Channel Configuration
NCS20081, NCV20081



SC70−5, SOT23−5 (TSOP−5)
SQ2, SN2 Pinout

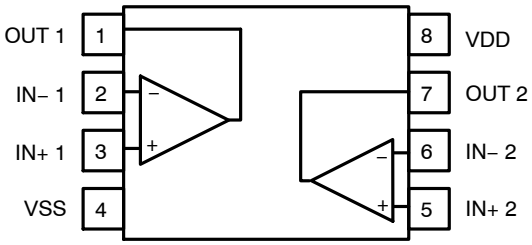


SC70−5, SOT23−5 (TSOP−5)
SQ3, SN3 Pinout



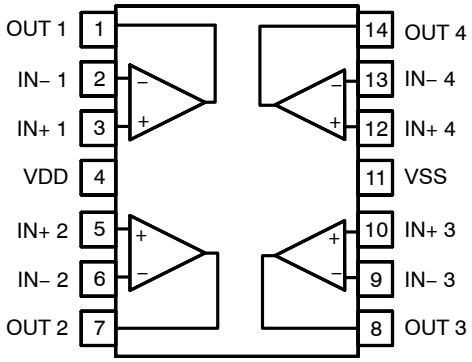
UDFN6 1.6 x 1.6

Dual Channel Configuration
NCS20082, NCV20082



Micro8/MSOP8, SOIC−8, TSSOP−8

Quadruple Channel Configuration
NCS20084, NCV20084



TSSOP−14, SOIC−14

Figure 1. Pin Connections

ORDERING INFORMATION

Device	Configuration	Automotive	Marking	Package	Shipping†
NCS20081SQ2T2G	Single	No	AAX	SC70	Contact local sales office for more information
NCS20081SQ3T2G			AAP	SC70	
NCS20081SN2T1G			AER	SOT23−5/TSOP−5	
NCS20081SN3T1G			AEU	SOT23−5/TSOP−5	
NCS20081MUTAG			AP	UDFN6	
NCV20081SQ2T2G*		Yes	AAX	SC70	
NCV20081SQ3T2G*			AAP	SC70	
NCV20081SN2T1G*			AER	SOT23−5/TSOP−5	
NCV20081SN3T1G*			AEU	SOT23−5/TSOP−5	
NCS20082DMR2G	Dual	No	2K82	Micro8/MSOP8	
NCS20082DR2G			NCS20082	SOIC−8	
NCS20082DTBR2G			K82	TSSOP−8	
NCV20082DMR2G*		Yes	2K82	Micro8/MSOP8	
NCV20082DR2G*			NCS20082	SOIC−8	
NCV20082DTBR2G*			K82	TSSOP−8	
NCS20084DR2G	Quad	No	20084	SOIC−14	
NCS20084DTBR2G			284	TSSOP−14	
NCV20084DR2G*		Yes	20084	SOIC−14	
NCV20084DTBR2G*			284	TSSOP−14	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Rating	Symbol	Limit	Unit
Supply Voltage (V_{DD} – V_{SS}) (Note 2)	V_S	6	V
Input Voltage	V_I	V_{SS} – 0.5 to V_{DD} + 0.5	V
Differential Input Voltage	V_{ID}	$\pm V_s$	V
Maximum Input Current	I_I	±10	mA
Maximum Output Current	I_O	±100	mA
Continuous Total Power Dissipation (Note 2)	P_D	200	mW
Maximum Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	–65 to 150	°C
Mounting Temperature (Infrared or Convection – 20 sec)	T_{mount}	260	°C
ESD Capability (Note 3) Human Body Model Charge Device Model	ESD_{HBM} ESD_{CDM}	2000 2000	V
Latch–Up Current (Note 4)	I_{LU}	100	mA
Moisture Sensitivity Level (Note 5)	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS for Safe Operating Area.
2. Continuous short circuit operation to ground at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of the maximum output current rating over the long term may adversely affect reliability. Shorting output to either VDD or VSS will adversely affect reliability.
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per JEDEC standard Js–001–2017 (AEC–Q100–002)
   ESD Charged Device Model tested per JEDEC standard JS–002–2014 (AEC–Q100–011)
4. Latch–up Current tested per JEDEC standard JESD78E (AEC–Q100–004)
5. Moisture Sensitivity Level tested per IPC/JEDEC standard: J–STD–020A

THERMAL INFORMATION

Parameter	Symbol	Channels	Package	Single Layer Board (Note 6)	Multi–Layer Board (Note 7)	Unit
Junction to Ambient Thermal Resistance	θ_{JA}	Single	SC–70	491	444	°C/W
			SOT23–5/TSOP–5	310	247	
			UDFN6	278	239	
		Dual	Micro8/MSOP8	236	167	
			SOIC–8	190	131	
			TSSOP–8	253	194	
		Quad	SOIC–14	130	99	
			TSSOP–14	178	140	

6. Value based on 1S standard PCB according to JEDEC51–3 with 1.0 oz copper and a 300 mm^2 copper area
7. Value based on 1S2P standard PCB according to JEDEC51–7 with 1.0 oz copper and a 100 mm^2 copper area

OPERATING RANGES

Parameter	Symbol	Min	Max	Unit
Operating Supply Voltage	V_S	1.8	5.5	V
Differential Input Voltage	V_{ID}		V_S	V
Input Common Mode Range	V_{ICM}	V_{SS} – 0.2	V_{DD} + 0.2	V
Ambient Temperature	T_A	–40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS AT V_S = 1.8 V

T_A = 25°C; $R_L \geq 10$ kΩ; $V_{CM} = V_{OUT}$ = mid−supply unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = −40°C to 125°C. (Note 8)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{OS}			0.5	3.5	mV
					4	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1		μV/°C
Input Bias Current (Note 8)	I_{IB}			1		pA
					1500	pA
Input Offset Current (Note 8)	I_{OS}			1		pA
					1100	pA
Channel Separation	XTLK	f = 1 kHz		125		dB
Differential Input Resistance	R_{ID}			10		GΩ
Common Mode Input Resistance	R_{IN}			10		GΩ
Differential Input Capacitance	C_{ID}			1		pF
Common Mode Input Capacitance	C_{CM}			5		pF
Common Mode Rejection Ratio	CMRR	$V_{CM} = V_{SS} - 0.2$ to $V_{DD} + 0.2$	48	73		dB
		$V_{CM} = V_{SS} + 0.2$ to $V_{DD} - 0.2$	**45**			
OUTPUT CHARACTERISTICS						
Open Loop Voltage Gain	A_{VOL}		86	120		dB
			80			
Short Circuit Current	I_{SC}	Output to positive rail, sinking current		15		mA
		Output to negative rail, sourcing current		11		
Output Voltage High	V_{OH}	Voltage output swing from positive rail $V_{OH} = V_{DD} - V_{OUT}$		3	19	mV
					20	
Output Voltage Low	V_{OL}	Voltage output swing from negative rail $V_{OL} = V_{OUT} - V_{SS}$		3	19	mV
					20	
AC CHARACTERISTICS						
Unity Gain Bandwidth	UGBW			1.2		MHz
Slew Rate at Unity Gain	SR	V_{IN} = 1.2 Vpp, Gain = 1		0.4		V/μs
Phase Margin	ψ_m			60		°
Gain Margin	A_m			19		dB
Settling Time	t_S	V_{IN} = 1.2 Vpp, Gain = 1; Settling time to 0.1%		5		μs
		V_{IN} = 1.2 Vpp, Gain = 1; Settling time to 0.01%		6		
Open Loop Output Impedance	Z_{OL}			See Figure 25		Ω
NOISE CHARACTERISTICS						
Total Harmonic Distortion plus Noise	THD+N	V_{IN} = 1.2 Vpp, f = 1 kHz, Av = 1		0.005		%
Input Referred Voltage Noise	e_n	f = 1 kHz		30		nV/√Hz
		f = 10 kHz		24		
Input Referred Current Noise	i_n	f = 1 kHz		300		fA/√Hz
SUPPLY CHARACTERISTICS						
Power Supply Rejection Ratio	PSRR	No Load	67	90		dB
			64			
Power Supply Quiescent Current	I_{DD}	Per channel, no load		42	**60**	μA

8. Performance guaranteed over the indicated operating temperature range by design and/or characterization.

ELECTRICAL CHARACTERISTICS AT V_S = 3.3 V

T_A = 25°C; $R_L \geq 10$ kΩ; $V_{CM} = V_{OUT}$ = mid−supply unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = −40°C to 125°C. (Note 9)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
INPUT CHARACTERISTICS							
Input Offset Voltage	V_{OS}				0.5	3.5	mV
						4	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$				1		μV/°C
Input Bias Current (Note 9)	I_{IB}				1		pA
						1500	pA
Input Offset Current (Note 9)	I_{OS}				1		pA
						1100	pA
Channel Separation	XTLK	f = 1 kHz			125		dB
Differential Input Resistance	R_{ID}				10		GΩ
Common Mode Input Resistance	R_{IN}				10		GΩ
Differential Input Capacitance	C_{ID}				1		pF
Common Mode Input Capacitance	C_{CM}				5		pF
Common Mode Rejection Ratio	CMRR	$V_{CM} = V_{SS} - 0.2$ to $V_{DD} + 0.2$		53	76		dB
		$V_{CM} = V_{SS} + 0.2$ to $V_{DD} - 0.2$		**48**			
OUTPUT CHARACTERISTICS							
Open Loop Voltage Gain	A_{VOL}			90	120		dB
				86			
Short Circuit Current	I_{SC}	Output to positive rail, sinking current			15		mA
		Output to negative rail, sourcing current			11		
Output Voltage High	V_{OH}	Voltage output swing from positive rail $V_{OH} = V_{DD} - V_{OUT}$			3	24	mV
						25	
Output Voltage Low	V_{OL}	Voltage output swing from negative rail $V_{OL} = V_{OUT} - V_{SS}$			3	24	mV
						25	
AC CHARACTERISTICS							
Unity Gain Bandwidth	UGBW				1.2		MHz
Slew Rate at Unity Gain	SR	V_{IN} = 2.5 Vpp, Gain = 1			0.4		V/μs
Phase Margin	ψ_m				60		°
Gain Margin	A_m				18		dB
Settling Time	t_S	V_{IN} = 2.5 Vpp, Gain = 1	Settling time to 0.1%		5		μs
			Settling time to 0.01%		6		
Open Loop Output Impedance	Z_{OL}				See Figure 25		Ω
NOISE CHARACTERISTICS							
Total Harmonic Distortion plus Noise	THD+N	V_{IN} = 2.5 Vpp, f = 1 kHz, Av = 1			0.005		%
Input Referred Voltage Noise	e_n	f = 1 kHz			30		nV/√Hz
		f = 10 kHz			24		
Input Referred Current Noise	i_n	f = 1 kHz			300		fA/√Hz
SUPPLY CHARACTERISTICS							
Power Supply Rejection Ratio	PSRR	No Load		67	90		dB
				64			
Power Supply Quiescent Current	I_{DD}	Per channel, no load			42	**60**	μA

9. Performance guaranteed over the indicated operating temperature range by design and/or characterization.

ELECTRICAL CHARACTERISTICS AT V_S = 5.5 V

T_A = 25°C; $R_L \geq 10$ kΩ; $V_{CM} = V_{OUT}$ = mid−supply unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = −40°C to 125°C. (Note 10)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{OS}			0.5	3.5	mV
					4	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1		μV/°C
Input Bias Current (Note 10)	I_{IB}			1		pA
					1500	pA
Input Offset Current (Note 10)	I_{OS}			1		pA
					1100	pA
Channel Separation	XTLK	f = 1 kHz		125		dB
Differential Input Resistance	R_{ID}			10		GΩ
Common Mode Input Resistance	R_{IN}			10		GΩ
Differential Input Capacitance	C_{ID}			1		pF
Common Mode Input Capacitance	C_{CM}			5		pF
Common Mode Rejection Ratio	CMRR	$V_{CM} = V_{SS} - 0.2$ to $V_{DD} + 0.2$	55	79		dB
		$V_{CM} = V_{SS} + 0.2$ to $V_{DD} - 0.2$	**51**			
OUTPUT CHARACTERISTICS						
Open Loop Voltage Gain	A_{VOL}		90	120		dB
			86			
Short Circuit Current	I_{SC}	Output to positive rail, sinking current		15		mA
		Output to negative rail, sourcing current		11		
Output Voltage High	V_{OH}	Voltage output swing from positive rail $V_{OH} = V_{DD} - V_{OUT}$		3	24	mV
					25	
Output Voltage Low	V_{OL}	Voltage output swing from negative rail $V_{OL} = V_{OUT} - V_{SS}$		3	24	mV
					25	
AC CHARACTERISTICS						
Unity Gain Bandwidth	UGBW			1.2		MHz
Slew Rate at Unity Gain	SR	V_{IN} = 5 Vpp, Gain = 1		0.4		V/μs
Phase Margin	ψ_m			60		°
Gain Margin	A_m			17		dB
Settling Time	t_S	V_{IN} = 5 Vpp, Gain = 1; Settling time to 0.1%		5		μs
		V_{IN} = 5 Vpp, Gain = 1; Settling time to 0.01%		6		
Open Loop Output Impedance	Z_{OL}			See Figure 25		Ω
NOISE CHARACTERISTICS						
Total Harmonic Distortion plus Noise	THD+N	V_{IN} = 5 Vpp, f = 1 kHz, Av = 1		0.005		%
Input Referred Voltage Noise	e_n	f = 1 kHz		30		nV/√Hz
		f = 10 kHz		24		
Input Referred Current Noise	i_n	f = 1 kHz		300		fA/√Hz
SUPPLY CHARACTERISTICS						
Power Supply Rejection Ratio	PSRR	No Load	67	90		dB
			64			
Power Supply Quiescent Current	I_{DD}	Per channel, no load		48	**70**	μA

10. Performance guaranteed over the indicated operating temperature range by design and/or characterization.
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, R_L ≥ 10 kΩ, V_{CM} = V_{OUT} = mid−supply unless otherwise specified

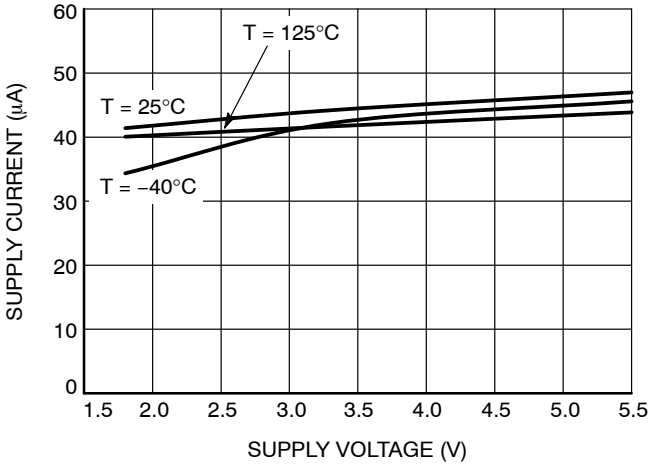


Figure 2. Quiescent Current per Channel vs. Supply Voltage

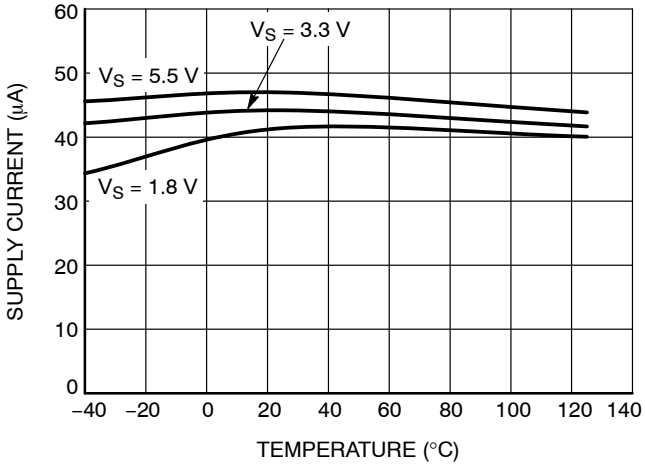


Figure 3. Quiescent Current vs. Temperature

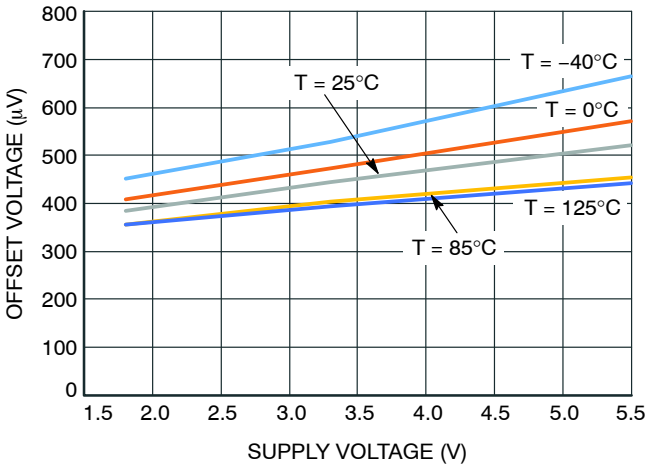


Figure 4. Offset Voltage vs. Supply Voltage

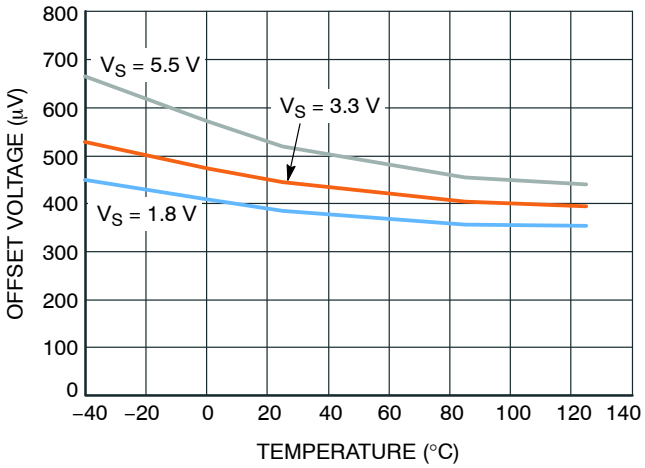


Figure 5. Offset Voltage vs. Temperature

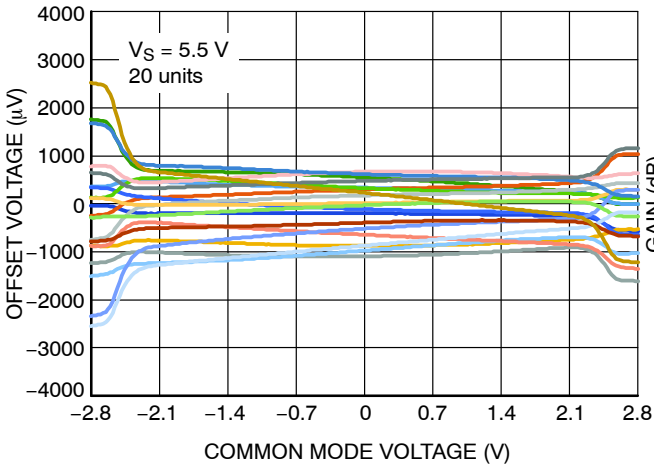


Figure 6. Offset Voltage vs. Common Mode Voltage

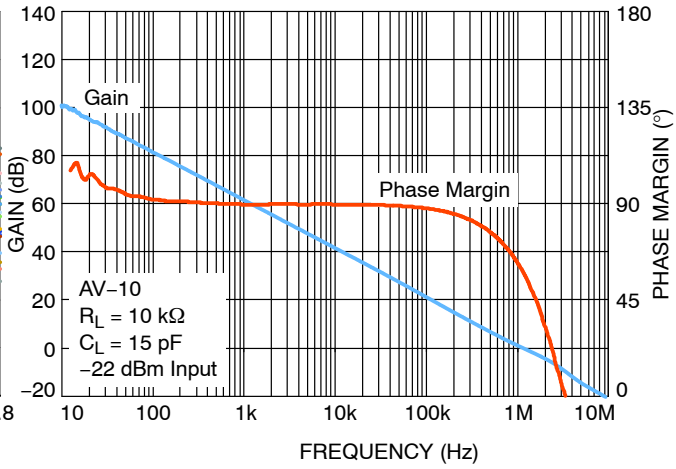


Figure 7. Open−loop Gain and Phase Margin vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, R_L ≥ 10 kΩ, V_{CM} = V_{OUT} = mid−supply unless otherwise specified

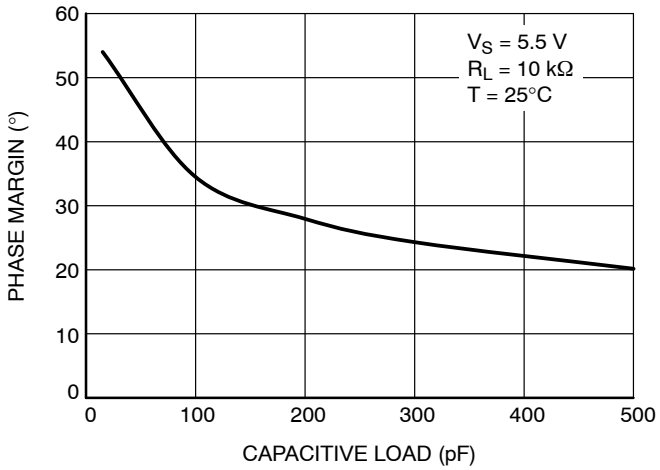


Figure 8. Phase Margin vs. Capacitive Load

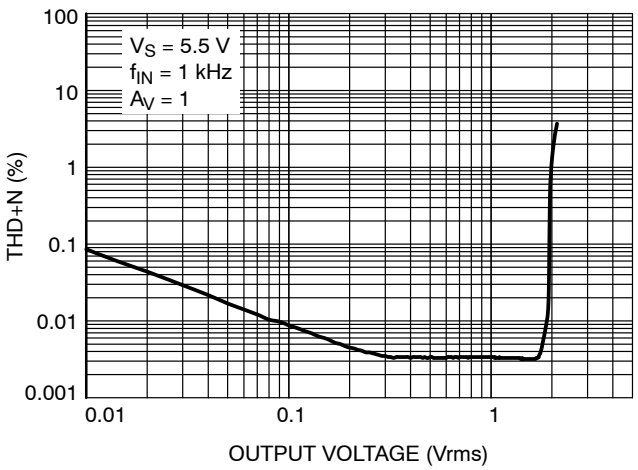


Figure 9. THD + N vs. Output Voltage

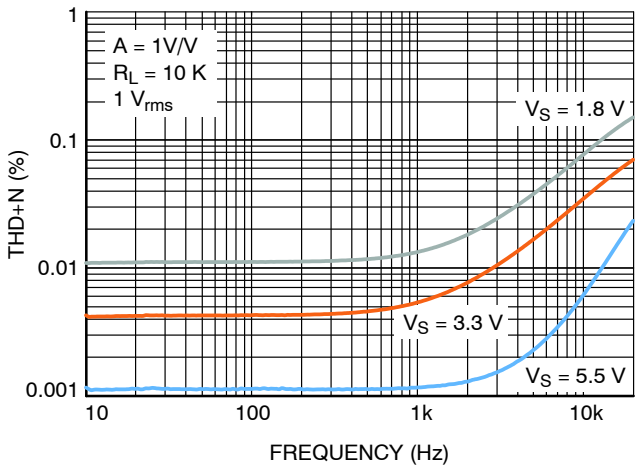


Figure 10. THD + N vs. Frequency

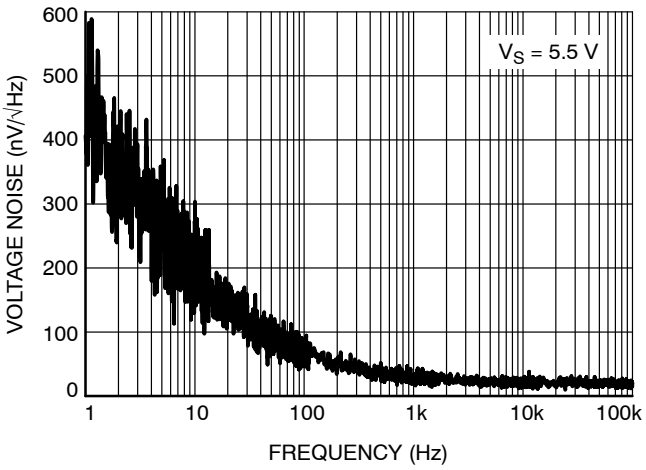


Figure 11. Input Voltage Noise vs. Frequency

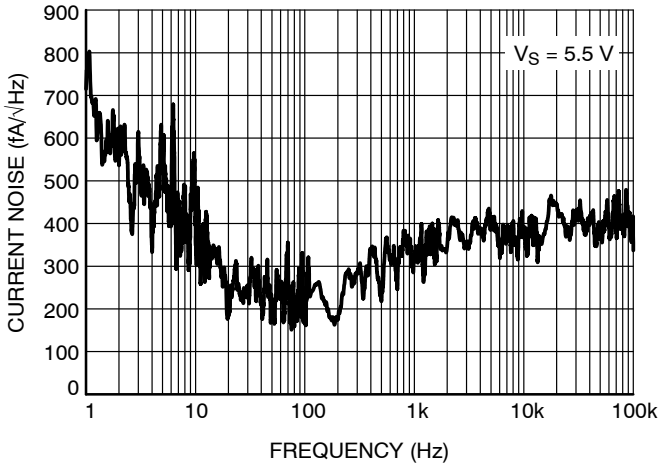


Figure 12. Input Current Noise vs. Frequency

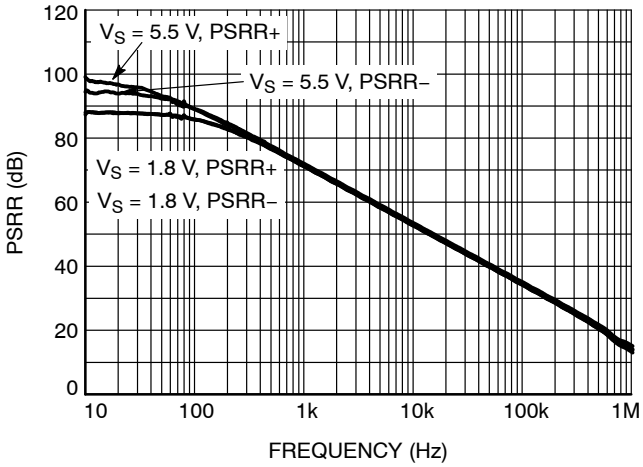


Figure 13. PSRR vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, R_L ≥ 10 kΩ, V_{CM} = V_{OUT} = mid−supply unless otherwise specified

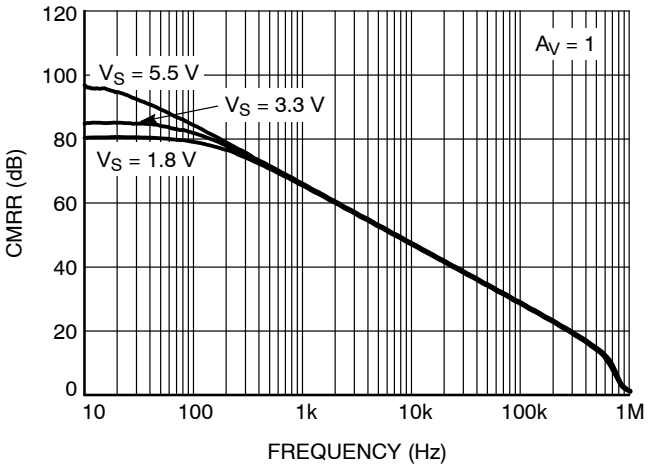


Figure 14. CMRR vs. Frequency

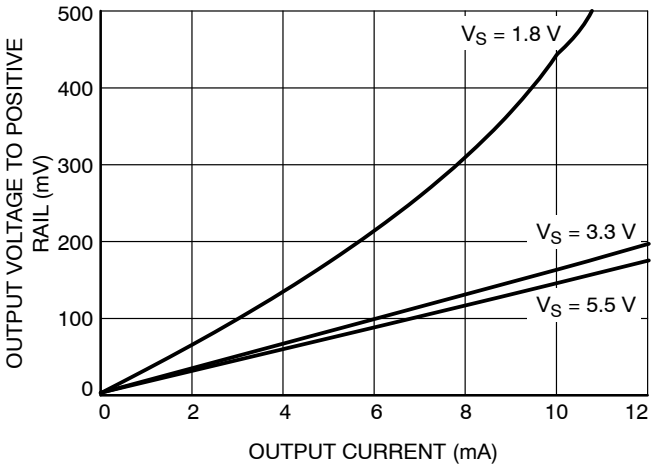


Figure 15. Output Voltage High to Rail

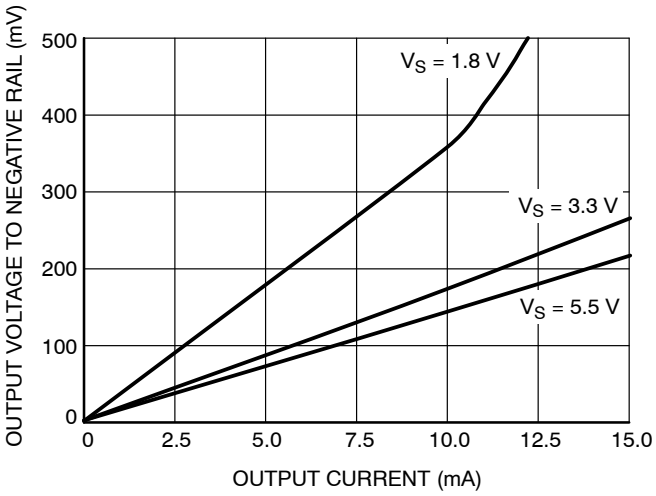


Figure 16. Output Voltage Low to Rail

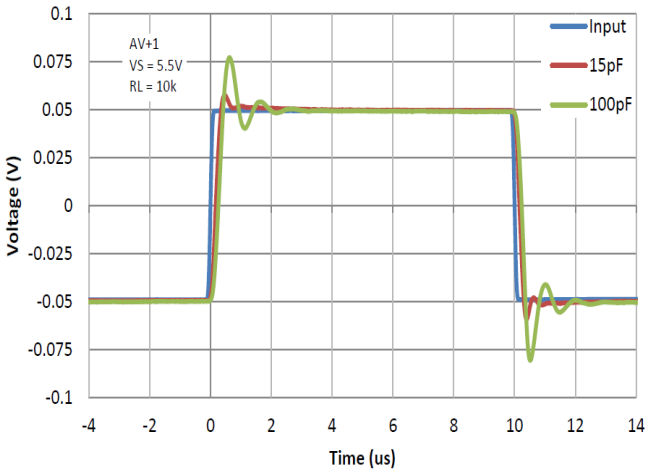


Figure 17. Non−Inverting Small Signal Transient Response

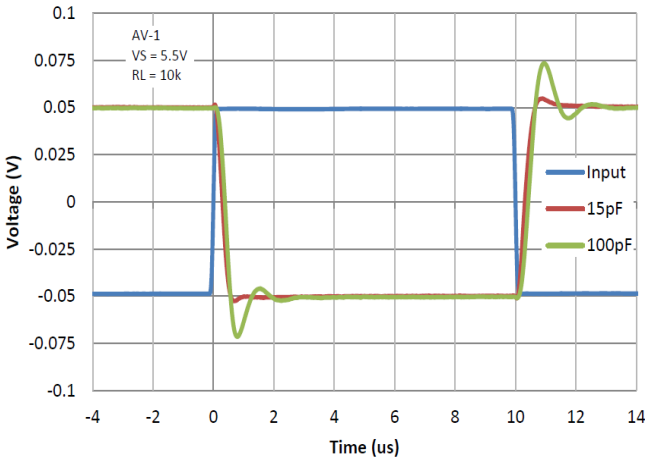


Figure 18. Inverting Small Signal Transient Response

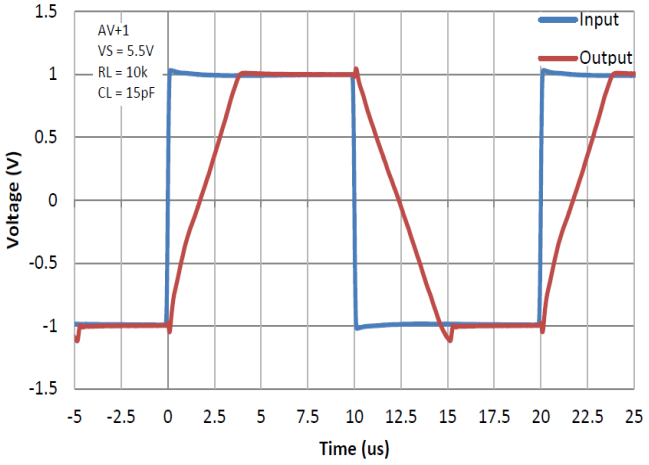


Figure 19. Non−Inverting Large Signal Transient Response

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, R_L ≥ 10 kΩ, V_{CM} = V_{OUT} = mid−supply unless otherwise specified

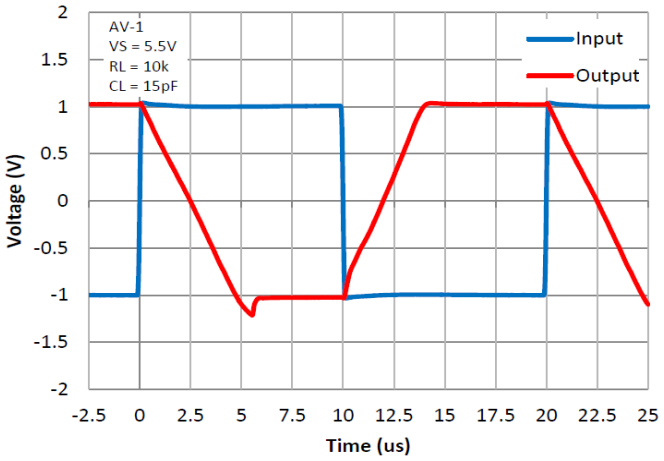


Figure 20. Inverting Large Signal Transient Response

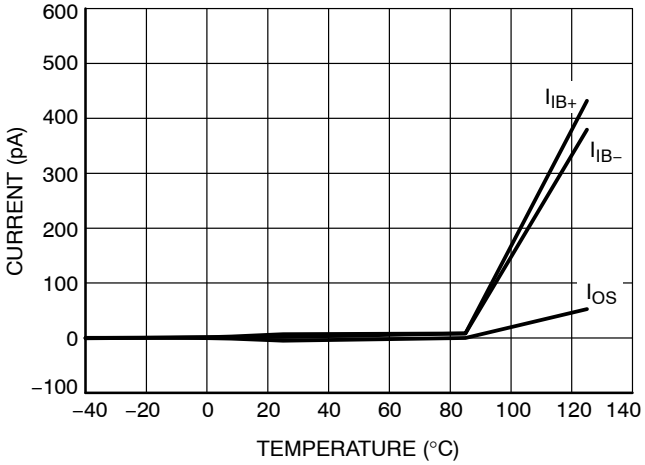


Figure 21. Input Bias and Offset Current vs. Temperature

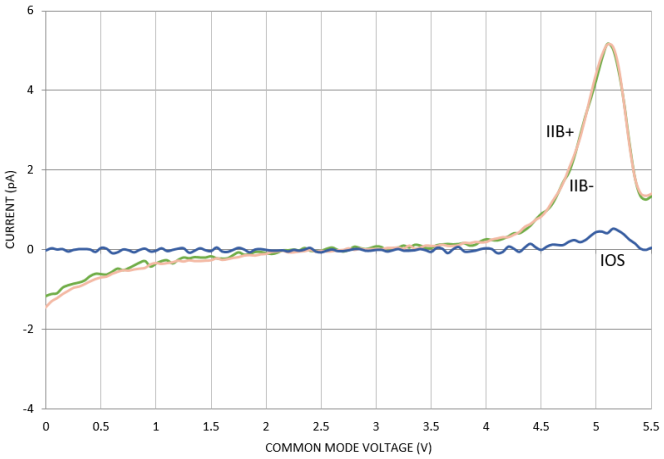


Figure 22. Input Bias Current vs. Common Mode Voltage

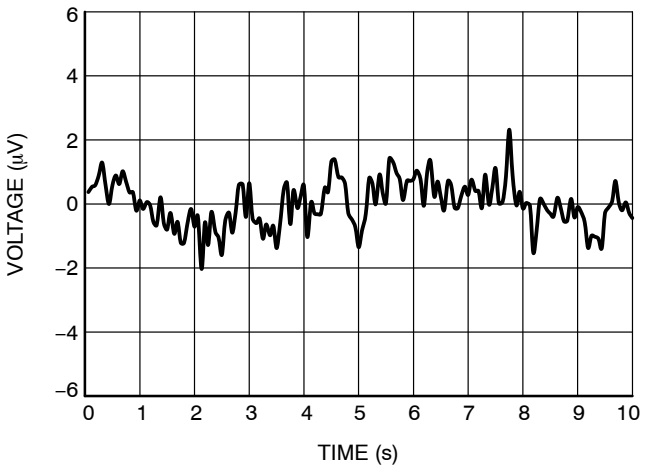


Figure 23. 0.1 Hz to 10 Hz Noise

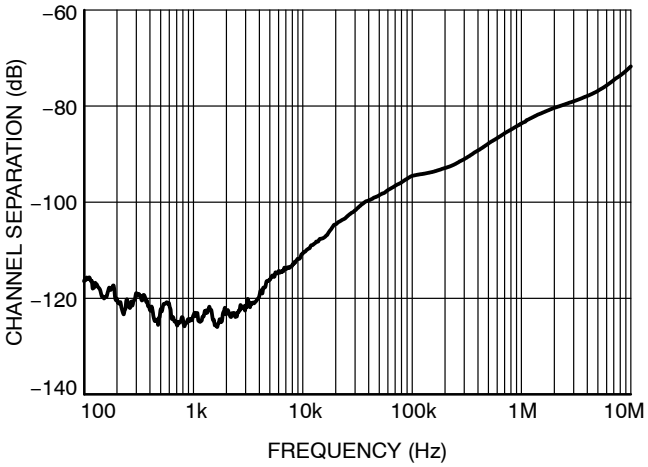


Figure 24. Channel Separation vs. Frequency

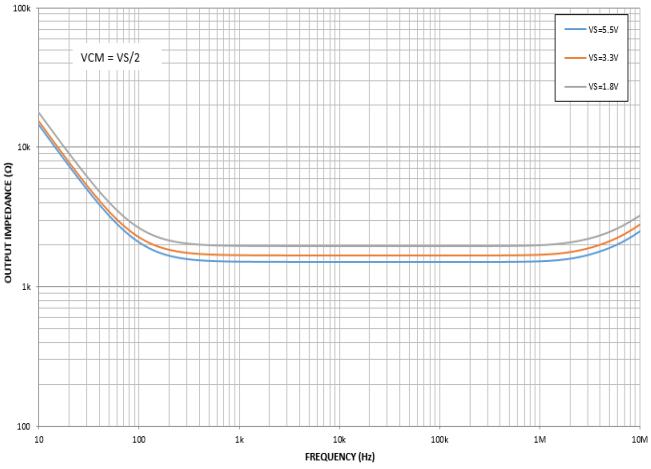


Figure 25. Open Loop Output Impedance vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, $R_L \geq 10$ kΩ, $V_{CM} = V_{OUT}$ = mid−supply unless otherwise specified

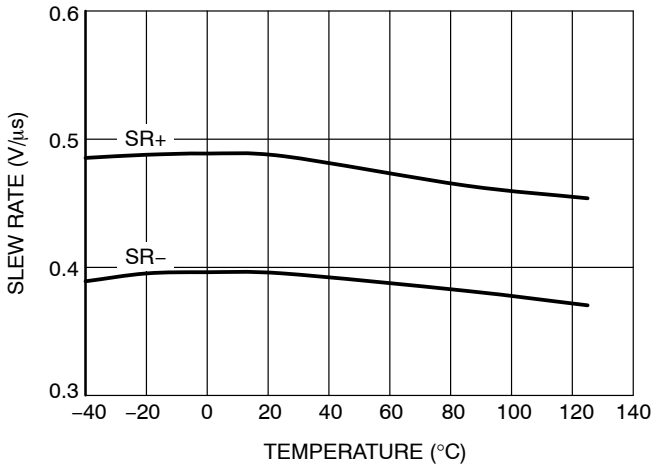


Figure 26. Slew Rate vs. Temperature

Application Information

The NCS/NCV20081/2/4 family of operational amplifiers is manufactured using ON Semiconductor's CMOS process. Products in this class are general purpose, unity−gain stable amplifiers and include single, dual and quad configurations.

Rail−to−Rail Input with No Phase Reversal

The NCS operational amplifiers are designed to prevent phase reversal or any similar issues when the input pins potential exceed the supply voltages by up to 100 mV. Figure 6 shows the input voltage exceeding the supply limits.

The input stage of the NCS/NCV 20081/2/4 family consists of two differential CMOS input stages connected in parallel: the first is constructed using paired PMOS devices and it operates at low common mode input voltages (VCM) ; the second stage is build using paired NMOS devices to operate at high VCM. The transition between the two input stages occurs at a common mode input voltage of approximately VDD–1.3V and it is visible in Figure 6 (Offset vs. VCM).

Limiting Input Voltages

In order to prevent damage and/or improper operation of these amplifiers, the application circuit must never expose the input pins to voltages or currents higher than the Absolute Maximum Ratings.

The internal ESD structure includes special diodes to protect the input stages while maintaining a low Input Bias (IIB) current. The input protection circuitry clamp the inputs when the signals applied exceed more than one diode drop below VSS or one diode drop above VDD. Very fast ESD events (within the limits specified) trigger the protection structure so the operational amplifier is not damaged.

However, in some applications, it can be necessary to prevent excessive voltages from reaching the operational amplifier inputs by adding external clamp diodes. A possible solution is presented in Figure 27, where the four low−drop fast diodes (Shottky preferred) are used in parallel with the internal structure to divert the excessive energy to the supply rails where it can be easily dissipated or absorbed by the supply capacitors. The application designer should also take into account that these external diodes add leakage currents and parasitic capacitance that must be considered when evaluating the end−to−end performance of the amplifier stage.

Limiting Input Currents

In order to prevent damage/ improper operation of these amplifiers, the application circuit must limit the currents flowing in and out of the input pins. A possible solution is presented in Figure 27 by means of the two added series resistors. The minimum value for R_IN− and R_IN+ should be calculated using Ohm's Law so they limit the input pin currents to less than the absolute maximum values specified. The application designer should take into account that these resistors also add parasitic inductance that must be considered when evaluating performance.

Combining the current limiting resistors with the voltage limiting diodes creates a solid input protection structure, that can be used to insure reliable operation of the amplifier even in the hardest conditions.

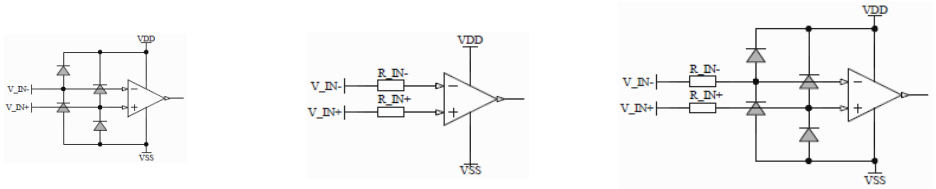


Figure 27. Typical Protection of the Operational Amplifier Inputs

Rail−to−Rail Output

The maximum output voltage swing is dependent of the particular output load. According to the specification, the output can reach within 25 mV of either supply rail when load resistance is 10 kΩ. Figure 15 and Figure 16 shows the load drive capabilities of the part under different conditions. Output current is internally limited to 15 mA typ.

Capacitive Loads

Driving capacitive loads can create stability problems for voltage feedback opamps, as it is a known possible cause for:

- degraded phase margin
- lowered bandwidth
- gain peaking of the frequency response
- overshoot and ringing of the step response.

While the NCS(V)20081/2/4 family of opamps are capable of driving capacitive loads up to 100 pF, adding a small resistor in series to the output (R_ISO in Figure 28) will increase the feedback loop's phase margin. This leads to higher stability by making the equivalent load more resistive at high frequencies.

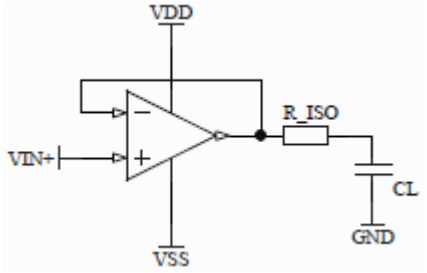


Figure 28. Driving Capacitive Loads

Simulating the application with ON Semiconductor's SPICE models is a good starting point for selecting the isolation resistor's value, and then bench testing the frequency and step response can be used to fine−tune the value according to the desired characteristic.

Unity Gain Bandwidth

Interfacing a high impedance sensor's output to a relatively low−impedance ADC input usually requires an intermediate stage to avoid unwanted interference of the two devices, and this stage needs to have a high input impedance, a low output impedance and high output current.

The unity gain buffer is recommended here (Figure 29).The ADC's internal sampling capacitor requires a buffer front−end to recharge it faster than the sampling time, and this problem is even worse if more channels are sampled by the same ADC using an internal multiplexer. In order to achieve a settling time shorter than the multiplexed sampling rate, an RC stage is recommended between the buffer and the ADC input. The R resistor's value should be low enough to charge the capacitor quickly, but at the same time large enough to isolate the capacitive load from the opamp's output to preserve phase margin. When transients are generated by the sensor's output, first the two opamp's inputs see a high differential voltage between them, then the output settles and brings the inverting input back to the correct voltage.

To successfully accommodate for example a 0.1 V to 4 V sensor signal, the opamp's differential input range of the NCS(V) 20081/2/4 series is close to the supply range VDD−VSS, and the output will match the input. The differential input voltage is limited only by the ESD protection structure and not by back−to−back diodes between inputs.

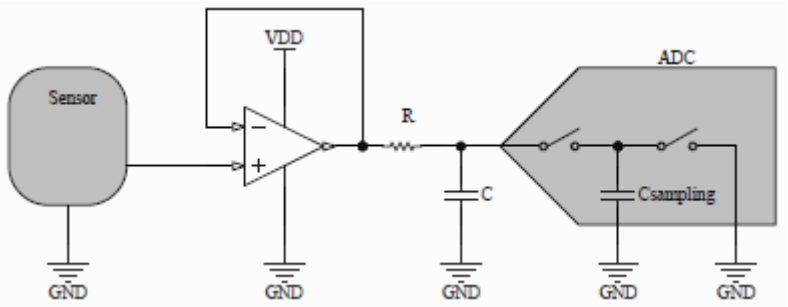


Figure 29. Unity Gain Buffer Stage for Sampling with ADC

Power Supply Bypassing

For AC, the power supply pins (VDD and VSS for split supply, VDD for single supply) should be bypassed locally with a quality capacitor in the range of 100 nF (ceramics are recommended for their low ESR and good high frequency response) as close as possible to the opamp's supply pins.

For DC, a bulk capacitor in the range of 1 μF within inches distance from the opamp can provide the increased currents required to drive higher loads.

Unused Operational Amplifiers

Occasionally not all the opamps offered in the quad packages are needed for a specific application. They can be connected as "buffering ground" as shown in Figure 30, a solution that does not need any extra parts. Connecting them differently (inputs split to rails, left floating, etc.) can sometimes cause unwanted oscillation, crosstalk, increased current consumption, or add noise to the supply rails.

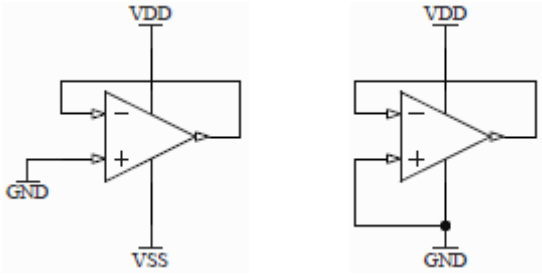


Figure 30. Unused Operational Amplifiers

PCB Surface Leakage

The Printed Circuit Board's surface leakage effects should be estimated if the lowest possible input bias current is critical. Dry environment surface current increases further when the board is exposed to humidity, dust or chemical contamination. For harsh environment conditions, protecting the entire board surface (with all the exposed

metal pins and soldered areas) is advised. Conformal coating or potting the board in resin proves effective in most cases.

An alternate solution for reduced leakage is the use of guard rings around sensitive pins and pads. A proper guard ring should have low impedance and be biased to the same voltage as the sensitive pin so no current flows in between.

For an inverting amplifier, the non−inverting input is usually connected to supply's ground (or virtual ground at half the rail voltage in single supply applications) so it can represent a good ring solution. When routing the PCB traces, create a closed perimeter around the inverting input pad (which carries the signal) and connect it to the non−inverting input.

For a non−inverting amplifier, use a similarly shaped (rectangle or circle) copper trace around the non−inverting input pad (which carries the signal) and connect it to the inverting input pin, which presents a much lower impedance thanks to the feedback network.

PCB Routing Recommendations

Even when some operational amplifier is expected to amplify only the useful DC signal, it can also pick some high frequency noise altogether and amplify it accordingly, if the design allows it. In order to reach the specified operational amplifier parameters and to avoid high frequency interference issues, it is recommended that the PCB layout respects some basic guidelines:

- A dedicated layer for the ground plane should be used whenever possible and all supply decoupling capacitors should connect to it by vias.
- Copper traces should be as short as possible.
- High current paths should not be shared by small signal or low current traces.
- If present, switching power supply blocks should be kept away from the analog sensitive areas to avoid potential conducted and radiated noise issues.
- When different circuit taxonomies share the same board, it is recommended to keep separated the power areas, the digital areas and the small signal analog areas. Small−signal parts in the signal path should be placed as close as possible to the opamp's input pins.
- Metal shielding the sensitive areas and the "offender" blocks may be required in some cases.

In a sensitive application, a good PCB design can take longer but it will save troubleshooting time.

Applications Example

Second Order Active Low Pass Filter

Using an opamp with a low input bias current allows the use of higher value resistors and smaller capacitors for the same filter application. As a trade−off for the increased impedance and lower consumption obtained, the higher value resistors may also bring higher noise and sensibility to board contamination, and possibly frequency response changes (the increased R*C time constant due to parasitic capacitances can change the gain vs. frequency plot).

An example of an active low−pass filter using the NCS2008x operational amplifier can be found in Figure 31. The filter's 3 dB Bandwidth is approximately 25 KHz, followed by a −40 dB/dec roll−off as in Figure 32. Such filters with flat response in the sampled signal band are recommended as a front−end for ADC's to avoid aliasing.

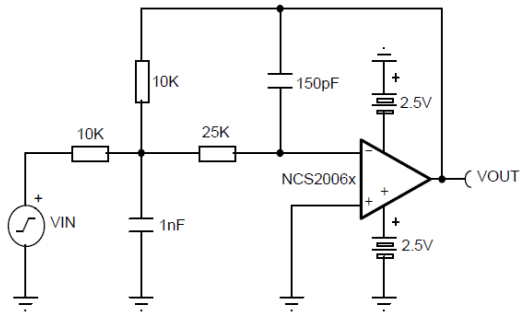


Figure 31. Second Order Active Low Pass Filter

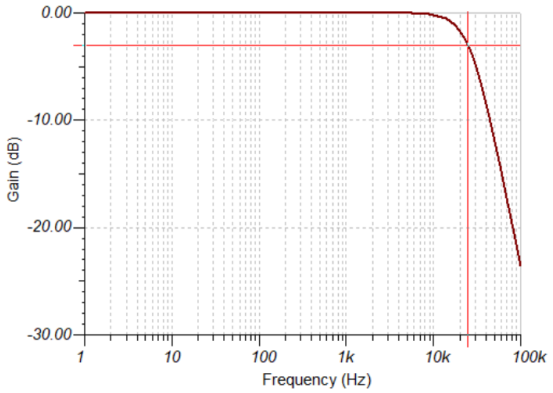


Figure 32. Filter's Frequency Response

Using the P−SPICE models provided by ON Semiconductor is recommended as a starting point for component selection, and then values can be further fine−tuned during bench testing the application.

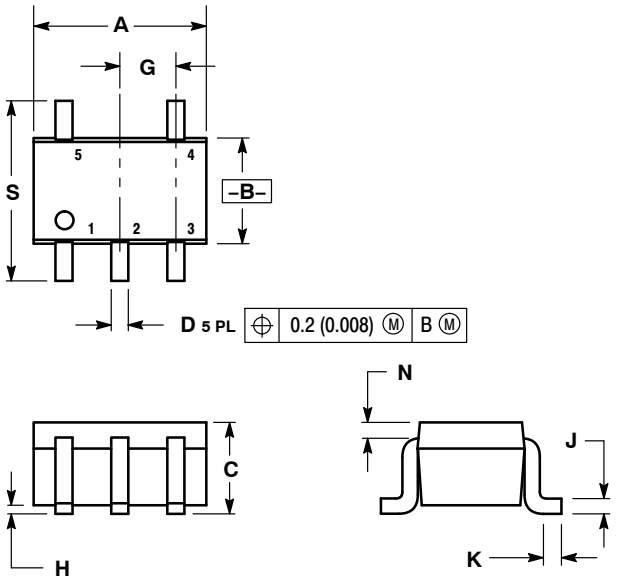
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE L

SCALE 2:1

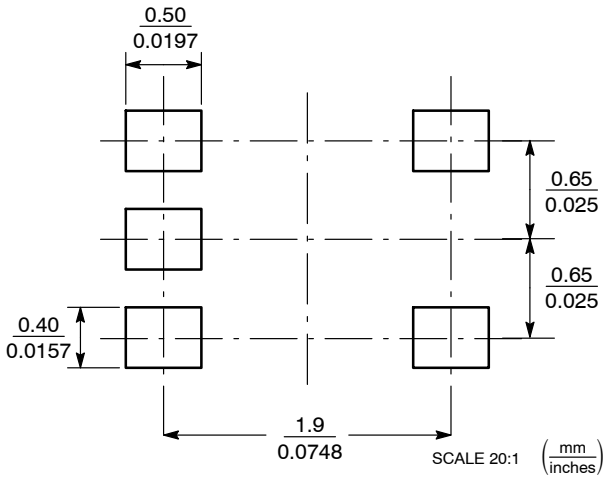
DATE 17 JAN 2013



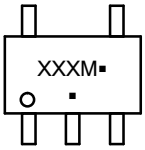
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

SOLDER FOOTPRINT



GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

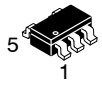
STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

DOCUMENT NUMBER:	98ASB42984B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SC−88A (SC−70−5/SOT−353)	PAGE 1 OF 1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

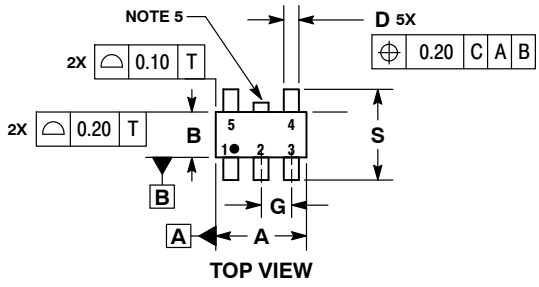
ON Semiconductor®



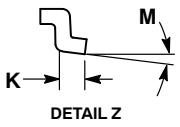
SCALE 2:1

TSOP−5
CASE 483
ISSUE N

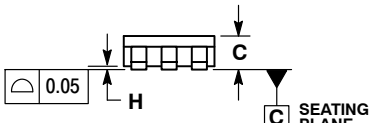
DATE 12 AUG 2020



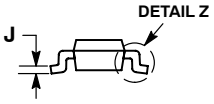
TOP VIEW



DETAIL Z



SIDE VIEW

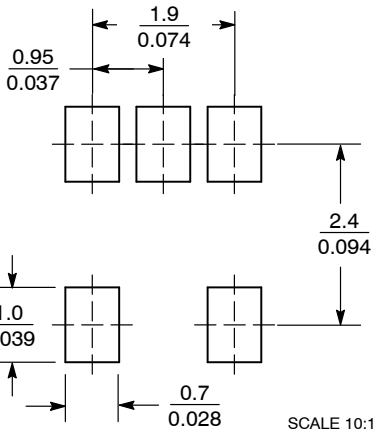


END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0 °	10 °
S	2.50	3.00

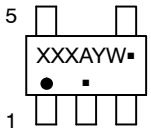
SOLDERING FOOTPRINT*



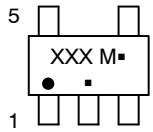
SCALE 10:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



Analog



Discrete/Logic

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	98ARB18753C	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	TSOP−5	PAGE 1 OF 1

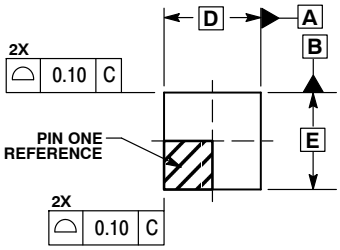
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

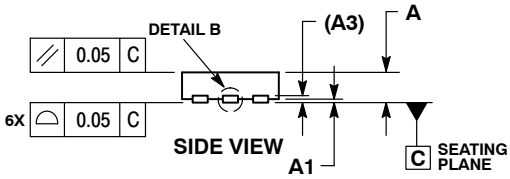
UDFN6 1.6x1.6, 0.5P
CASE 517AP
ISSUE O

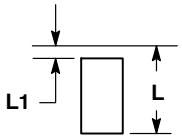
DATE 26 OCT 2007

SCALE 4:1

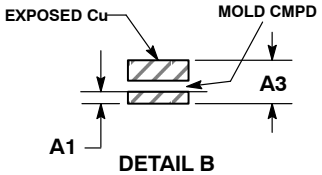


TOP VIEW

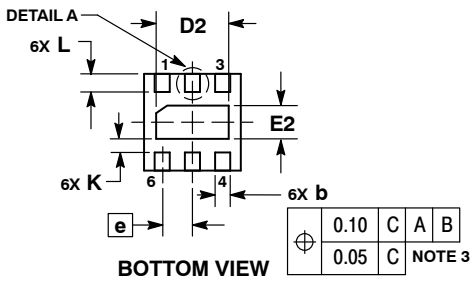




DETAIL A
OPTIONAL CONSTRUCTION

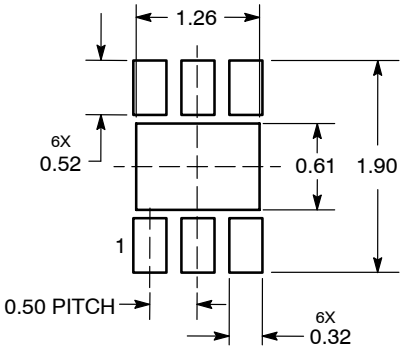


DETAIL B
OPTIONAL CONSTRUCTION



BOTTOM VIEW

SOLDERMASK DEFINED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.20	0.30
D	1.60 BSC	
E	1.60 BSC	
e	0.50 BSC	
D2	1.10	1.30
E2	0.45	0.65
K	0.20	−−−
L	0.20	0.40
L1	0.00	0.15

GENERIC MARKING DIAGRAM*

XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	**98AON25711D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**6 PIN UDFN, 1.6X1.6, 0.5P**		**PAGE 1 OF 1**

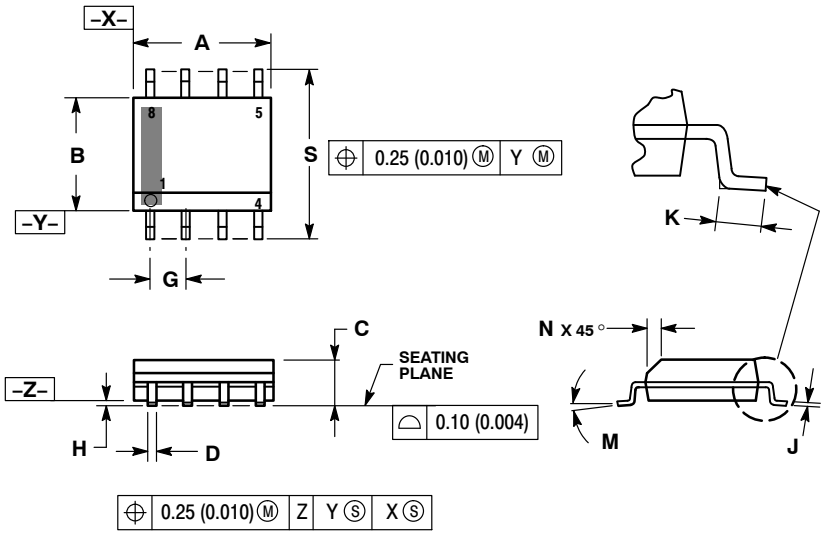
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

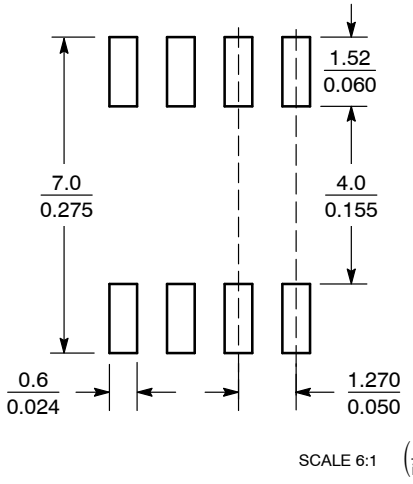
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

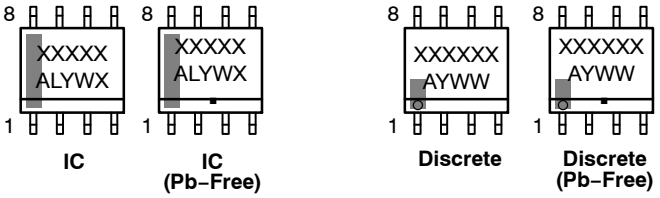
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

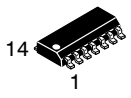
STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 2 OF 2**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

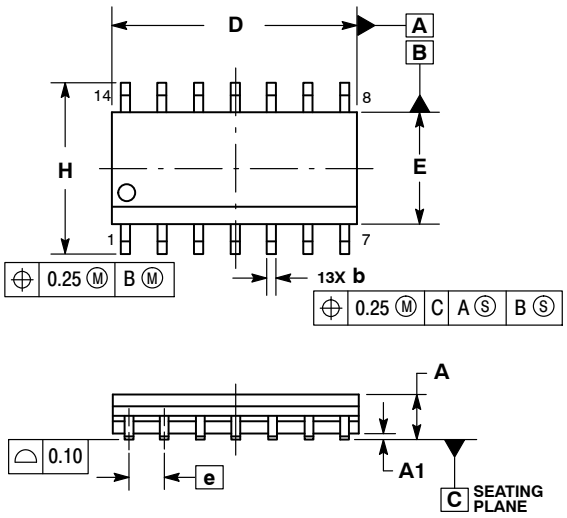
ON Semiconductor®

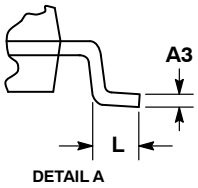


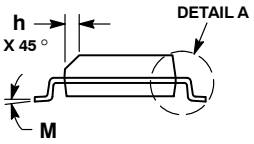
SCALE 1:1

SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



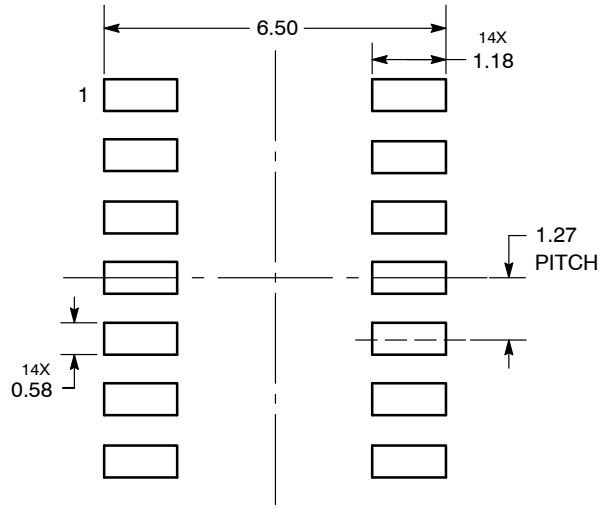




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

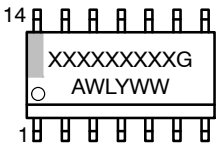
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42565B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	SOIC−14 NB		PAGE 1 OF 2

SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

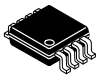
STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

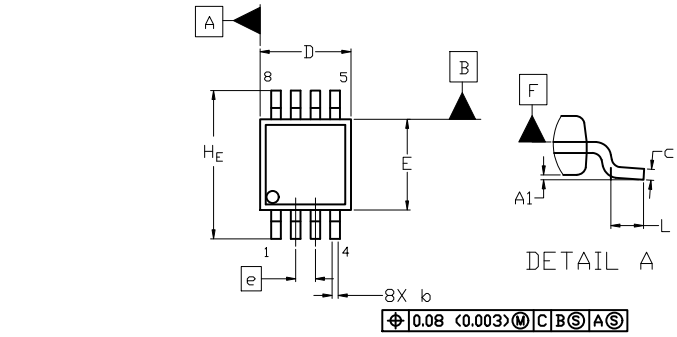
ON Semiconductor®

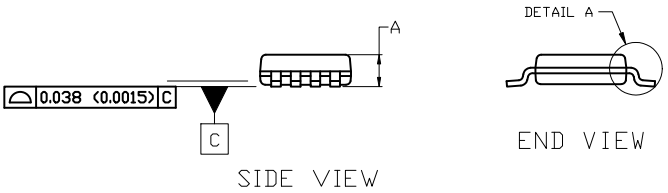


SCALE 2:1

Micro8
CASE 846A−02
ISSUE K

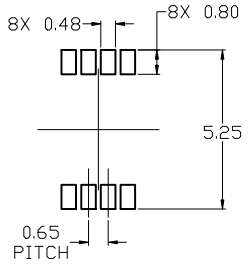
DATE 16 JUL 2020





NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

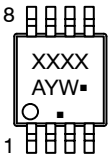


RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
b	0.25	0.33	0.40
c	0.13	0.18	0.23
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	0.65 BSC		
H_E	4.75	4.90	5.05
L	0.40	0.55	0.70

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:
PIN 1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

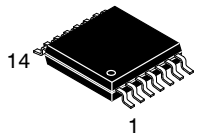
DOCUMENT NUMBER:	**98ASB14087C**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**MICRO8**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

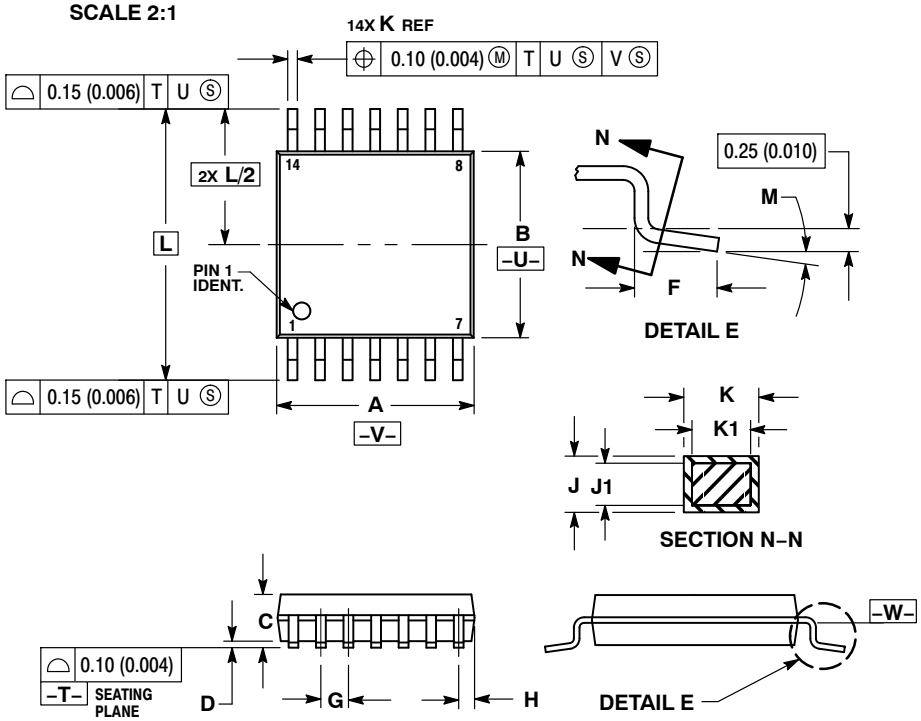
ON Semiconductor®

TSSOP−14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016



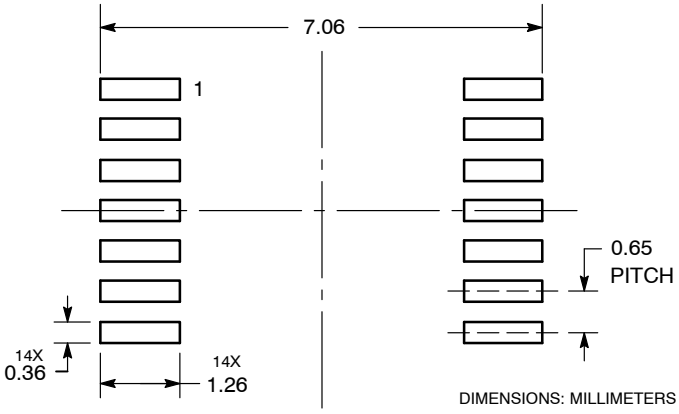
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

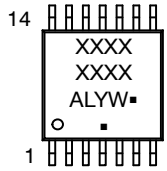
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

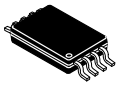
DOCUMENT NUMBER:	**98ASH70246A**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**TSSOP−14 WB**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

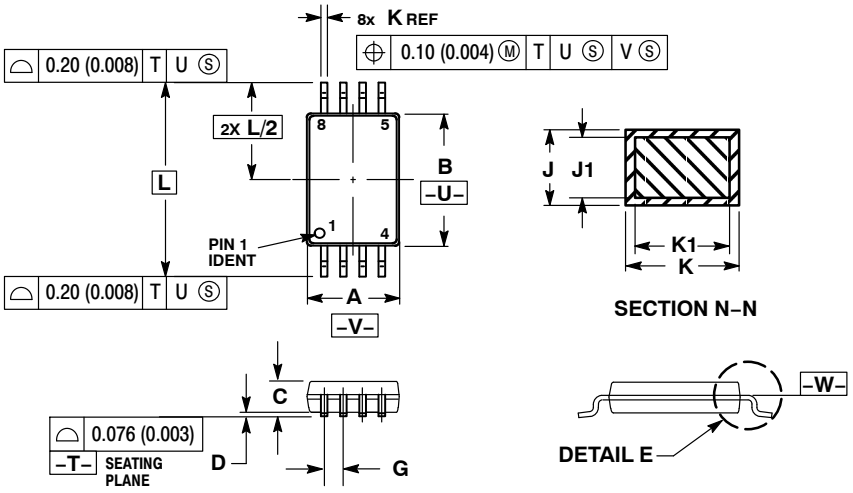
ON Semiconductor®

TSSOP−8
CASE 948S−01
ISSUE C

DATE 20 JUN 2008



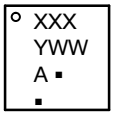
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	4.30	4.50	0.169	0.177
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.70	0.020	0.028
G	0.65 BSC		0.026 BSC	
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	98AON00697D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	TSSOP−8	PAGE 1 OF 2

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION.	18 APR 2000
A	ADDED MARKING DIAGRAM INFORMATION. REQ. BY V. BASS.	13 JAN 2006
B	CORRECTED MARKING DIAGRAM PIN 1 LOCATION AND MARKING. REQ. BY C. REBELLO.	13 MAR 2006
C	REMOVED EXPOSED PAD VIEW AND DIMENSIONS P AND P1. CORRECTED MARKING INFORMATION. REQ. BY C. REBELLO.	20 JUN 2008