NCV4254C

Low Dropout Voltage Tracking Regulator

The NCV4254C is a monolithic integrated low dropout tracking voltage regulator designed to provide an adjustable buffered output voltage that closely tracks the reference input voltage. The output delivers up to 70 mA while being able to be configured higher, lower or equal to the reference voltages.

The part can be used in automotive applications with remote sensors or any situation where it is necessary to isolate the output of the other regulator. The NCV4254C also enables the user to bestow a quick upgrade to their module when added current is needed and the existing regulator cannot provide.

Features

- Up to 70 mA Source Capability
- Low Output Tracking Tolerance
- Low Dropout (typ. 220 mV @ 70 mA)
- Low Disable Current in Stand−by Mode
- Wide Input Voltage Operating Range
- Protection Features:
  - Current Limitation
  - Thermal Shutdown
  - Reverse Input Voltage and Reverse Bias Voltage
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Grade 1 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

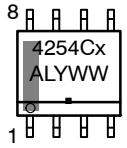
- Off the module loads (e.g. sensors power supply)

ON Semiconductor®

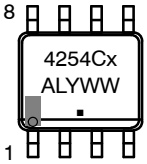
www.onsemi.com

MARKING DIAGRAMS

SOIC8
D SUFFIX
CASE 751



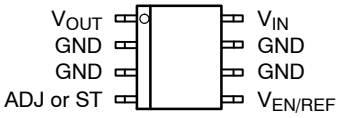
SOIC8 EP
PD SUFFIX
CASE 751AC



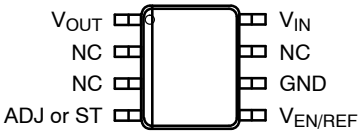
x	= A for Adjust version S for Status version
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
▪	= Pb−Free Device

(Note: Microdot may be in either location)

PIN CONNECTIONS



SOIC−8 (Top View)



SOIC−8 EP (Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

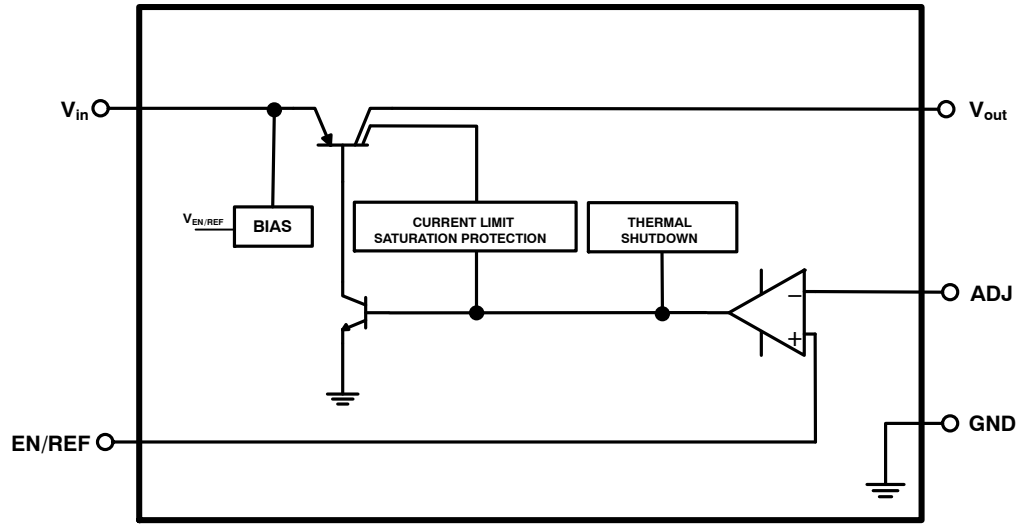


Figure 1. Block Diagram for Adjust Version NCV4254C

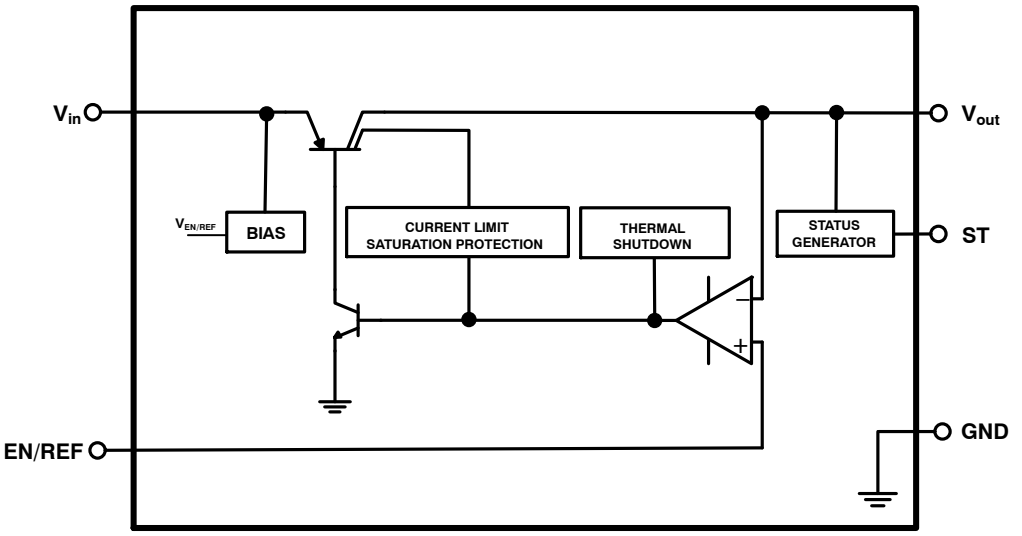


Figure 2. Block Diagram for Status Output for NCV4254C

Table 1. PIN FUNCTION DESCRIPTION

Pin No. SOIC−8	Pin No. SOIC−8 EP	Pin Name	Description
1	1	V_{out}	Tracker Output Voltage. Connect 2.2 μF capacitor with ESR < 5 Ω to ground be connected directly or by a voltage divider for lower output voltages.
2, 3, 6, 7	6	GND	Power Supply Ground.
–	2, 3, 7	NC	Not Connected. Connect to GND
4	4	ADJ	Voltage Adjust Input. The adjust input can be connected directly to output pin for V_{out} = $V_{EN/REF}$ or by a voltage divider for higher/lower output voltages. The adjust pin can be also connected to ground in case of using this device as a High−Side Driver.
4	4	ST	Tracking Regulator Status Output. Open collector output. Connect via a pull−up resistor to a positive voltage rail. A low signal indicates fault conditions at the regulator's output.
5	5	EN/REF	Enable / Reference. Connect the reference to this pin. A low signal disables the IC; a high signal switches it on. The reference voltage can be connected directly or by a voltage divider for lower output voltages.
8	8	V_{in}	Positive Power Supply Input. Connect 0.1 μF capacitor to ground.
–	PAD	PAD	Exposed Pad. Connect to GND

Table 2. MAXIMUM RATINGS

Rating		Symbol	Min	Max	Unit
Input Voltage DC (Note 1)	DC	V_{in}	−20	45	V
Peak Transient Voltage (Load Dump) (Note 2)		V_{in}		45	V
Output Voltage		V_{out}	−5	40	V
Enable / Reference Input Voltage	DC	$V_{EN/REF}$	−20	40	V
Adjust Voltage (Adjust Version)	DC	V_{ADJ}	−20	40	V
Status output Voltage (Status Output Version)	DC	V_{ST}	−0.3	7	V
Maximum Junction Temperature		$T_{J(max)}$	−40	150	°C
Storage Temperature		T_{STG}	−55	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. Load Dump Test B (with centralized load dump suppression) according to ISO16750−2 standard. Guaranteed by design. Not tested in production. Passed Class B according to ISO16750−1.

Table 3. ESD CAPABILITY (Note 3)

Rating	Symbol	Min	Max	Unit
ESD Capability, Human Body Model	ESD_{HBM}	−4	4	kV

3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (JS−001−2010)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Field Induced Charge Device Model ESD characterization is not performed on plastic molded packages with body sizes <50 mm^2 due to the inability of a small package body to acquire and retain enough charge to meet the minimum CDM discharge current waveform characteristic defined in JEDEC JS−002−2014

Table 4. LEAD SOLDERING TEMPERATURE AND MSL (Note 4)

Rating		Symbol	Min	Max	Unit
Moisture Sensitivity Level	SOIC−8 SOIC−8 EP	MSL	1 2		–

4. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

Table 5. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, SOIC−8 Thermal Resistance, Junction−to−Ambient (Note 5) Thermal Reference, Junction−to−Case Top (Note 5)	 $R_{\theta JA}$ $R_{\Psi JT}$	 115 11.5	°C/W
Thermal Characteristics, SOIC−8 EP Thermal Resistance, Junction−to−Ambient (Note 5) Thermal Reference, Junction−to−Case Top (Note 5)	 $R_{\theta JA}$ $R_{\Psi JT}$	 75 11.5	°C/W

5. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

Table 6. RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Input Voltage	V_{in}	4	45	V
Enable / Reference Input Voltage	$V_{EN/REF}$	2	–	V
Junction Temperature	T_J	−40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 7. ELECTRICAL CHARACTERISTICS V_{in} = 13.5 V, $V_{EN/REF}$ >= 2.5 V, C_{in} = 0.1 μF, C_{out} = 2.2 μF, for typical values T_J = 25°C, for min/max values T_J = −40°C to 150°C; unless otherwise noted. (Note 6)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
REGULATOR OUTPUT						
Output Voltage Tracking Accuracy	V_{in} = 5.7 V to 26 V, I_{out} = 0.1 mA to 60 mA 2.5 V ≤ $V_{EN/REF}$ ≤ (V_{IN} − 600 mV)	ΔV_{out}	−3	–	3	mV
Output Voltage Tracking Accuracy	V_{in} = 5.5 V to 26 V, I_{out} = 0.1 mA to 60 mA $V_{EN/REF}$ = 5 V	ΔV_{out}	−10	–	10	mV
Output Voltage Tracking Accuracy	V_{in} = 5.5 V to 32 V, I_{out} = 0.1 mA to 30 mA $V_{EN/REF}$ = 5 V	ΔV_{out}	−10	–	10	mV
Line Regulation	V_{in} = 5.5 V to 32 V, I_{out} = 5 mA, $V_{EN/REF}$ = 5 V	Reg_{line}	−5	–	5	mV
Load Regulation	I_{out} = 0.1 mA to 70 mA, $V_{EN/REF}$ = 5 V	Reg_{load}	−5	–	5	mV
Dropout Voltage (Note 7)	I_{out} = 70 mA, $V_{EN/REF}$ = 5 V	V_{DO}	–	220	400	mV
DISABLE AND QUIESCENT CURRENTS						
Disable Current, Stand−by Mode	$V_{EN/REF}$ ≤ 0.4 V, T_J ≤ 125°C	I_{DIS}	–	0.01	5	μA
Quiescent Current, I_q = I_{in} − I_{out}	I_{out} ≤ 0.1 mA, $V_{EN/REF}$ = 5 V I_{out} ≤ 70 mA, $V_{EN/REF}$ = 5 V	I_q	– –	65 1	80 2	μA mA
CURRENT LIMIT PROTECTION						
Current Limit	V_{out} = ($V_{EN/REF}$ − 0.1 V), $V_{EN/REF}$ = 5 V	I_{LIM}	71	110	150	mA
REVERSE CURRENT PROTECTION						
Reverse Current	V_{in} = 0 V, V_{out} = 32 V, $V_{EN/REF}$ = 5 V	I_{out_rev}	−15	−10	–	mA
Reverse Current at Negative Input Voltage	V_{in} = −16 V, V_{out} = 0 V, $V_{EN/REF}$ = 5 V	I_{in_rev}	−1	−0.2	–	mA
PSRR						
Power Supply Ripple Rejection (Note 8)	f = 100 Hz, 1 V_{p-p}	PSRR	–	60	–	dB
ENABLE / REFERENCE						
Enable / Reference Input Threshold Voltage Logic Low Logic High	 V_{out} = 0 V, I_{out} ≤ 5 μA, Tj ≤ 125°C $\|V_{out} - V_{EN/REF}\|$ < 10 mV	$V_{th(EN/REF)}$	 – 2	 – –	 0.4 –	V

6. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
7. Measured when output voltage falls 100 mV below the regulated voltage at Vin = 13.5 V.
8. Values based on design and/or characterization.

Table 7. ELECTRICAL CHARACTERISTICS V_{in} = 13.5 V, $V_{EN/REF}$ >= 2.5 V, C_{in} = 0.1 μF, C_{out} = 2.2 μF, for typical values T_J = 25°C, for min/max values T_J = −40°C to 150°C; unless otherwise noted. (Note 6)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
ENABLE / REFERENCE						
Enable / Reference Input Current	$V_{EN/REF}$ = 5 V	$I_{EN/REF}$	–	2	3	μA
Enable / Reference Input Current if Input tied to GND	V_{in} = 0 V, $V_{EN/REF}$ = 5 V	$I_{EN/REF}$	–	0.003	0.6	mA
Enable / Reference Internal Pull−Down Resistor		$R_{EN/REF}$	1.7	2.2	3.3	MΩ
ADJUST (only Adjust Version)						
Adjust Input Biasing Current	V_{ADJ} = 5 V	I_{ADJ}	–	0.03	0.5	μA
STATUS OUTPUT (only Status Version)						
Status Switching Threshold, Undervoltage	V_{out} decreasing	V_{out_UV}	$V_{EN/REF}$ −120	$V_{EN/REF}$ −77	$V_{EN/REF}$ −50	mV
Status Switching Threshold, Overvoltage	V_{out} increasing	V_{out_OV}	$V_{EN/REF}$ +50	$V_{EN/REF}$ +77	$V_{EN/REF}$ +120	mV
Status reaction Time		t_{ST}	10	23	33	μs
Status Output Low Voltage	I_{ST} = 1 mA, V_{in} ≥ 4 V	V_{ST_low}	–	–	0.4	V
Status Output Sink Current Limitation	V_{ST} = 0.8 V	I_{ST_max}	1	–	–	mA
Status Output Leakage Current	V_{out} = $V_{EN/REF}$, V_{ST} = 5 V	I_{ST_leak}	–	–	2	μA
THERMAL SHUTDOWN						
Thermal Shutdown Temperature (Note 8)		T_{SD}	151	175	200	°C

6. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
7. Measured when output voltage falls 100 mV below the regulated voltage at Vin = 13.5 V.
8. Values based on design and/or characterization.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

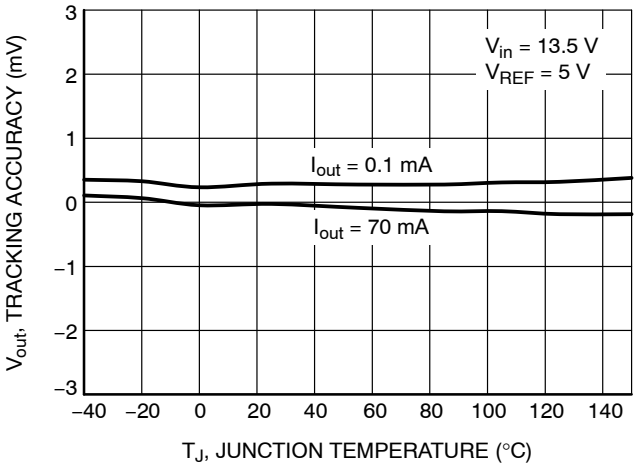


Figure 3. Tracking Accuracy ΔV_{out} vs. Junction Temperature T_j

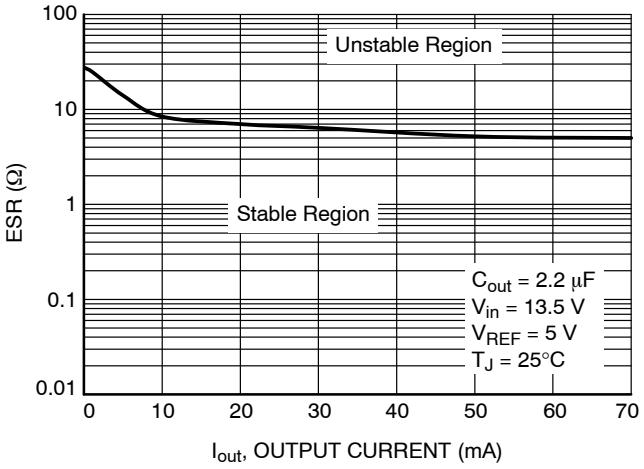


Figure 4. Output Capacitor Series Resistor ESR vs. Output Current I_{out}

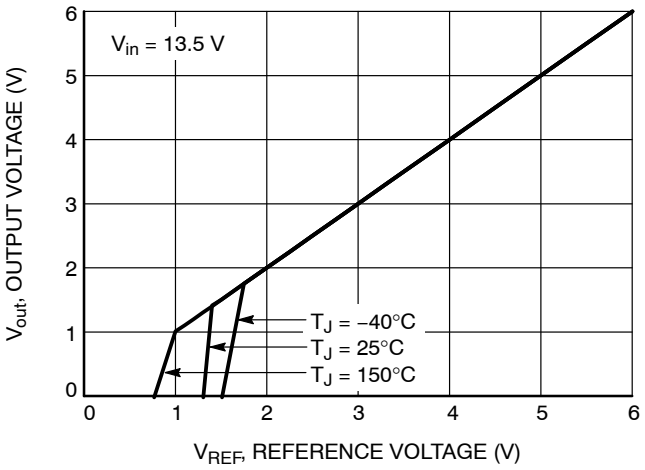


Figure 5. Output Voltage V_{out} vs. Reference Voltage $V_{EN/REF}$

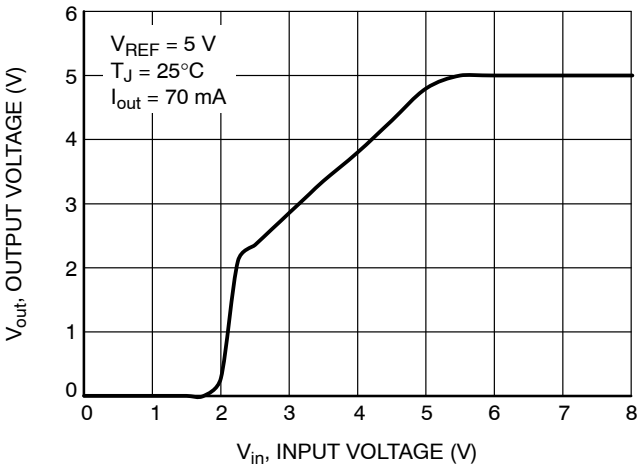


Figure 6. Output Voltage V_{out} vs. Input Voltage V_{in}

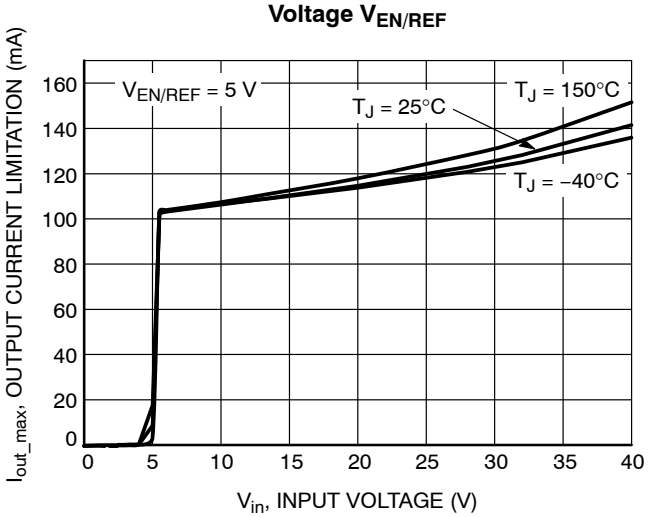


Figure 7. Output Current Limitation I_{out_max} vs. Input Voltage V_{in}, V_{REF} = 5 V

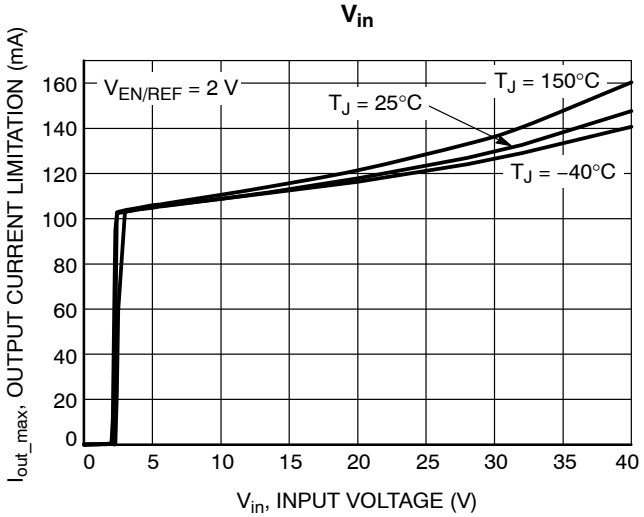


Figure 8. Output Current Limitation I_{out_max} vs. Input Voltage V_{in}, V_{REF} = 2 V

TYPICAL CHARACTERISTICS

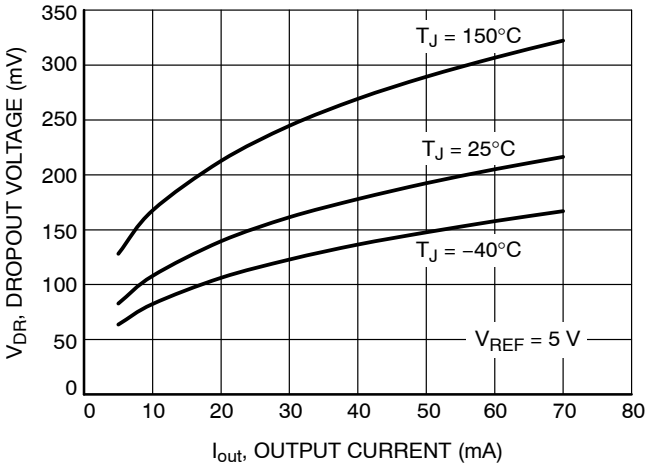


Figure 9. Dropout Voltage V_{DR} vs. Output Current I_{out}

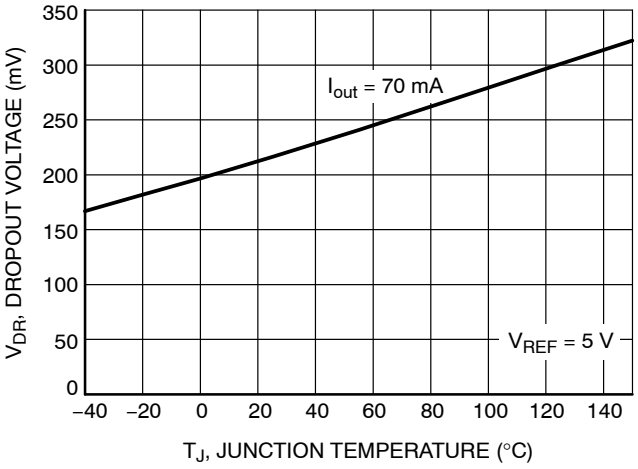


Figure 10. Dropout Voltage V_{DR} vs. Junction Temperature T_j

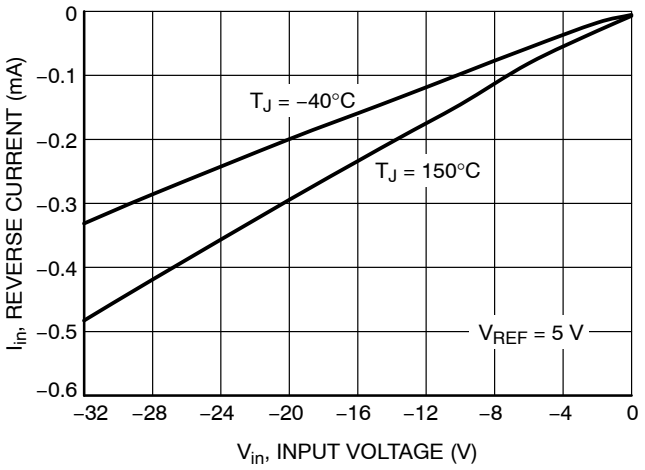


Figure 11. Reverse Current I_{in} vs. Input Voltage V_{in}

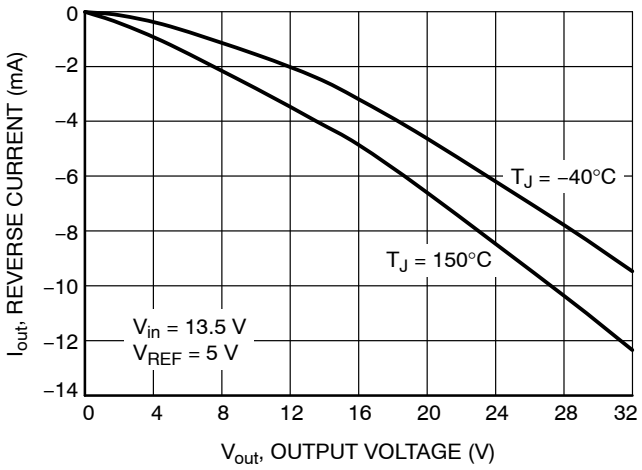


Figure 12. Reverse Current I_{in} vs. Output Voltage V_{out}

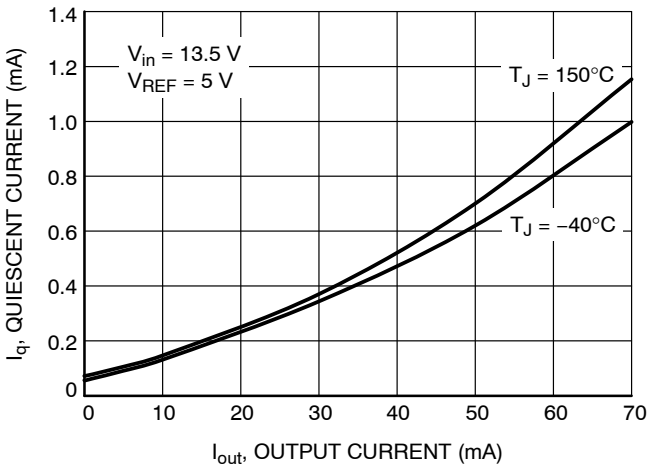


Figure 13. Quiescent Current I_q vs. Output Current I_{out}

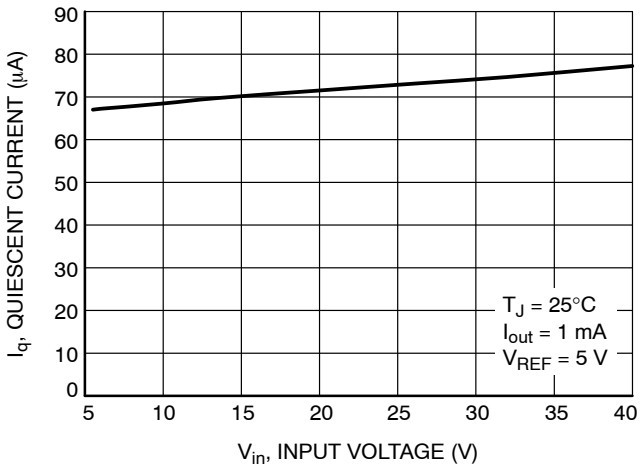


Figure 14. Quiescent Current I_q vs. Input Voltage V_{in}

TYPICAL CHARACTERISTICS

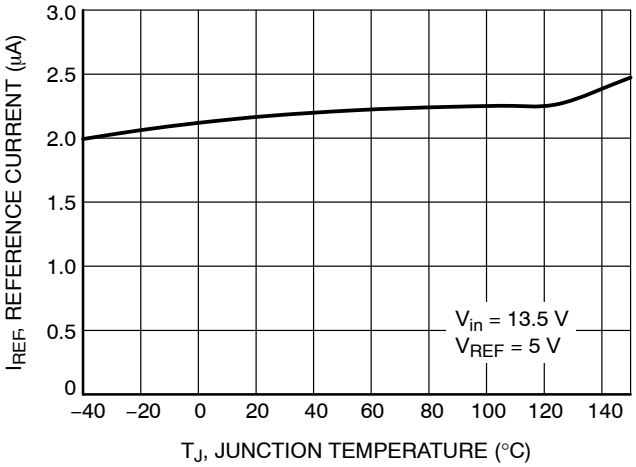


Figure 15. Enable / Reference Input Current $I_{EN/REF}$ vs. Junction Temperature T_j

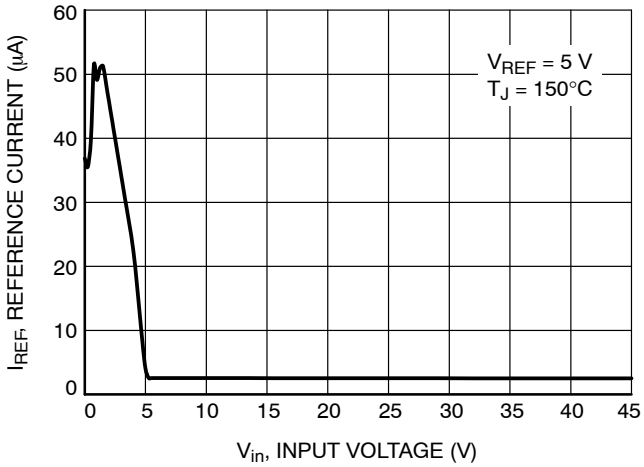


Figure 16. Enable / Reference Input Current $I_{EN/REF}$ vs. Input Voltage V_{in}

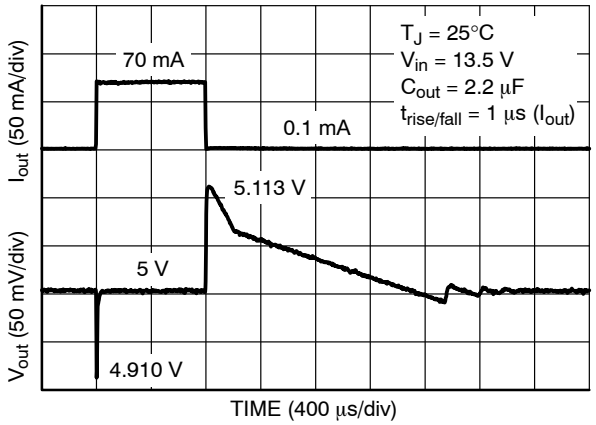


Figure 17. Load Transient

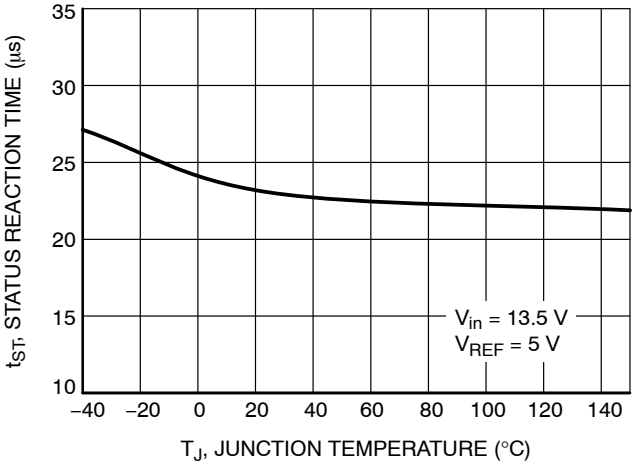


Figure 18. Status Reaction Time t_{ST} vs. Junction Temperature T_J

APPLICATION INFORMATION

The NCV4254C tracking regulator is self−protected with internal thermal shutdown and internal current limit. Typical characteristics are shown in Figure 3 to Figure 18.

Input Decoupling (C_{in})

A ceramic or tantalum 0.1 μF capacitor is recommended and should be connected close to the NCV4254C package. Higher capacitance and lower ESR will improve the overall line and load transient response.

If extremely fast input voltage transients are expected then appropriate input filter must be used in order to decrease rising and/or falling edges below 50 V/μs for proper operation. The filter can be composed of several capacitors in parallel.

Output Decoupling (C_{out})

The output capacitor for the NCV4254C is required for stability. Without it, the regulator output will oscillate. Actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) is also a factor in the IC stability. Worst−case is determined at the minimum ambient temperature and maximum load expected.

The output capacitor can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltage during brief conditions of negative input transients that might be characteristic of a particular system.

The capacitor must also be rated at all ambient temperatures expected in the system. To maintain regulator stability down to −40°C, a capacitor rated at that temperature must be used.

Tracking Regulator

The output voltage V_{out} is controlled by comparing it to the voltage applied at pin EN/REF and driving a PNP pass transistor accordingly. The control loop stability depends on the output capacitor C_{out}, the load current, the chip temperature and the poles/zeros introduced by the integrated circuit.

Protection circuitry prevents the IC as well as the application from destruction in case of catastrophic events. These safeguards contain output current limitation, reverse polarity protection as well as thermal shutdown in case of over temperature.

In order to avoid excessive power dissipation that could never be handled by the pass element and the package, the maximum output current is decreased at high input voltages.

The over temperature protection circuit prevents the IC from immediate destruction under fault conditions (e.g. Output continuously short−circuited) by reducing the output current. A thermal balance below 200°C junction temperature is established. Please note that a junction temperature above 150°C is outside the maximum ratings and reduces the IC lifetime.

The NCV4254C allows a negative supply voltage. However, several small currents are flowing into the IC. For details see electrical characteristics table and typical performance graphs. The thermal protection circuit is not operating during reverse polarity condition.

Thermal Considerations

As power in the NCV4254C increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCV4254C has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCV4254C can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \qquad \text{(eq. 1)}$$

Since T_J is not recommended to exceed 150°C, then the NCV4254C (SOIC−8 EP) soldered on 645 mm^2, 1 oz copper area, FR4 can dissipate up to 1.667 W when the ambient temperature (T_A) is 25°C. See Figure 19 and 20 for $R_{\theta JA}$ versus PCB Cu area. The power dissipated by the NCV4254C can be calculated from the following equations:

$$P_D \approx V_{in}\left(I_q @ I_{out}\right) + I_{out}\left(V_{in} - V_{out}\right) \qquad \text{(eq. 2)}$$

or

$$V_{in(MAX)} \approx \frac{P_{D(MAX)} + \left(V_{out} \times I_{out}\right)}{I_{out} + I_q} \qquad \text{(eq. 3)}$$

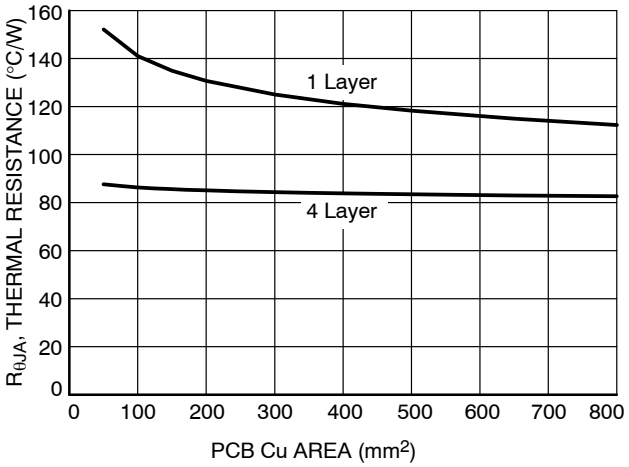


Figure 19. $R_{\theta JA}$ vs. PCB CU Area (SOIC−8 Package)

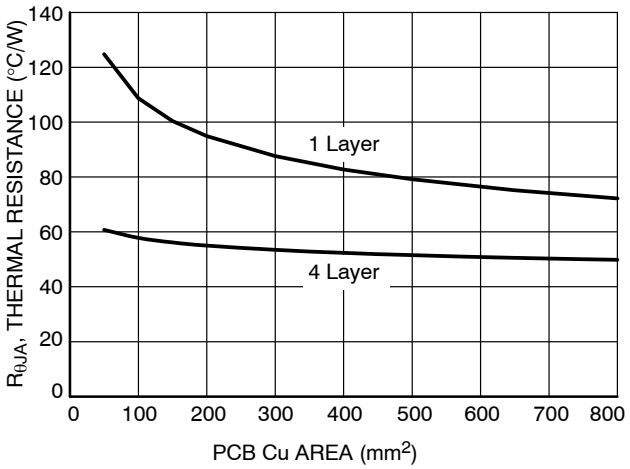


Figure 20. $R_{\theta JA}$ vs. PCB CU Area (SOIC−8 EP Package)

Hints

V_{in} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCV4254C and make traces as short as possible.

The NCV4254C is not developed in compliance with ISO26262 standard. If application is safety critical then the below application diagram shown in Figure 21 or 22 can be used.

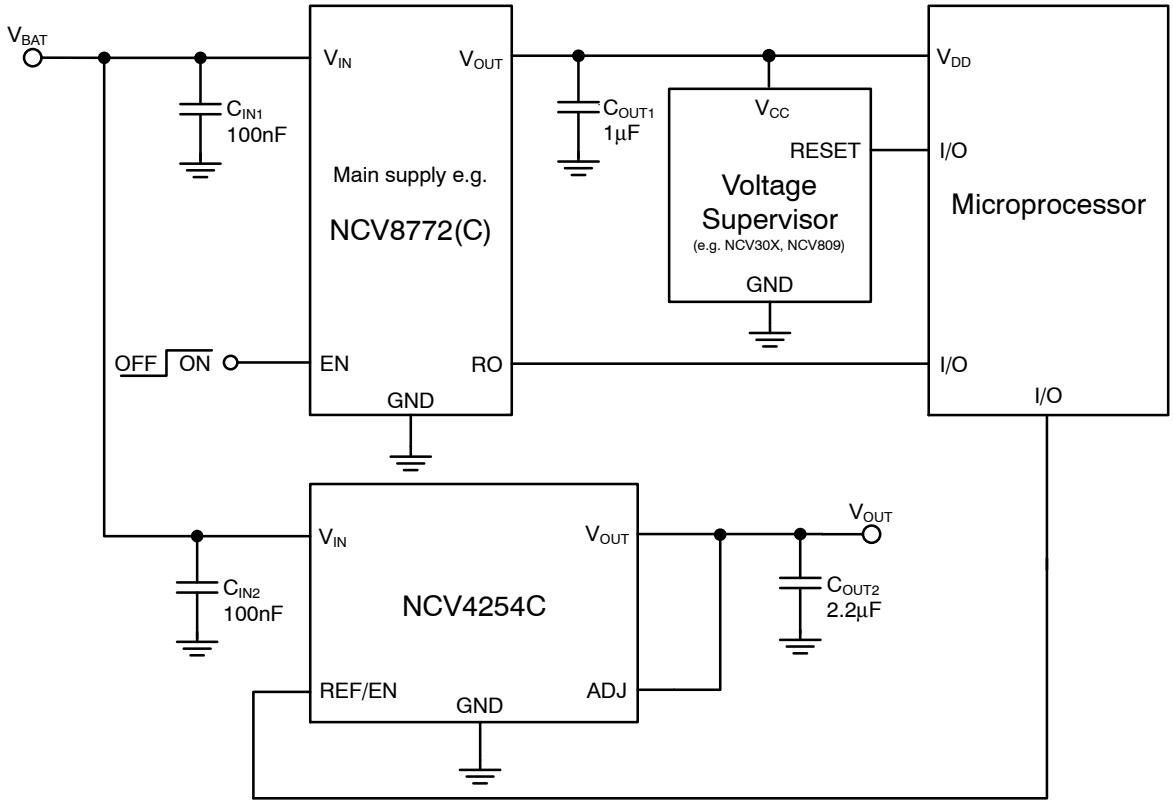


Figure 21. Application Diagram for ADJ version

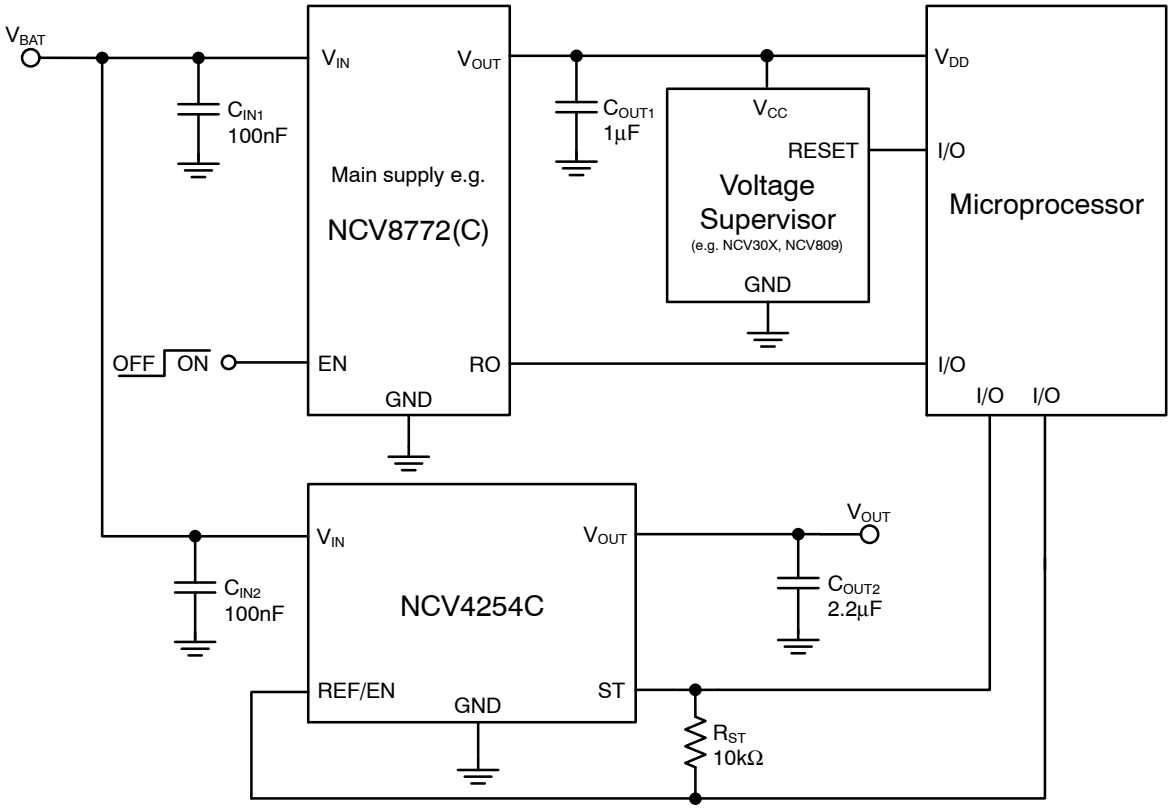


Figure 22. Application Diagram for ST version

CIRCUIT DESCRIPTION

ENABLE Function

By pulling the $V_{REF/EN}$ lead below 0.4 V typically, the IC is disabled and enters a Stand−by mode where the device draws less then 5 μA from supply. When the $V_{REF/EN}$ lead is greater then 1.75 V, V_{OUT} tracks the $V_{REF/EN}$ lead normally.

STATUS Output

The status output is used as the power on indicator to the microcontroller. This signal indicates when the output voltage is suitable for reliable operation of the sensor. It pulls low when the output is not considered to be ready. ST is pulled up to V_{REF} (Figure 23) or V_{out} (Figure 24) by an external resistor, typically 10 kΩ.

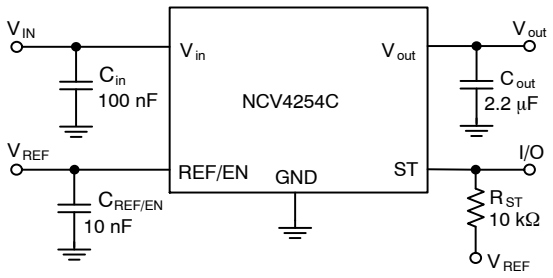


Figure 23. Status Version Application Circuit: Status to Reference Voltage

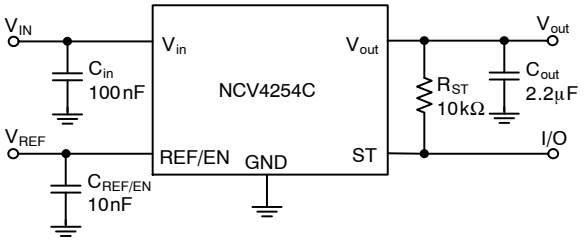


Figure 24. Status Version Application Circuit: Status to Output Voltage

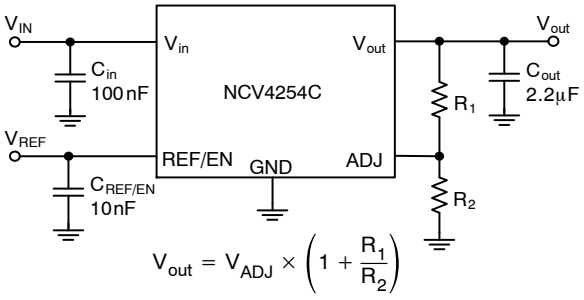


Figure 25. Adjust Version Application Circuit: Output Voltage Higher Than the Reference Voltage

Output Voltage

The output is capable of supplying 70 mA to the load while configured as a similar (Figure 26), lower (Figure 27) or higher (Figure 25) voltage as the reference lead. The Adj lead acts as the inverting terminal of the op amp and the V_{REF} lead as the non−inverting.

The device can also be configured as a high−side driver as displayed in Figure 28.

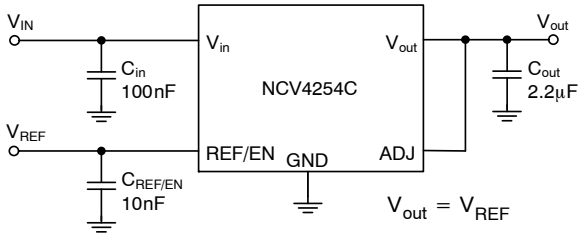


Figure 26. Adjust Version Application Circuit: Output Voltage Equal to the Reference Voltage

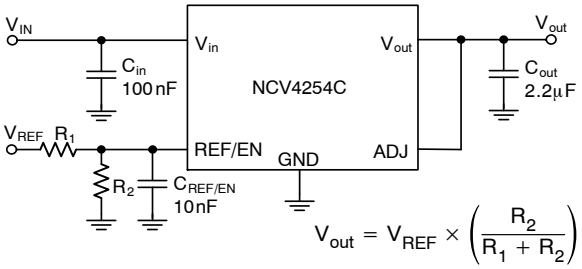


Figure 27. Adjust Version Application Circuit: Output Voltage Lower Than the Reference Voltage

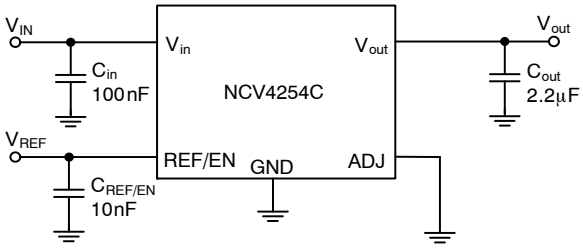


Figure 28. Adjust Version Application Circuit: High−Side Driver

ORDERING INFORMATION

Device	Version	Package	Shipping†
NCV4254CDAJR2G	ADJ	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCV4254CDSTR2G	ST		
NCV4254CPDAJR2G	ADJ	SOIC−8 EP (Pb−Free)	2500 / Tape & Reel
NCV4254CPDSTR2G	ST		

†For information on tape and reel specifications,including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

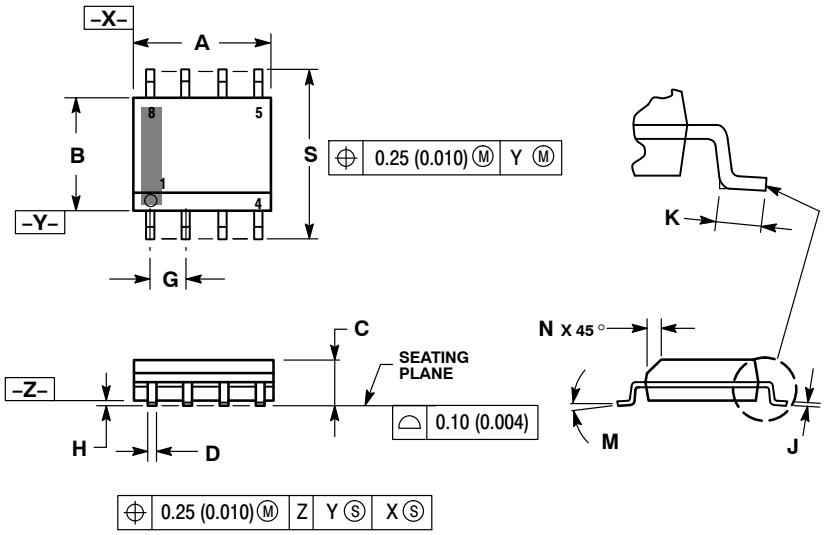
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

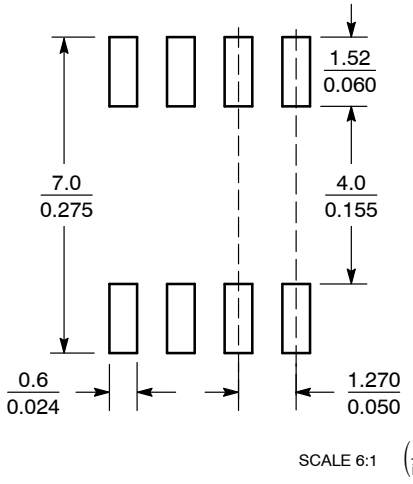
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

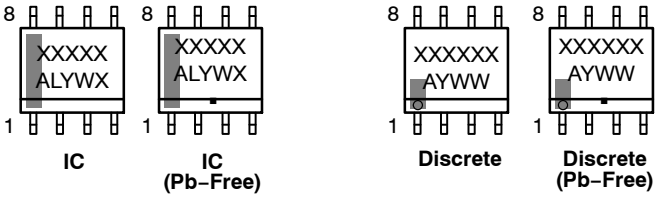
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 2 OF 2**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

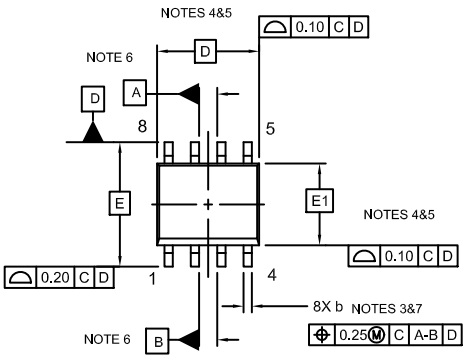
SCALE 1:1

SOIC−8 EP
CASE 751AC
ISSUE D

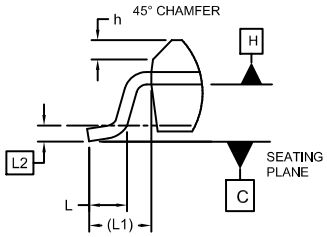
DATE 02 APR 2019

NOTES:

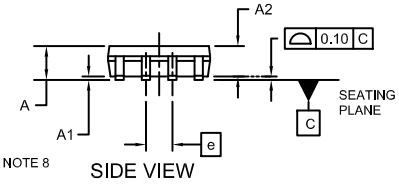
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



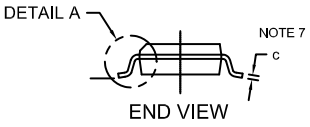
TOP VIEW



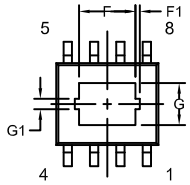
DETAIL A



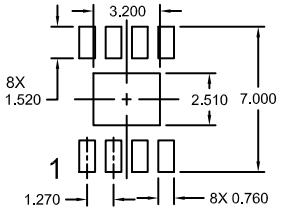
SIDE VIEW



END VIEW



BOTTOM VIEW

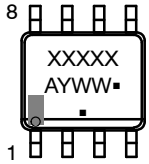


RECOMMENDED
MOUNTING FOOTPRINT*

DIM	MILLIMETERS		
	MIN.	NOM..	MAX.
A	1.35	1.55	1.75
A1	−−−	0.05	0.10
A2	1.35	1.50	1.65
b	0.31	0.41	0.51
c	0.17	0.21	0.23
D	4.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
F	2.24	2.72	3.20
F1	0.15	0.20	0.25
G	1.55	2.03	2.51
G1	0.41	0.46	0.51
h	0.25	0.38	0.50
L	0.40	0.84	1.27
L1	1.04 REF		
L2	0.25 REF		
Ø	0°	4°	8°

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D."

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present and may be in either location. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON14029D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC−8 EP	PAGE 1 OF 1