NCV4276B

400 mA Low-Drop Voltage Regulator

The NCV4276B is a 400 mA output current integrated low dropout regulator family designed for use in harsh automotive environments. It includes wide operating temperature and input voltage ranges. The device is offered with 3.3 V, 5.0 V, and adjustable voltage versions available in 2% output voltage accuracy. It has a high peak input voltage tolerance and reverse input voltage protection. It also provides overcurrent protection, overtemperature protection and inhibit for control of the state of the output voltage. The NCV4276B family is available in DPAK and D^{2}PAK surface mount packages. The output is stable over a wide output capacitance and ESR range. The NCV4276B has improved startup behavior during input voltage transients.

Features

- 3.3 V, 5.0 V, and Adjustable Voltage Version (from 2.5 V to 20 V) ±2% Output Voltage
- 400 mA Output Current
- 500 mV (max) Dropout Voltage (5.0 V Output)
- Inhibit Input
- Very Low Current Consumption
- Fault Protection
  - +45 V Peak Transient Voltage
  - −42 V Reverse Voltage
  - Short Circuit
  - Thermal Overload
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements
- These are Pb-Free Devices

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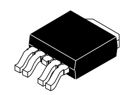
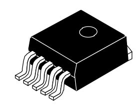
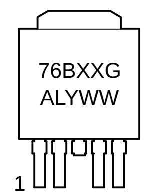


DPAK
CASE 175AA

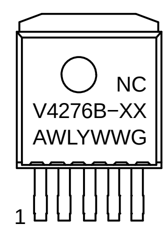


D^{2}PAK
CASE 936A

MARKING DIAGRAMS



DPAK
5-PIN



D^{2}PAK
5-PIN

*Tab is connected to Pin 3 on all packages.

A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb-Free Device
XX	= 33 (3.3 V)
	= 50 (5.0 V)
	= AJ (Adj. Voltage)

ORDERING INFORMATION

See detailed ordering and shipping information in the ordering information section on page 16 of this data sheet.

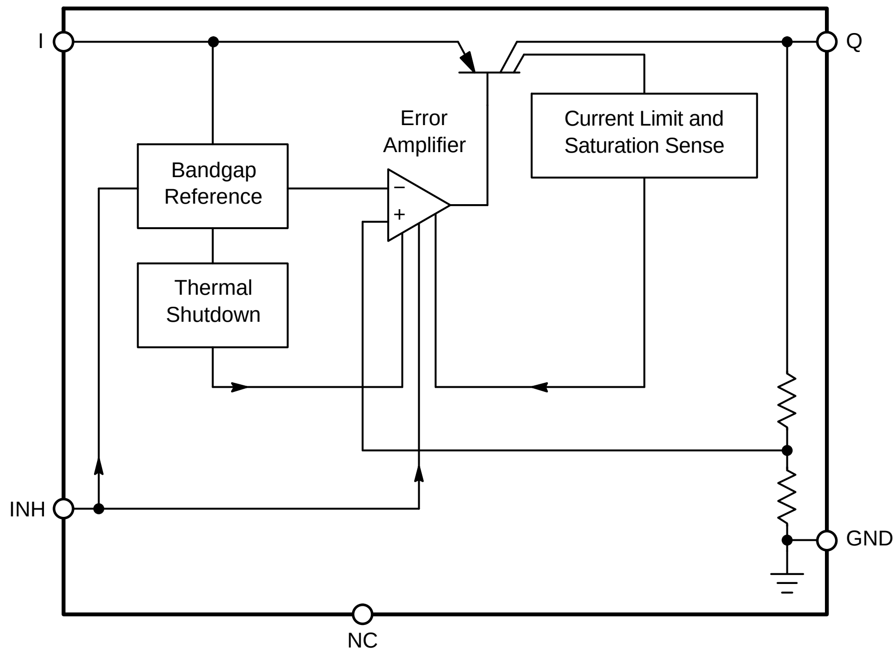


Figure 1. NCV4276B Block Diagram

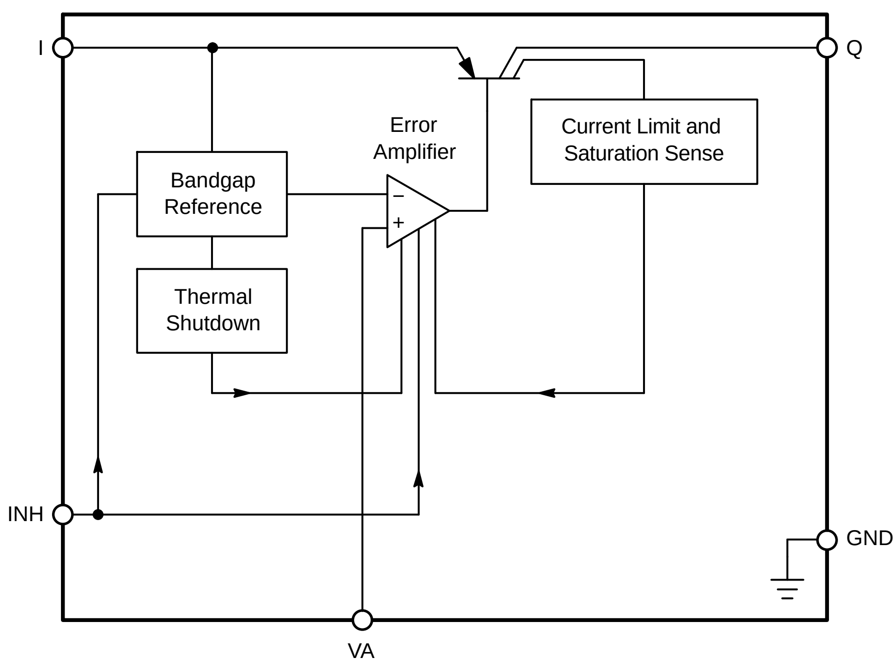


Figure 2. NCV4276B Adjustable Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Description
1	I	Input; Battery Supply Input Voltage.
2	INH	Inhibit; Set low-to inhibit.
3	GND	Ground; Pin 3 internally connected to heatsink.
4	NC/VA	Not connected for fixed voltage version/Voltage Adjust Input for adjustable voltage version; use an external voltage divider to set the output voltage
5	Q	Output: Bypass with a capacitor to GND. See Figures 3 to 7 and Regulator Stability Considerations section.

Table 2. MAXIMUM RATINGS*

Rating		Symbol	Min	Max	Unit
Input Voltage		V_I	−42	45	V
Input Peak Transient Voltage		V_I	−	45	V
Inhibit INH Voltage		V_{INH}	−42	45	V
Voltage Adjust Input VA		V_{VA}	−0.3	10	V
Output Voltage		V_Q	−1.0	40	V
Ground Current		I_q	−	100	mA
Input Voltage Operating Range		V_I	V_Q + 0.5 V or 4.5 V (Note 1)	40	V
ESD Susceptibility	(Human Body Model)	−	4.0	−	kV
	(Machine Model)	−	250	−	V
	(Charged Device Model)	−	1.25	−	kV
Junction Temperature		T_J	−40	150	°C
Storage Temperature		T_{stg}	−50	150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*During the voltage range which exceeds the maximum tested voltage of I, operation is assured, but not specified. Wider limits may apply. Thermal dissipation must be observed closely.

1. Minimum V_I = 4.5 V or (V_Q + 0.5 V), whichever is higher.

Table 3. LEAD TEMPERATURE SOLDERING REFLOW (Note 2)

Lead Temperature Soldering	T_{SLD}			°C
Reflow (SMD styles only), Leaded, 60−150 s above 183, 30 s max at peak		−	240	
Reflow (SMD styles only), Lead Free, 60−150 s above 217, 40 s max at peak		−	265	
Wave Solder (through hole styles only), 12 sec max		−	310	

2. Per IPC/JEDEC J−STD−020C.

Table 4. THERMAL CHARACTERISTICS (Notes 3 and 4)

Characteristic	Test Conditions (Typical Value)		Unit
DPAK 5-PIN PACKAGE			
	Min Pad Board (Note 5)	**1″ Pad Board** (Note 6)	
Junction-to-Tab (psi-JLx, ψ_{JLx})	4.2	4.7	C/W
Junction-to-Ambient ($R_{\theta JA}$, θ_{JA})	100.9	46.8	C/W
D²PAK 5-PIN PACKAGE			
	0.4 sq. in. Spreader Board (Note 7)	**1.2 sq. in. Spreader Board** (Note 8)	
Junction-to-Tab (psi-JLx, ψ_{JLx})	3.8	4.0	C/W
Junction-to-Ambient ($R_{\theta JA}$, θ_{JA})	74.8	41.6	C/W

3. Minimum V_I = 4.5 V or (V_Q + 0.5 V), whichever is higher.
4. Per IPC/JEDEC J−STD−020C.
5. 1 oz. copper, 0.26 inch^2 (168 mm^2) copper area, 0.062″ thick FR4.
6. 1 oz. copper, 1.14 inch^2 (736 mm^2) copper area, 0.062″ thick FR4.
7. 1 oz. copper, 0.373 inch^2 (241 mm^2) copper area, 0.062″ thick FR4.
8. 1 oz. copper, 1.222 inch^2 (788 mm^2) copper area, 0.062″ thick FR4.

Table 5. ELECTRICAL CHARACTERISTICS (V_I = 13.5 V; −40°C < T_J < 150°C; unless otherwise noted.)

Characteristic	Symbol	Test Conditions	NCV4276B Min	Typ	Max	Unit
OUTPUT						
Output Voltage, 5.0 V Version	V_Q	5.0 mA < I_Q < 400 mA, 6.0 V < V_I < 28 V	4.9	5.0	5.1	V
Output Voltage, 5.0 V Version	V_Q	5.0 mA < I_Q < 200 mA, 6.0 V < V_I < 40 V	4.9	5.0	5.1	V
Output Voltage, 3.3 V Version	V_Q	5.0 mA < I_Q < 400 mA, 4.5 V < V_I < 28 V	3.234	3.3	3.366	V
Output Voltage, 3.3 V Version	V_Q	5.0 mA < I_Q < 200 mA, 4.5 V < V_I < 40 V	3.234	3.3	3.366	V
Output Voltage, Adjustable Version	AV_Q	5.0 mA < I_Q < 400 mA V_Q+1 < V_I < 40 V V_I > 4.5 V	−2%	−	+2%	V
Output Current Limitation	I_Q	V_Q = 90% V_{QTYP} (V_{QTYP} = 2.5 V for ADJ Version)	400	700	1100	mA
Quiescent Current (Sleep Mode) $I_q = I_I - I_Q$	I_q	V_{INH} = 0 V	−	−	10	μA
Quiescent Current, $I_q = I_I - I_Q$	I_q	I_Q = 1.0 mA	−	130	200	μA
Quiescent Current, $I_q = I_I - I_Q$	I_q	I_Q = 250 mA	−	10	15	mA
Quiescent Current, $I_q = I_I - I_Q$	I_q	I_Q = 400 mA	−	25	35	mA
Dropout Voltage, Adjustable Version	V_{DR}	I_Q = 250 mA, $V_{DR} = V_I - V_Q$ V_I > 4.5 V	−	250	500	mV
Dropout Voltage (5.0 V Version)	V_{DR}	I_Q = 250 mA (Note 9)	−	250	500	mV
Load Regulation	$\Delta V_{Q,LO}$	I_Q = 5.0 mA to 400 mA	−	3.0	20	mV
Line Regulation	ΔV_Q	ΔV_I = 12 V to 32 V, I_Q = 5.0 mA	−	4.0	15	mV
Power Supply Ripple Rejection	PSRR	f_r = 100 Hz, V_r = 0.5 V_{PP}	−	70	−	dB
Temperature Output Voltage Drift	$d_{VQ/dT}$	−	−	0.5	−	mV/K
INHIBIT						
Inhibit Voltage, Output High	V_{INH}	$V_Q \geq V_{QMIN}$	−	2.3	2.8	V
Inhibit Voltage, Output Low (Off)	V_{INH}	$V_Q \leq$ 0.1 V	1.8	2.2	−	V
Input Current	I_{INH}	V_{INH} = 5.0 V	5.0	10	20	μA
THERMAL SHUTDOWN						
Thermal Shutdown Temperature*	T_{SD}	I_Q = 5.0 mA	150	−	210	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

*Guaranteed by design, not tested in production.

9. Measured when the output voltage V_Q has dropped 100 mV from the nominal valued obtained at V = 13.5 V.

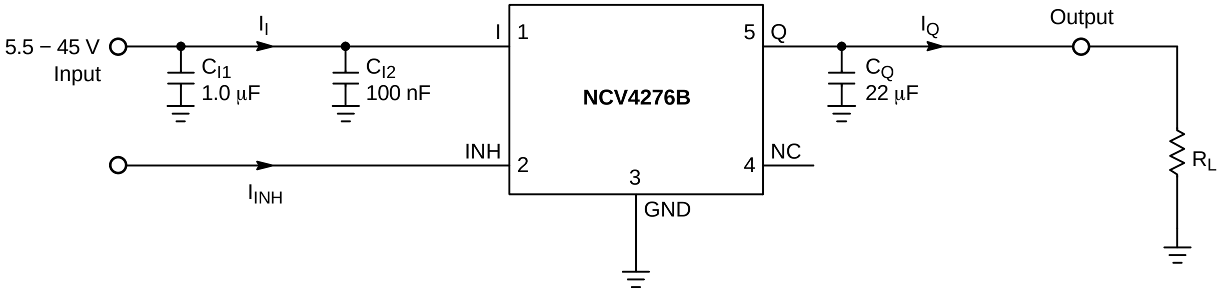
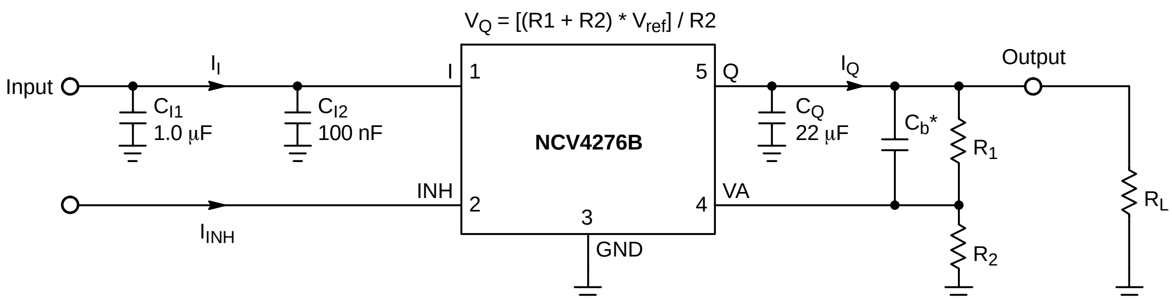


Figure 3. Applications Circuit; Fixed Voltage Version



C_b* − Required if usage of low ESR output capacitor C_Q is demand, see Regulator Stability Considerations section

Figure 4. Applications Circuit; Adjustable Voltage Version

TYPICAL PERFORMANCE CHARACTERISTICS

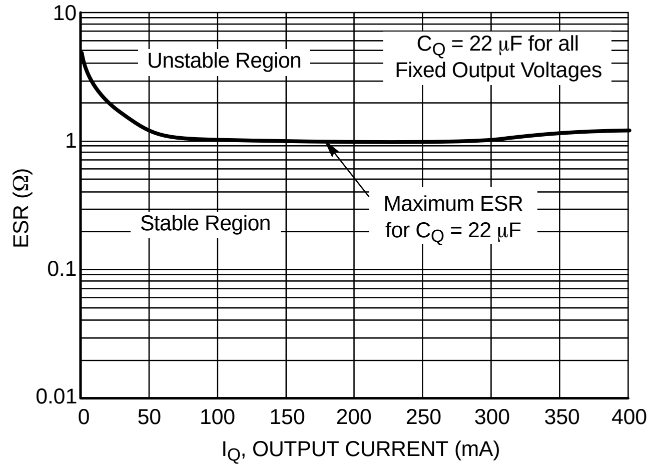


Figure 5. Output Stability with Output Capacitor ESR, 5.0 V and 3.3 V Regulator

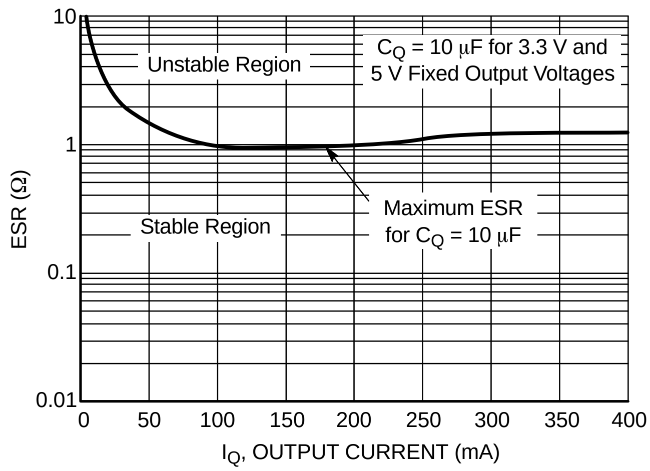


Figure 6. Output Stability with Output Capacitor ESR, 5.0 V and 3.3 V Regulator

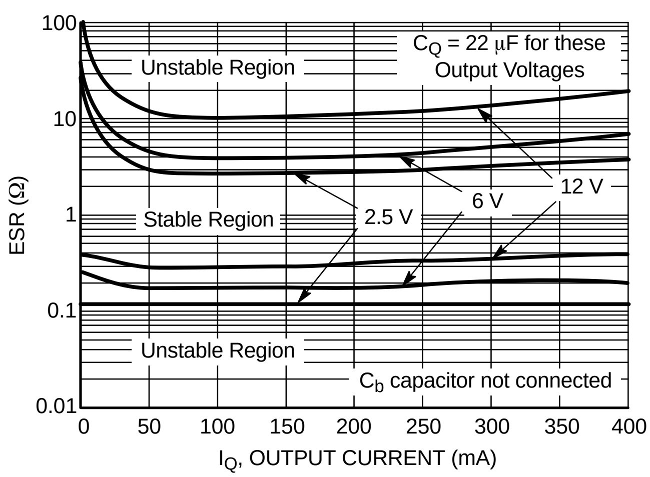


Figure 7. Output Stability with Output Capacitor ESR, Adjustable Regulator

TYPICAL PERFORMANCE CHARACTERISTICS − 4276B Version

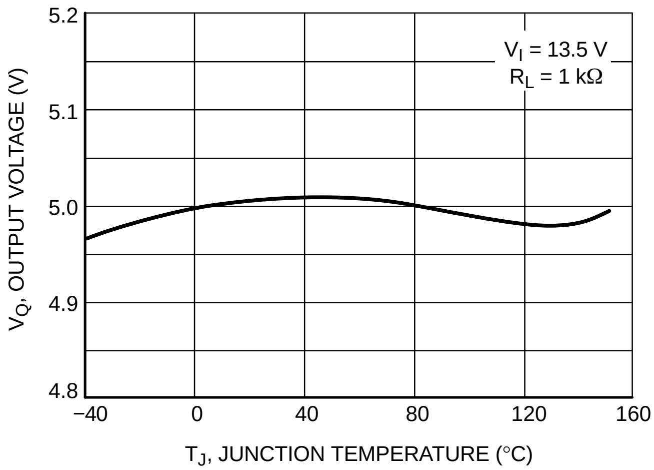


Figure 8. Output Voltage vs. Junction Temperature, 5.0 V Version

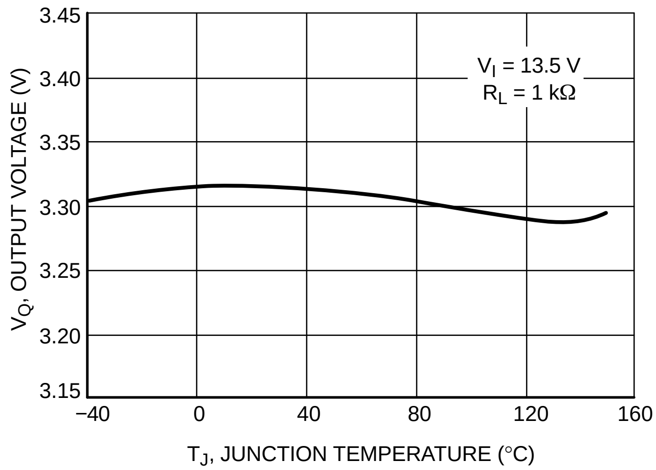


Figure 9. Output Voltage vs. Junction Temperature, 3.3 V Version

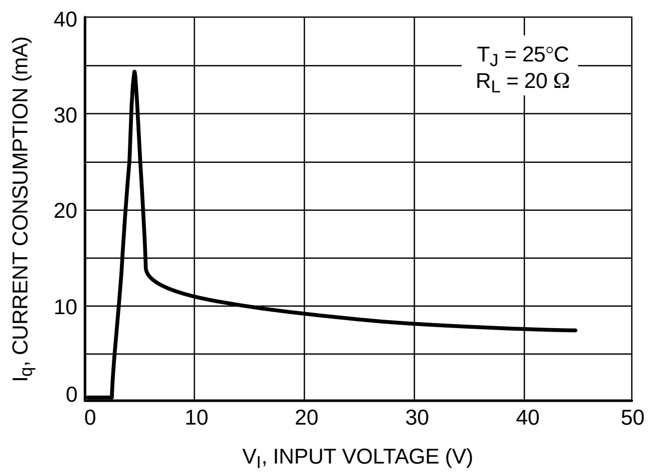


Figure 10. Current Consumption vs. Input Voltage, 5.0 V Version

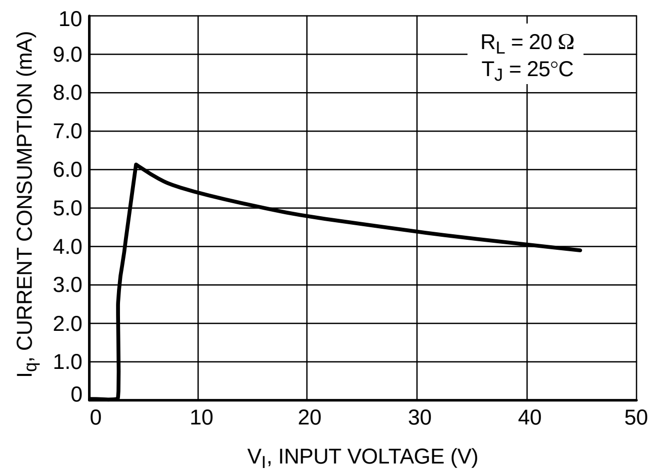


Figure 11. Current Consumption vs. Input Voltage, 3.3 V Version

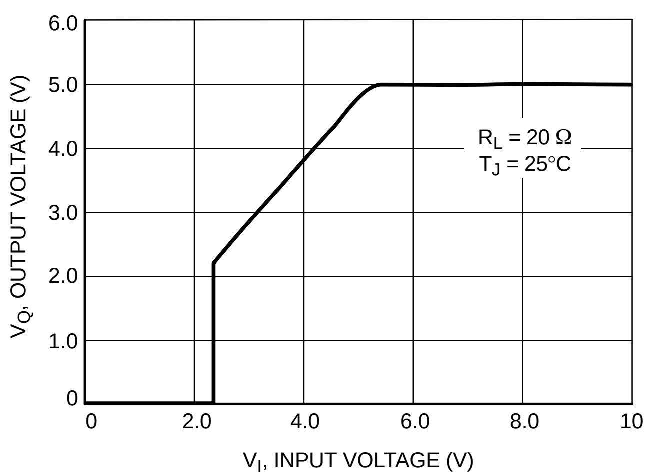


Figure 12. Low Voltage Behavior, 5.0 V Version

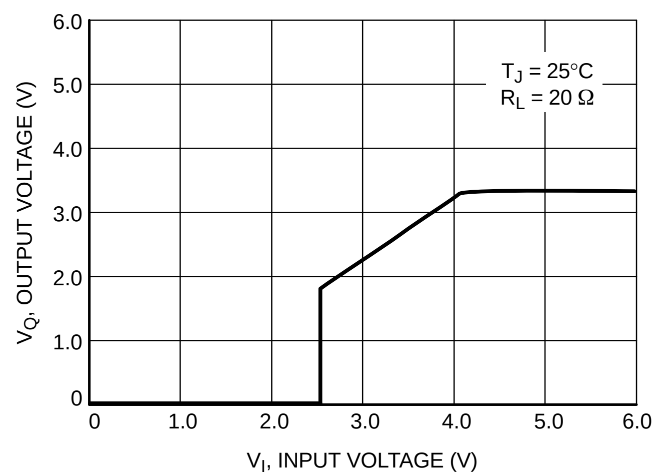


Figure 13. Low Voltage Behavior, 3.3 V Version

TYPICAL PERFORMANCE CHARACTERISTICS − 4276B Version

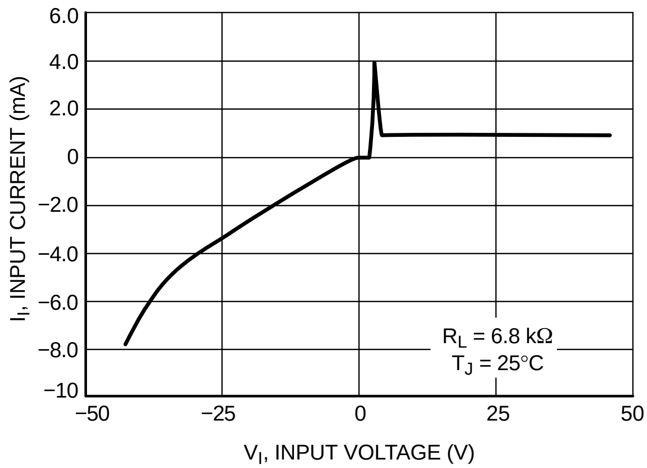


Figure 14. Input Current vs. Input Voltage, 5.0 V Version

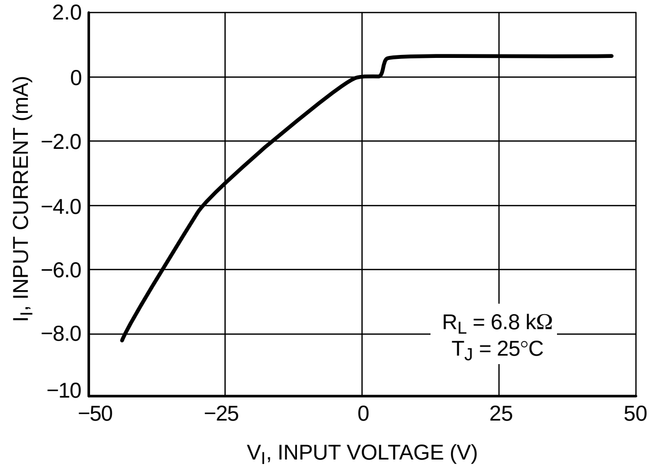


Figure 15. Input Current vs. Input Voltage, 3.3 V Version

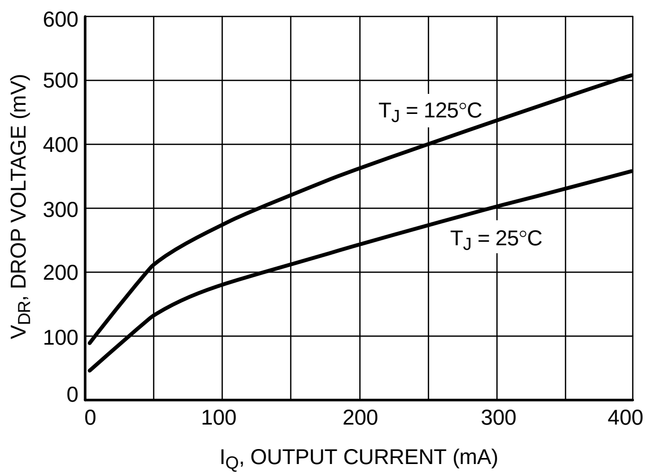


Figure 16. Dropout Voltage vs. Output Current

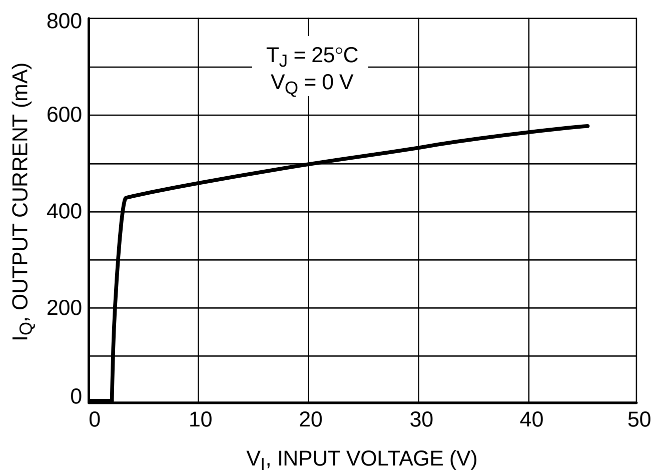


Figure 17. Maximum Output Current vs. Input Voltage

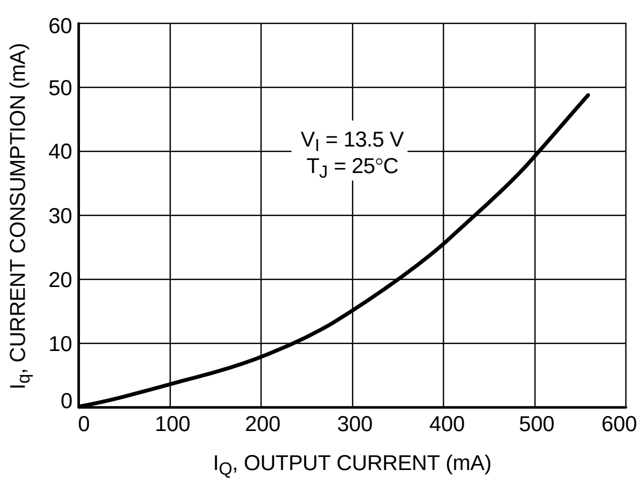


Figure 18. Current Consumption vs. Output Current (High Load)

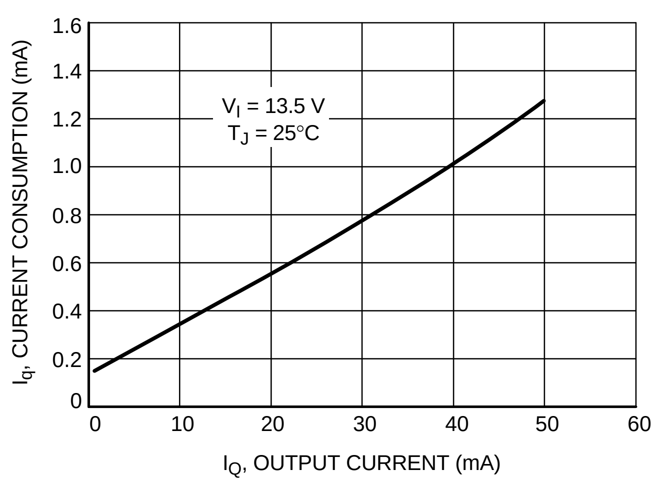


Figure 19. Current Consumption vs. Output Current (Low Load)

TYPICAL PERFORMANCE CHARACTERISTICS − Adjustable Version

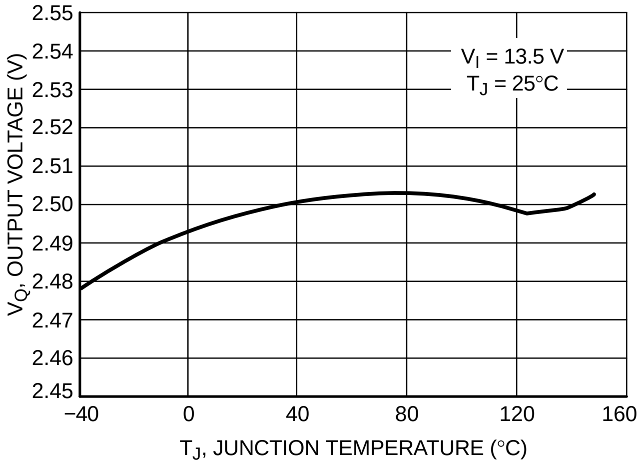


Figure 20. Output Voltage vs. Junction Temperature, Adjustable Version

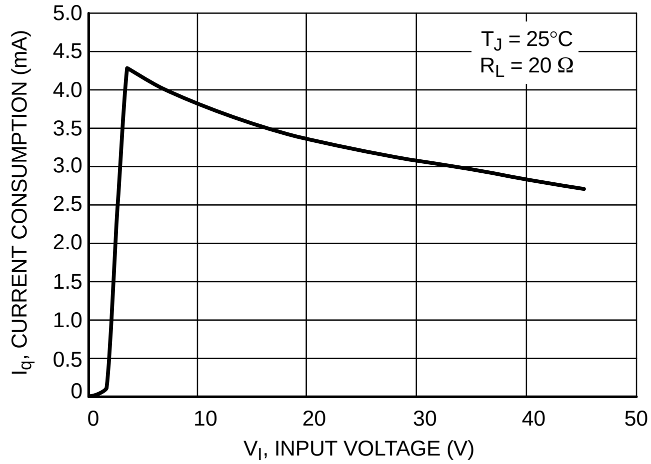


Figure 21. Current Consumption vs. Input Voltage, Adjustable Version

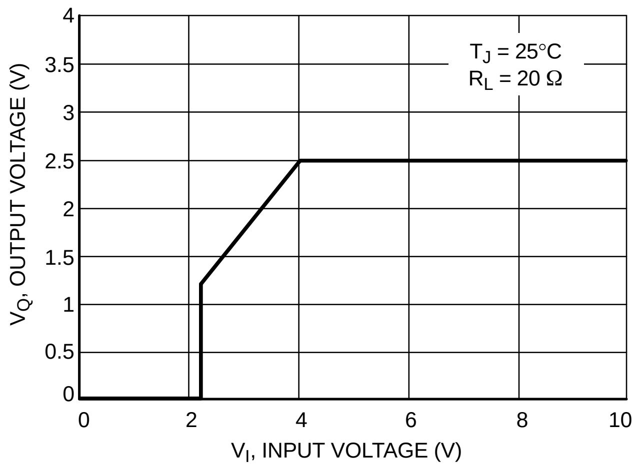


Figure 22. Low Voltage Behavior, Adjustable Version

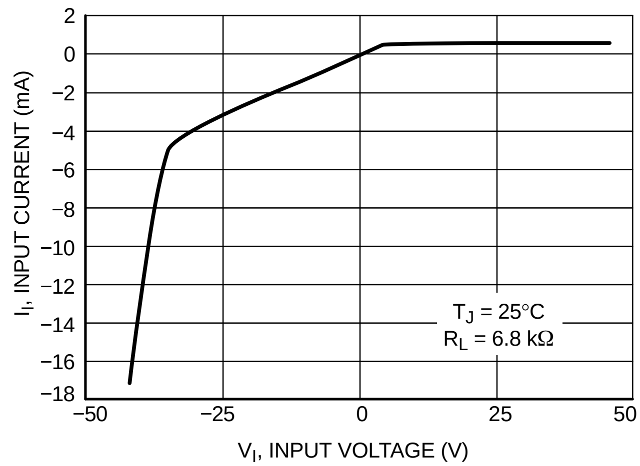


Figure 23. High Voltage Behavior, Adjustable Version

TYPICAL PERFORMANCE CHARACTERISTICS − Adjustable Version

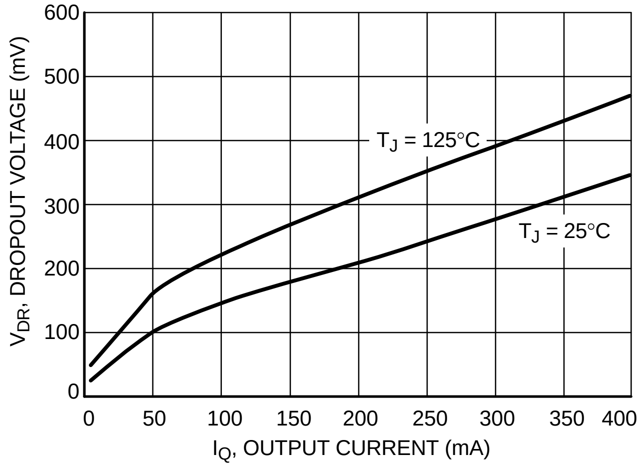


Figure 24. Dropout Voltage vs. Output Current, Regulator Set at 5.0 V, Adjustable Version

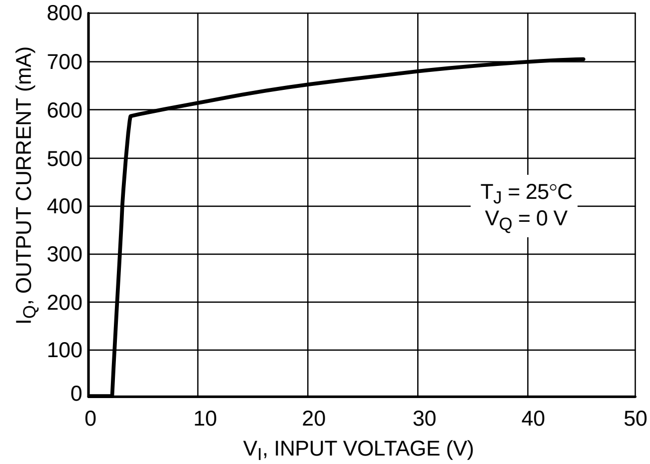


Figure 25. Maximum Output Current vs. Input Voltage, Adjustable Version

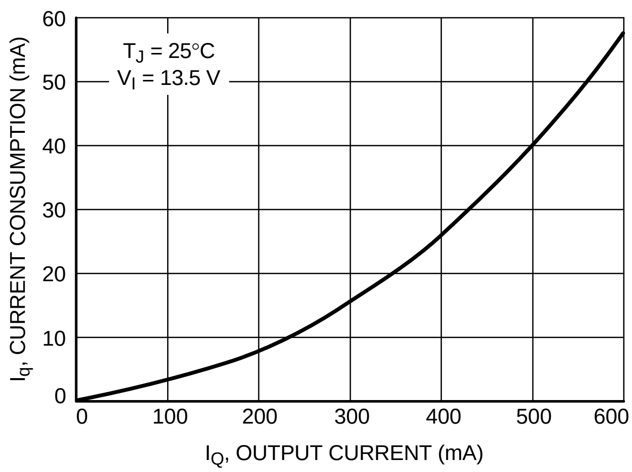


Figure 26. Current Consumption vs. Output Current (High Load), Adjustable Version

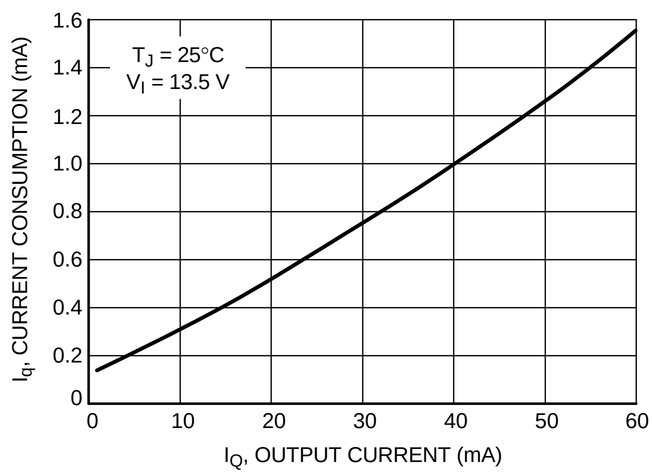


Figure 27. Current Consumption vs. Output Current (Low Load), Adjustable Version

Circuit Description

The NCV4276B is an integrated low dropout regulator that provides a regulated voltage at 400 mA to the output. It is enabled with an input to the inhibit pin. The regulator voltage is provided by a PNP pass transistor controlled by an error amplifier with a bandgap reference, which gives it the lowest possible dropout voltage. The output current capability is 400 mA, and the base drive quiescent current is controlled to prevent oversaturation when the input voltage is low or when the output is overloaded. The regulator is protected by both current limit and thermal shutdown. Thermal shutdown occurs above 150°C to protect the IC during overloads and extreme ambient temperatures.

Regulator

The error amplifier compares the reference voltage to a sample of the output voltage (V_Q) and drives the base of a PNP series pass transistor via a buffer. The reference is a bandgap design to give it a temperature-stable output. Saturation control of the PNP is a function of the load current and input voltage. Oversaturation of the output power device is prevented, and quiescent current in the ground pin is minimized. See Figure 4, Test Circuit, for circuit element nomenclature illustration.

Regulator Stability Considerations

The input capacitors (C_{I1} and C_{I2}) are necessary to stabilize the input impedance to avoid voltage line influences. Using a resistor of approximately 1.0 Ω in series with C_{I2} can stop potential oscillations caused by stray inductance and capacitance.

The output capacitor helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability. The capacitor value and type should be based on cost, availability, size and temperature constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer’s data sheet usually provides this information.

The value for the output capacitor C_Q, shown in Figure 3, should work for most applications; see also Figures 5 to 7 for output stability at various load and Output Capacitor ESR conditions. Stable region of ESR in Figures 5 to 7 shows ESR values at which the LDO output voltage does not have any permanent oscillations at any dynamic changes of output load current. Marginal ESR is the value at which the output voltage waving is fully damped during four periods after the load change and no oscillation is further observable.

ESR characteristics were measured with ceramic capacitors and additional series resistors to emulate ESR. Low duty cycle pulse load current technique has been used to maintain junction temperature close to ambient temperature.

Minimum ESR for C_Q = 22 μF is native ESR of ceramic capacitor with which the fixed output voltage devices are performing stable. Murata ceramic capacitors were used,

GRM32ER71C226KE18 (22 μF, 16 V, X7R, 1210),

GRM31CR71C106KAC7 (10 μF, 16 V, X7R, 1206).

Calculating Bypass Capacitor

If usage of low ESR ceramic capacitors is demand in case of Adjustable Regulator, connect the bypass capacitor C_b between Voltage Adjust pin and Q pin according to Applications circuit at Figure 4.

Parallel combination of bypass capacitor C_b with the feedback resistor R_1 contributes in the device transfer function as an additional zero and affects the device loop stability, therefore its value must be optimized. Attention to the Output Capacitor value and its ESR must be paid. See also Stability in High Speed Linear LDO Regulators Application Note, AND8037/D for more information.

Optimal value of bypass capacitor is given by following expression

$$C_b = \frac{1}{2 \times \pi \times f_z \times R_1} \cdot (F) \qquad \text{(eq. 1)}$$

where

R_1 = the upper feedback resistor

f_z = the frequency of the zero added into the device transfer function by R_1 and C_b external components.

Set the R_1 resistor according to output voltage requirement. Chose the f_z with regard on the output capacitance C_Q, refer to the table below.

C_Q (μF)	10	22	47	100
f_z Range (kHz)	20 - 50	14 - 35	10 - 20	7 – 14

Ceramic capacitors and its part numbers listed bellow have been used as low ESR output capacitors C_Q from the table above to define the frequency ranges of additional zero required for stability.

GRM31CR71C106KAC7 (10 μF, 16 V, X7R, 1206)

GRM32ER71C226KE18 (22 μF, 16 V, X7R, 1210)

GRM32ER61C476ME15 (47 μF, 16 V, X5R, 1210)

GRM32ER60J107ME20 (100 μF, 6.3 V, X5R, 1210)

Inhibit Input

The inhibit pin is used to turn the regulator on or off. By holding the pin down to a voltage less than 1.8 V, the output of the regulator will be turned off. When the voltage on the Inhibit pin is greater than 2.8 V, the output of the regulator will be enabled to power its output to the regulated output voltage. The inhibit pin may be connected directly to the input pin to give constant enable to the output regulator.

Setting the Output Voltage (Adjustable Version)

The output voltage range of the adjustable version can be set between 2.5 V and 20 V. This is accomplished with an external resistor divider feeding back the voltage to the IC back to the error amplifier by the voltage adjust pin VA. The internal reference voltage is set to a temperature stable reference of 2.5 V.

The output voltage is calculated from the following formula. Ignoring the bias current into the VA pin:

$$V_Q = [(R1 + R2) * V_{ref}] / R2 \qquad \text{(eq. 2)}$$

Use R2 < 50 k to avoid significant voltage output errors due to VA bias current.

Connecting VA directly to Q without R1 and R2 creates an output voltage of 2.5 V.

Designers should consider the tolerance of R1 and R2 during the design phase.

The input voltage range for operation (pin 1) of the adjustable version is between (V_Q + 0.5 V) and 40 V. Internal bias requirements dictate a minimum input voltage of 4.5 V. The dropout voltage for output voltages less than 4.0 V is (4.5 V − V_Q).

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 28) is:

$$P_{D(max)} = [V_{I(max)} - V_{Q(min)}] I_{Q(max)} + V_{I(max)} I_q \qquad \text{(eq. 3)}$$

where:

- $V_{I(max)}$ is the maximum input voltage,
- $V_{Q(min)}$ is the minimum output voltage,
- $I_{Q(max)}$ is the maximum output current for the application,
- I_q is the quiescent current the regulator consumes at $I_{Q(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = \frac{150^{o}C - T_A}{P_D} \qquad \text{(eq. 4)}$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$ less than the calculated value in Equation 4 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

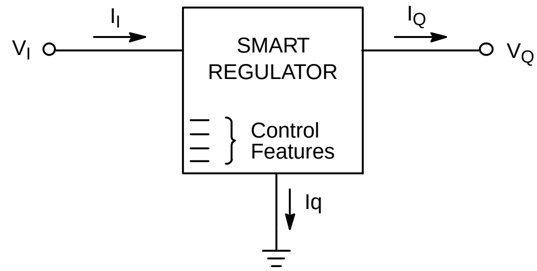


Figure 28. Single Output Regulator with Key Performance Parameters Labeled

Heatsinks

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \qquad \text{(eq. 5)}$$

where:

- $R_{\theta JC}$ is the junction-to-case thermal resistance,
- $R_{\theta CS}$ is the case-to-heatsink thermal resistance,
- $R_{\theta SA}$ is the heatsink-to-ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in data sheets of heatsink manufacturers.

Thermal, mounting, and heatsinking considerations are discussed in the ON Semiconductor application note AN1040/D.

Thermal Model

See pages 13 to 16 for detailed information about thermal model parameters.

Table 6. DPAK 5-LEAD THERMAL RC NETWORK MODELS

Drain Copper Area (1 oz thick)			**168 mm^2**	**736 mm^2**		**168 mm^2**	**736 mm^2**	
(SPICE Deck Format)			**Cauer Network**			**Foster Network**		
			168 mm^2	736 mm^2	Units	Tau	Tau	Units
C_C1	**Junction**	**GND**	1.00E−06	1.00E−06	W−s/C	1.36E−08	1.361E−08	sec
C_C2	**node1**	**GND**	1.00E−05	1.00E−05	W−s/C	7.41E−07	7.411E−07	sec
C_C3	**node2**	**GND**	6.00E−05	6.00E−05	W−s/C	1.04E−05	1.029E−05	sec
C_C4	**node3**	**GND**	1.00E−04	1.00E−04	W−s/C	3.91E−05	3.737E−05	sec
C_C5	**node4**	**GND**	4.36E−04	3.64E−04	W−s/C	1.80E−03	1.376E−03	sec
C_C6	node5	GND	6.77E−02	1.92E−02	W−s/C	3.77E−01	2.851E−02	sec
C_C7	node6	GND	1.51E−01	1.27E−01	W−s/C	3.79E+00	9.475E−01	sec
C_C8	node7	GND	4.80E−01	1.018	W−s/C	2.65E+01	1.173E+01	sec
C_C9	node8	GND	3.740	2.955	W−s/C	8.71E+01	8.59E+01	sec
C_C10	node9	GND	10.322	0.438	W−s/C			sec
			168 mm^2	736 mm^2		R's	R's	
R_R1	**Junction**	**node1**	0.015	0.015	C/W	0.0123	0.0123	C/W
R_R2	**node1**	**node2**	0.08	0.08	C/W	0.0585	0.0585	C/W
R_R3	**node2**	**node3**	0.4	0.4	C/W	0.0304	0.0287	C/W
R_R4	**node3**	**node4**	0.2	0.2	C/W	0.3997	0.3772	C/W
R_R5	**node4**	**node5**	2.97519	2.6171	C/W	3.115	2.68	C/W
R_R6	node5	node6	8.2971	1.6778	C/W	3.571	1.38	C/W
R_R7	node6	node7	25.9805	7.4246	C/W	12.851	5.92	C/W
R_R8	node7	node8	46.5192	14.9320	C/W	35.471	7.39	C/W
R_R9	node8	node9	17.7808	19.2560	C/W	46.741	28.94	C/W
R_R10	node9	GND	0.1	0.1758	C/W			C/W

NOTE: Bold face items represent the package without the external thermal system.

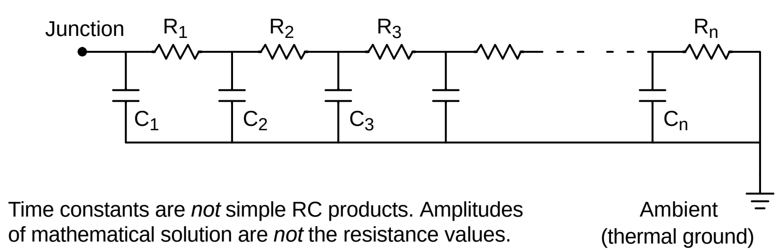


Figure 29. Grounded Capacitor Thermal Network ("Cauer" Ladder)

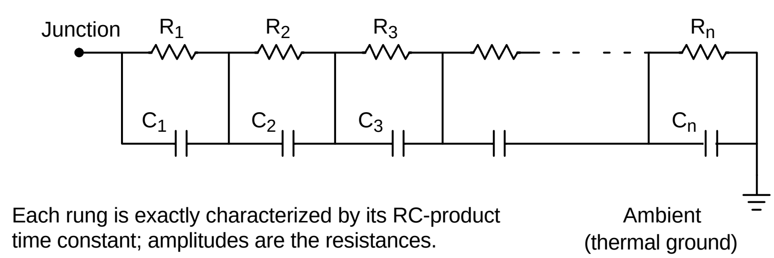


Figure 30. Non-Grounded Capacitor Thermal Ladder ("Foster" Ladder)

Table 7. D²PAK 5-LEAD THERMAL RC NETWORK MODELS

Drain Copper Area (1 oz thick)			**241 mm^2**	**788 mm^2**		**241 mm^2**	**788 mm^2**	
(SPICE Deck Format)			**Cauer Network**			**Foster Network**		
			241 mm^2	653 mm^2	Units	Tau	Tau	Units
C_C1	**Junction**	**GND**	1.00E−06	1.00E−06	W−s/C	1.361E−08	1.361E−08	sec
C_C2	**node1**	**GND**	1.00E−05	1.00E−05	W−s/C	7.411E−07	7.411E−07	sec
C_C3	**node2**	**GND**	6.00E−05	6.00E−05	W−s/C	1.005E−05	1.007E−05	sec
C_C4	**node3**	**GND**	1.00E−04	1.00E−04	W−s/C	3.460E−05	3.480E−05	sec
C_C5	**node4**	**GND**	2.82E−04	2.87E−04	W−s/C	7.868E−04	8.107E−04	sec
C_C6	node5	GND	5.58E−03	5.95E−03	W−s/C	7.431E−03	7.830E−03	sec
C_C7	node6	GND	4.25E−01	4.61E−01	W−s/C	2.786E+00	2.012E+00	sec
C_C8	node7	GND	9.22E−01	2.05	W−s/C	2.014E+01	2.601E+01	sec
C_C9	node8	GND	1.73	4.88	W−s/C	1.134E+02	1.218E+02	sec
C_C10	node9	GND	7.12	1.31	W−s/C			sec
			241 mm^2	653 mm^2		R's	R's	
R_R1	**Junction**	**node1**	0.015	0.0150	C/W	0.0123	0.0123	C/W
R_R2	**node1**	**node2**	0.08	0.0800	C/W	0.0585	0.0585	C/W
R_R3	**node2**	**node3**	0.4	0.4000	C/W	0.0257	0.0260	C/W
R_R4	**node3**	**node4**	0.2	0.2000	C/W	0.3413	0.3438	C/W
R_R5	**node4**	**node5**	1.85638	1.8839	C/W	1.77	1.81	C/W
R_R6	node5	node6	1.23672	1.2272	C/W	1.54	1.52	C/W
R_R7	node6	node7	9.81541	5.3383	C/W	4.13	3.46	C/W
R_R8	node7	node8	33.1868	18.9591	C/W	6.27	5.03	C/W
R_R9	node8	node9	27.0263	13.3369	C/W	60.80	29.30	C/W
R_R10	node9	GND	1.13944	0.1191	C/W			C/W

NOTE: Bold face items represent the package without the external thermal system.

The Cauer networks generally have physical significance and may be divided between nodes to separate thermal behavior due to one portion of the network from another. The Foster networks, though when sorted by time constant (as above) bear a rough correlation with the Cauer networks, are really only convenient mathematical models. Cauer networks can be easily implemented using circuit simulating tools, whereas Foster networks may be more easily implemented using mathematical tools (for instance, in a spreadsheet program), according to the following formula:

$$R(t) = \sum_{i=1}^{n} R_i \left(1 - e^{-t/tau_i}\right) \qquad \text{(eq. 6)}$$

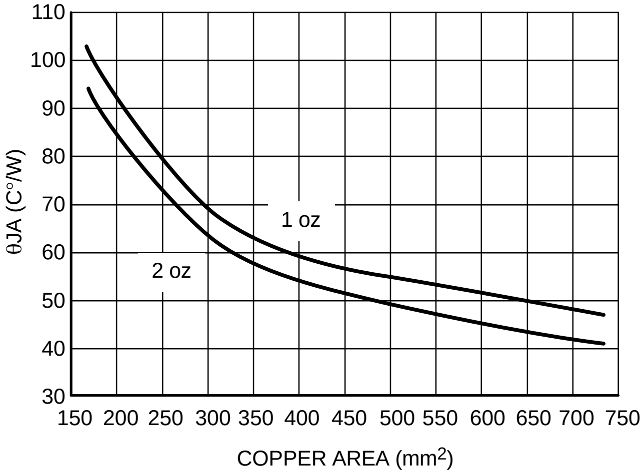


Figure 31. θJA vs. Copper Spreader Area, DPAK 5-Lead

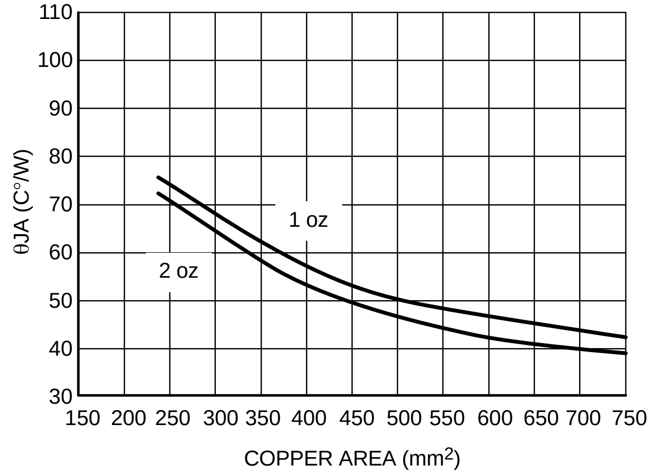


Figure 32. θJA vs. Copper Spreader Area, D^2PAK 5-Lead

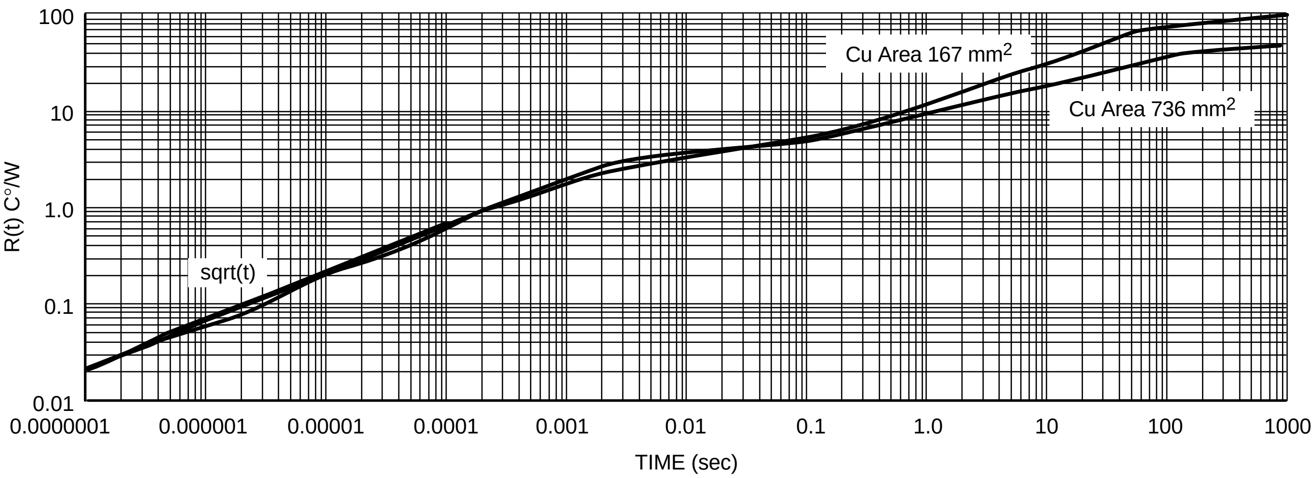


Figure 33. Single-Pulse Heating Curves, DPAK 5-Lead

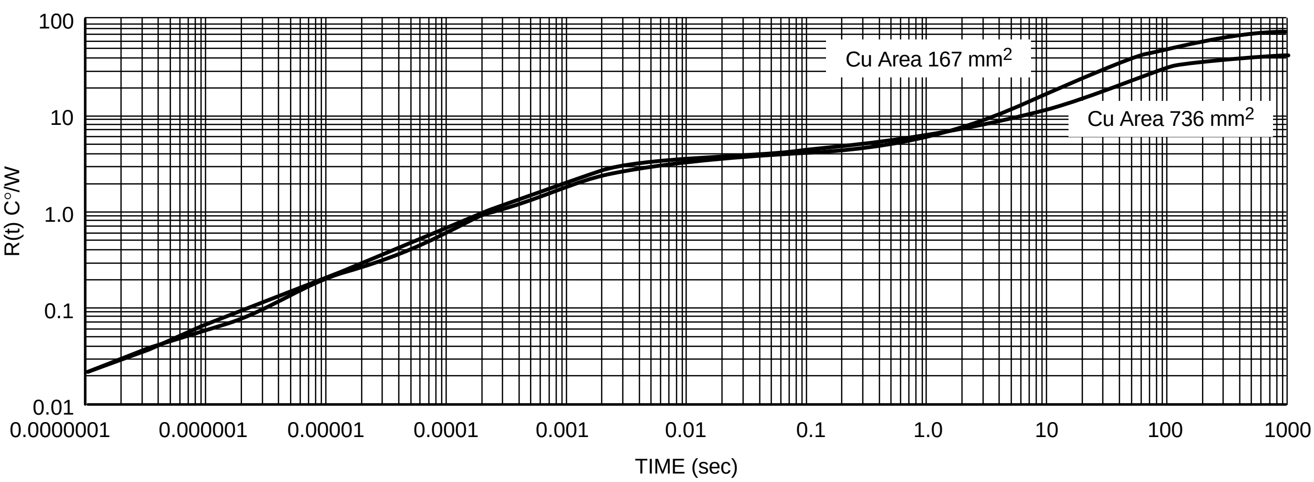


Figure 34. Single-Pulse Heating Curves, D^2PAK 5-Lead

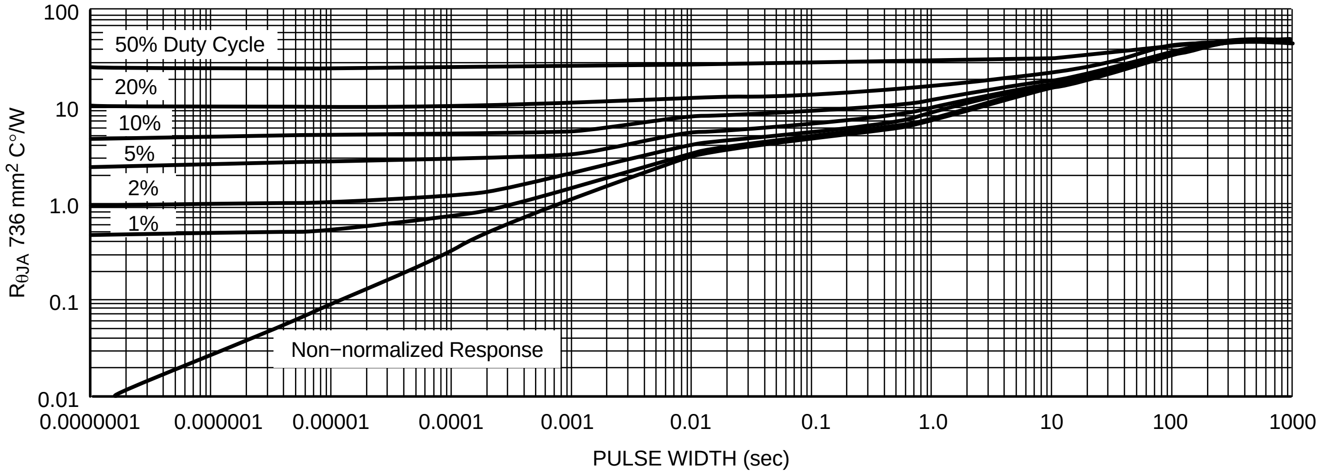


Figure 35. Duty Cycle for 1″ Spreader Boards, DPAK 5-Lead

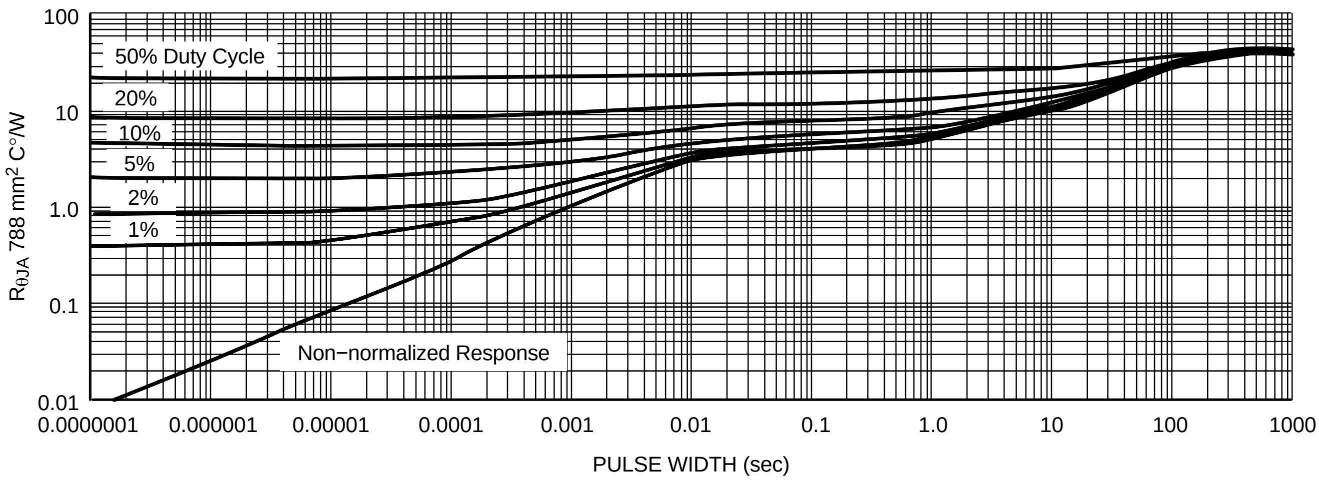


Figure 36. Duty Cycle for 1″ Spreader Boards, D²PAK 5-Lead

Table 8. ORDERING INFORMATION

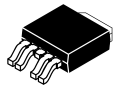
Device	Output Voltage Accuracy	Output Voltage	Package	Shipping†
NCV4276BDT33RKG	2%	3.3 V	DPAK, 5-Pin (Pb-Free)	2,500 / Tape & Reel
NCV4276BDS33R4G			D²PAK, 5-Pin (Pb-Free)	800 / Tape & Reel
NCV4276BDT50RKG		5.0 V	DPAK, 5-Pin (Pb-Free)	2,500 / Tape & Reel
NCV4276BDS50R4G			D²PAK, 5-Pin (Pb-Free)	800 / Tape & Reel
NCV4276BDTADJRKG		Adjustable	DPAK, 5-Pin (Pb-Free)	2,500 / Tape & Reel
NCV4276BDSADJR4G			D²PAK, 5-Pin (Pb-Free)	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

DPAK−5, CENTER LEAD CROP

CASE 175AA
ISSUE B

DATE 15 MAY 2014



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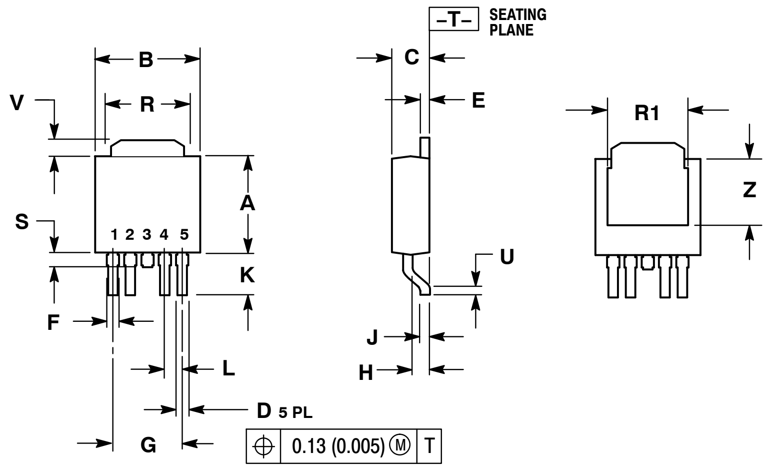
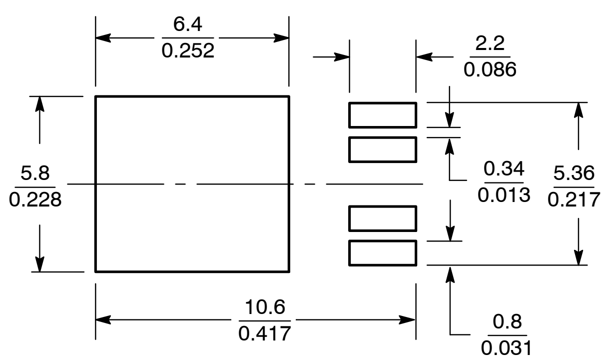


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.020	0.028	0.51	0.71
E	0.018	0.023	0.46	0.58
F	0.024	0.032	0.61	0.81
G	0.180 BSC		4.56 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.045 BSC		1.14 BSC	
R	0.170	0.190	4.32	4.83
R1	0.185	0.210	4.70	5.33
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	0.170	3.93	4.32

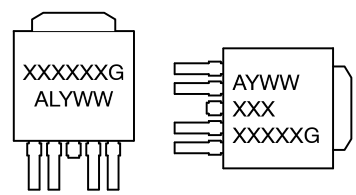
RECOMMENDED SOLDERING FOOTPRINT*



SCALE 4:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAMS*



IC   Discrete

XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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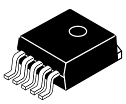
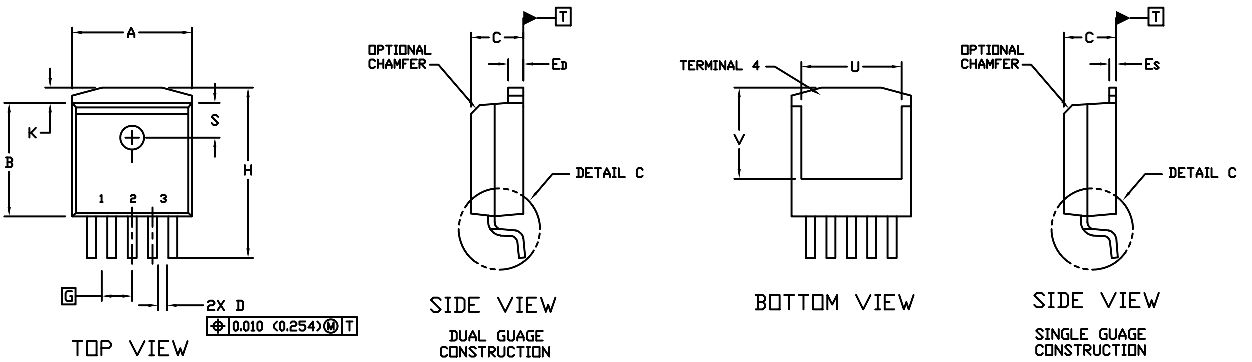
DESCRIPTION:	DPAK−5 CENTER LEAD CROP	PAGE 1 OF 1

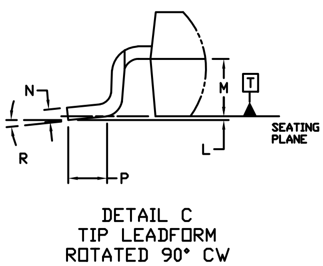


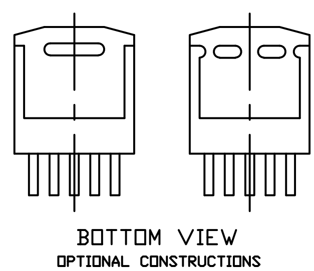
SCALE 1:1

D²PAK 5−LEAD
CASE 936A−02
ISSUE E

DATE 28 JUL 2021

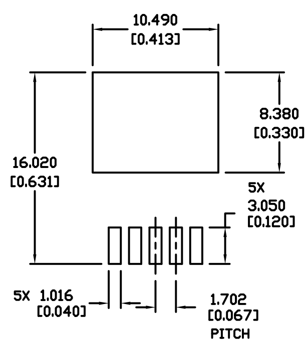






NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCHES
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 4.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

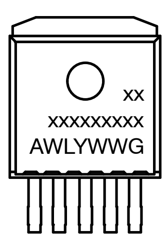
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.
A	0.396	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
ED	0.045	0.055	1.143	1.397
ES	0.018	0.026	0.457	0.660
G	0.067 BSC		1.702 BSC	
H	0.539	0.579	13.691	14.707
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	0°	8°	0°	8°
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	



RECOMMENDED
MOUNTING FOOTPRINT *

* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



xxxxxx	= Device Code	
A	= Assembly Location	
WL	= Wafer Lot	
Y	= Year	
WW	= Work Week	
G	= Pb−Free Package	

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	D2PAK 5−LEAD	PAGE 1 OF 1