NCV48220

LDO Regulator - Very Low Quiescent Current, Charge Pump Boost Converter

150 mA

The NCV48220 is very low quiescent current 150 mA LDO regulator with integrated battery voltage charge pump boost converter for automotive applications requiring full functionality during battery voltage drop events (e.g. cranking). The NCV48220 require very low number of external components. Very low quiescent current as low as 35 μA typical for NCV48220 makes it suitable for applications permanently connected to battery requiring very low quiescent current. The Enable function can be used for further decrease of quiescent current down to 1 μA. The NCV48220 contains protection functions as current limit, thermal shutdown and reverse bias current protection.

Features

- Output Voltage: 5 V
- LDO Output Current: up to 150 mA
- Very Wide Input Voltage Operation Range: from 3 V to 40 V
- Very Low Quiescent Current: typ 35 μA
- Enable Function (1.0 μA max quiescent current when disabled)
- Microprocessor Compatible Control Functions:
  - Reset Output
- AEC−Q100 Grade 1 Qualified and PPAP Capable
- Protection Features:
  - Current Limitation
  - Thermal Shutdown
  - Reverse Bias Output Current
- This is a Pb−Free Device

Typical Applications

- Stop−Start Applications
- Instruments and Clusters
- Infotainment

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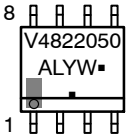
MARKING DIAGRAMS

SOIC−8
D SUFFIX
CASE 751



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

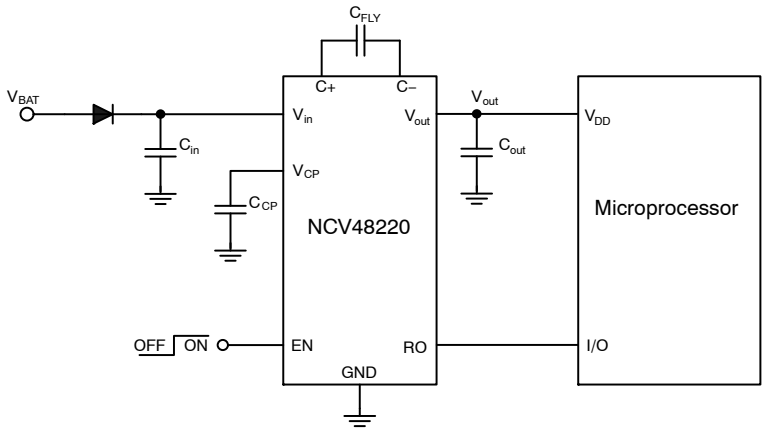


Figure 1. Application Schematic

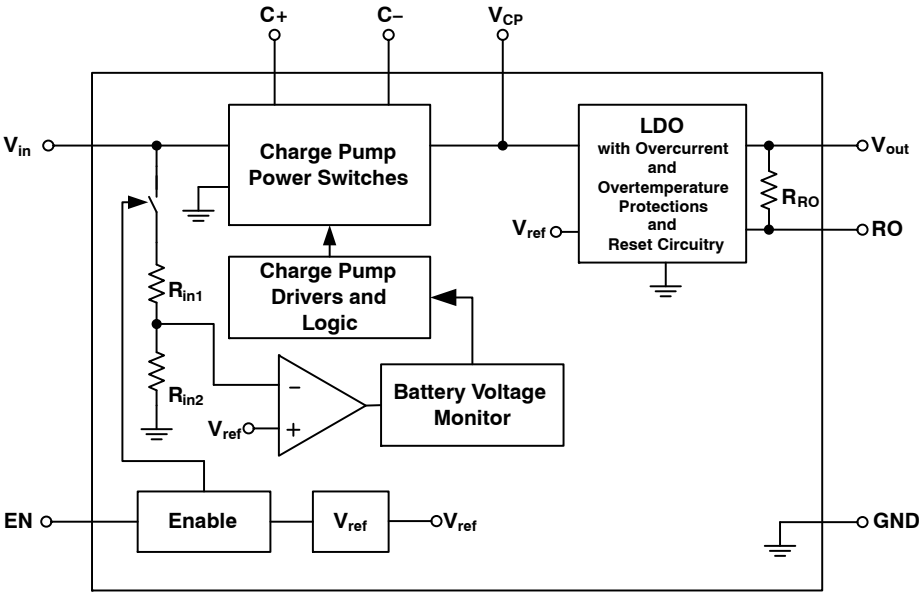


Figure 2. Simplified Block Diagram

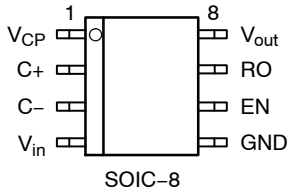


Figure 3. Pin Connections (Top Views)

Table 1. PIN FUNCTION DESCRIPTION

Pin No. SOIC−8	Pin Name	Description
1	V_{CP}	Charge Pump Output Voltage (Input Voltage of LDO).
2	C+	Flying Capacitor Positive Connection.
3	C−	Flying Capacitor Negative Connection.
4	V_{in}	Charge Pump Input Voltage.
5	GND	Power Supply Ground.
6	EN	Enable Input; low level disables the IC.
7	RO	Reset Output. 30 kΩ internal Pull−up resistor connected between RO and V_{out}. RO goes Low when V_{out} is out of regulation. See ELECTRICAL CHARACTERISTICS table for delay time specifications.
8	V_{out}	Regulated Output Voltage of LDO.

MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Charge Pump Input Voltage DC (Note 1)	V_{in}	−0.3	40	V
Charge Pump Input Voltage (Note 2) Load Dump − Suppressed	U_S	−	45	V
Charge Pump Output Voltage	V_{CP}	−0.3	16	V
Positive Flying Capacitor Voltage	V_{C+}	−0.3	16	V
Negative Flying Capacitor Voltage	V_{C-}	−0.3	7	V
Regulated Output Voltage	V_{out}	−0.3	7	V
Enable Input Voltage DC DC Transient, t < 100 ms	V_{EN}	 −0.3 −	 40 45	V
Reset Output Voltage	V_{RO}	−0.3	7	V
Maximum Junction Temperature	$T_{J(max)}$	−	150	°C
Storage Temperature Range	T_{STG}	−55	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. Load Dump Test B (with centralized load dump suppression) according to ISO16750−2 standard. Guaranteed by design. Not tested in production. Passed Class A according to ISO16750−1.

ESD CAPABILITY (Note 3)

Rating	Symbol	Min	Max	Unit
ESD Capability, Human Body Model	ESD_{HBM}	−2	2	kV

3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (JS−001−2010)
   Field Induced Charge Device Model ESD characterization is not performed on plastic molded packages with body sizes <50mm^2 due to the inability of a small package body to acquire and retain enough charge to meet the minimum CDM discharge current waveform characteristic defined in JEDEC JS−002−2014.

LEAD SOLDERING TEMPERATURE AND MSL (Note 4)

Rating	Symbol	Min	Max	Unit
Moisture Sensitivity Level	MSL	1		−

4. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, SOIC−8 Thermal Resistance, Junction−to−Air (Note 5) Thermal Reference, Junction−to−Lead (Note 5) Thermal Resistance, Junction−to−Air (Note 6) Thermal Reference, Junction−to−Lead (Note 6)	 $R_{\theta JA}$ $R_{\psi JL1}$ $R_{\theta JA}$ $R_{\psi JL1}$	 106 62.5 74 59.5	°C/W

5. Values based on 1s0p board with copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.
6. Values based on 2s2p board with copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness for inner layers, 2 oz copper thickness for single layers and FR4 PCB substrate.

RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Charge Pump Input Voltage	V_{in}	3.0	40	V
LDO Input Voltage	V_{CP}	3.5	14	V
Junction Temperature	T_J	−40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{in} = 13.5 V, V_{EN} = 3 V, I_{CP} = 0 mA, C_{FLY} = 10 μF with ESR ≈ 10 mΩ, C_{CP} = 10 μF for typical values T_J = 25°C; for min/max values −40°C ≤ T_J ≤ 150°C, unless otherwise noted.) (Note 7)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
CHARGE PUMP OUTPUT						
Undervoltage Lockout	V_{in} rising V_{in} falling	V_{in_UVLO}	2.6 2.2	2.8 2.4	3.0 2.6	V
Charge Pump Operating Threshold	V_{in} rising, Charge Pump deactivated V_{CP} falling, Charge Pump activated	$V_{CP\_ON\_OFF}$	6.1 5.3	6.3 5.5	6.5 5.7	V
Charge Pump Voltage Drop ($V_{in} - V_{CP}$)	V_{in} = 7 V, I_{out} = 150 mA	V_{DO_CP}	–	320	800	mV
Charge Pump Output Voltage Limit	V_{in} = 15 V to 40 V I_{out} = 0.1 mA to 150 mA	V_{CP_LIM}	13	14	15	V
Charge Pump Output Current Limit	V_{CP} = 0 V (shorted to GND)	I_{CP_LIM}	–	–	650	mA
Charge Pump Output Impedance	V_{in} = 3 V, I_{out} = 75 mA	R_{out_CP}	–	12	–	Ω
Switching Frequency	V_{in} = 3 V	f_{SW}	400	450	500	kHz
REGULATOR OUTPUT						
Output Voltage (Accuracy %)	V_{in} = 7 V to 29 V (LDO mode, CP inactive) I_{out} = 0.1 mA to 150 mA	V_{out}	4.9 (−2 %)	5.0	5.1 (+2%)	V
Output Voltage (Accuracy %)	V_{in} = 3 V (CP active, boosting mode) I_{out} = 55 mA	V_{out}	4.8 (−4 %)	–	–	V
Output Voltage (Accuracy %)	T_J = −40°C to 125°C V_{in} = 3.3 V (CP active, boosting mode) I_{out} = 120 mA	V_{out}	4.8 (−4 %)	–	–	V
Line Regulation	V_{in} = 7 V to 29 V, I_{out} = 5 mA	Reg_{line}	−20	0	20	mV
Load Regulation	I_{out} = 0.1 mA to 150 mA	Reg_{load}	−40	10	40	mV
Dropout Voltage (Note 8)	I_{out} = 150 mA	V_{DO}	–	150	300	mV
DISABLE AND QUIESCENT CURRENTS						
Disable Current	V_{EN} = 0 V,T_J < 85°C	I_{DIS}	–	–	1.0	μA
Quiescent Current, $I_q = I_{in} - I_{out}$	I_{out} = 0.1 mA, T_J = 25°C I_{out} = 0.1 mA, T_J < 85°C	I_q	– –	35 –	40 45	μA
CURRENT LIMIT PROTECTION						
Current Limit	V_{out} = 0.96 x V_{out_nom}	I_{LIM}	205	–	450	mA
Short Circuit Current Limit	V_{out} = 0 V	I_{SC}	–	320	–	mA
PSRR						
Power Supply Ripple Rejection	f = 100 Hz, 0.5 V_{p-p}	PSRR	–	60	–	dB
ENABLE						
Enable Input Threshold Voltage Logic Low Logic High		$V_{th(EN)}$	– 2.5	– –	0.8 –	V
Enable Input Current Logic High Logic Low	V_{EN} = 5 V, T_J < 125 °C V_{EN} = 0 V, T_J < 125 °C	I_{EN_ON} I_{EN_OFF}	– –	3 –	5 1	μA
RESET OUTPUT						
Reset Output Thresholds High Low	V_{out} decreasing V_{out} increasing	$V_{th(RO)}$	90 90.5	92.5 –	95 97	% of V_{out}
Reset Output Low Voltage	I_{RO} < 200 μA, V_{out} > 1 V	V_{ROL}	–	0.15	0.25	V
Integrated Reset Output Pull Up Resistor		R_{RO}	15	30	50	kΩ

ELECTRICAL CHARACTERISTICS (V_{in} = 13.5 V, V_{EN} = 3 V, I_{CP} = 0 mA, C_{FLY} = 10 μF with ESR ≈ 10 mΩ, C_{CP} = 10 μF for typical values T_J = 25°C; for min/max values −40°C ≤ T_J ≤ 150°C, unless otherwise noted.) (Note 7)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
RESET OUTPUT						
Reset Delay Time (Note 9)	Min Available Time Max Available Time	t_{RD}	– 102.4	0 128	– 153.6	ms
Reset Reaction Time		t_{RR}	16	25	38	μs
THERMAL SHUTDOWN						
Thermal Shutdown Temperature (Note 10)		T_{SD}	150	175	195	°C
Thermal Shutdown Hysteresis (Note 10)		T_{SH}	–	10	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
8. Measured when output voltage falls 100 mV below the regulated voltage at V_{CP} = 13.5 V.
9. Reset Delay Times can be chosen from list: 0, 2, 4, 8, 16, 32, 64, 128 ms (Reset Delay Time 0 ms represents Power Good function) and these delay times are factory preset.
10. Values based on design and/or characterization.

TYPICAL CHARACTERISTICS

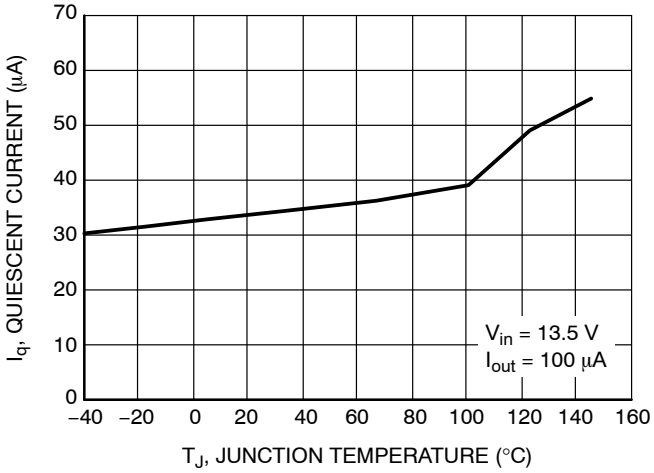


Figure 4. Quiescent Current vs. Junction Temperature

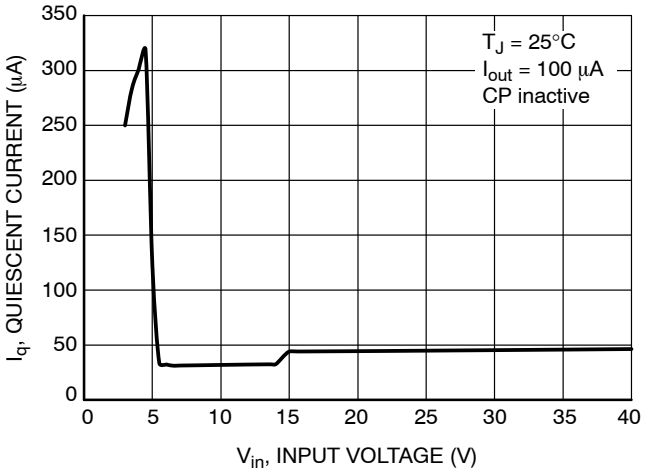


Figure 5. Quiescent Current vs. Input Voltage

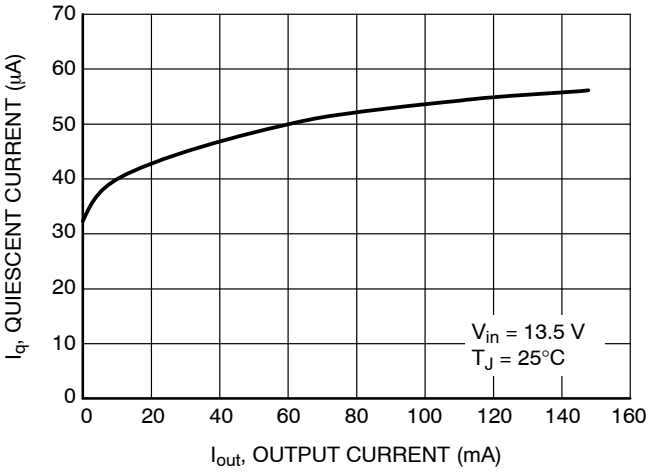


Figure 6. Quiescent Current vs. Output Current

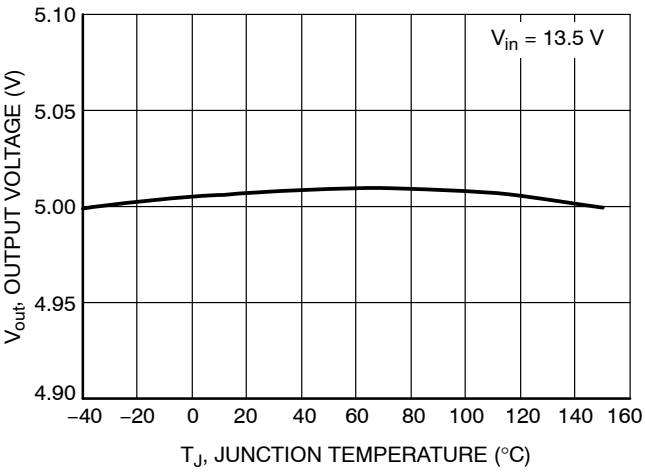


Figure 7. Output Voltage vs. Junction Temperature

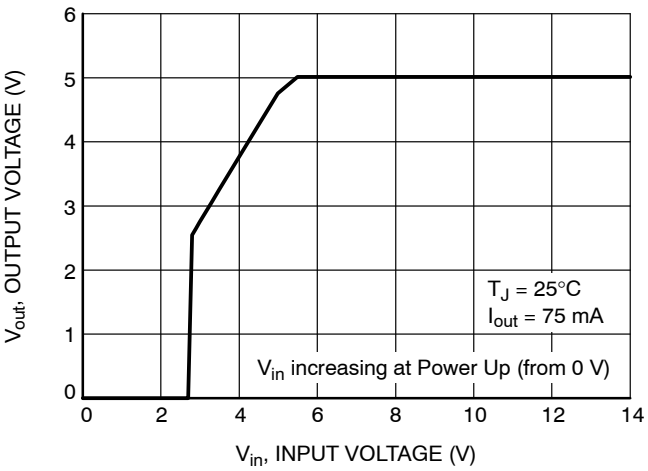


Figure 8. Output Voltage vs. Input Voltage

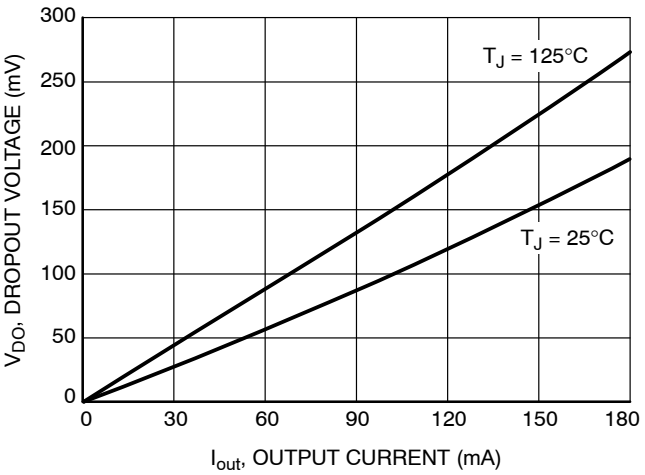


Figure 9. Dropout Voltage vs. Output Current

TYPICAL CHARACTERISTICS

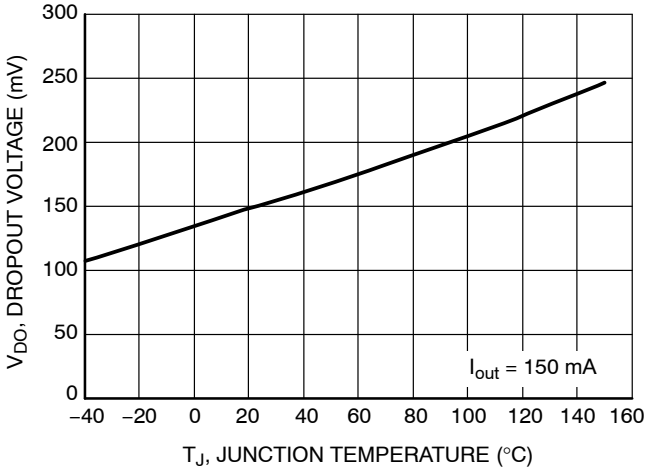


Figure 10. Dropout Voltage vs. Junction Temperature

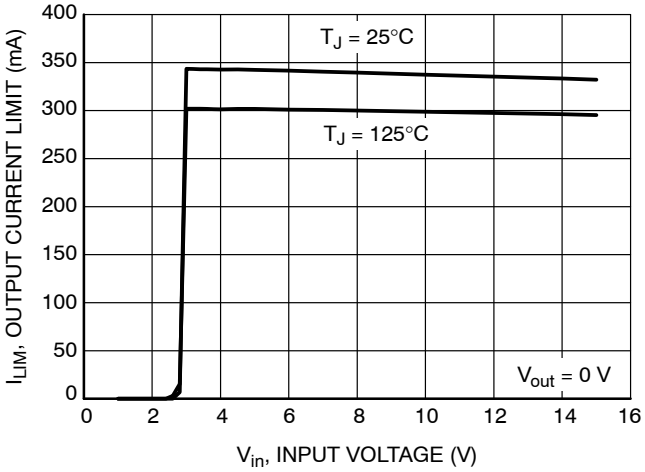


Figure 11. Output Current Limit vs. Input Voltage

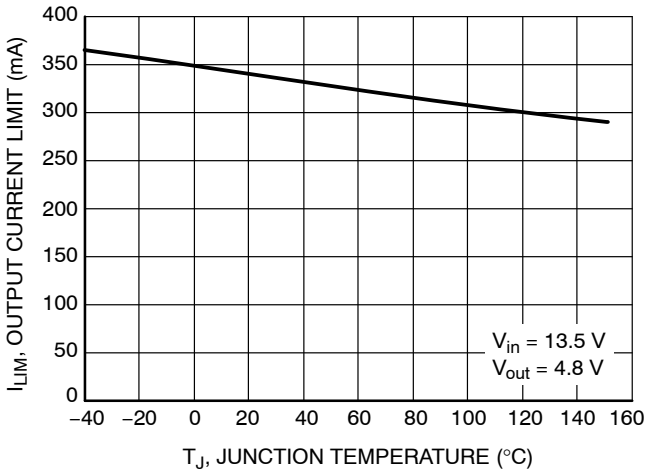


Figure 12. Output Current Limit vs. Junction Temperature

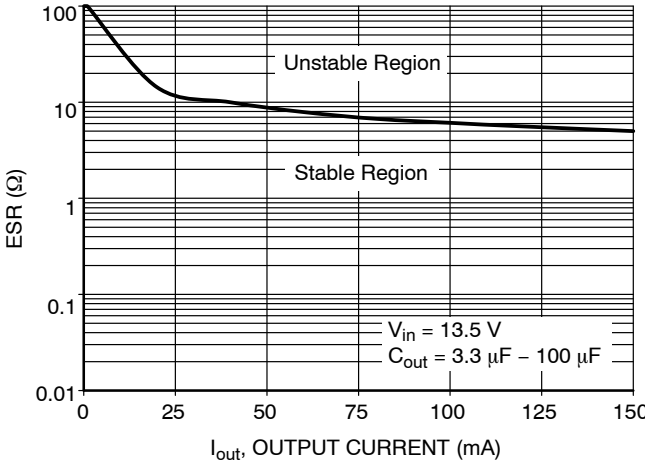


Figure 13. Output Stability with Output Capacitor ESR

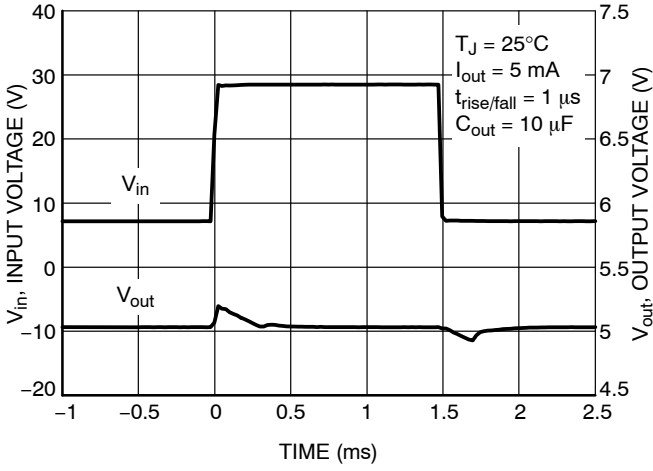


Figure 14. Line Transient

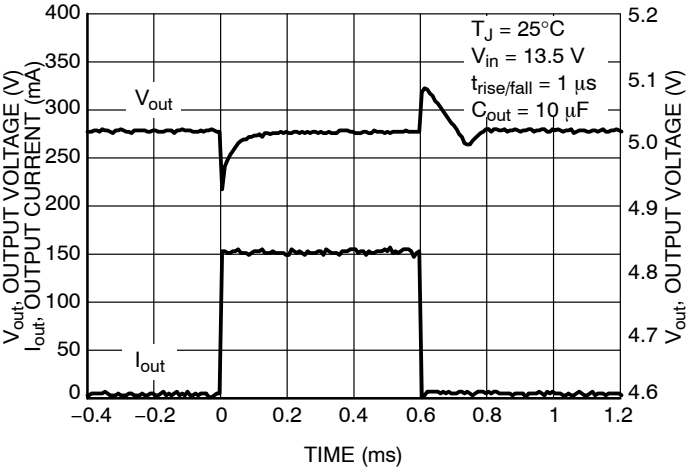


Figure 15. Load Transient

TYPICAL CHARACTERISTICS

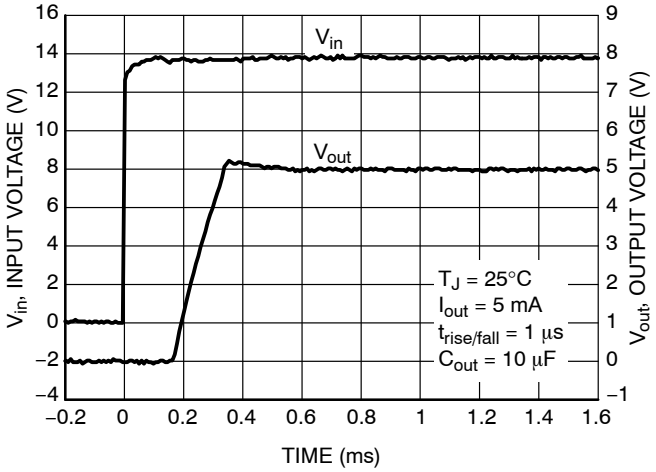


Figure 16. Power Up Transient

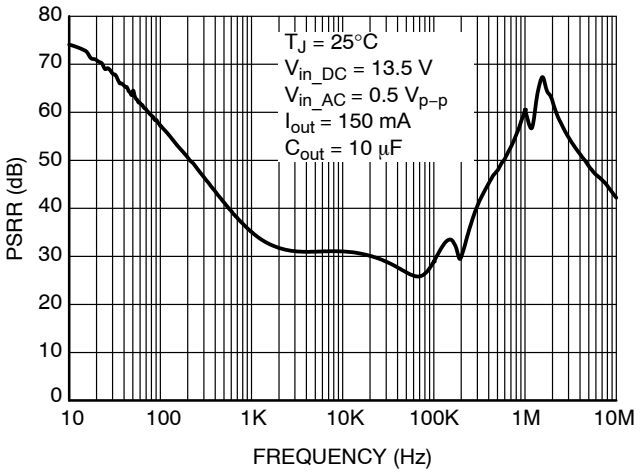


Figure 17. PSRR vs. Frequency

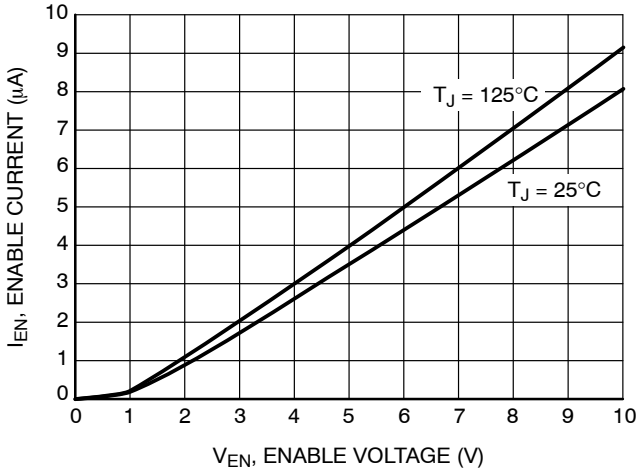


Figure 18. Enable Current vs. Enable Voltage

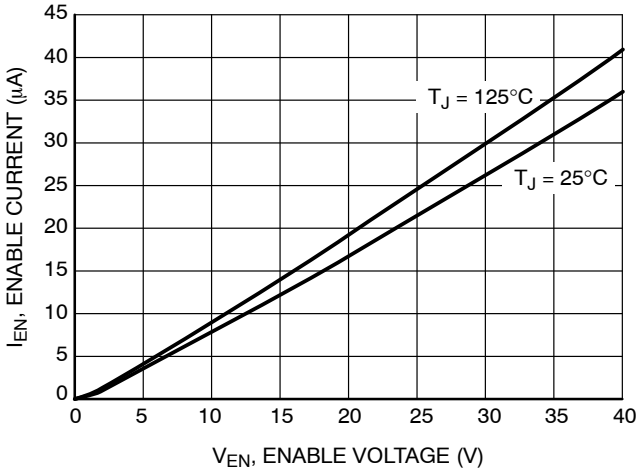


Figure 19. Enable Current vs. Enable Voltage

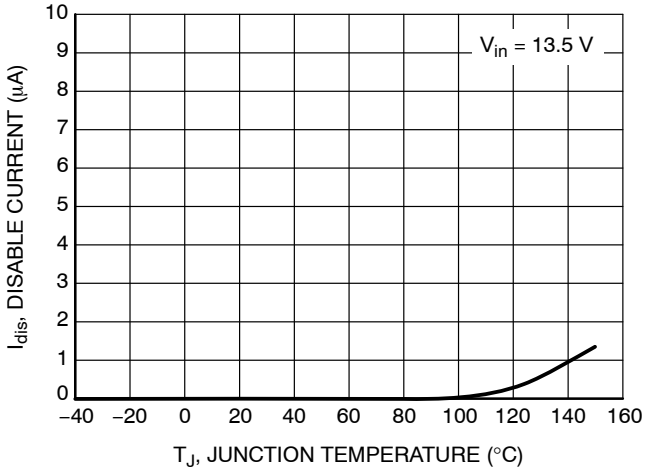


Figure 20. Disable Current vs. Junction Temperature

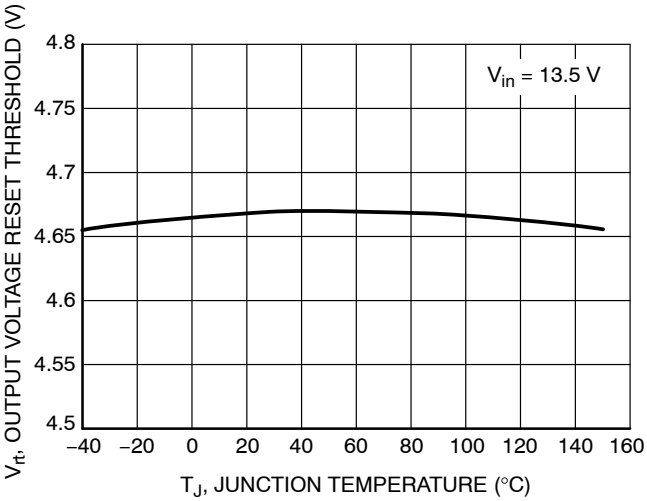


Figure 21. Output Voltage Reset Threshold vs. Junction Temperature

TYPICAL CHARACTERISTICS

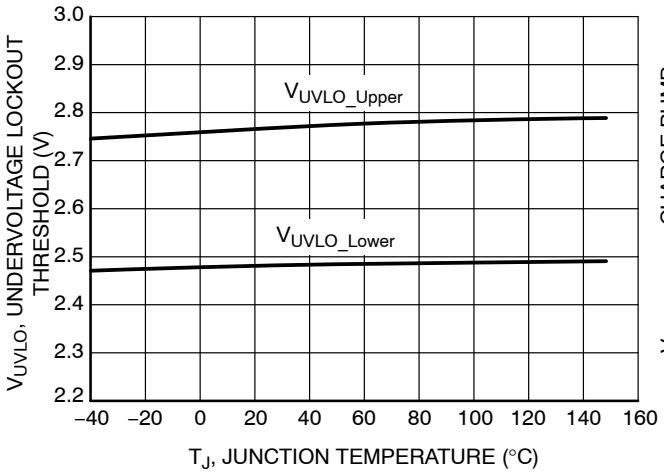


Figure 22. Undervoltage Lockout vs. Junction Temperature

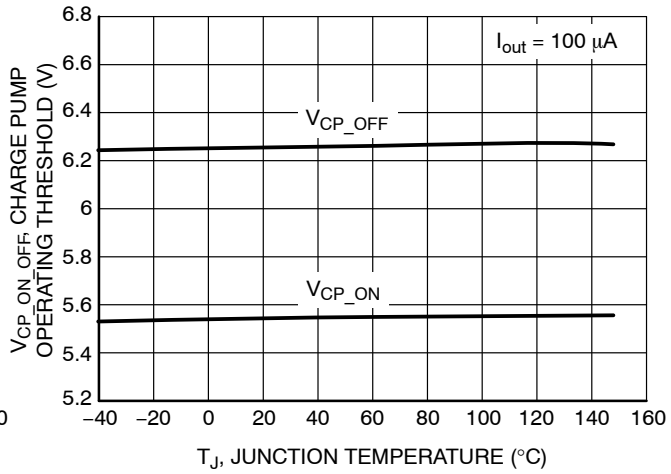


Figure 23. Charge Pump Operating Threshold vs. Junction Temperature

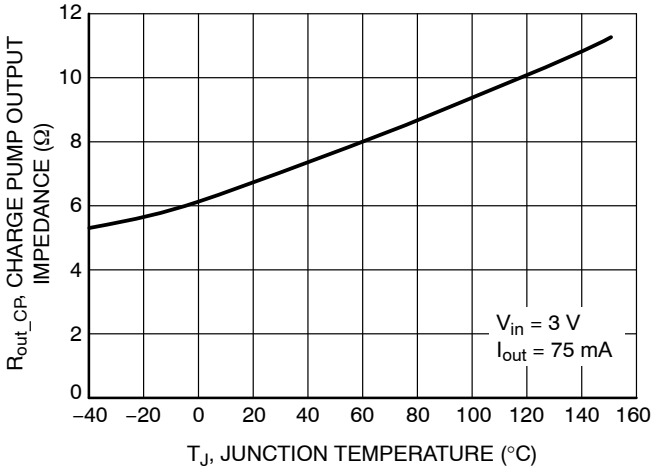


Figure 24. Charge Pump Output Impedance vs. Junction Temperature

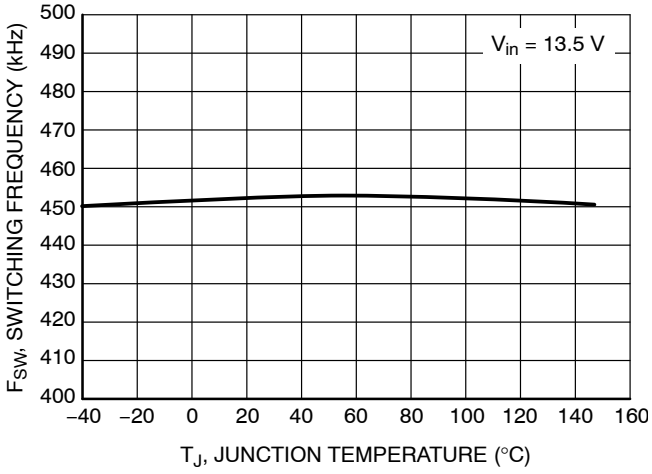


Figure 25. Switching Frequency vs. Junction Temperature

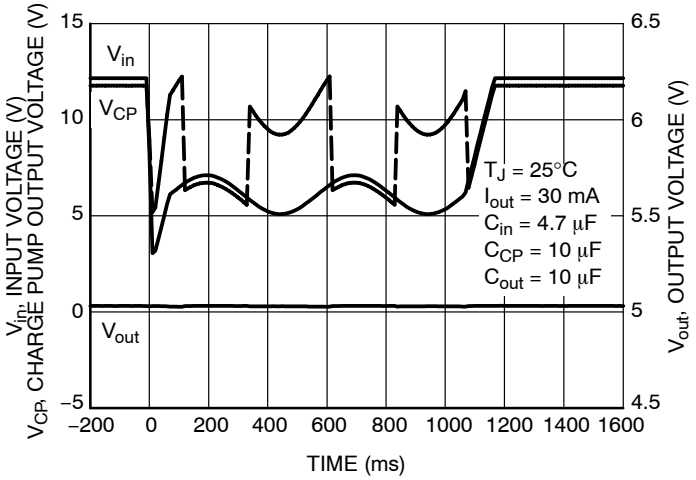


Figure 26. Starting Profile Transient

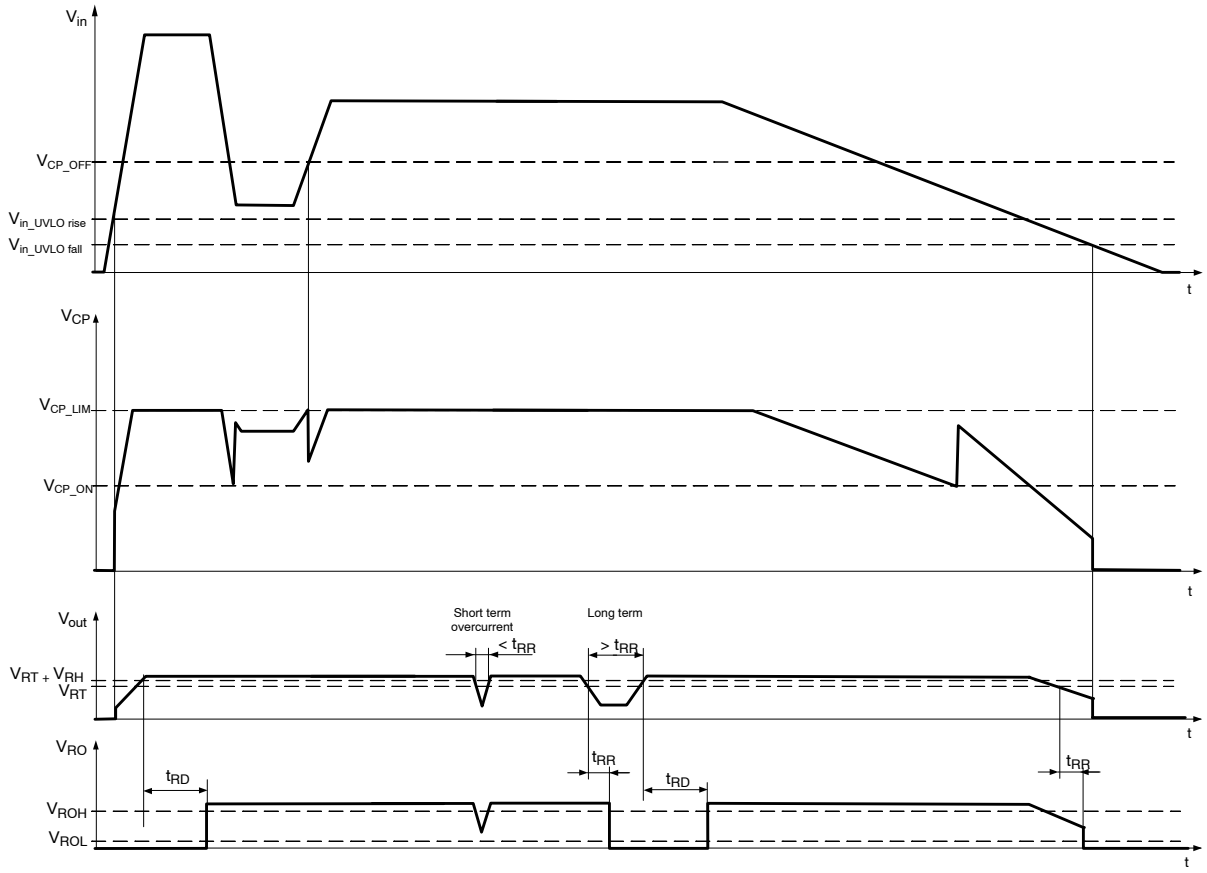


Figure 27. Reset Function, Charge Pump Function and Timing Diagram

DEFINITIONS

General

All measurements are performed using short pulse low duty cycle techniques to maintain junction temperature as close as possible to ambient temperature.

Output voltage

The output voltage parameter is defined for specific temperature, input voltage and output current values or specified over Line, Load and Temperature ranges.

Line Regulation

The change in output voltage for a change in input voltage measured for specific output current over operating ambient temperature range.

Load Regulation

The change in output voltage for a change in output current measured for specific input voltage over operating ambient temperature range.

Dropout Voltage

The input to output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. It is measured when the output drops 100 mV below its nominal value. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

Quiescent and Disable Currents

Quiescent Current (I_q) is the difference between the input current (measured through the LDO input pin) and the output load current. If Enable pin is set to LOW the regulator reduces its internal bias and shuts off the output, this term is called the disable current (I_{DIS}).

Current Limit

Current Limit is value of output current by which output voltage drops below 96 % of its nominal value.

PSRR

Power Supply Rejection Ratio is defined as ratio of output voltage and input voltage ripple. It is measured in decibels (dB).

Line Transient Response

Typical output voltage overshoot and undershoot response when the input voltage is excited with a given slope.

Load Transient Response

Typical output voltage overshoot and undershoot response when the output current is excited with a given slope between low−load and high−load conditions.

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 175°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

Maximum Package Power Dissipation

The power dissipation level is maximum allowed power dissipation for particular package or power dissipation at which the junction temperature reaches its maximum operating value, whichever is lower.

APPLICATIONS INFORMATION

Circuit Description

The NCV48220 is an integrated low dropout regulator with integrated battery voltage charge pump boost converter that provides a regulated voltage at 150 mA to the output. Device is enabled with an input to the enable pin. The regulator voltage is provided by a PMOS pass transistor controlled by an error amplifier with a bandgap reference, which gives it the lowest possible dropout voltage. The output current capability is 150 mA, and the base drive quiescent current is controlled to prevent oversaturation when the input voltage is low or when the output is overloaded. Charge pump boost converter is active only during charge pump output voltage (input voltage of LDO) decreasing under charge pump operating activation threshold and inactive after input voltage increasing over charge pump operating deactivation threshold. Thermal shutdown occurs above 150°C to protect the IC during overloads and extreme ambient temperatures.

Regulator

The error amplifier compares the reference voltage to a sample of the output voltage (V_{out}) and drives the gate of a PMOS series pass transistor via a buffer. The reference is a bandgap design to give it a temperature−stable output. Saturation control of the PMOS is a function of the load current and input voltage. Oversaturation of the output power device is prevented, and quiescent current in the ground pin is minimized. Current limit and voltage monitors complement the regulator design to give safe operating signals to the processor and control circuits.

Regulator Stability Considerations

The input capacitor (C_{in}) and charge pump output capacitor (C_{CP}) is necessary to stabilize the input impedance to avoid voltage line influences. The output capacitor (C_{out}) helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability. The capacitor value and type should be based on cost, availability, size and temperature constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information. The value for the output capacitor C_{out}, shown in Figure 1 should work for most applications; see also Figure 13 for output stability at various load and Output Capacitor ESR conditions. Stable region of ESR in Figure 13 shows ESR values at which the LDO output voltage does not have any permanent oscillations at any dynamic changes of output load current. Marginal ESR is the value at which the output voltage waving is fully damped during four periods after the load change and no oscillation is further observable.

ESR characteristics were measured with ceramic capacitors and additional series resistors to emulate ESR. Low duty cycle pulse load current technique has been used to maintain junction temperature close to ambient temperature.

List of recommended output capacitors:
GCM31CR71H225MA55 (2.2 μF, 50 V, X7R, 1206)
GCM31CR71C335KA37 (3.3 μF, 16 V, X7R, 1206)
GCM31CR71E475MA55 (4.7 μF, 25 V, X7R, 1206)
GCM31CC71E106MA03 (10 μF, 25 V, X7S, 1206)
KCM55WC71E107MH13 (100 μF, 25 V, X7S, 2220)

CGA5L3X7R1H225M (2.2 μF, 50 V, X7R, 1206)
CGA5L1X7R1E335M (3.3 μF, 25 V, X7R, 1206)
CGA5L1X7R1E475M (4.7 μF, 25 V, X7R, 1206)
CGA5L1X7R1E106M (10 μF, 25 V, X7R, 1206)
CKG57NX7S1C107M (100 μF, 16 V, X7S, 2220)

Charge Pump Capacitor Selection

Low ESR capacitors are necessary to minimize power losses, especially at high load current during active charge pump boost mode. The exact value of C_{FLY} and C_{CP} is not important. Charge pump output impedance (R_{out_CP}) is given by equation 1.

$$R_{out\_CP} \cong 2 \times \Sigma(R_{SW}) + \frac{1}{f_{SW} \times C_{FLY}} + 4 \times ESR_{FLY} + ESR_{C_{CP}} \quad \text{(eq. 1)}$$

Charge pump output voltage ripple is determined by the value of C_{CP} and the load current (I_{out}). C_{CP} is charged and discharged at a current roughly equal to the load current.

$$V_{ripple\_CP} = \frac{I_{OUT}}{2 \times f_{SW} \times C_{CP}} \quad \text{(eq. 2)}$$

This equation doesn't including the impact of non−overlap time and C_{CP} capacitor ESR. Since the output is not being driven during the non−overlap time, this time should be included in the ripple calculation. C_{CP} capacitor discharge time is approximately 60 % of a switching period

$$V_{ripple\_CP} = I_{OUT} \times \left(\frac{0.6}{f_{SW} \times C_{CP}} + 2 \times ESR_{C_{CP}} \right) \quad \text{(eq. 3)}$$

For example, with a 450 kHz switching frequency, a 10 μF C_{CP} capacitor with an ESR of 0.25 Ω and a 100 mA load the ripple voltage is 65 mV peak to peak.

Enable Input

The enable pin is used to turn the regulator on or off. By holding the pin below 0.8 V, the output of the regulator will be turned off. When the voltage on the enable pin is greater than 2.5 V, the output of the regulator will be enabled to power its output to the regulated output voltage. The enable pin may be connected directly to the input pin to give constant enable to the output regulator.

Thermal Considerations

As power in the NCV48220 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCV48220 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCV48220 can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} + T_A\right]}{R_{\Theta JA}} \quad \text{(eq. 4)}$$

Since T_J is not recommended to exceed 150°C, then the NCV48220 soldered on 645 mm^2, 1 oz copper area, FR4 can dissipate up to 1.2 W and up to 1.7 W for 4 layers PCB (all layers are 1 oz) when the ambient temperature (T_A) is 25 °C. See Figure 28 for $R_{\Theta JA}$ versus PCB area.

Power dissipated is given by three main parts. The first is dependent on the charge pump boost mode activation. The second part including the power dissipated on LDO and the last represent current consumption.

CP active : $$P_{D\_CP1} = (2 \times V_{IN} - V_{CP}) \times I_{OUT} \quad \text{(eq. 5)}$$

CP inactive : $$P_{D\_CP2} = \left(V_{IN} - V_{CP\left(\text{max. } V_{CP\_LIM}\right)}\right) \times I_{Out} \quad \text{(eq. 6)}$$

$$P_{D\_LDO} = \left(V_{CP\left(\text{max. } V_{CP\_LIM}\right)} - V_{OUT}\right) \times I_{Out} \quad \text{(eq. 7)}$$

$$P_{D\_Iq} = V_{in} \times \left(I_{q@I_{OUT}}\right) \quad \text{(eq. 8)}$$

The power dissipated by the NCV48220 can be calculated from the following equations:

$$P_{D1} = P_{D\_CP1} + P_{D\_LDO} + P_{D\_Iq} \quad \text{(eq. 9)}$$

$$P_{D2} = P_{D\_CP2} + P_{D\_LDO} + P_{D\_Iq} \quad \text{(eq. 10)}$$

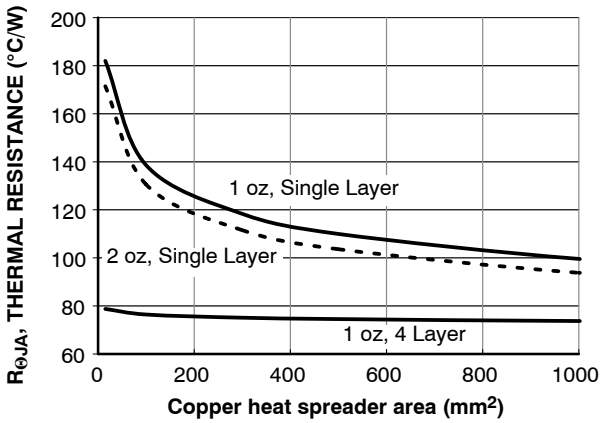


Figure 28. Thermal Resistance vs. PCB Copper Area

Hints

V_{in} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the device and make traces as short as possible.

Place filter components as near as possible to the device to increase EMC performance.

Input Capacitor C_{in} is required if regulator is located far from power supply filter. If extremely fast input voltage transients are expected with slew rate in excess of 4 V/μs then appropriate input filter must be used. The filter can be composed of several capacitors in parallel.

ORDERING INFORMATION

Device	Output Voltage	Reset Delay Time††	Marking	Package	Shipping†
NCV48220D50R2G	5.0 V	0 ms	V4822050	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

††For information about another Output Voltage, Reset Delay Time, Packages options contact factory. Reset Delay Time can be chosen from following list of values: 0, 2, 4, 8, 16, 32, 64 and 128 ms.

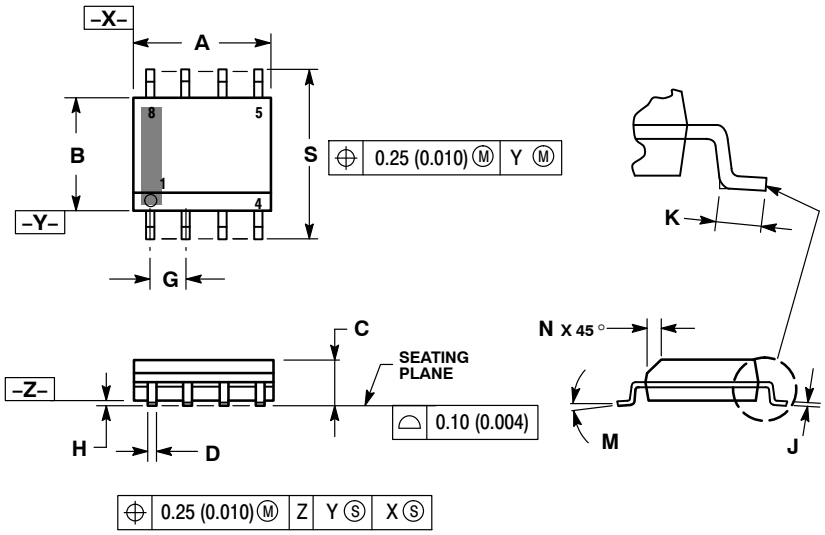
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

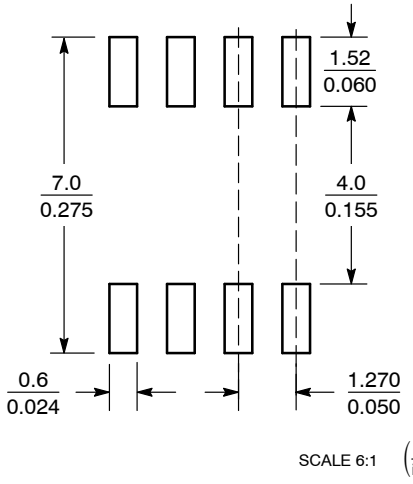
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

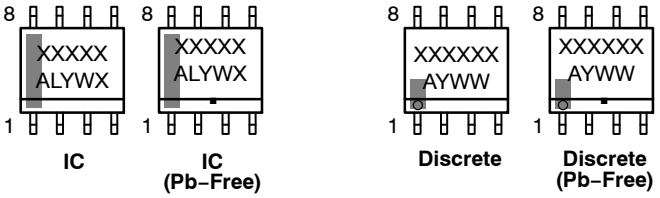
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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