

# NCV8720

## CMOS Voltage Regulator, Very Low Dropout Bias Rail, 350mA

The NCV8720 is a 350 mA VLDO equipped with NMOS pass transistor and a separate bias supply voltage ( $V_{BIAS}$ ). The device provides very stable, accurate output voltage with low noise suitable for space constrained, noise sensitive applications. In order to optimize performance for battery operated applications, the NCV8720 features low  $I_Q$  consumption. The NCV8720 is offered in WDFN6 2 mm x 2 mm package, wettable flanks option available for Enhanced Optical Inspection.

### Features

- Input Voltage Range: 0.8 V to 5.5 V
- Bias Voltage Range: 2.4 V to 5.5 V
- Fixed Output Voltage Device
- Output Voltage Range: 0.8 V to 2.1 V
- $\pm 2\%$  Accuracy over Temperature
- Ultra-Low Dropout: 110 mV typically at 350 mA
- Very Low Bias Input Current of Typ. 80  $\mu$ A
- Very Low Bias Input Current in Disable Mode: Typ. 0.5  $\mu$ A
- Low Noise, High PSRR
- Built-In Soft-Start with Monotonic  $V_{OUT}$  Rise
- Stable with a 2.2  $\mu$ F Ceramic Capacitor
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable; Device Temperature Grade 1:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  Ambient Operating Temperature Range
- These are Pb-Free Devices

### Typical Applications

- Automotive, Consumer and Industrial Equipment Point of Load Regulation
- Battery-Powered Equipment
- FPGA, DSP and Logic Power Supplies
- Switching Power Supply Post Regulation
- Cameras, DVRs, STB and Camcorders

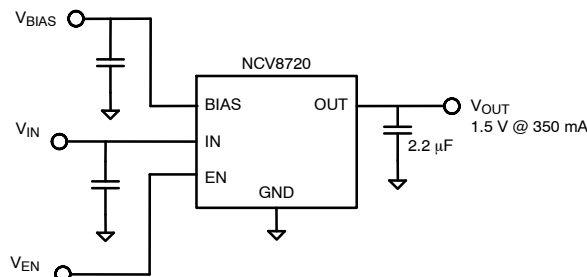


Figure 1. Typical Application Schematics



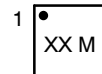
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### MARKING DIAGRAM

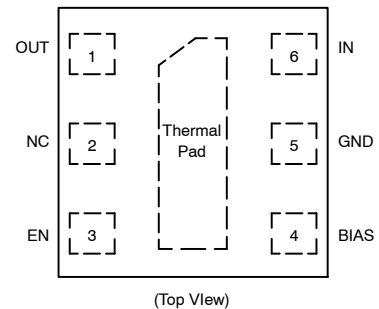


WDFN6  
CASE 511BR



XX = Specific Device Code  
M = Date Code

### PIN CONNECTIONS



(Top View)

### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 9 of this data sheet.

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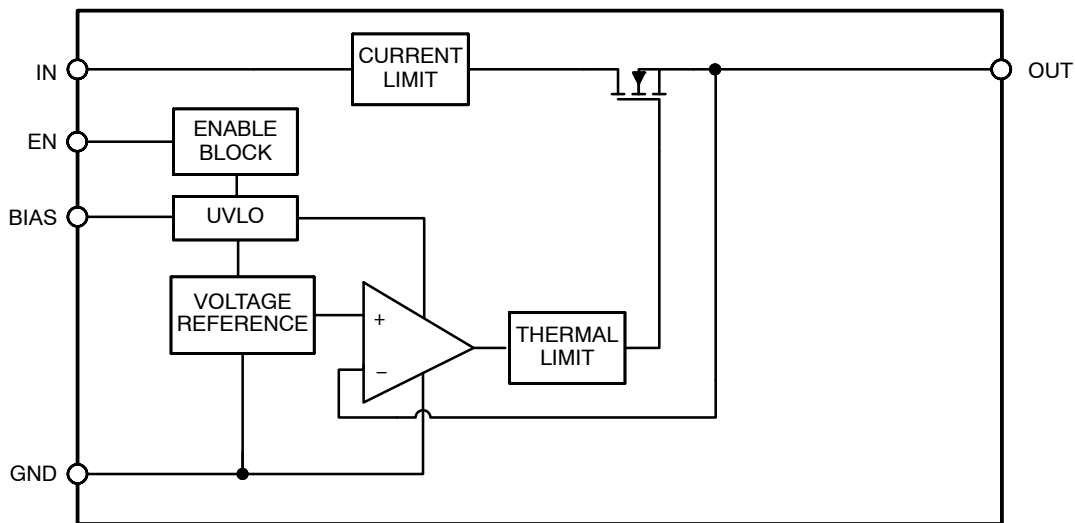


Figure 2. Simplified Schematic Block Diagram

## PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	OUT	Regulated Output Voltage pin
2	N/C	Not internally connected
3	EN	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode.
4	BIAS	Bias voltage supply for internal control circuits. This pin is monitored by internal Under-Voltage Lockout Circuit.
5	GND	Ground pin
6	IN	Input Voltage Supply pin
Pad		Should be soldered to the ground plane for increased thermal performance.

**ABSOLUTE MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	$V_{IN}$	-0.3 to 6	V
Output Voltage	$V_{OUT}$	-0.3 to $(V_{IN}+0.3) \leq 6$	V
Chip Enable and Bias Input	$V_{EN}, V_{BIAS}$	-0.3 to 6	V
Output Short Circuit Duration	$t_{SC}$	unlimited	s
Maximum Junction Temperature	$T_J$	150	°C
Operating Ambient Temperature Range	$T_A$	-40 to 125	°C
Storage Temperature	$T_{STG}$	-55 to 150	°C
ESD Capability, Human Body Model (Note 2)	$ESD_{HBM}$	2000	V
ESD Capability, Machine Model (Note 2)	$ESD_{MM}$	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection (except OUT pin) and is tested by the following methods:  
 ESD Human Body Model tested per AEC-Q100-002  
 ESD Machine Model tested per AEC-Q100-003  
 Latchup Current Maximum Rating  $\pm 100$  mA per AEC-Q100-004.

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Min	Max	Unit
Input Voltage	$V_{IN}$	$(V_{OUT} + V_{DO\_IN})$	5.5	V
Bias Voltage	$V_{BIAS}$	$(V_{OUT} + 1.4) \geq 2.4$	5.5	V
Junction Temperature	$T_J$	-40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**THERMAL CHARACTERISTICS**

Rating	Symbol	Value	Unit
Thermal Characteristics, WDFN6 2 mm x 2 mm Thermal Resistance, Junction-to-Air (Note 3)	$R_{\theta JA}$	65	°C/W

3. This data was derived by thermal simulations based on the JEDEC JESD51 series standards methodology. Only a single device mounted at the center of a high-K (2s2p) 3in x 3in multilayer board with 1-ounce internal planes and 2-ounce copper on top and bottom. Top copper layer has a dedicated 125 sqmm copper area.

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## ELECTRICAL CHARACTERISTICS

Over Operating Temperature Range ( $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ),  $V_{\text{BIAS}} = (V_{\text{OUT}} + 1.4 \text{ V})$  or  $2.5 \text{ V}$ , whichever is greater;  $V_{\text{IN}} \geq V_{\text{OUT}} + 0.5 \text{ V}$ ,  $I_{\text{OUT}} = 1 \text{ mA}$ ,  $V_{\text{EN}} = 1.1 \text{ V}$ ,  $C_{\text{OUT}} = 2.2 \mu\text{F}$ , unless otherwise noted. Typical values are at  $T_J = +25^{\circ}\text{C}$ .

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit	
Operating Input Voltage Range		$V_{\text{IN}}$	$V_{\text{OUT}} + V_{\text{DO\_IN}}$		5.5	V	
Operating Bias Voltage Range		$V_{\text{BIAS}}$	$(V_{\text{OUT}} + 1.4) \geq 2.4$		5.5	V	
Output Voltage Range (Note 4)			0.8		2.1	V	
Output Voltage Accuracy	Nominal	$T_J = +25^{\circ}\text{C}$	$V_{\text{OUT}}$		$\pm 0.5$	%	
	Over $V_{\text{BIAS}}$ , $V_{\text{IN}}$ , $I_{\text{OUT}}$ , $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	$V_{\text{OUT}} + 1.4 \text{ V} \leq V_{\text{BIAS}} \leq 5.5 \text{ V}$ , $V_{\text{OUT}} + 0.5 \text{ V} \leq V_{\text{IN}} \leq 4.5 \text{ V}$ , $0 \text{ mA} \leq I_{\text{OUT}} \leq 350 \text{ mA}$	$V_{\text{OUT}}$		-2	%	
$V_{\text{IN}}$ Line Regulation	$V_{\text{IN}} = (V_{\text{OUT}} + 0.5 \text{ V})$ to $4.5 \text{ V}$ , $I_{\text{OUT}} = 1 \text{ mA}$	$\Delta V_{\text{OUT}}/\Delta V_{\text{IN}}$		5.0		$\mu\text{V/V}$	
$V_{\text{BIAS}}$ Line Regulation	$V_{\text{BIAS}} = (V_{\text{OUT}} + 1.4 \text{ V})$ or $2.5 \text{ V}$ (whichever is greater) to $5.5 \text{ V}$ , $I_{\text{OUT}} = 1 \text{ mA}$	$\Delta V_{\text{OUT}}/\Delta V_{\text{BIAS}}$		16		$\mu\text{V/V}$	
Load Regulation	$0 \text{ mA} \leq I_{\text{OUT}} \leq 350 \text{ mA}$ (no load to full load)	$\Delta V_{\text{OUT}}/\Delta I_{\text{OUT}}$		-1.0		$\mu\text{V/mA}$	
$V_{\text{IN}}$ Dropout Voltage (Note 5)	$V_{\text{IN}} = V_{\text{OUT(NOM)}} - 0.1 \text{ V}$ , $(V_{\text{BIAS}} - V_{\text{OUT(NOM)}}) = 1.4 \text{ V}$ , $I_{\text{OUT}} = 350 \text{ mA}$	$V_{\text{DO\_IN}}$		110	200	mV	
$V_{\text{BIAS}}$ Dropout Voltage (Note 6)	$V_{\text{IN}} = V_{\text{OUT(NOM)}} + 0.3 \text{ V}$ , $I_{\text{OUT}} = 350 \text{ mA}$	$V_{\text{DO\_BIAS}}$		1.15	1.4	V	
Output Current Limit	$V_{\text{OUT}} = 0.9 \times V_{\text{OUT(NOM)}}$	$I_{\text{CL}}$	420	600	1000	mA	
Bias Pin Current	$I_{\text{OUT}} = 0 \text{ mA}$ to $350 \text{ mA}$	$I_{\text{BIAS}}$		80	110	$\mu\text{A}$	
Shutdown Current ( $I_{\text{GND}}$ )	$V_{\text{EN}} \leq 0.4 \text{ V}$ , $T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	$I_{\text{SHDN}}$		0.5	2.0	$\mu\text{A}$	
$V_{\text{IN}}$ Power-Supply Rejection Ratio	$V_{\text{IN}} - V_{\text{OUT}} \geq 0.5 \text{ V}$ , $I_{\text{OUT}} = 350 \text{ mA}$	PSRR ( $V_{\text{IN}}$ )	$f = 10 \text{ Hz}$		52		dB
			$f = 100 \text{ Hz}$		56		
			$f = 1 \text{ kHz}$		65		
			$f = 10 \text{ kHz}$		46		
			$f = 100 \text{ kHz}$		37		
			$f = 1 \text{ MHz}$		25		
$V_{\text{BIAS}}$ Power-Supply Rejection Ratio	$V_{\text{IN}} - V_{\text{OUT}} \geq 0.5 \text{ V}$ , $I_{\text{OUT}} = 350 \text{ mA}$	PSRR ( $V_{\text{BIAS}}$ )	$f = 10 \text{ Hz}$		65		dB
			$f = 100 \text{ Hz}$		65		
			$f = 1 \text{ kHz}$		70		
			$f = 10 \text{ kHz}$		50		
			$f = 100 \text{ kHz}$		35		
			$f = 1 \text{ MHz}$		24		
Output Noise Voltage	$\text{BW} = 10 \text{ Hz}$ to $100 \text{ kHz}$	$V_{\text{N}}$		40		$\mu\text{VRMS}$	
Inrush Current on $V_{\text{IN}}$		$I_{\text{VIN\_INRUSH}}$		$100 + I_{\text{LOAD}}$		mA	
Startup Time	$V_{\text{OUT}} = 95\% V_{\text{OUT(NOM)}}$ , $I_{\text{OUT}} = 350 \text{ mA}$ , $C_{\text{OUT}} = 2.2 \mu\text{F}$	$t_{\text{STR}}$		140		$\mu\text{s}$	
Enable Pin High (enabled)		$V_{\text{EN(HI)}}$	1.1			V	
Enable Pin Low (disabled)		$V_{\text{EN(LO)}}$	0		0.4	V	
Enable Pin Current	$V_{\text{EN}} = 5.5 \text{ V}$	$I_{\text{EN}}$		0.3	2.0	$\mu\text{A}$	
Undervoltage Lock-out	$V_{\text{BIAS}}$ rising	UVLO		1.6		V	
Hysteresis	$V_{\text{BIAS}}$ falling			0.2		V	
Thermal Shutdown Temperature	Shutdown, temperature increasing	$T_{\text{SD}}$		+160		$^{\circ}\text{C}$	
	Reset, temperature decreasing			+140		$^{\circ}\text{C}$	
Operating Junction Temperature		$T_J$	-40		+125	$^{\circ}\text{C}$	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4.  $V_{\text{OUT}}$  nominal value is factory programmable.

5. Measured for devices with  $V_{\text{OUT(NOM)}} \geq 1.2\text{V}$ .

6.  $V_{\text{BIAS}} - V_{\text{OUT}}$  with  $V_{\text{OUT}} = V_{\text{OUT(NOM)}} - 0.1\text{V}$ . Measured for devices with  $V_{\text{OUT(NOM)}} \geq 1.4 \text{ V}$ .

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## APPLICATIONS INFORMATION



Figure 3. Typical Application: Low-Voltage Post-Regulator with ON/OFF functionality

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## TYPICAL CHARACTERISTICS

$V_{OUT(NOMINAL)} = 1.5\text{ V}$ ,  $V_{BIAS} = (V_{OUT} + 1.4\text{ V})$  or  $2.5\text{ V}$ , whichever is greater,  $V_{IN} = V_{OUT} + 0.5\text{ V}$ ,  $I_{OUT} = 1\text{ mA}$ ,  
 $V_{EN} = 1.1\text{ V}$ ,  $C_{OUT} = 2.2\text{ }\mu\text{F}$ ,  $T_J = 25^\circ\text{C}$  unless otherwise noted.



Figure 4.  $V_{IN}$  Dropout Voltage vs. Output Current



Figure 5.  $V_{BIAS}$  Dropout Voltage vs. Temperature



Figure 6. Output Voltage vs. Temperature

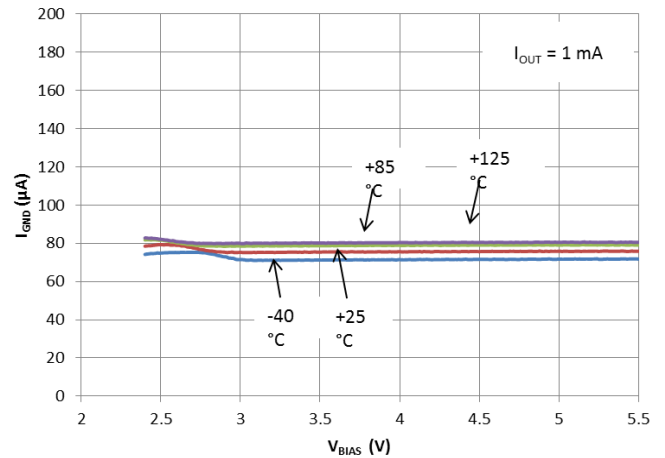


Figure 7. Bias Pin Current vs.  $V_{BIAS}$  Input Voltage

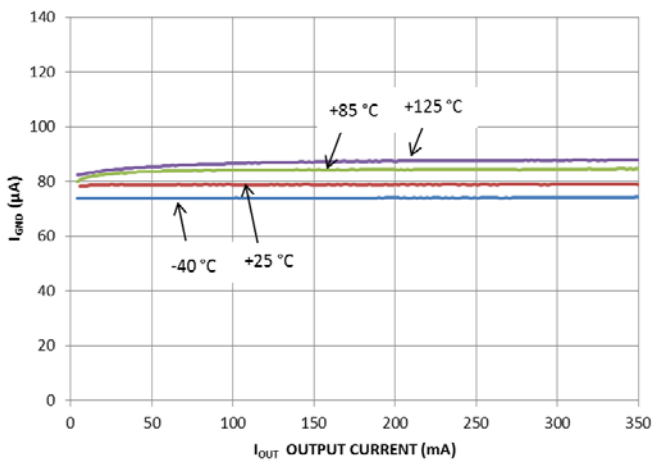


Figure 8. Bias Pin Current vs. Output Current

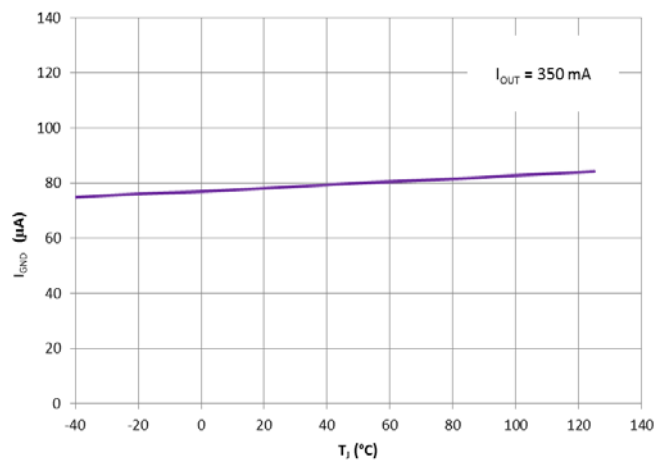


Figure 9. Bias Pin Current vs. Temperature

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## TYPICAL CHARACTERISTICS

$V_{OUT(NOMINAL)} = 1.5\text{ V}$ ,  $V_{BIAS} = (V_{OUT} + 1.4\text{ V})$  or  $2.5\text{ V}$ , whichever is greater,  $V_{IN} = V_{OUT} + 0.5\text{ V}$ ,  $I_{OUT} = 1\text{ mA}$ ,  
 $V_{EN} = 1.1\text{ V}$ ,  $C_{OUT} = 2.2\text{ }\mu\text{F}$ ,  $T_J = 25^\circ\text{C}$  unless otherwise noted.



Figure 10. Shutdown Current vs.  $V_{BIAS}$  Input Voltage



Figure 11. Current Limit vs.  $V_{BIAS}$  Input Voltage



Figure 12. Current Limit vs.  $V_{IN}$  Input Voltage



Figure 13.  $V_{IN}$  Power Supply Ripple Rejection vs. Frequency



Figure 14.  $V_{BIAS}$  Power Supply Ripple Rejection vs. Frequency

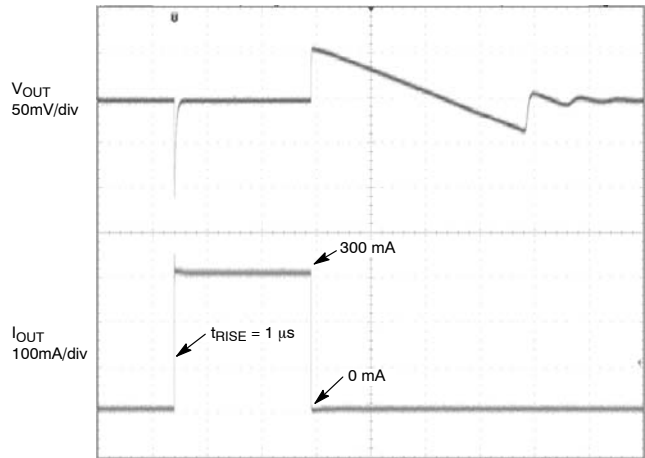


Figure 15. Load Transient Response

**APPLICATIONS INFORMATION**

The NCV8720 dual-rail very low dropout voltage regulator is using NMOS pass transistor for output voltage regulation from  $V_{IN}$  voltage. All the low current internal control circuitry is powered from the  $V_{BIAS}$  voltage.

The use of an NMOS pass transistor offers several advantages in applications. Unlike a PMOS topology devices, the output capacitor has reduced impact on loop stability.  $V_{IN}$  to  $V_{OUT}$  operating voltage difference can be very low compared with standard PMOS regulators in very low  $V_{IN}$  applications.

The NCV8720 offers built-in Soft-Start with monotonic  $V_{OUT}$  rise. The controlled voltage rising limits the inrush current.

The Enable (EN) input is equipped with internal hysteresis.

NCV8720 is a Fixed Voltage linear regulator.

**Dropout Voltage**

Because of two power supply inputs  $V_{IN}$  and  $V_{BIAS}$  and one  $V_{OUT}$  regulator output, there are two Dropout voltages specified.

The first, the  $V_{IN}$  Dropout voltage is the voltage difference ( $V_{IN} - V_{OUT}$ ) at which the regulator output no longer maintains regulation against further reductions in input voltage.  $V_{BIAS}$  is high enough, specific value is published in the Electrical Characteristics table.

The second,  $V_{BIAS}$  dropout voltage is the voltage difference ( $V_{BIAS} - V_{OUT}$ ) at which the regulator output no longer maintains regulation against further reductions in  $V_{BIAS}$  voltage.  $V_{IN}$  is high enough.

**Input and Output Capacitors**

The device is designed to be stable for ceramic output capacitors with Effective capacitance in the range from 2.2  $\mu$ F to 10  $\mu$ F. The device is also stable with multiple capacitors in parallel, having the total effective capacitance in the specified range.

In applications where no low input supplies impedance available (PCB inductance in  $V_{IN}$  and/or  $V_{BIAS}$  inputs as example), the recommended  $C_{IN} = 1 \mu$ F and  $C_{BIAS} = 0.1 \mu$ F or greater. Ceramic capacitors are recommended. For the best performance all the capacitors should be connected to

the NCV8720 respective pins directly in the device PCB copper layer, not through vias having not negligible impedance.

When using small ceramic capacitor, their capacitance is not constant but varies with applied DC biasing voltage, temperature and tolerance. The effective capacitance can be much lower than their nominal capacitance value, most importantly in negative temperatures and higher LDO output voltages. That is why the recommended Output capacitor capacitance value is specified as Effective value in the specific application conditions.

**Enable Operation**

The enable pin will turn the regulator on or off. The threshold limits are covered in the electrical characteristics table in this data sheet. If the enable function is not to be used then the pin should be connected to  $V_{IN}$  or  $V_{BIAS}$ . When enabled, the device consumes roughly 20  $\mu$ A from  $V_{in}$  supply per 1 V nominal output voltage. That is why using the enable / disable function in power saving applications is recommended.

**Current Limitation**

The internal Current Limitation circuitry allows the device to supply the full nominal current and surges but protects the device against Current Overload or Short.

**Thermal Protection**

Internal thermal shutdown (TSD) circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When TSD activated, the regulator output turns off. When cooling down under the low temperature threshold, device output is activated again. This TSD feature is provided to prevent failures from accidental overheating.

**Power Dissipation**

The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. For reliable operation junction temperature should be limited to +125°C.



# NCV8720

## ORDERING INFORMATION

Device	Nominal Output Voltage	Marking	Package	Shipping <sup>†</sup>
NCV8720BMT090TBG	0.90 V	LU	WDFN6 (Non-Wettable Flank) (Pb-Free)	3000 / Tape & Reel
NCV8720BMT100TBG	1.00 V	LA		
NCV8720BMT105TBG	1.05 V	LC		
NCV8720BMT110TBG	1.10 V	LD		
NCV8720BMT115TBG	1.15 V	LE		
NCV8720BMT120TBG	1.20 V	LF		
NCV8720BMT125TBG	1.25 V	LG		
NCV8720BMT130TBG	1.30 V	LH		
NCV8720BMT135TBG	1.35 V	LJ		
NCV8720BMT140TBG	1.40 V	LK		
NCV8720BMT145TBG	1.45 V	LL		
NCV8720BMT150TBG	1.50 V	LM		
NCV8720BMT160TBG	1.60 V	LN		
NCV8720BMT170TBG	1.70 V	LP		
NCV8720BMT180TBG	1.80 V	LQ		
NCV8720BMTW090TBG	0.90 V	KU	WDFN6 (Wettable Flank) (Pb-Free)	3000 / Tape & Reel
NCV8720BMTW110TBG	1.10 V	KD		
NCV8720BMTW120TBG	1.20 V	KF		
NCV8720BMTW130TBG	1.30 V	KH		
NCV8720BMTW150TBG	1.50 V	KM		
NCV8720BMTW180TBG	1.80 V	KQ		

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

To order other package and voltage variants, please contact your ON sales representative

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

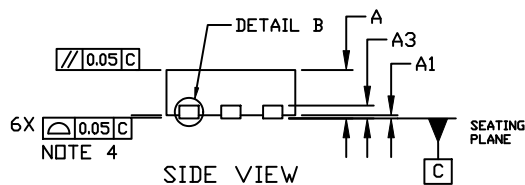


WDFN6 2x2, 0.65P  
CASE 511BR  
ISSUE C

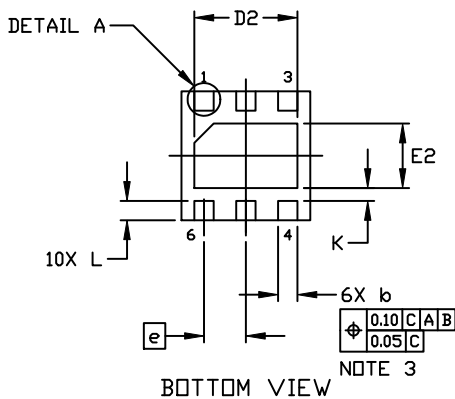
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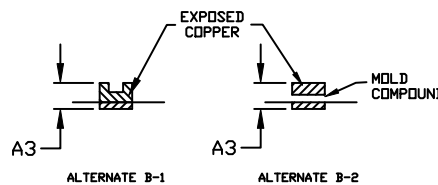
TOP VIEW



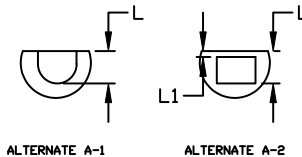
SIDE VIEW



BOTTOM VIEW

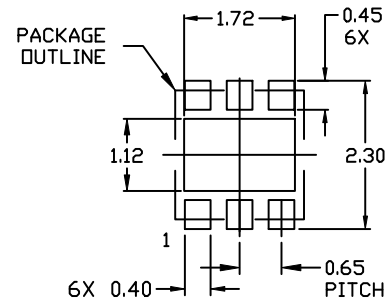


DETAIL B  
ALTERNATE CONSTRUCTION



DETAIL A  
ALTERNATE CONSTRUCTIONS

DIM	MILLIMETERS		
	MIN.	NDM.	MAX.
A	0.70	0.75	0.80
A1	0.00	---	0.05
A3	0.20 REF		
b	0.25	0.30	0.35
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
E	1.90	2.00	2.10
E2	0.90	1.00	1.10
e	0.65 BSC		
K	0.20 REF		
L	0.20	0.30	0.40
L1	---	---	0.15



RECOMMENDED  
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

### GENERIC MARKING DIAGRAM\*



XX = Specific Device Code  
M = Date Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "\*", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	WDFN6 2X2, 0.65P	PAGE 1 OF 1

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