ON Semiconductor

Test Procedure for the NCV8853GEVB Evaluation Board

Table 1. DEMONSTRATION BOARD TERMINALS

Pin Name	Function
VIN	Positive dc input voltage
VOUT	Regulated dc output voltage
GND	Common dc return
EN/SYNC	Enable input and external clock synchronization input
PG	Digital power good output
PG+	Power good pull-up. Use this pin only when pulling-up PG to an external voltage source.

Table 2. ABSOLUTE MAXIMUM RATINGS
(Voltages are with respect to GND)

Rating	Value	Units
Dc supply voltage (VIN)	-0.3 to 36	V
Dc supply voltage (EN/SYNC, PG, PG+)	-0.3 to 6.0	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. ELECTRICAL CHARACTERISTICS
(T_A = 25°C, 6.0 V ≤ V_{IN} ≤ 36 V, $V_{EN/SYNC}$ = 5.0 V, 0 ≤ I_{OUT} ≤ 2.0 A, unless otherwise specified)

Characteristics	Conditions	Typical Value	Units
Regulation			
Output Voltage		5.0	V
Voltage Accuracy		2	%
Line Regulation	I_{OUT} = 1.0 A	0.04	%
Load Regulation	V_{IN} = 13.2 V	0.12	%
Switching			
Switching Frequency		340	kHz
Soft-start Time		2.0	ms
SYNC Input Frequency Range		270 to 500	kHz
Current Limit			
Average Current Limit		3.33	A
Cycle-by-cycle Current Limit		5.0	A
Protections			
Input Undervoltage Lockout (UVLO)	V_{IN} decreasing	3.1	V
Thermal Shutdown	T_J rising	170	°C

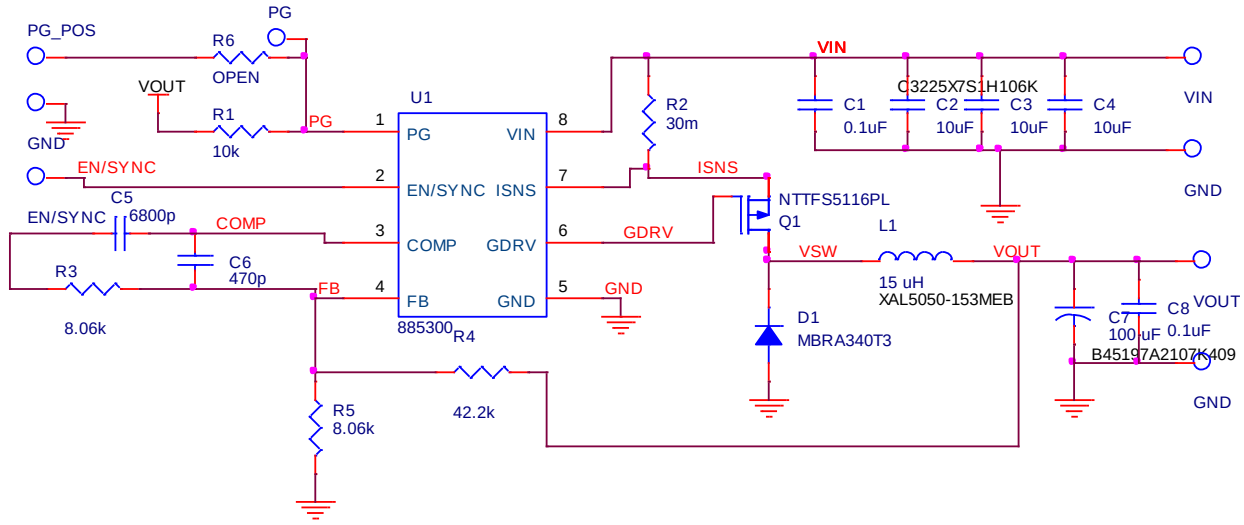

Figure 1: NCV885300EVB Board Schematic

Operational Guidelines

1. Connect a dc input voltage, within the 6.0 V to 36 V range, between VIN and GND
2. Connect a load between VOUT and GND
3. Connect a dc enable voltage, within the 2.0 V to 5.5 V range, between EN/SYNC and GND
4. Optionally, for external clock synchronization, connect a pulse source between EN/SYNC and GND. The high state level should be within the 2.0 V to 5.5 V range, and the low state level within the 0.0 V to 0.8 V range, with a frequency within the 170 kHz to 500 kHz range.
5. Make sure that the output maintains 1 A at 5 volts.
6. Using an oscilloscope, test the switching frequency of the GDRV pin (pin 6) of U1. It should be ≈340 kHz when internally synchronized.
7. If using the optional external clock synchronization from step 4 the switching frequency should match the input source frequency.
8. To check the Input Undervoltage Lockout (UVLO) slowly decrease the input down towards 0 V. The board should turn off at around 3.1 V.

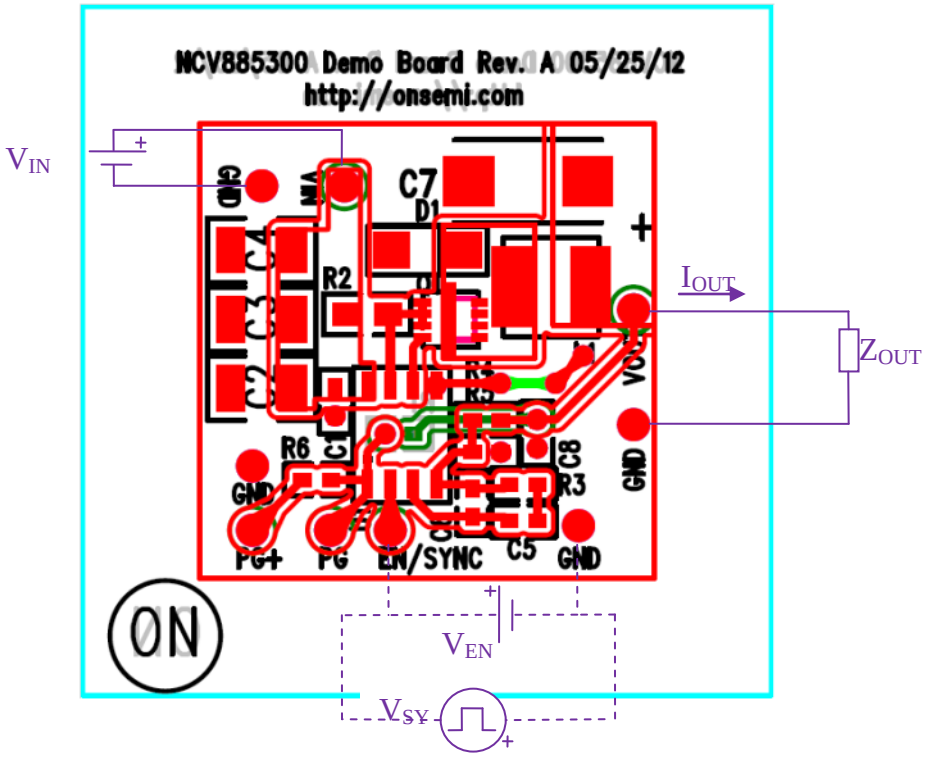

Figure 2: NCV885300EVB Board Connections

Power Good Operation

1. The Power Good pin (PG) allows you to digitally monitor the output voltage. When above 90% of the expected value, the PG signal is in a high state. By default, it is pulled high to VOUT through a 10kΩ resistor.
2. Optional: To pull the PG pin high using a signal other than VOUT, please make the following board modifications:
    a. Remove R1 from the board.
    b. Populate R6 with a 10 kΩ resistor.
    c. Connect the a voltage source between PG+ and GND (please see the Absolute Maximum Ratings table for more information).
    d. PG is now ready to digitally monitor VOUT using an external pull-up.