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Configurable 3.0 A PWM Step Down Converter

NCV91300

The NCV91300 is a synchronous PWM buck converter optimized to supply the different sub systems of automotive applications post regulation system from 2.0 V up to 5 V input. The device is able to deliver up to 3.0 A, with programmable output voltage from 0.6 V to 3.3 V. Operation at up to 2.15 MHz switching frequency allows the use of small components. Synchronous rectification and automatic PFM−PWM transitions improve overall solution efficiency. The NCV91300 is housed in low profile 3.0 x 3.0 mm QFNW−16 package.

Features

- Power Input Voltage Range from 1.9 V to 5.5 V
- Analog Input Voltage Range from 3.0 V to 5.5 V
- Power Capability: 3.0 A at T_A = 105°C ($R_{\theta JA}$ = 40°C/W)
- Programmable Output Voltage: 0.6 V to 3.3 V in 5 mV, 10 mV and 20 mV Steps
- Up to 2.15 MHz Switching Frequency with On Chip Oscillator
- Spread Spectrum or Sync Input Pin for EMI Optimization
- Uses 1.0 μH Inductor and at Least 20 μF Capacitors for Optimized Footprint and Solution Thickness
- PFM/PWM Operation for Optimum Efficiency
- Low 65 μA Quiescent Current
- I^2C Control Interface with Interrupt and Dynamic Voltage Scaling Support
- Enable Pin, Power Good / Interrupt Signaling
- Thermal Protections and Temperature Management
- 3.0 x 3.0 mm / 0.5 mm pitch QFN 16 package
- These are Pb−Free Devices

Typical Applications

- Automotive Point Of Load (POL)
- Automotive Telematics Clusters – Camera
- Automotive Infotainment – Instrumentation
- Automotive Advanced Driver−Assistance System (ADAS)
  - Front Camera – Rear View Camera
  - Surround View
  - Blind Spot Monitoring
  - Radar
- Automotive Space−Optimized systems

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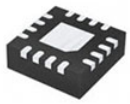
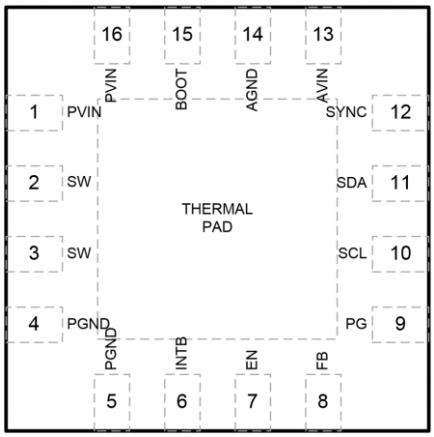


QFNW16 3x3, 0.5P
CASE 484AL

MARKING DIAGRAM

91300 = Specific Device Code
XX = 2 Fixed Characters Corresponding to the OPN
  • W3 = NCV91300MNWBTXG (V_{OUT} 1.1 V)
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

PIN ASSIGNMENT



(Top View)
16 Pins 0.50 mm pitch QFN

ORDERING INFORMATION

See detailed ordering and shipping information on page 37 of this data sheet.

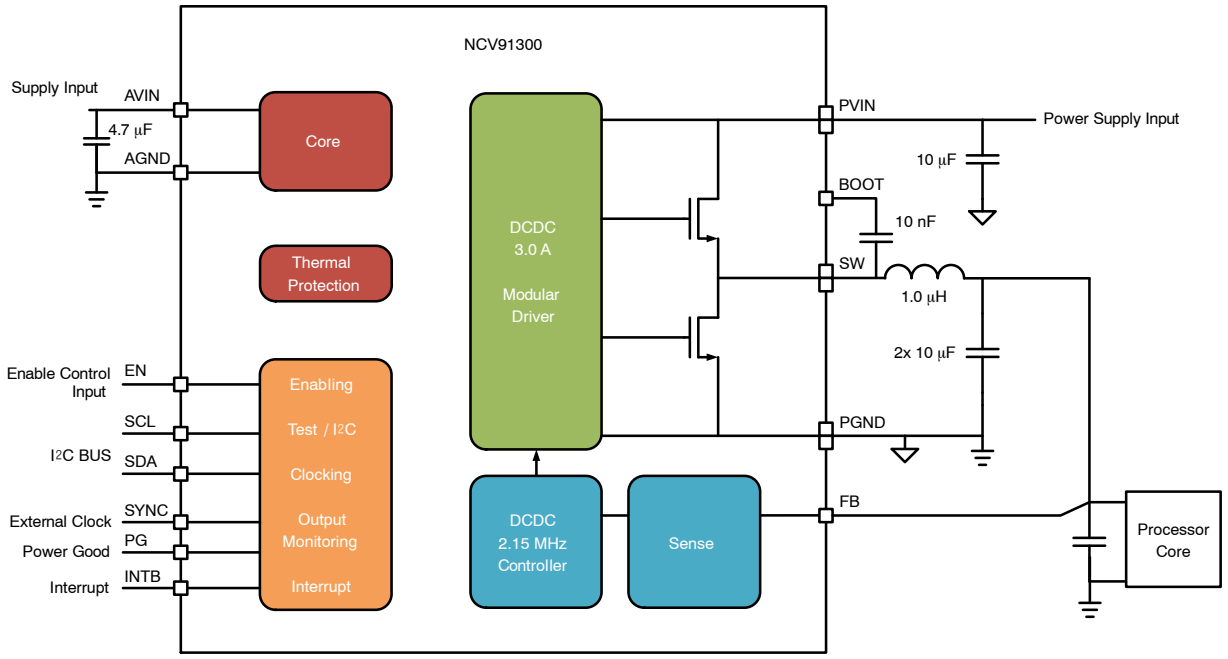


Figure 1. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

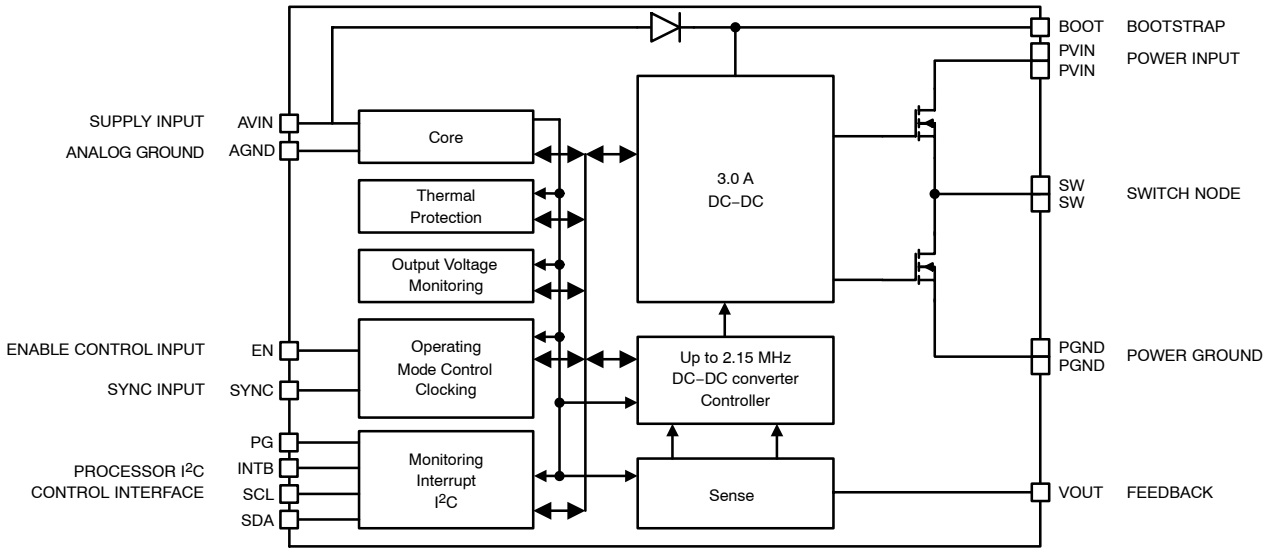


Figure 2. Simplified Block Diagram

PIN OUT DESCRIPTION

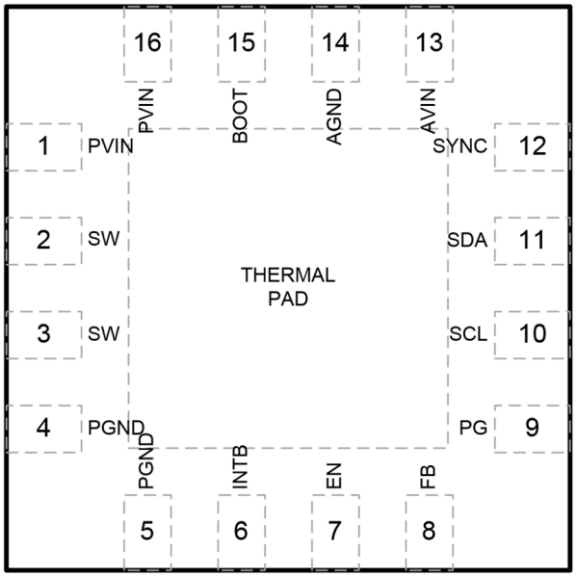


Figure 3. Pin Out (Top View)

PIN FUNCTION DESCRIPTION

Pin	Name	Type	Description
13	AVIN	Analog Input	*Analog Supply.* This pin is the device analog and digital supply. Could be connected directly to the VIN plane with a dedicated 4.7 μF decoupling ceramic capacitor
14	AGND	Analog Ground	*Analog Ground.* Analog and digital modules ground. Must be connected to the system ground.
6	INTB	Digital Output	*Interrupt* open drain output. Must be connected to the ground plane if not used.
7	EN	Digital Input	*Enable Control.* Active high will enable the part. There is an internal pull down resistor on this pin.
9	PG	Digital Output	*Power Good* open drain output. Must be connected to the ground plane if not used.
10	SCL	Digital Input	*I^2C interface Clock line.* There is an internal pull down resistor on this pin; could be connected to the ground plane if not used.
11	SDA	Digital Input Output	*I^2C interface Bi−directional Data line.* There is an internal pull down resistor on this pin; could be connected to the ground plane if not used.
12	SYNC	Digital Input	*External synchronization Input.*
1, 16	PVIN	Power Input	*Power Supply.* These pins must be decoupled to ground by a 10 μF ceramic capacitor. It should be placed as close as possible to these pins. All pins must be used with short and large enough connections.
2, 3	SW	Power Output	*Switch Node.* These pins drive power to the inductor. Typical application uses 1.0 μH inductor; refer to application section for more information. All pins must be used with short and large enough connections.
4, 5	PGND	Power Ground	*Switch Ground.* This pin is the power ground and carries the high switching current. High quality ground must be provided to prevent noise spikes. To avoid high−density current flow in a limited PCB track, a local ground plane that connects all PGND pins together is recommended. Analog and power grounds should only be connected together in one location with a trace.
8	FB	Analog Input	*Feedback Voltage Input.* Must be connected to the output capacitor positive terminal with a trace, not to a plane. This is the positive input to the error amplifier.
15	BOOT	Analog Input Output	*Bootstrap* pin for optimizing output stage R_{DSON}. Connect a 10 nF capacitor between BOOST and SW.
	THERMAL PAD	Analog Ground	*Exposed Thermal Pad.* Must be soldered to system Ground plane to achieve power dissipation performances. This pin is internally connected to the analog ground.

MAXIMUM RATINGS

Symbol	Parameter	Min	Typ	Max	Unit
V_{A-DC}	Analog Pins DC Non Switching: AVIN, PG, INTB, FB (Note 1)	−0.3	–	6.0	V
V_{P-DC}	Power Pin DC Non Switching: PVIN, SW (Note 1)	−0.3	–	6.0	V
V_{P-TR}	Between PVIN−PGND Pins, Transient 3 ns − 2.15 MHz (Note 1)	−0.3	–	7.5	V
V_{BOOT}	BOOT Pin: Between BOOT−SW (Note 1)	−0.3	–	V_{A-DC} + 0.3 ≤ 6.0	V
V_{I2C}	I^2C Pins: SDA, SCL	−0.3	–	V_{A-DC}	V
V_{DG}	Digital Pins Input Voltage: EN, SYNC	−0.3	–	V_{A-DC}	V
HBM	Human Body Model (HBM) ESD Rating (Note 2)	2000	–	–	V
CDMc	Charged Device Model (CDM) ESD Rating for Corner Pins (Not Applicable with this Package) (Note 2)	–	–	–	V
CDMo	Charged Device Model (CDM) ESD Rating for All Other Pins (Applicable to All Pin with this Package) (Note 2)	500	–	–	V
I_{LU}	Latch Up Current (Note 3)	–	100	–	mA
T_{STG}	Storage Temperature Range	−65	–	150	°C
T_{JMAX}	Junction Temperature Range	−40	–	T_{SD}	°C
MSL	Moisture Sensitivity (Note 4)	–	Level1	–	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. This device series contains ESD protection and passes the following ratings:
   Human Body Model (HBM) ±2 kV per ANSI/ESDA/JEDEC JS−001 standard.
   Charged Device Model (CDM) 750 V (corner pins) and 500 V (other pins) per AEC−Q100−011 standard.
3. Latch up Current per JEDEC JESD78 class II standard.
4. Moisture Sensitivity Level (MSL) 1: per IPC/JEDEC J−STD−020 standard.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
AV_{INR}	Analog Input Supply Range. Must Be Greater or Equal to PV_{INR}	3.0	5.0	5.5	V
PV_{INR}	Power Input Supply Range	1.9	3.3	5.5	V
T_{JR}	Junction Temperature Range (Note 6)	−40	25	+150	°C
L_{OUT}	Inductor for DC−DC Converter (Note 5)	0.67	1.0	1.3	μH
C_{OUT}	Output Capacitor for DC−DC Converter (Note 5)	12.8	20	150	μF
C_{BOOT}	Bootstrap Capacitor (Note 5)	6.4	10	15	nF
C_{AVIN}	Input Capacitor for Analog Supply (Note 5)	2.5	4.7	–	μF
C_{PVIN}	Input Capacitor for Power Supply (Note 5)	4.7	10	–	μF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Including de−ratings (Refer to the Application Information section of this document for further details)
6. The thermal shutdown set to 167°C (typical) avoids potential irreversible damage on the device due to power dissipation.

THERMAL INFORMATION

Symbol	Parameter	JEDEC JESD51−3 (Calculated)	Demo Board (Measured)	Unit
θ_{JA}	Thermal Resistance Junction to Ambient (Note 9)	75.3	37.9	°C/W
Ψ_{JCTOP}	Thermal Characterization Parameter Junction to Case Top (Note 7)	107	–	°C/W
Ψ_{JB}	Thermal Characterization Parameter Junction to Board. Measured on the AGND Footprint (Note 8)	12.6	–	°C/W
CC_{85}	Current Capability $T_A \le 85°C$ (Note 10)	–	>3.50	A
CC_{105}	Current Capability $T_A \le 105°C$ (Note 10)	–	>3.50	A
CC_{125}	Current Capability $T_A \le 125°C$ (Note 10)	–	3.40	A

7. Calculated with infinite heatsink affixed to case top without any board present.
8. Calculated with infinite heatsink affixed to case bottom without any board present.
9. The $R\theta_{JA}$ is dependent of the PCB heat dissipation. Refer to AND8215/D
10. The current capability (CC) is dependent by input voltage, maximum output current, pcb stack up and layout as well as external components selected. Filled with AVin = 5 V, PVin = 3.3 V, Vout = 1.1 V

ELECTRICAL CHARACTERISTICS (Refer to the Application Information section of this data sheet for more details.

Min and Max Limits apply for T_J range (T_{JR}), AVIN range (AV_{INR}), PVIN range (PV_{INR}) and default configuration, unless otherwise specified. Typical values are referenced to T_J = +25°C, AVIN = 5.0 V, PVIN = 3.3 V and default configuration, unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit
SUPPLY CURRENT: PINS AVIN – PVINx					
I_{Q-PWM}	Operating Quiescent Current in PWM Mode DC−DC Active in Forced PWM, No Load	–	7	–	mA
$I_{Q\ PFM}$	Operating Quiescent Current in PFM Mode} DC−DC Active in Auto Mode, No Load – Minimal Switching	–	65	–	μA
I_{SLEEP}	Product Sleep Mode Current EN High and DC−DC Off or EN Low and SLEEP_MODE Bit High VIN = 5.5 V – T_J = 105°C	–	20	–	μA
I_{OFF}	Product in Off Mode EN Low and SLEEP_MODE Bit Low VIN = 5.5 V – T_J = 105°C	–	3.0	–	μA
DC−DC CONVERTER					
I_{OUT00}	Load Current Range: Ipeak[1..0] = 00 (Note 11)	0	–	2.0	A
I_{OUT01}	Load Current Range: Ipeak[1..0] = 01 (Note 11)	0	–	2.5	A
I_{OUT10}	Load Current Range: Ipeak[1..0] = 10 (Note 11)	0	–	3.0	A
I_{OUT11}	Load Current Range: Ipeak[1..0] = 11 (Note 11)	0	–	3.5	A
ΔV_{OUT1}	Output Voltage DC Error PWM Mode, PVIN, AVIN Range, No Load	−1.5	–	1.5	%
ΔV_{OUT2}	Output Voltage DC Error PWM Mode, PVIN Range, AVIN Range, I_{OUT} up to I_{OUTxx}	−2	–	2	%
ΔV_{OUT3}	Output Voltage DC Error Auto Mode, PVIN Range, AVIN Range, I_{OUT} up to I_{OUTxx}	−3	–	2	%
T_{ONMIN1}	Minimum On Time (Measured at SW) in PWM Mode AVIN = 5.5 V – PVIN = 3.3 V	–	–	95	ns
T_{ONMIN2}	Minimum On Time (Measured at SW) in PWM Mode AVIN = 3.3 V – PVIN = 3.3 V	–	–	101	ns
F_{SW}	Switching Frequency (Internal Oscillator, No Spread Spectrum)	2.00	2.15	2.30	MHz
$F_{SPREAD00}$	Spread Spectrum: FSS[1..0] = 00 (No Spread)	–	0	–	%
$F_{SPREAD01}$	Spread Spectrum: FSS[1..0] = 01	−5	0	5	%
$F_{SPREAD10}$	Spread Spectrum: FSS[1..0] = 10	−10	0	10	%
$F_{SPREAD11}$	Spread Spectrum: FSS[1..0] = 11	−10	0	10	%

ELECTRICAL CHARACTERISTICS (Refer to the Application Information section of this data sheet for more details.
Min and Max Limits apply for T_J range (T_{JR}), AVIN range (AV_{INR}), PVIN range (PV_{INR}) and default configuration, unless otherwise specified.
Typical values are referenced to T_J = +25°C, AVIN = 5.0 V, PVIN = 3.3 V and default configuration, unless otherwise specified.) (continued)

Symbol	Parameter	Min	Typ	Max	Unit
DC−DC CONVERTER					
R_{ONHS}	High Side MOSFET On Resistance AVIN = 5.0 V	30	62	110	mΩ
R_{ONLS}	Low Side MOSFET On Resistance AVIN = 5.0 V	40	65	130	mΩ
R_{BOOT}	BOOT Charge Resistance	–	7.6	–	Ω
I_{PK00}	Peak Inductor Current Ipeak[1..0] = 00 (Note 11)	2.3	3.0	3.6	A
I_{PK01}	Peak Inductor Current Ipeak[1..0] = 01 (Note 11)	2.9	3.5	4.1	A
I_{PK10}	Peak Inductor Current Ipeak[1..0] = 10 (Note 11)	–	4.0	–	A
I_{PK11}	Peak Inductor Current Ipeak[1..0] = 11 (Note 11)	–	4.5	–	A
I_{PKN}	Negative Current Limit: Open Loop (Note 11)	–	1.3	–	A
DC_{LOAD}	Load Regulation: I_{OUTxx} Range, PWM Mode	–	5	–	mV
DC_{LINE}	Line Regulation: PVIN Range, AVIN Range, PWM Mode	–	5	–	mV
$AC_{LOAD1.5A}$	Transient Load Response: tr = tf = 1 μs, C_{OUT} = 4 x 10 μF Load Step 1.5 A	–	±32	–	mV
AC_{TRECOV}	Load/Line Transient Recovery Time Time Rail Takes to Come Back to Nominal V_{OUT} − 10 mV	–	40	–	μs
AC_{LINE}	Transient Line Response: t_r = t_f = 10 μs, Line Step 3.0 V / 3.6 V	–	±40	–	mV
t_{START}	Turn On Time: Time from EN Transitions from Low to High to 90% of Output Voltage, (DVS[1..0] = 00b), VOUT = 1.10 V	90	110	155	μs
$R_{DISDCDC}$	DC−DC Active Output Discharge: V_{OUT} = 1.10 V	–	8.5	27	Ω
EN PIN					
V_{ENIH}	High Input Voltage	1.10	–	–	V
V_{ENIL}	Low Input Voltage	–	–	0.4	V
T_{ENFTR}	Digital Input EN Filter: Rising and Falling DBN_Time = 01	0.5	–	4.5	μs
I_{ENPD}	EN Input Pull−Down, (Input Bias Current)	–	0.15	1.00	μA
INTB PIN					
V_{INTBL}	INTB Low Output Voltage: I_{INTB} = 5 mA	–	–	0.2	V
V_{INTBH}	INTB High Output Voltage: Open Drain	–	–	AV_{IN}	V
P_{INTBLK}	INTB Leakage Current: 3.3 V at INTB Pin when No Interrupt, T_J = 105°C	–	–	100	nA
PG PIN					
V_{PGF}	Power Good Threshold: Falling Edge as a Percentage of Nominal Output Voltage	86	90	94	%
V_{PGHYS}	Power Good Hysteresis	0	4	7	%
T_{RTF}	Power Good Reaction Time for DC−DC: Falling	–	2	–	μs
T_{RTR}	Power Good Reaction Time for DC−DC: Rising	3.5	11	14	μs
V_{PGL}	Power Good Low Output Voltage: I_{PG} = 5 mA	–	–	0.2	V
V_{PGH}	Power Good High Output Voltage: Open Drain	–	–	AV_{IN}	V
P_{PGLK}	Power Good Leakage Current: 3.3 V at PG Pin when Power Good Valid, T_J = 105 °C	–	–	100	nA

ELECTRICAL CHARACTERISTICS (Refer to the Application Information section of this data sheet for more details.
Min and Max Limits apply for T_J range (T_{JR}), AVIN range (AV_{INR}), PVIN range (PV_{INR}) and default configuration, unless otherwise specified.
Typical values are referenced to T_J = +25°C, AVIN = 5.0 V, PVIN = 3.3 V and default configuration, unless otherwise specified.) (continued)

Symbol	Parameter	Min	Typ	Max	Unit
SYNC PIN					
$SYNC_R$	Synchronization Frequency Range	1.90	2.15	2.4	MHz
$SYNC_{VIL}$	SYNC Low Input Voltage	–	–	0.4	V
$SYNC_{VIH}$	SYNC High Input Voltage	1.5	–	AV_{IN}	V
$SYNC_{DC}$	SYNC Clock Duty Cycle	40	–	60	%
I^2C BUS					
V_{I2CINT}	High Level at SCL/SDA Line	1.7	–	4.5	V
V_{I2CIL}	SCL, SDA Low Input Voltage (Note 12)	–	–	0.4	V
$V_{I2CIHSCL}$	SCL high Input Voltage (Note 12)	1.6	–	4.5	V
$V_{I2CIHSDA}$	SDA high Input Voltage (Note 12)	1.21	–	4.5	V
V_{I2COL}	SDA Low Output Voltage: I_{SINK} = 3 mA	–	–	0.4	V
F_{SCL}	I^2C Clock Frequency	0.4	–	3.4	MHz
TOTAL DEVICE					
V_{AUVLO}	AVIN Under Voltage Lockout: V_{AVIN} Falling	–	–	2.8	V
V_{AUVLOH}	AVIN Under Voltage Lockout Hysteresis: V_{AVIN} Rising	50	–	100	mV
$V_{AUVLORT}$	AVIN UVLO Reaction Time	–	3.5	–	μs
$V_{PVINUVP}$	PVIN Under Voltage Protection threshold: V_{PVIN} Falling	–	–	1.5	V
$V_{PVINUVPH}$	PVIN Under Voltage Protection hysteresis: V_{PVIN} Rising	50	–	200	mV
$V_{PVINOVPR}$	PVIN Overvoltage Protection: Rising Threshold	–	5.8	–	V
$V_{PVINOVPF}$	PVIN Overvoltage Protection: Falling Threshold	5.5	5.65	–	V
V_{PVINRT}	PVIN UVP and OVP Reaction Time	1	–	12	μs
T_{SD}	Thermal Shut Down Protection	–	168	–	°C
T_{WAR}	Warning Rising Edge	–	154	–	°C
T_{PWAR}	Pre – Warning Threshold: TPWTH[1..0] = 10	–	132	–	°C
T_{SDH}	Thermal Shut Down Hysteresis	–	24	–	°C
T_{WARH}	Thermal Warning Hysteresis	–	10	–	°C
T_{PWARH}	Thermal Pre–Warning Hysteresis	–	6	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

11. Junction temperature must be maintained below 150°C. Output load current capability depends on the application thermal capability.
12. Devices that use non–standard supply voltages, which do not conform to the intent I^2C bus system levels, must relate their input levels to the VDD voltage to which the pull–up resistors RP are connected.

TYPICAL OPERATING CHARACTERISTICS (A_{VIN} = 5.0 V, P_{VIN} = 3.3 V, T_A = +25°C

V_{OUT} = 1.10 V, I_{PEAK} = 3.5 A (Unless otherwise noted). L = 1.0 μH – C_{OUT} = 4 x 10 μF, C_{PVIN} = 10 μF, C_{AVIN} = 10 μF)

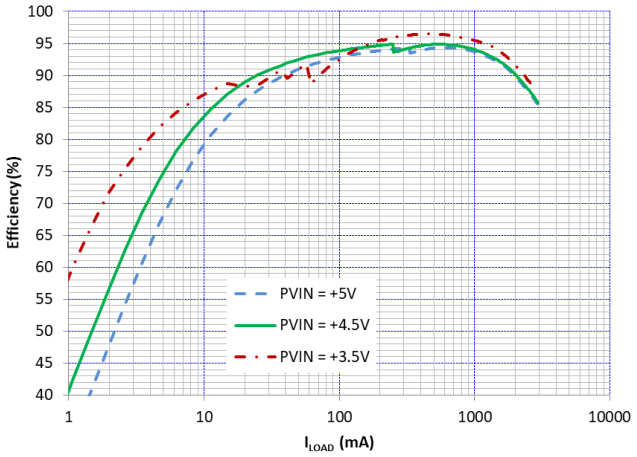


Figure 4. Efficiency vs. I_{LOAD} and P_{VIN}
V_{OUT} = 3.3 V, A_{VIN} = 5.0 V, Auto Mode
L = TDK TFM252012ALMA1R0MTAA

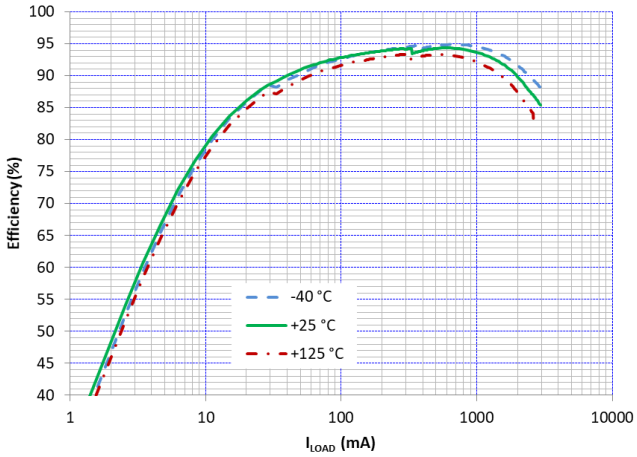


Figure 5. Efficiency vs. I_{LOAD} and Temperature
V_{OUT} = 3.3 V, A_{VIN} = P_{VIN} = 5.0 V, Auto Mode
L = TDK TFM252012ALMA1R0MTAA

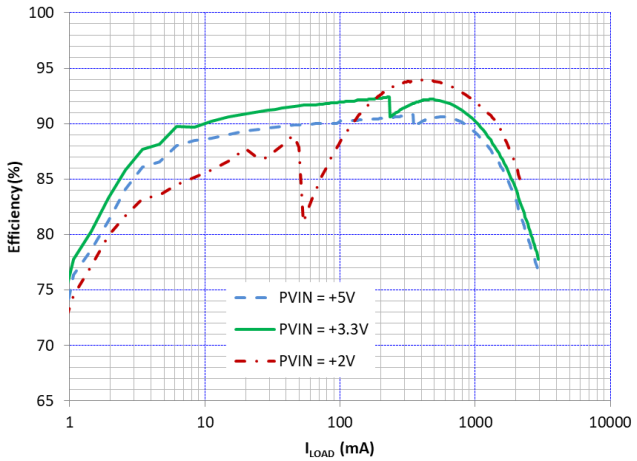


Figure 6. Efficiency vs. I_{LOAD} and P_{VIN}
V_{OUT} = 1.8 V, A_{VIN} = 5.0 V, Auto Mode
L = TDK TFM252012ALMA1R0MTAA

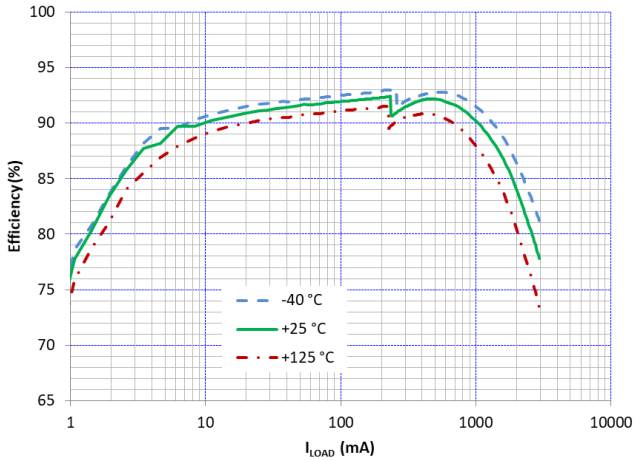


Figure 7. Efficiency vs. I_{LOAD} and Temperature
V_{OUT} = 1.8 V, A_{VIN} = 5.0 V, P_{VIN} = 3.3 V, Auto Mode
L = TDK TFM252012ALMA1R0MTAA

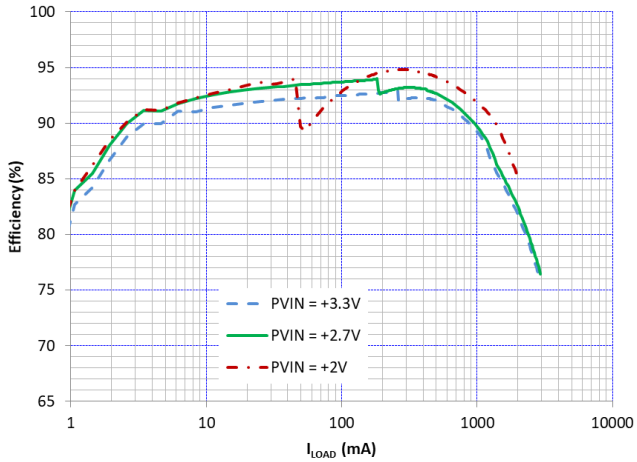


Figure 8. Efficiency vs. I_{LOAD} and P_{VIN}
V_{OUT} = 1.8 V, A_{VIN} = 3.3 V, Auto Mode
L = TDK TFM252012ALMA1R0MTAA

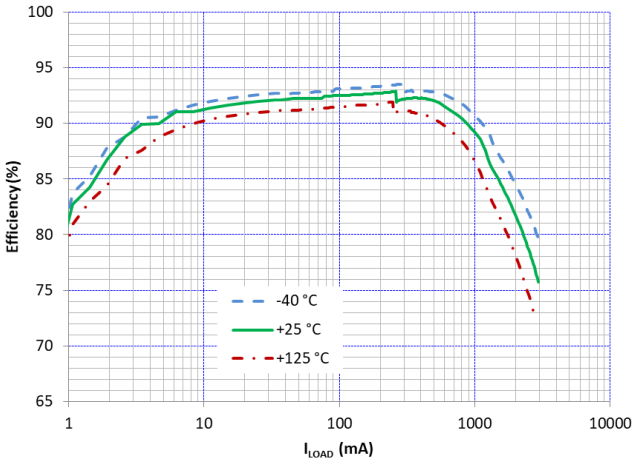


Figure 9. Efficiency vs. I_{LOAD} and Temperature
V_{OUT} = 1.8 V, A_{VIN} = 3.3 V, P_{VIN} = 3.3 V, Auto Mode
L = TDK TFM252012ALMA1R0MTAA

TYPICAL OPERATING CHARACTERISTICS (A_{VIN} = 5.0 V, P_{VIN} = 3.3 V, T_A = +25°C
V_{OUT} = 1.10 V, I_{PEAK} = 3.5 A (Unless otherwise noted). L = 1.0 μH – C_{OUT} = 4 x 10 μF, C_{PVIN} = 10 μF, C_{AVIN} = 10 μF) (continued)

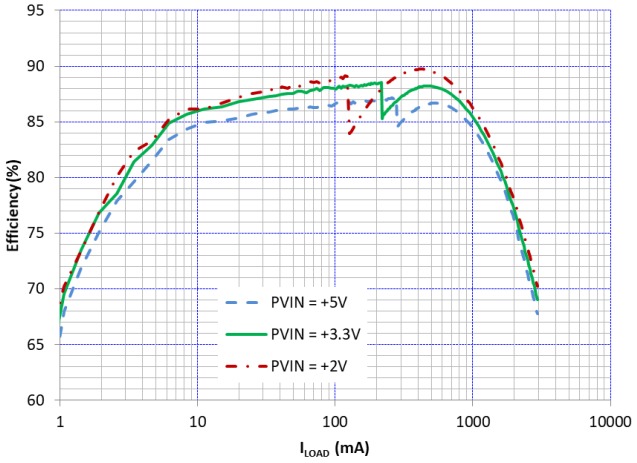


Figure 10. Efficiency vs. I_{LOAD} and P_{VIN}
V_{OUT} = 1.1 V, A_{VIN} = 5.0 V, Auto Mode
L = TDK TFM252012ALMA1R0MTAA

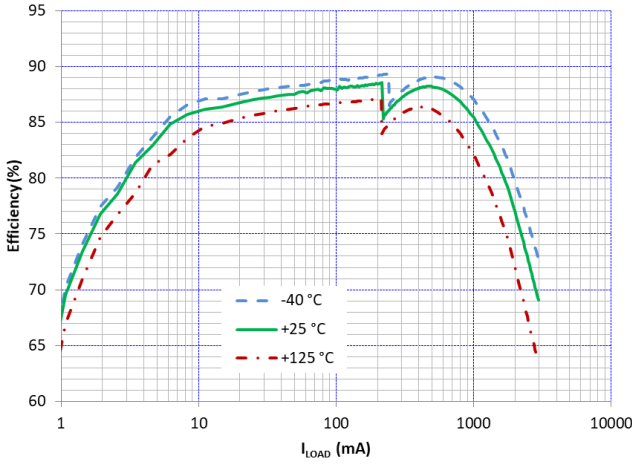


Figure 11. Efficiency vs. I_{LOAD} and Temperature
V_{OUT} = 1.1 V, A_{VIN} = 5.0 V, P_{VIN} = 3.3 V, Auto Mode
L = TDK TFM252012ALMA1R0MTAA

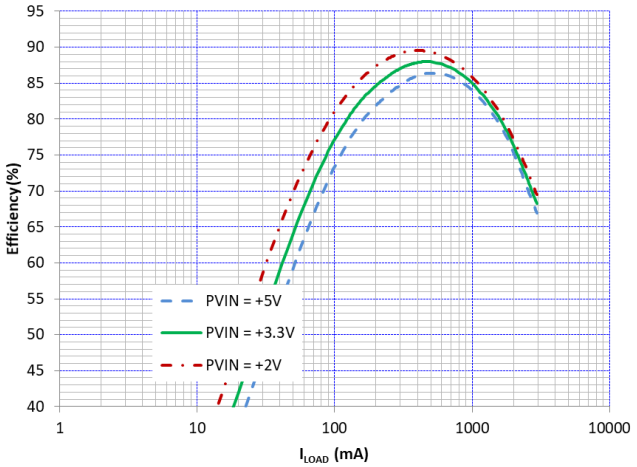


Figure 12. Efficiency vs. I_{LOAD} and P_{VIN}
V_{OUT} = 1.1 V, A_{VIN} = 5.0 V Forced PWM Mode
L = TDK TFM252012ALMA1R0MTAA

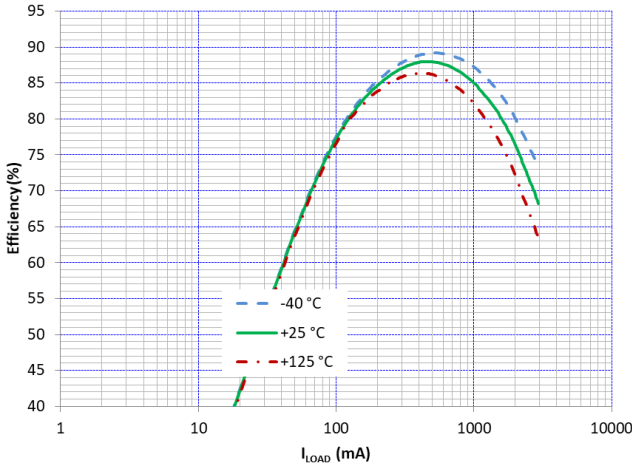


Figure 13. Efficiency vs. I_{LOAD} and Temperature
V_{OUT} = 1.1 V, A_{VIN} = 5.0 V, P_{VIN} = 3.3 V Forced PWM Mode
L = TDK TFM252012ALMA1R0MTAA

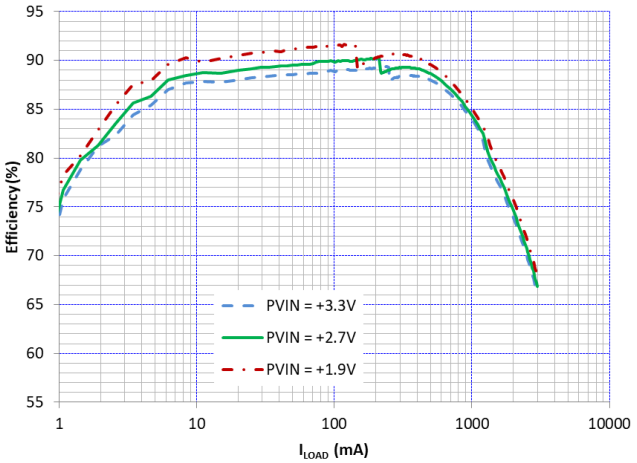


Figure 14. Efficiency vs. I_{LOAD} and P_{VIN}
V_{OUT} = 1.1 V, A_{VIN} = 3.3 V, Auto Mode
L = TDK TFM252012ALMA1R0MTAA

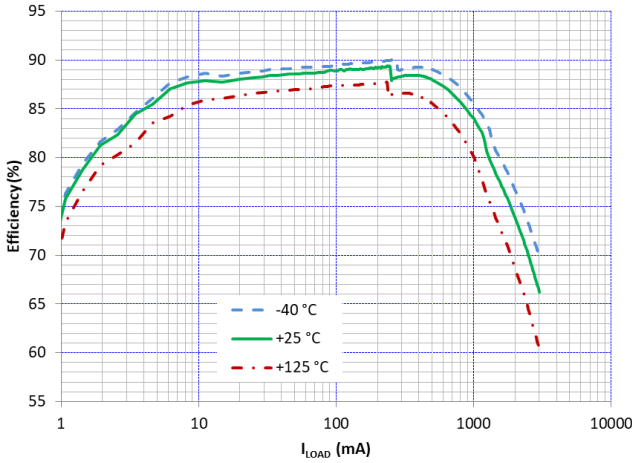


Figure 15. Efficiency vs. I_{LOAD} and V_{IN}
V_{OUT} = 1.1 V, A_{VIN} = 3.3 V, P_{VIN} = 3.3 V, Auto Mode
L = TDK TFM252012ALMA1R0MTAA

TYPICAL OPERATING CHARACTERISTICS (A_{VIN} = 5.0 V, P_{VIN} = 3.3 V, T_A = +25°C

V_{OUT} = 1.10 V, I_{PEAK} = 3.5 A (Unless otherwise noted). L = 1.0 μH – C_{OUT} = 4 x 10 μF, C_{PVIN} = 10 μF, C_{AVIN} = 10 μF) (continued)

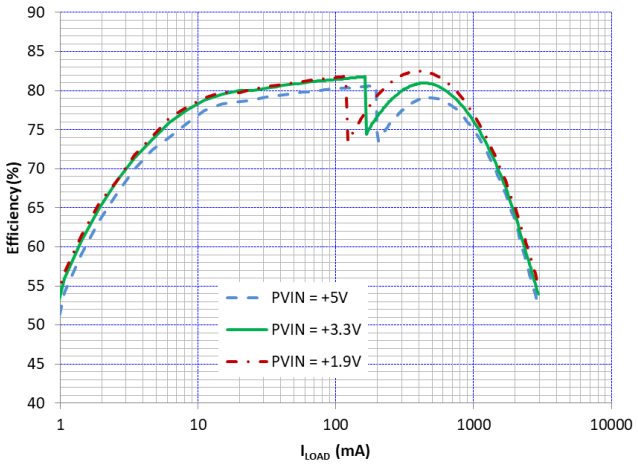


Figure 16. Efficiency vs. I_{LOAD} and P_{VIN}
V_{OUT} = 0.6 V, A_{VIN} = 5.0 V, Auto Mode
L = TDK TFM252012ALMA1R0MTAA

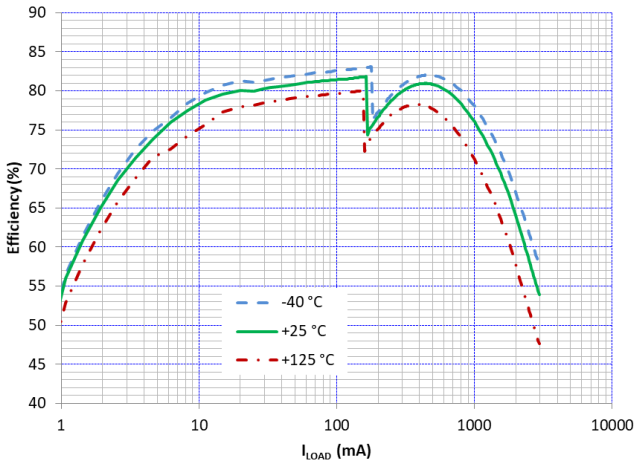


Figure 17. Efficiency vs. I_{LOAD} and Temperature
V_{OUT} = 0.6 V, A_{VIN} = 5.0 V, P_{VIN} = 3.3 V, Auto Mode
L = TDK TFM252012ALMA1R0MTAA

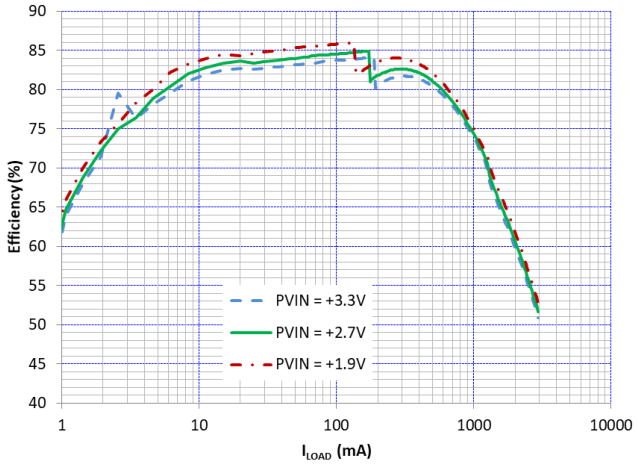


Figure 18. Efficiency vs. I_{LOAD} and P_{VIN}
V_{OUT} = 0.6 V, A_{VIN} = 3.3 V, Auto Mode
L = TDK TFM252012ALMA1R0MTAA

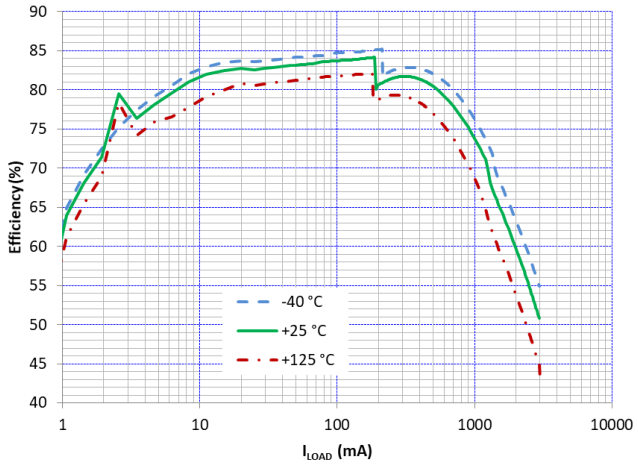


Figure 19. Efficiency vs. I_{LOAD} and Temperature
V_{OUT} = 0.6 V, A_{VIN} = 3.3 V, P_{VIN} = 3.3 V, Auto Mode
L = TDK TFM252012ALMA1R0MTAA

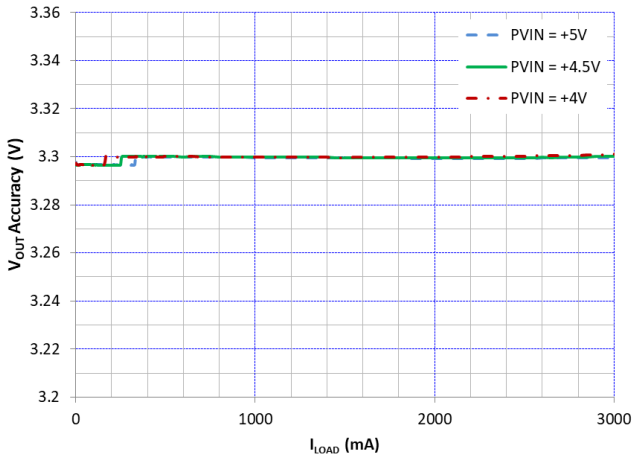


Figure 20. V_{OUT} Accuracy vs. I_{LOAD} and P_{VIN}
V_{OUT} = 3.3 V, A_{VIN} = 5.0 V, Auto Mode

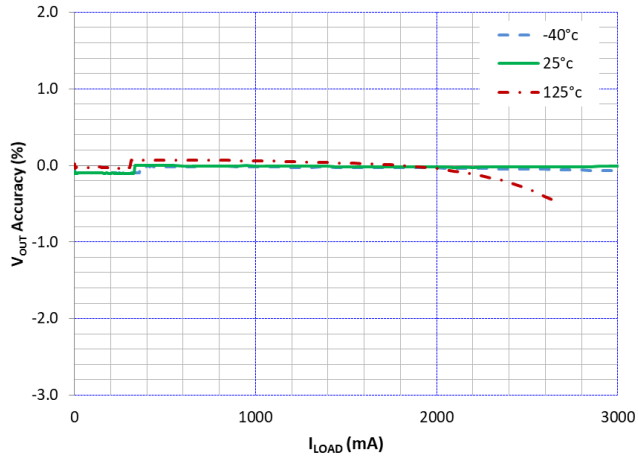


Figure 21. V_{OUT} Accuracy vs. I_{LOAD} and Temperature
V_{OUT} = 3.3 V; A_{VIN} = 5.0 V, P_{VIN} = 5.0 V, Auto Mode

TYPICAL OPERATING CHARACTERISTICS (A_{VIN} = 5.0 V, P_{VIN} = 3.3 V, T_A = +25°C

V_{OUT} = 1.10 V, I_{PEAK} = 3.5 A (Unless otherwise noted). L = 1.0 μH – C_{OUT} = 4 x 10 μF, C_{PVIN} = 10 μF, C_{AVIN} = 10 μF) (continued)

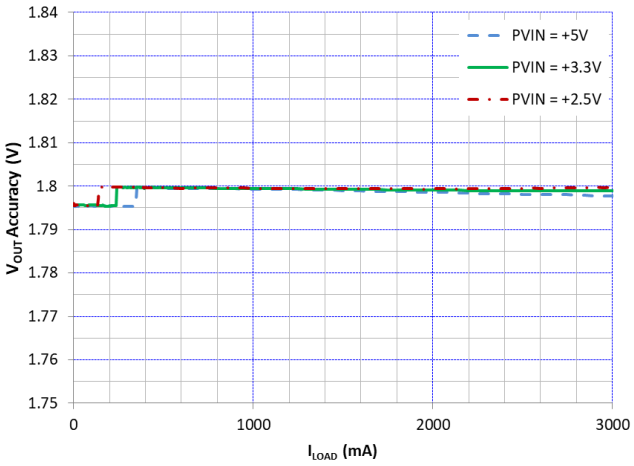


Figure 22. V_{OUT} Accuracy vs. I_{LOAD} and P_{VIN} V_{OUT} = 1.8 V, A_{VIN} = 5.0 V, Auto Mode

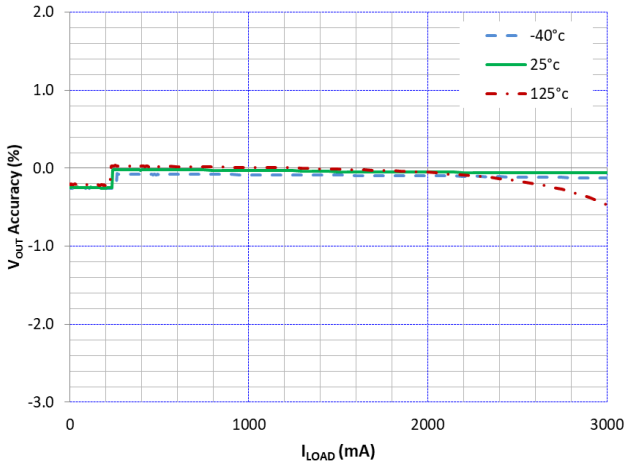


Figure 23. V_{OUT} Accuracy vs. I_{LOAD} and Temperature V_{OUT} = 1.8 V; A_{VIN} = 5.0 V, P_{VIN} = 3.3 V, Auto Mode

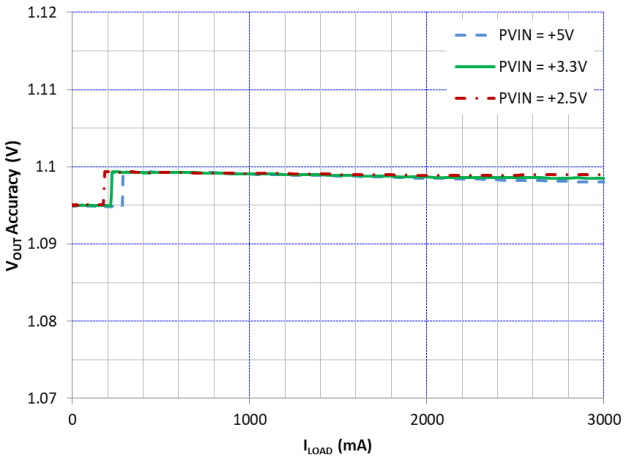


Figure 24. V_{OUT} Accuracy vs. I_{LOAD} and P_{VIN} V_{OUT} = 1.1 V, A_{VIN} = 5.0 V, Auto Mode

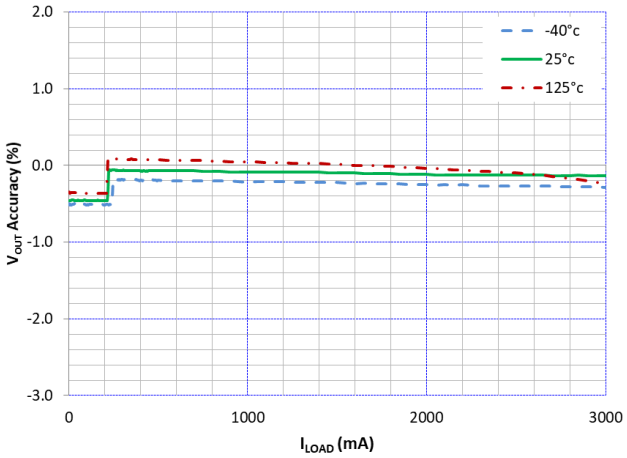


Figure 25. V_{OUT} Accuracy vs. I_{LOAD} and Temperature V_{OUT} = 1.1 V; A_{VIN} = 5.0 V, P_{VIN} = 3.3 V, Auto Mode

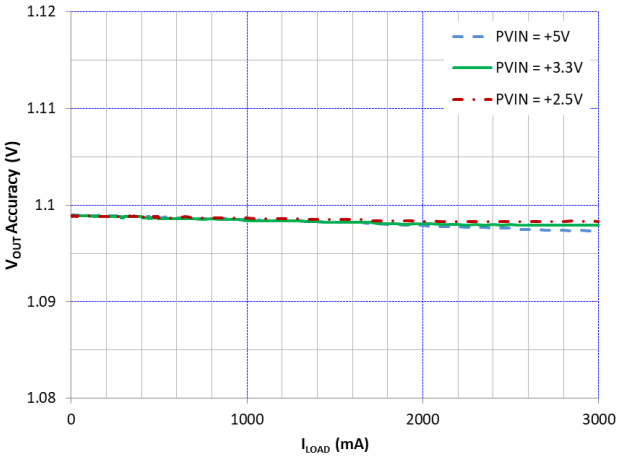


Figure 26. V_{OUT} Accuracy vs. I_{LOAD} and P_{VIN} V_{OUT} = 1.1 V, A_{VIN} = 5.0 V, Forced PWM Mode

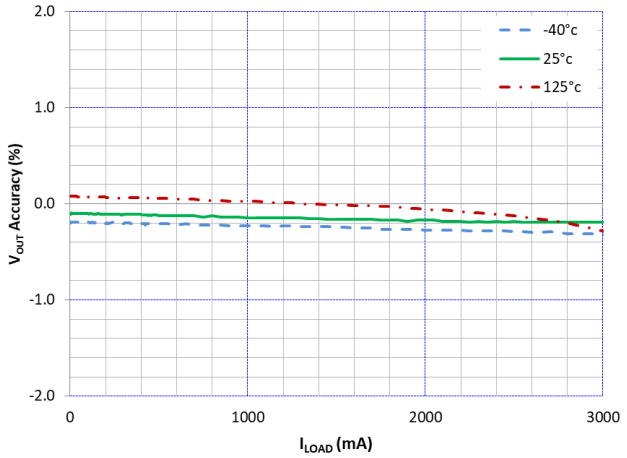


Figure 27. V_{OUT} Accuracy vs. I_{LOAD} and Temperature V_{OUT} = 1.1 V; A_{VIN} = 5.0 V, P_{VIN} = 3.3 V, Forced PWM Mode

TYPICAL OPERATING CHARACTERISTICS (A_{VIN} = 5.0 V, P_{VIN} = 3.3 V, T_A = +25°C
V_{OUT} = 1.10 V, I_{PEAK} = 3.5 A (Unless otherwise noted). L = 1.0 μH – C_{OUT} = 4 x 10 μF, C_{PVIN} = 10 μF, C_{AVIN} = 10 μF) (continued)

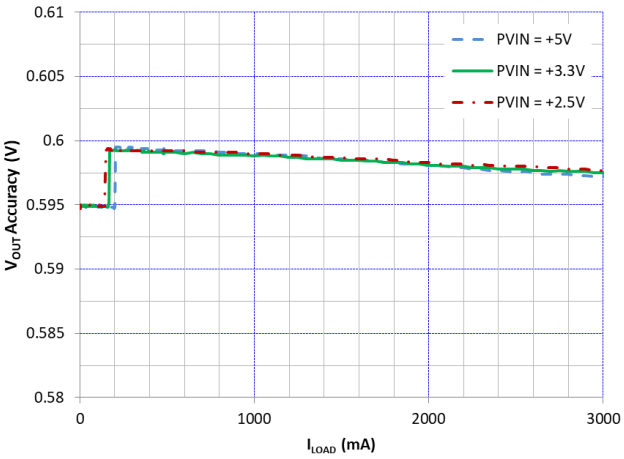


Figure 28. V_{OUT} Accuracy vs. I_{LOAD} and P_{VIN} V_{OUT} = 0.6 V, A_{VIN} = 5.0 V, Auto Mode

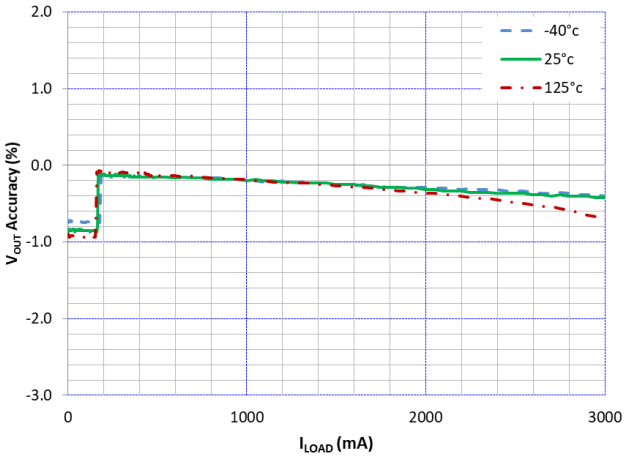


Figure 29. V_{OUT} Accuracy vs. I_{LOAD} and Temperature V_{OUT} = 0.6 V; A_{VIN} = 5.0 V, P_{VIN} = 3.3 V, Auto Mode

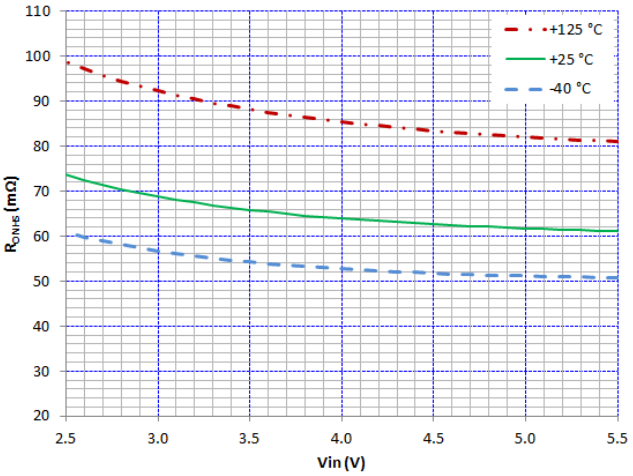


Figure 30. HSS R_{DSON} vs. V_{IN} and Temperature

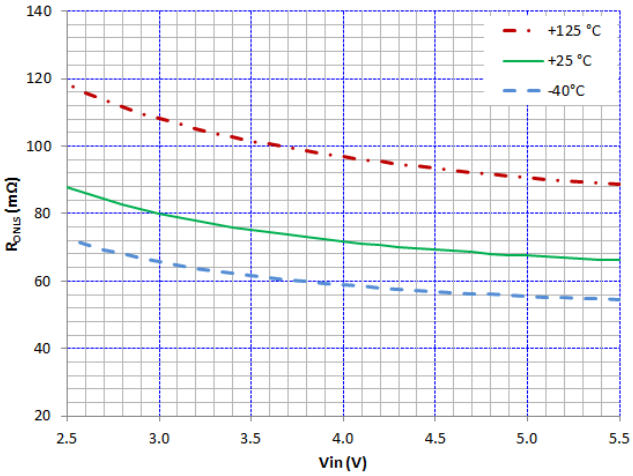


Figure 31. LSS R_{DSON} vs. V_{IN} and Temperature

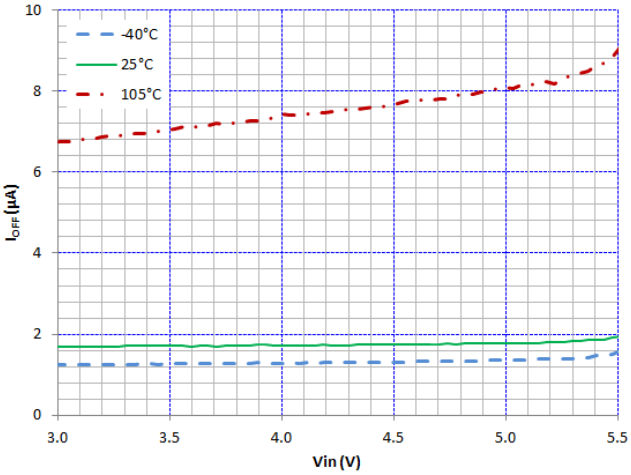


Figure 32. I_{OFF} vs. V_{IN} and Temperature

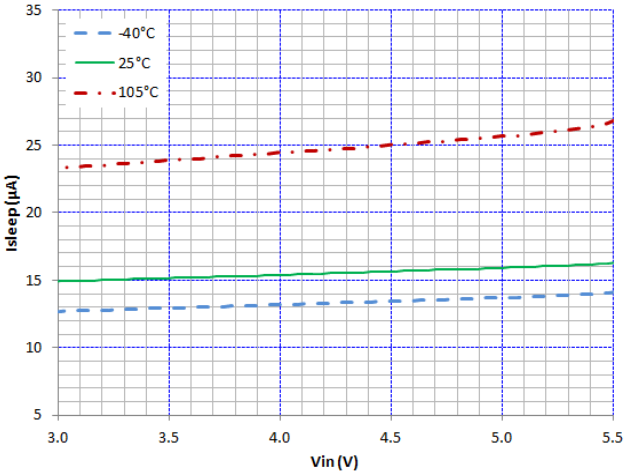


Figure 33. I_{SLEEP} vs. V_{IN} and Temperature

TYPICAL OPERATING CHARACTERISTICS (A_{VIN} = 5.0 V, P_{VIN} = 3.3 V, T_A = +25°C
V_{OUT} = 1.10 V, I_{PEAK} = 3.5 A (Unless otherwise noted). L = 1.0 μH – C_{OUT} = 4 x 10 μF, C_{PVIN} = 10 μF, C_{AVIN} = 10 μF) (continued)

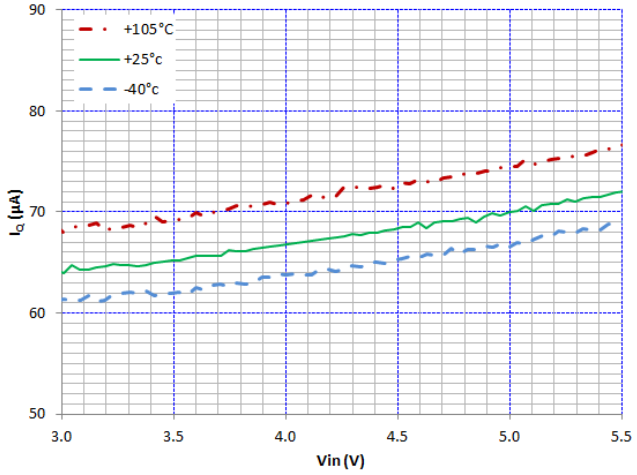


Figure 34. $I_{Q\ PFM}$ vs. V_{IN} and Temperature V_{OUT} = 1.1 V

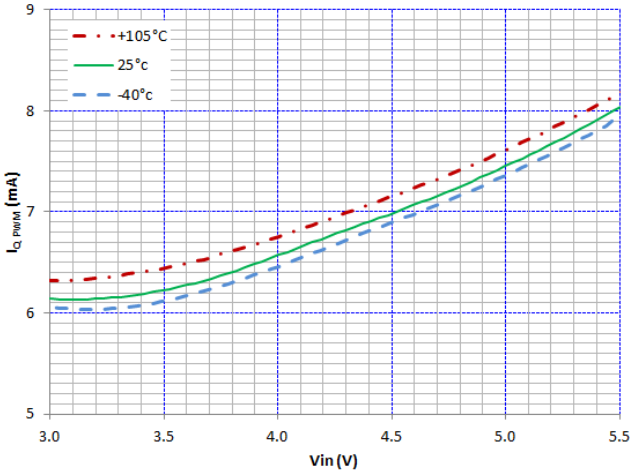


Figure 35. $I_{Q\ PWM}$ vs. V_{IN} and Temperature V_{OUT} = 1.1 V

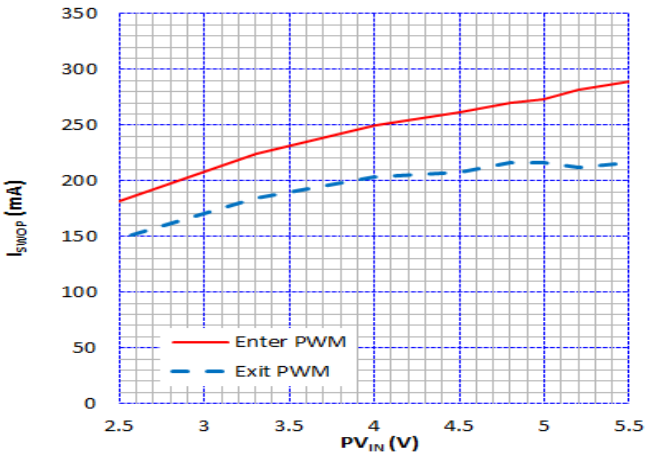


Figure 36. Switchover Point V_{OUT} = 1.1 V, A_{VIN} = 5.5 V

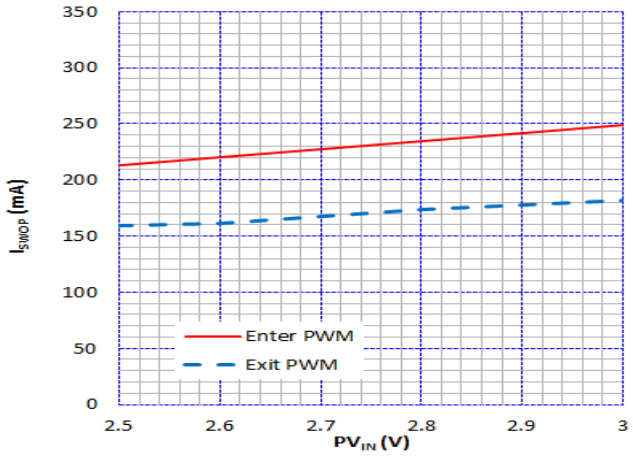


Figure 37. Switchover Point V_{OUT} = 1.1 V, A_{VIN} = 3.3 V

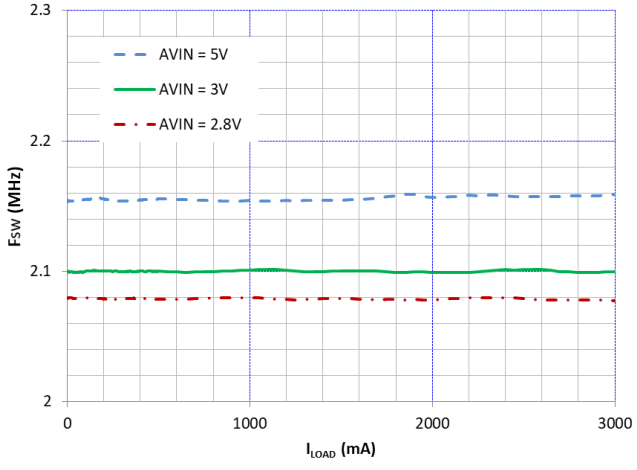


Figure 38. Switching Frequency vs. I_{LOAD} and A_{VIN} V_{OUT} = 1.1 V, P_{VIN} = 1.9 V

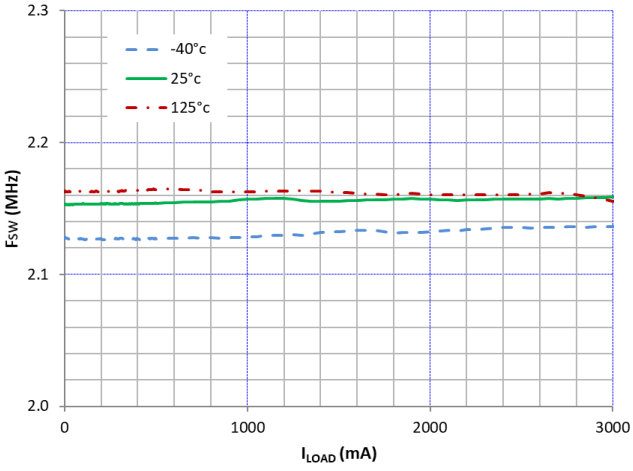


Figure 39. Switching Frequency vs I_{LOAD} and Temperature V_{OUT} = 1.1 V, P_{VIN} = 3.3 V

TYPICAL OPERATING CHARACTERISTICS (A_{VIN} = 5.0 V, P_{VIN} = 3.3 V, T_A = +25°C
V_{OUT} = 1.10 V, I_{PEAK} = 3.5 A (Unless otherwise noted). L = 1.0 μH – C_{OUT} = 4 x 10 μF, C_{PVIN} = 10 μF, C_{AVIN} = 10 μF) (continued)

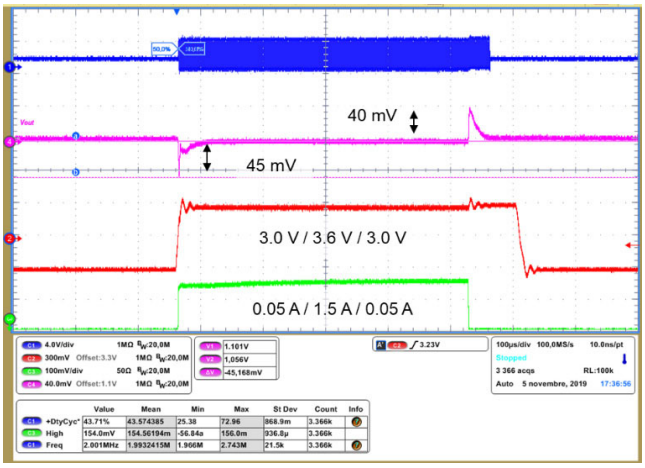


Figure 40. Transient Load 0.05 to 1.5 A Transient Line 3.0 – 3.6 V, Auto Mode, V_{OUT} = 1.1 V

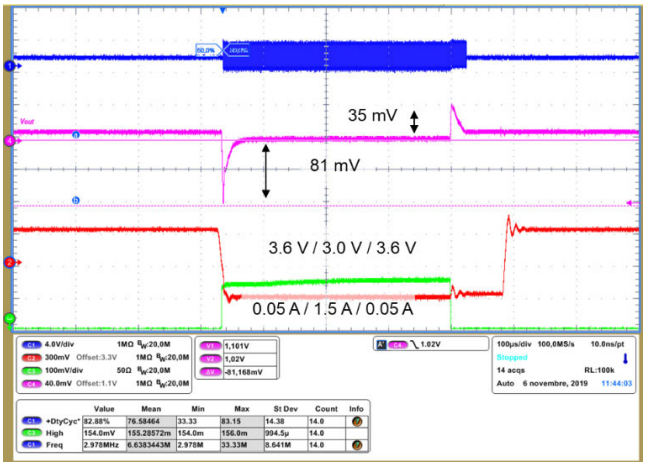


Figure 41. Transient Load 0.05 to 1.5 A Transient Line 3.0 – 3.6 V, Auto Mode, V_{OUT} = 1.1 V

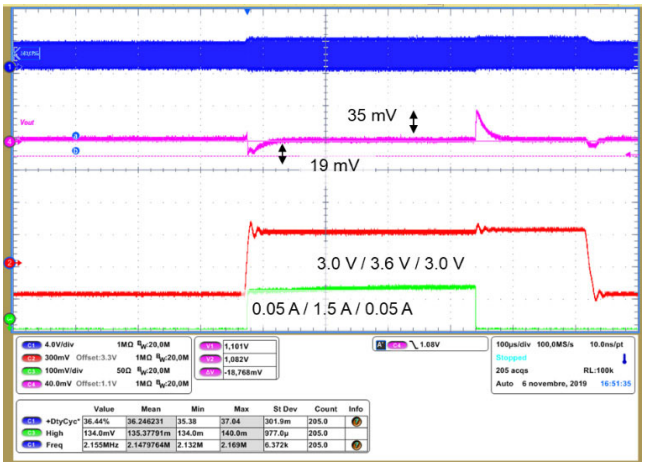


Figure 42. Transient Load 0.05 to 1.5 A Transient Line 3.0 – 3.6 V, Forced PWM Mode, V_{OUT} = 1.1 V

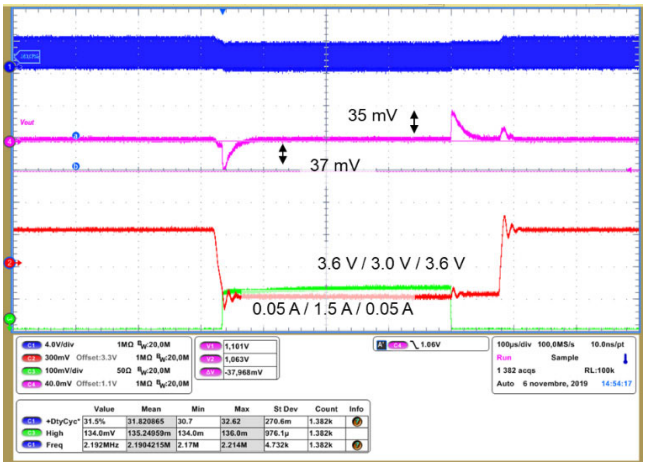


Figure 43. Transient Load 0.05 to 1.5 A Transient Line 3.0 – 3.6 V, Forced PWM Mode, V_{OUT} = 1.1 V

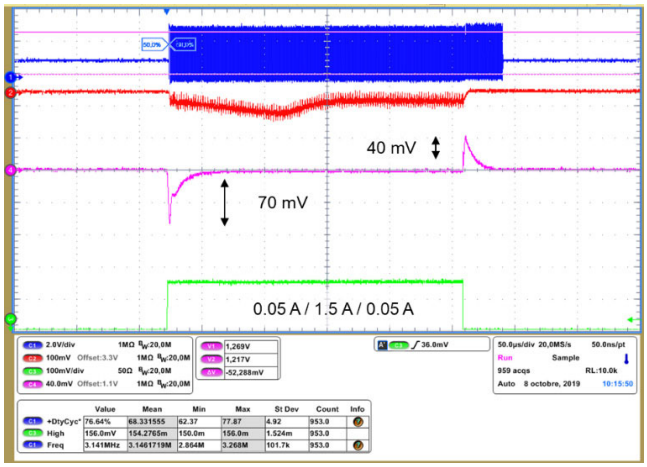


Figure 44. Transient Load 0.05 to 1.5 A Auto Mode, V_{OUT} = 1.1 V

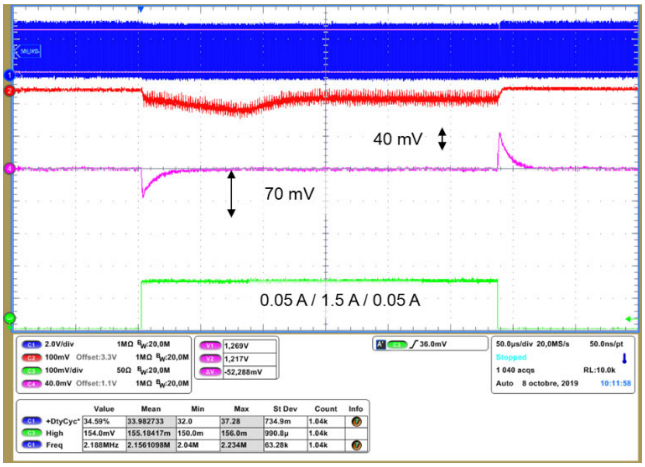


Figure 45. Transient Load 0.05 to 1.5 A Forced PWM Mode, V_{OUT} = 1.1 V

DETAILED OPERATING DESCRIPTION

Detailed Descriptions

The NCV91300 is a voltage mode standalone synchronous PWM DC−DC converter optimized to supply the different sub systems of automotive applications post regulation system from 2.0V up to 5V input. It can deliver up to 3.0 A at an I^2C selectable voltage ranging from 0.6 V to 3.30 V. The switching frequency up to 2.15 MHz allows the use of small output filter components. Power Good indicator and external synchronization are available. Synchronous rectification and automatic PFM−PWM transitions improve overall solution efficiency. Forced PWM mode is also configurable.

Operating modes, configuration, and output power can be easily selected by programming a set of registers using an I^2C compatible interface. Default I^2C settings are factory programmable.

The NCV91300 is in low profile 3.0 x 3.0 mm QFN−16 package

DC−DC Converter Operation

The converter integrates both high side and low side (synchronous) switches. Neither external transistors nor diodes are required for NCV91300 operation. Feedback and compensation network are also fully integrated.

It can operate in two different modes: PFM and PWM. The transition between modes can occur automatically or the switcher can be placed in forced PWM mode by I^2C programming (PWM bit of COMMAND register).

PWM (Pulse Width Modulation) Operating Mode

In medium and high load conditions, NCV91300 operates in PWM mode from the internal (oscillator) or external (SYNC) clock. In this mode, the inductor current is in CCM (Continuous Conduction Mode) and the voltage is regulated by PWM. The internal Low Side switch operates as synchronous rectifier and is driven complementary to the High Side switch.

PFM (Pulse Frequency Modulation) Operating Mode

In order to save power and improve efficiency at low loads, the NCV91300 operates in PFM mode when the inductor current drops into DCM (Discontinuous Conduction Mode). The High Side switch on−time is kept constant and the switching frequency becomes proportional to the loading current. As it does in PWM mode, the internal Low Side switch operates as a synchronous rectifier after each High Side switch on−pulse until there is no longer current in the coil.

When the load increases and the current in the inductor become continuous again, the controller automatically turns back to PWM mode.

Forced PWM

The PWM bit of the COMMAND register forces the NCV91300 to only use the PWM mode, meaning the transition to the PFM mode is no more allowed. This is generally used when a fixed switching frequency is mandatory, knowing that current consumption is degraded.

Output Voltage

The output voltage is internally set by an integrated resistor bridge and no extra components are needed to set it. Writing in the Vout [7..0] bits of the PROG register changes the output voltage by:

- 5 mV steps when V_{OUT} is between 0.6 V and 1.0 V,
- 10 mV steps when V_{OUT} is between 1.0 V and 2.0 V
- 20 mV steps when VOUT is between 2.0 V and 3.3 V

Output Stage

NCV91300 integrates both the High Side and the Low Side NMOS switches, and associated bootstrap regulator to provide the right gate drive voltage.

Inductor Peak Current Protection, Negative Current Protection and Short Circuit Protection

During normal operation, peak current limitation protection monitors and limits the inductor current by checking the current in the High Side switch. When this current exceeds the Ipeak threshold, the High Side switch is immediately opened.

For protecting against excessive load or short circuit to ground, the DC−DC is powered down and the ISHORT interrupt is flagged when 2 Ipeak are counted when in power fail (so when PG is low). The REARM bit (LIMCONF register) value defines the re−start:

- If REARM = 0, then NCV91300 does not re−start automatically, an EN pin toggle is required.
- If REARM = 1, NCV91300 re−starts automatically after 2 ms with register values set prior the fault condition.

This High Side switch current limitation is particularly useful to protect the inductor. The peak current can be set by writing IPEAK[1..0] bits in the LIMCONF register.

Table 1. Ipeak VALUES

IPEAK[1..0]	Inductor Peak Current (A)
00	3.0 – for 2.0 output current
01	3.5 – for 2.5 output current
10	4.0 – for 3.0 output current
11	4.5 – for 3.5 output current

In addition, to protect the Low Side switch, the negative current protection (Ipeakn) limits potential excessive current from output (for example, when fault condition causes the output voltage to be higher than the nominal output voltage).For protecting against excessive short to high voltage, the number of consecutive Ipeakn is counted. When the counter reaches 8, the DC−DC is powered down and the ISHORT interrupt is flagged, then

- If REARM = 0, then NCV91300 does not re−start automatically, an EN pin toggle is required.
- If REARM = 1, NCV91300 re−starts automatically after 2 ms with register values set prior the fault condition.

Active Output Discharge

To make sure that no residual voltage remains on the output of the DC−DC when disabled, an active discharge path can ground the NCV91300 output voltage. For maximum flexibility, this feature can be disabled or enabled with the DISCHG bit in the COMMAND register. Note that whatever the state of the DISCHG bit, the discharge path is enabled during the Wake−Up time.

AV_{IN} Under Voltage Lock Out (UVLO)

NCV91300 Analog core (AV_{IN}) does not operate for voltages below the Under Voltage Lock Out (AUVLO) threshold. Below this UVLO threshold, all internal circuitries (both analog and digital) are in reset. To avoid erratic on / off behavior, a maximum 100 mV hysteresis is implemented. Restart is guaranteed at 2.9 V when the supply voltage is recovering or rising. When in OFF mode, to reduce quiescent current, the UVLO threshold is relaxed.

PV_{IN} Input Power Voltage Protection

To protect the output stages, PV_{IN} valid range is defined by $V_{PVINOVPR}$ and $V_{PVINUVP}$.

When PV_{IN} exceeds $V_{PVINOVPR}$ (5.8 V), the IC stops switching to protect the circuit from internal spikes above 7.5 V. An internal filter prevents the circuit from shutting down due to noise spikes.

When PV_{IN} fails below $V_{PVINUVP}$, the output stage is also stopped to prevent any cross conduction.

To guaranty a smooth output voltage come back when the PVIN is recovering, a FPUS is initiated.

Enabling

Under proper supply conditions, the EN pin controls NCV91300 start up. The EN pin Low to High transition starts the power up sequencer.

If EN is made low, the DC−DC converter is turned off and device enters in SLEEP mode when the SLEEP_MODE bit is high, or in OFF mode when SLEEP_MODE bit is low.

Table 2. MODE OF OPERATION TABLE

EN	Sleep_Mode	ENABLE	Product Mode
Low	0	x	OFF
Low	1	x	SLEEP
High	x	0	SLEEP
High	x	1	ON

When the EN pin is set to a high level, the DC−DC converter can be enabled / disabled by writing the ENABLE bit of the COMMAND register.

Table 3. MODE OF OPERATION TABLE

EN	ENABLE	DC−DC
Low	x	Disabled
High	0	Disabled
High	1	Enabled

Power Up Sequence (PUS)

In order to power up the circuit, the input voltage AVIN has to rise above the AUVLO threshold. This triggers the internal core circuitry power up (=> “Wake Up Time” including “Bias Time”). This delay is internal and cannot be bypassed. EN pin transition within this delay corresponds to the “Initial power up sequence” (IPUS)

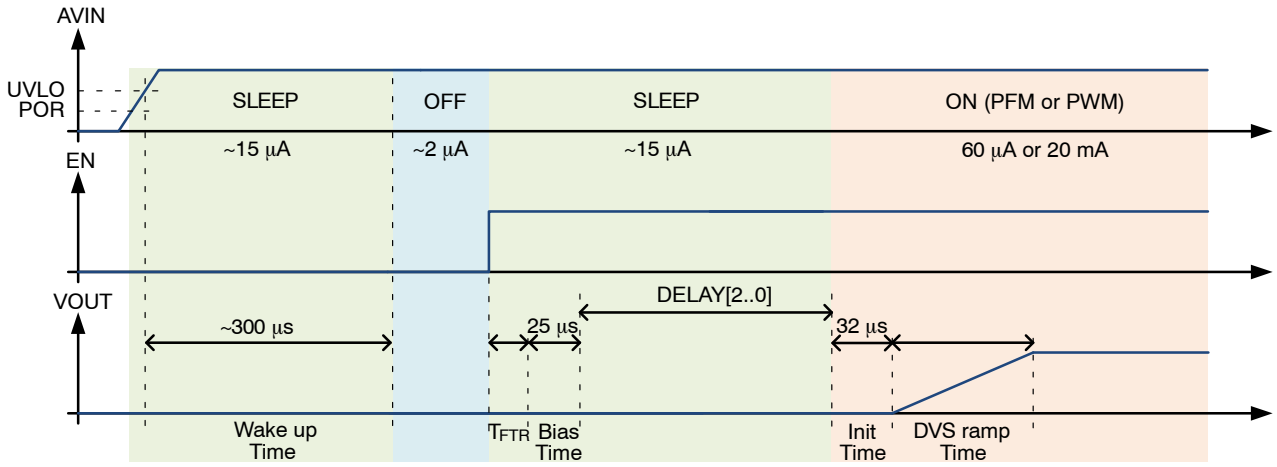


Figure 46. Power Up Sequence

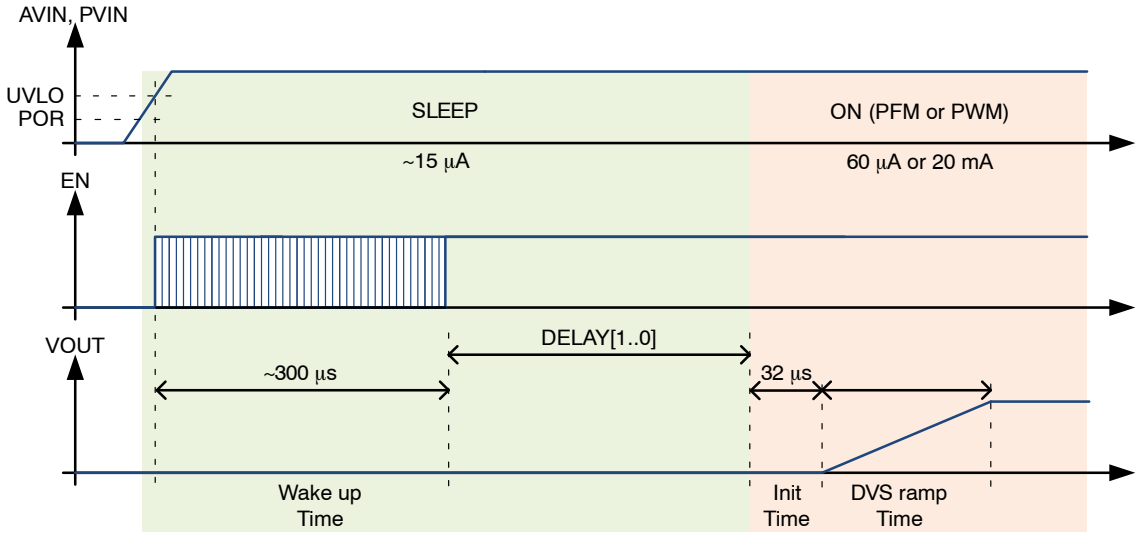


Figure 47. Initial Power Up Sequence

In addition, a programmable delay will take place between the Wake Up Time and the Init time: The DELAY[1..0] bits of the TIME register will set this programmable delay with a 2 ms resolution. Taking default delay of 0 ms, the NCV91300 IPUS takes roughly 332 μs, and the DC−DC converter output voltage will be ready within 385 μs.

NOTE: During the Wake Up time, the I^2C interface is not active. Any I^2C request to the IC during this time period will result in a NACK reply.

Normal, Quick and Fast Power Up Sequence (PUS)

3 different power up sequences are available depending on the mode and the trigger:

- Enabling the part by setting the EN pin from Off Mode will result in “Normal power up sequence” (NPUS, with DELAY[1..0]).

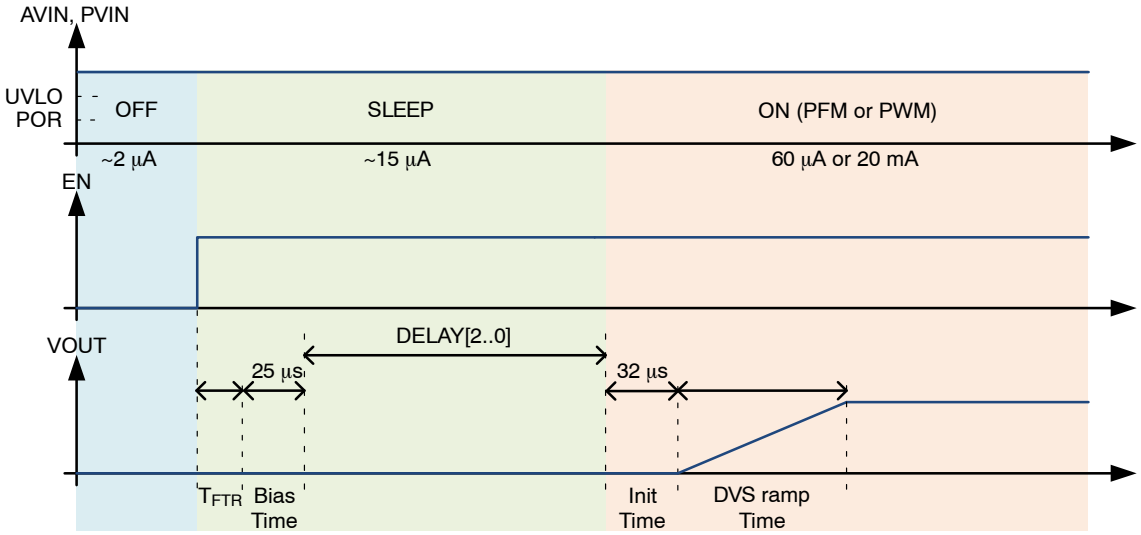


Figure 48. Normal Power Up Sequence

- Enabling the part by setting the EN pin from SLEEP Mode will result in “Quick power up sequence” (QPUS, with DELAY[1..0]).

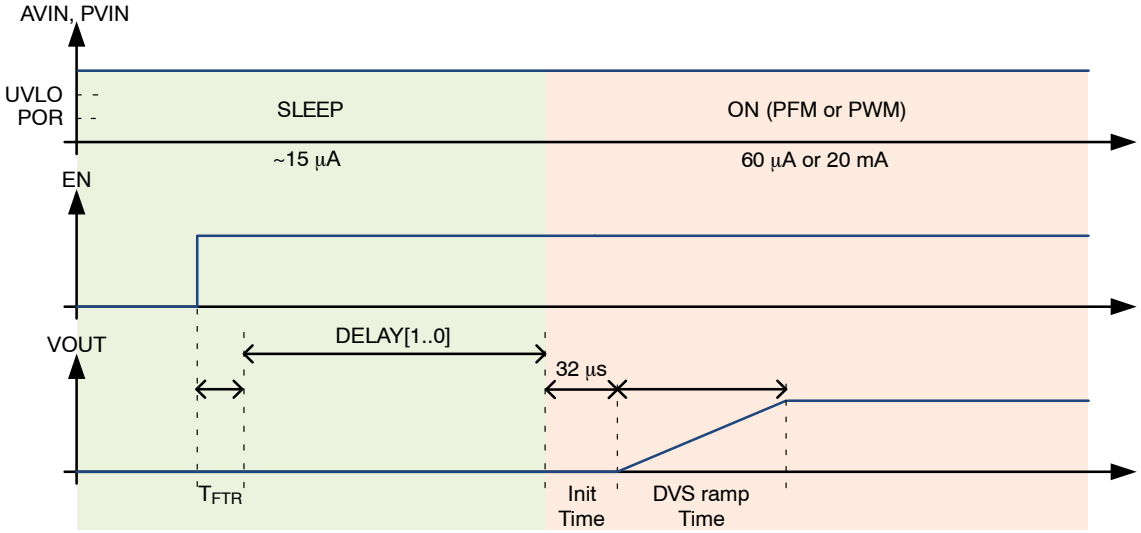


Figure 49. Quick Power Up Sequence

- Enabling the DC−DC converter by setting the ENABLE bit will results in “Fast power up sequence” (FPUS, without DELAY[1..0]).

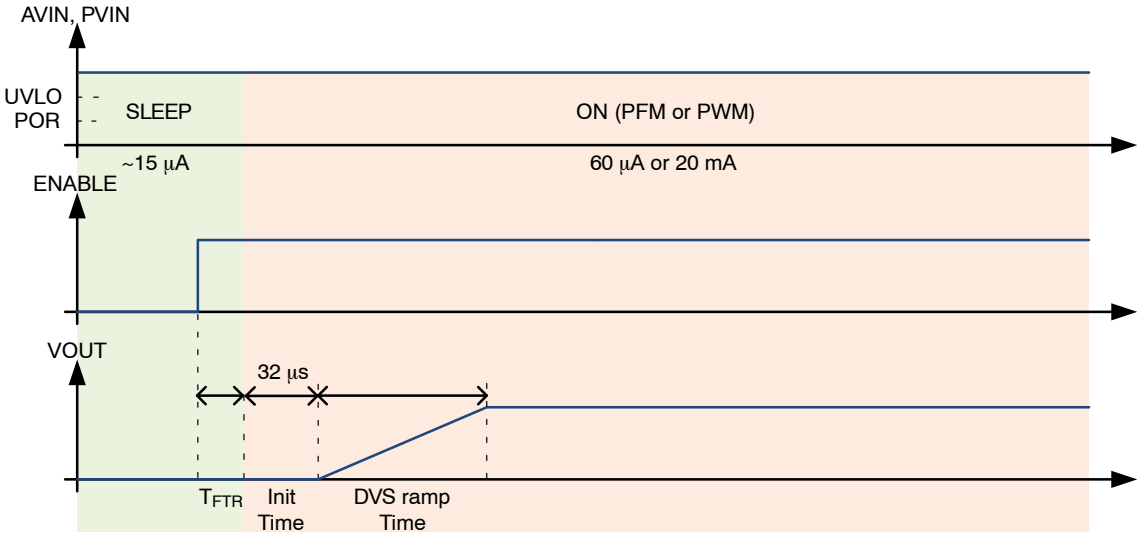


Figure 50. Fast Power Up Sequence

Power Down Sequence

DC−DC converter shutdown is initiated by either grounding the EN pin (Hardware Shutdown) or by clearing the ENABLE bit (Software shutdown) in the COMMAND register: The output voltage is disabled and, depending on the DISCHG bit state of the COMMAND register, the output may be discharged.

In hardware shutdown (EN = 0), the digital is still alive and I^2C accessible when I^2C pull up are present.

The internal core of the NCV91300 shuts down when:

- EN pin is low and no SLEEP_MODE
- AVIN falls below UVLO

Dynamic Voltage Scaling (DVS)

The NCV91300 supports dynamic voltage scaling (DVS) allowing the output voltage to be reprogrammed for providing the different voltages required by the processor. The change between set points is managed in a smooth fashion without disturbing the operation of the processor.

The DVS sequence is automatically initiated by changing the output voltage bits (VOUT[7..0] bits of the PROG register) via an I^2C command. The DVSMODE bit in the COMMAND register defines the DVS transition mode:

- Forced PWM mode (DVSMODE = 1) when accurate output voltage control is needed. DVS up and DVS down ramps are controlled with the DVS[1..0] bits in the TIME register.

Figure 51. DVS in Forced PWM Mode Diagram

- In Auto mode (DVSMODE = 0) when the output voltage must not be discharged. DVS up ramp is controlled by the DVS[1..0] as in Forced PWM mode, but the DVS down is no more controlled: it depends of the load and cannot be faster than the DVS[1..0] settings.

Figure 52. DVS in Auto Mode Diagram

Thermal Management

Thermal Shut Down (TSD)

The thermal capability of the NCV91300 can be exceeded due to the step down converter output stage power level. A thermal protection circuitry with associated interrupt is therefore implemented to prevent the IC from damage. This protection circuitry is only activated when the core is in active mode (output voltage is turned on). During thermal shut down, the output voltage is turned off.

When NCV91300 returns from thermal shutdown, it can re−start in 2 different configurations depending on the

REARM bit in the LIMCONF register:

- If REARM = 0 then NCV91300 does not re−start after TSD. To restart, an EN pin toggle is required.
- If REARM = 1, NCV91300 re−starts with register values set prior to thermal shutdown.

The thermal shut down threshold is set at 167°C (typical) and a 30°C hysteresis is implemented in order to avoid erratic on / off behavior. After a typical 167°C thermal shut down, NCV91300 will resume to normal operation when the die temperature cools to 140°C.

Thermal Warnings

In addition to the TSD, the die temperature monitoring circuitry includes a thermal warning and thermal pre−warning sensor and interrupts. These sensors can inform the processor that NCV91300 is close to its thermal shutdown and preventive measures to cool down die temperature can be taken by software.

The Warning threshold is set by hardware to 150°C typical. The Pre−Warning threshold is set by default to 130°C but it can be changed by setting the TPWTH[1..0] bits in the LIMCONF register.

IO Pins

Enable Pin

The EN pin controls NCV91300 start up. A built in pull down resistor disables the device when this pin is left unconnected or not driven..

SYNC Pin and Spread Spectrum

The NCV91300 can be synchronized to an external clock applied to the SYNC pin or use the internal oscillator. When using the internal oscillator, spread spectrum can be selected with the F_SPREAD[1..0] bits of the TIME register. These features help reduce and / or control the peak emissions at the switching frequency and harmonics.

Throughout the power−up sequence, the NCV91300 ignores both the signal applied on the SYNC pin and the selected spread spectrum, to work with the fixed internal 2.15 MHz clock (spread spectrum disabled)

Once power−up sequence is completed:

- If no clock is applied on the SYNC pin, the DC−DC continues switching with the internal oscillator, by activating the selected spread spectrum.
- As soon as a clock is present on the SYNC pin, for accurate frequency sensing, the internal oscillator is set to the fixed 2.15 MHz (spread spectrum disabled). Then, once the clock is sensed valid, the DC−DC mode is automatically set to Forced PWM, and the switching clock becomes the SYNC clock in a smooth way. By default the SYNC clock polarity is kept, but could be inverted upon request.

The NCV91300 switching reverts to the internal oscillator within no more than one missing cycle clock, when SYNC signal is no longer valid or removed. In the same time, the DC−DC mode returns to the PWM bit state and the programmed F_SPREAD[1..0] spread spectrum.

CLK interrupt (ACK_CLK bit) indicates if the switching clocks sources changed, whereas the CLK sense (SNS_CLK bit) defines the switching clock used by the DC−DC.

Power Good Pin

The Power Good monitoring with corresponding PG open drain pin indicates that the output voltage is up and running in the valid range.

When disabled (i.e. the PGDCDC bit of the COMMAND register set low), the PG pin stays in low impedance state.

In operation, when the output drops below 90% of the programmed level, the PG pin transitions immediately to the low impedance state, indicating a power failure. When the voltage returns above 95%, the PG pin becomes again in high impedance after a 10 µs typical delay (could be change to 2 ms upon request). For sure when the DCDC is turned off and during the power−up sequence, the PG is driven low indicating the output voltage is not ready.

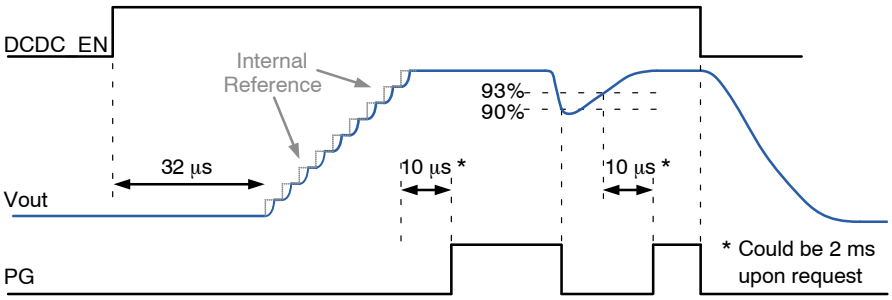


Figure 53. Power Good Signal when PGDCDC = 1

During DVS transitions, the Power Good monitoring is still active. However, the PGDVS bit of the COMMAND register forces the PG pin in low impedance during a positive DVS and it will follow again the state of the monitoring 10 µs typically (could be 2 ms upon request) after DVS transition completed.

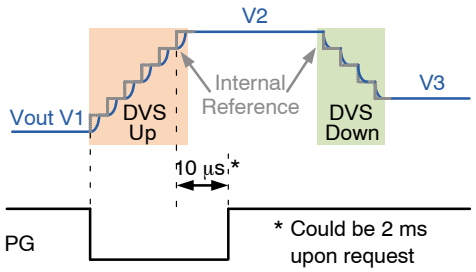


Figure 54. Power Good During DVS Transition (PGDVS = 1)

In addition to the above, the state of the synchronization can optionally be reflected on the PG pin through the PGCLK bit. This is of interest for RF critical applications where the switching of the DCDC's needs to be externally synchronized. With PGCLK set, the PG pin is forced low when the DCDC switching frequency is not the SYNC clock. With PGCLK not set, the state of the synchronization will have no influence on PG.

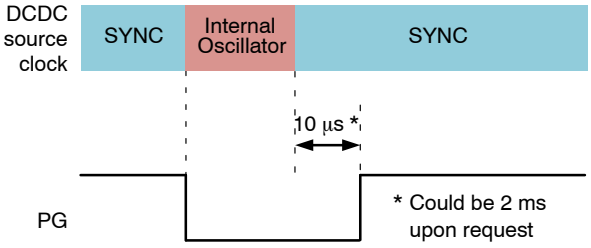


Figure 55. Power Good Behavior (PGCLK = 1)

Interrupt Pin

The interrupt controller continuously monitors internal interrupt sources (INT_SENx), generating an interrupt signal (INT_ACKx) when a system status change is detected (dual edge monitoring). The interrupt sources include:

Table 4. INTERRUPT SOURCES

Interrupt Name	Description
UVLO	AV_{IN} Under Voltage Lock Out
UVP	PV_{IN} Under Voltage Protection
OVP	PV_{IN} Over Voltage Protection
IDCDCHS	DC−DC converter Current Protection
IDCDCLS	DC−DC converter Negative Current Protection
ISHORT	DC−DC converter Short−Circuit Protection
CLK	Working Clock Indicator
PG	Power Good
TSD	Thermal Shut Down
TWARN	Thermal Warning
TPREW	Thermal Pre Warning
BUS	I^2C Write access error

Individual bits generating interrupts will be set to 1 in the INT_ACKx register, indicating the interrupt source. The INT_ACKx bit is automatically reset by writing a "1". The INT_SEN register (read only register) contains real time indicators of interrupt sources.

All interrupt sources can be masked by writing in the register INT_MSKx. Masked sources will never generate an interrupt request on the INTB pin (Open drain output).

A non−masked interrupt request will result in the INTB pin being driven low. When the host writes the INT_ACKx bits generating interrupt to "1", the INTB pin is released to high impedance and the corresponding interrupt bits INT_ACKx is cleared.

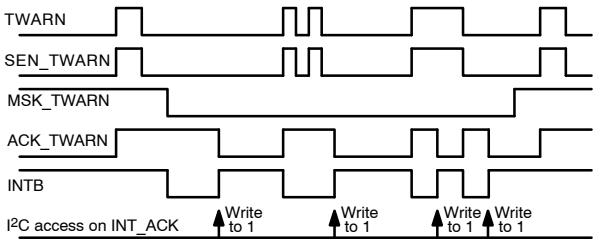


Figure 56. Interrupt Operation TWARN Example

By default no interrupt is associated with the INTB pin.

CONFIGURATION

Default output voltages, DC−DC modes, current limit and other parameters can be factory programmed upon request.

Below is the default configurations pre−defined:

Table 5. NCV91300 CONFIGURATION

Configuration	2.5 A NCV91300B	
Default I²C Address PID Product Identification RID Revision Identification FID Feature Identification	ADD1 − 14h: 0010100R/W 93h 85h 01h	
Default VOUT	1.1 V	
Default MODE	Forced PWM	
Default IPEAK	3.5 A	
OPN	NCV91300MNWBTXG	
Marking	W3	
Output Filter	4 x 10 μF	

I²C Compatible Interface

NCV91300 can support a subset of the I²C protocol as detailed below (Read, Write, Write then read sequences).

I²C Communication Description

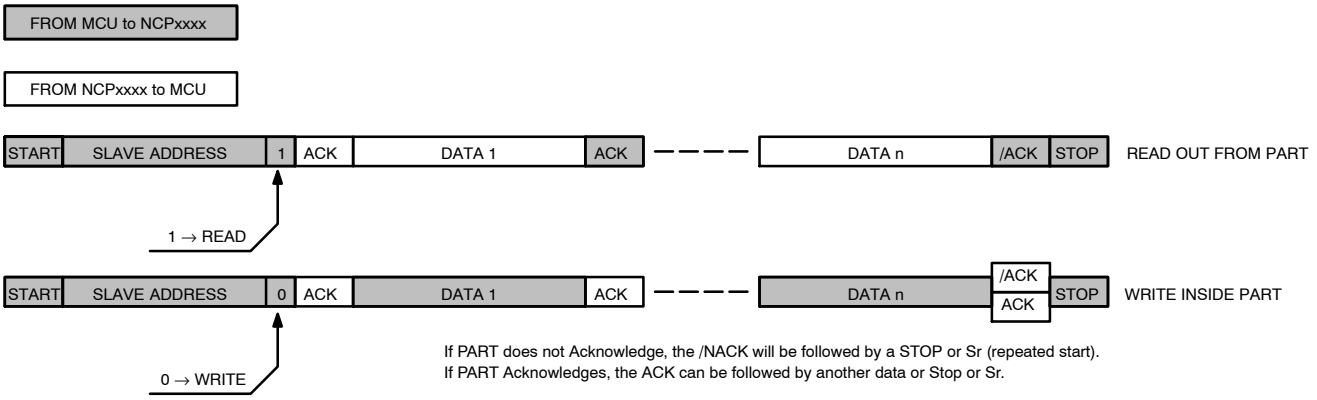


Figure 57. General Protocol Description

The first byte transmitted is the Chip address (with the LSB bit set to 1 for a read operation, or set to 0 for a Write operation). The following data will be:

- During a Write operation, the register address (@REG) is written in, followed by the data. The writing process is auto−incremental, so the first data will be written in @REG, the contents of @REG are incremented and the next data byte is placed in the location pointed to by @REG + 1 …., etc.
- During a Read operation, the NCV91300 will output the data from the last register that has been accessed by the last write operation. Like the writing process, the reading process is auto−incremental.

Read Sequence

The Master will first make a “Pseudo Write” transaction with no data to set the internal address register. Then, a Stop then Start or a Repeated Start will initiate the read transaction from the register address the initial write transaction has pointed to:

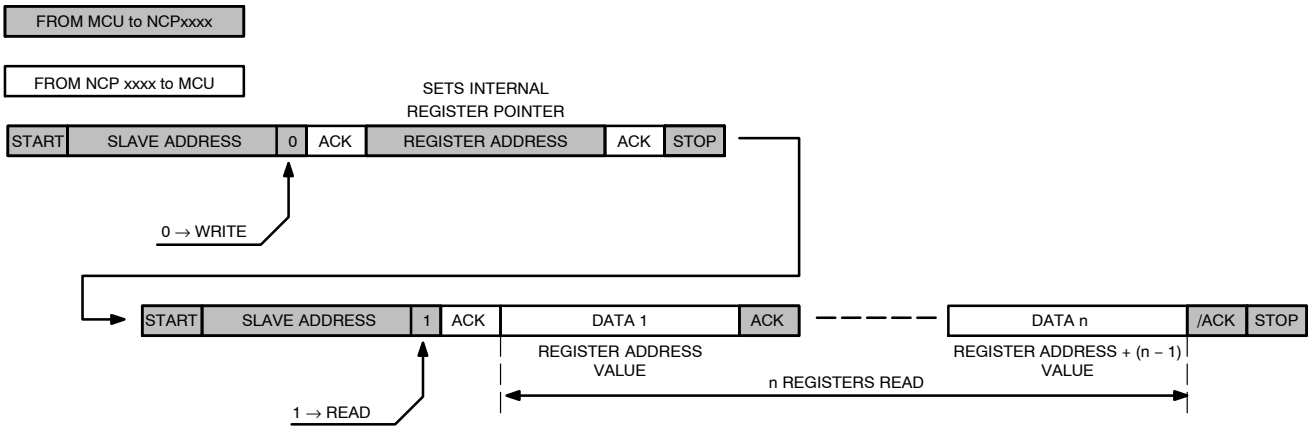


Figure 58. Read Sequence

The first Write sequence will set the internal pointer to the register that is selected. Then the read transaction will start at the address the write transaction has initiated.

Write Sequence

Write operation will be achieved by only one transaction. After chip address, the REG address has to be set, then following data will be the data we want to write in REG, REG + 1, REG + 2, …, REG + n.

Write n Registers:

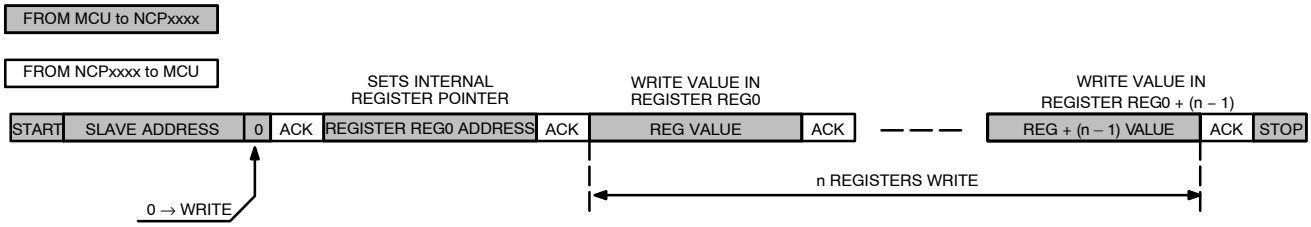


Figure 59. Write Sequence

Write then Read Sequence

With Stop Then Start

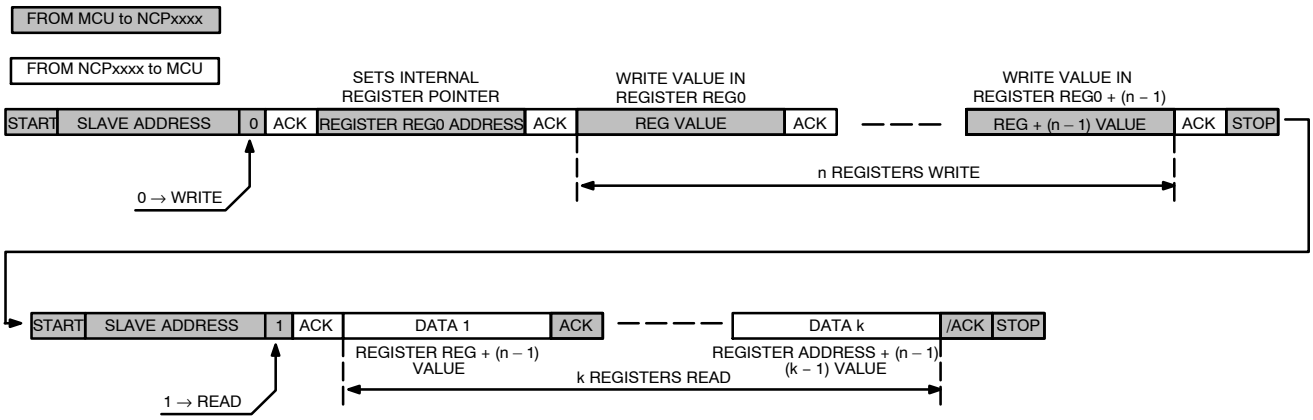


Figure 60. Write Followed by Read Transaction

Robust I²C Description

NCV91300 integrates a two consecutive single byte writes feature to improve robustness of the communication against non−systematic bit errors. During a write access, the NCV91300 compare the two consecutive single byte writes:

- If the second consecutive accesses is identical, the write is confirmed and executed
- If the second consecutive accesses is different, the write is ignores and BUS interrupt is flagged

This feature is controlled with ROBUSTI2C bit of the LIMCONF register.

NOTE: In case of multi slave, repeated start is highly recommended to increase robustness of the protocol. In addition to the double write, a dedicated interrupt has to be added to signal improper write attempt.

I²C Slave Address

The NCV91300 has 8 available I²C addresses selectable by factory settings (ADD0 to ADD7). Different address settings can be generated upon request to ON Semiconductor. See [Table 5 (NCV91300 Configuration) for the default I²C address.

Table 6. I²C SLAVE ADDRESS

I²C Slave Address	Hex	A7	A6	A5	A4	A3	A2	A1	A0
ADD0	W 0x20 R 0x21	0	0	1	0	0	0	0	R/W
	Add	0x10							–
ADD1	W 0x28 R 0x29	0	0	1	0	1	0	0	R/W
	Add	0x14							–
ADD2	W 0x30 R 0x31	0	0	1	1	0	0	0	R/W
	Add	0x18							–
ADD3	W 0x38 R 0x39	0	0	1	1	1	0	0	R/W
	Add	0x1C							–
ADD4	W 0Xc0 R 0xC1	1	1	0	0	0	0	0	R/W
	Add	0x60							–
ADD5	W 0xC8 R 0xC9	1	1	0	0	1	0	0	R/W
	Add	0x64							–
ADD6	W 0xD0 R 0xD1	1	1	0	1	0	0	0	R/W
	Add	0x68							–
ADD7	W 0xD8 R 0xD9	1	1	0	1	1	0	0	R/W
	Add	0x6C							–

Register Map

The tables below describe the I²C registers.

Registers / Bits Operations:

R	Read only register
W1C	Write to 1 to Clear
RW	Read and Write register
Reserved	Address is reserved and register / bit is not physically designed
Spare	Address is reserved and register / bit is physically designed

In bold default can be factory programmed upon request.

Table 7. I²C REGISTERS MAP CONFIGURATION (NCV91300MNWBTXG)

Add.	Register Name	Type	Def.	Function
00h	INT_ACK1	W1C	00h	Interrupt register 1
01h	INT_ACK2	W1C	00h	Interrupt register 2
02h	INT_SEN1	R	00h	Sense register 1 (real time status)
03h	INT_SEN2	R	00h	Sense register 2 (real time status)
04h	INT_MSK1	RW	FFh	Mask register 1 to enable or disable interrupt sources (trim)
05h	INT_MSK2	RW	FFh	Mask register 2 to enable or disable interrupt sources (trim)
06h	PID	R	93h	Product Identification
07h	RID	R	85h	Revision Identification
08h	FID	R	01h	Features Identification (trim)
09h	PROG	RW	5Ah	Output voltage settings (trim)
0Ah	COMMAND	RW	D7h	Operating mode, Power good and active discharge settings register (trim)
0Bh	TIME	RW	2F	Enabling and DVS timings register (trim)
0Ch	LIMCONF	RW	52h	Reset and limit configuration register (trim)
0Dh to FFh	–	–	–	Reserved. Test Registers

Registers Description

Table 8. INTERRUPT ACKNOWLEDGE REGISTER 1

Name: INTACK1				Address: 00h			
Type: W1C				Default: 00000000b (00h)			
Trigger: Dual Edge [D7..D0]							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0	ACK_UVLO	ACK_UVP	ACK_OVP	Spare = 0	ACK_ISHORT	ACK_IDCDCHS	ACK_IDCDCLS

Bit	Bit Description
ACK_IDCDCLS	DC−DC Negative Over Current Sense Acknowledgement 0: Cleared 1: DC−DC Negative Over Current Event detected
ACK_IDCDCHS	DC−DC Over Current Sense Acknowledgement 0: Cleared 1: DC−DC Over Current Event detected
ACK_ISHORT	DC−DC Short−Circuit Protection Sense Acknowledgement 0: Cleared 1: DC−DC Short circuit protection detected
ACK_OVP	PV_{IN} Overvoltage Protection Sense Acknowledgement 0: Cleared 1: OVP Event detected
ACK_UVP	PV_{IN} Undervoltage Protection Sense Acknowledgement 0: Cleared 1: UVP Event detected
ACK_UVLO	Under Voltage Sense Acknowledgement 0: Cleared 1: Under Voltage Event detected

Table 9. INTERRUPT ACKNOWLEDGE REGISTER 2

Name: INTACK2				Address: 01h			
Type: W1C				Default: 00000000b (00h)			
Trigger: Dual Edge [D7..D0]							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0	ACK_TSD	ACK_TWARN	ACK_TPREW	Spare = 0	ACK_BUS	ACK_CLK	ACK_PG

Bit	Bit Description
ACK_PG	Power Good Sense Acknowledgement 0: Cleared 1: DC−DC Power Good Event detected
ACK_CLK	Working Clock Indicator Acknowledgement 0: Cleared 1: DC−DC switching frequency source changed
ACK_BUS	Double write Error Acknowledgement 0: Cleared 1: Invalid double write access
ACK_TPREW	Thermal Pre Warning Sense Acknowledgement 0: Cleared 1: Thermal Pre Warning Event detected
ACK_TWARN	Thermal Warning Sense Acknowledgement 0: Cleared 1: Thermal Warning Event detected
ACK_TSD	Thermal Shutdown Sense Acknowledgement 0: Cleared 1: Thermal Shutdown Event detected

Table 10. INTERRUPT SENSE REGISTER 1

Name: INTSEN1				Address: 02h			
Type: R				Default: 00000000b (00h)			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0	SEN_UVLO	SEN_UVP	SEN_OVP	Spare = 0	Spare = 0	SEN_IDCDCHS	SEN_IDCDCLS

Bit	Bit Description
SEN_IDCDCLS	DC−DC negative over current sense 0: DC−DC negative current is below limit 1: DC−DC negative current is over limit
SEN_IDCDCHS	DC−DC over current sense 0: DC−DC output current is below limit 1: DC−DC output current is over limit
SEN_OVP	PV_{IN} Overvoltage Protection Sense 0: OVP not detected 1: OVP detected
SEN_UVP	PV_{IN} Undervoltage Protection Sense 0: UVP not detected 1: UVP detected
SEN_UVLO	Under Voltage Sense 0: Input Voltage higher than UVLO threshold 1: Input Voltage lower than UVLO threshold

Table 11. INTERRUPT SENSE REGISTER 2

Name: INTSEN2				Address: 03h			
Type: R				Default: 00000000b (00h)			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0	SEN_TSD	SEN_TWARN	SEN_TPREW	Spare = 0	SEN_BUS	SEN_CLK	SEN_PG

Bit	Bit Description
SEN_PG	Power Good Sense 0: DC−DC Output Voltage below target 1: DC−DC Output Voltage within nominal range
SNS_CLK	Working Clock Indicator Sense 0: DC−DC switching frequency follows the Internal Oscillator 1: DC−DC switching frequency follows the SYNC pin
SEN_BUS	Double write Error Sense 0: No error 1: Invalid double write access
SEN_TPREW	Thermal Pre Warning Sense 0: Junction temperature below thermal pre−warning limit 1: Junction temperature over thermal pre−warning limit
SEN_TWARN	Thermal Warning Sense 0: Junction temperature below thermal warning limit 1: Junction temperature over thermal warning limit
SEN_TSD	Thermal Shutdown Sense 0: Junction temperature below thermal shutdown limit 1: Junction temperature over thermal shutdown limit

Table 12. INTERRUPT MASK REGISTER 1

Name: INTMSK1				Address: 04h			
Type: RW				Default: See Register Map			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 1	**MSK_UVLO**	**MSK_UVP**	**MSK_OVP**	Spare = 1	**MSK_ISHORT**	**MSK_IDCDCHS**	**MSK_IDCDCLS**

Bit	Bit Description
MSK_IDCDCLS	DC−DC negative over current interrupt mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_IDCDCHS	DC−DC over current interrupt mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_ISHORT	DC−DC Short−Circuit Protection mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_OVP	PV_{IN} Over Voltage interrupt Mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_UVP	PV_{IN} Under Voltage interrupt Mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_UVLO	Under Voltage interrupt mask 0: Interrupt is Enabled 1: Interrupt is Masked

Table 13. INTERRUPT MASK REGISTER 2

Name: INTMSK2				Address: 05h			
Type: RW				Default: See Register Map			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 1	**MSK_TSD**	**MSK_TWARN**	**MSK_TPREW**	Spare = 1	**MSK_BUS**	**MSK_CLK**	**MSK_PG**

Bit	Bit Description
MSK_PG	Power Good interrupt source mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_CLK	Working Clock Indicator interrupt Mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_BUS	Double write Error interrupt source mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_TPREW	Thermal Pre Warning interrupt mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_TWARN	Thermal Warning interrupt mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_TSD	Thermal Shutdown interrupt mask 0: Interrupt is Enabled 1: Interrupt is Masked

Table 14. PRODUCT ID REGISTER

Name: PID				Address: 06h			
Type: R				Default: 00011011b (93h)			
Trigger: N/A				Reset on N/A			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PID_7	PID_6	PID_5	PID_4	PID_3	PID_2	PID_1	PID_0

Table 15. PRODUCT ID REGISTER

Name: RID				Address: 07h			
Type: R				Default: See Register Map			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RID_7	RID_6	RID_5	RID_4	RID_3	RID_2	RID_1	RID_0
Bit	**Bit Description**						
RID[7..0]	Revision Identification						

Table 16. FEATURE ID REGISTER

Name: FID				Address: 08h			
Type: R				Default: See Register Map			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare	Spare	Spare	Spare	**FID_3**	**FID_2**	**FID_1**	FID_0
Bit	**Bit Description**						
FID[3..0]	Feature Identification						

Table 17. DC−DC VOLTAGE PROG REGISTER

Name: PROG				Address: 09h			
Type: RW				Default: See Register Map			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Vout [7..0]							
Bit	**Bit Description**						
Vout [7..0]	Sets the DC−DC converter output voltage 00000000b = 600 mV (5mV step) 00000001b = 605 mV (5 mV step) … 01001111b = 995 mV (5 mV step) 01010000b = 1000 mV (10 mV step) 01010001b = 1010 mV (10 mV step) … 10110011b = 1990 mV (10 mV step) 10110100b = 2000 mV (20 mV step) 10110101b = 2020 mV (20 mV step) … 11110100b = 3280 mV (20 mV step) 11110101b = 3300 mV (20 mV step) … 11111111b = 3300 mV							

Table 18. COMMAND

Name: COMMAND				Address: 0Ah			
Type: RW				Default: See Register Map			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
DVSMODE	**PWM**	**SLEEP_MODE**	**DISCHG**	**PGCLK**	**ENABLE**	**PGDVS**	**PGDCDC**

Bit	Bit Description
PGDCDC	Power Good Enabling 0 = Disabled 1 = Enabled
PGDVS	Power Good Active On DVS 0 = Disabled 1 = Enabled
ENABLE	EN Pin Gating 0: Disabled 1: Enabled
PGCLK	Power Good CLK Enabling 0 = Disabled 1 = Enabled
DISCHG	Active discharge bit Enabling 0 = Discharge path disabled 1 = Discharge path enabled
SLEEP_MODE	Sleep mode 0 = Low Iq mode when EN low 1 = Force product in sleep mode
PWM	Operating mode selection 0 = Auto 1 = Forced PWM
DVSMODE	DVS transition mode selection 0 = Auto 1 = Forced PWM

Table 19. TIMING REGISTER

Name: TIME				Address: 0Bh			
Type: RW				Default: See Register Map			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
DELAY[1..0]		**F_SPREAD[1..0]**		**DVS[1..0]**		**DBN_Time[1..0]**	

Bit	Bit Description
DBN_Time[1..0]	EN debounce time 00 = 1 – 2 μs 01 = 1 – 2 μs 10 = 2 – 3 μs 11 = 3 – 4 μs
DVS[1..0]	DVS Speed 00 = 10 mV step / 0.465 μs 01 = 10 mV step / 0.930 μs 10 = 10 mV step / 1.860 μs 11 = 10 mV step / 3.720 μs
F_SPREAD[1..0]	Spread Spectrum 00 = No Spread Spectrum 01 = ±5 % spread spectrum 10 = ±10 % spread spectrum 11 = ±10 % spread spectrum
DELAY[1..0]	Delay applied upon enabling (ms) 00b = 0 ms – 11b = 6 ms (Steps of 2 ms)

Table 20. LIMITS CONFIGURATION REGISTER

Name: LIMCONF				Address: 0Ch			
Type: RW				Default: See Register Map			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
IPEAK[1..0]		**TPWTH[1..0]**		**ROBUSTI2C**	FORCERST	RSTSTATUS	**REARM**

Bit	Bit Description
REARM	Rearming of device after TSD / ISHORT 0: No re−arming after TSD / ISHORT 1: Re−arming active after TSD / ISHORT with no reset of I^2C registers: FPUS (Fast power up sequence) is initiated with previously programmed I^2C registers values
RSTSTATUS	Reset Indicator Bit 0: Must be written to 0 after register reset 1: Default (loaded after Registers reset)
FORCERST	Force Reset Bit 0 = Default value. Self−cleared to 0 1: Force reset of internal registers to default
TPWTH[1..0]	Thermal pre−Warning threshold settings 00 = 110°C 01 = 120°C 10 = 130°C 11 = 140°C
ROBUSTI2C	I^2C protocol setting 0: Classic I^2C protocol 1: Double write access I^2C protocol
IPEAK	Inductor peak current settings 00 = 3.0 A (for 2.0 A output current) 01 = 3.5 A (for 2.5 A output current) 10 = 4.0 A (for 3.0 A output current) 11 = 4.5 A (for 3.5 A output current)

APPLICATION INFORMATION

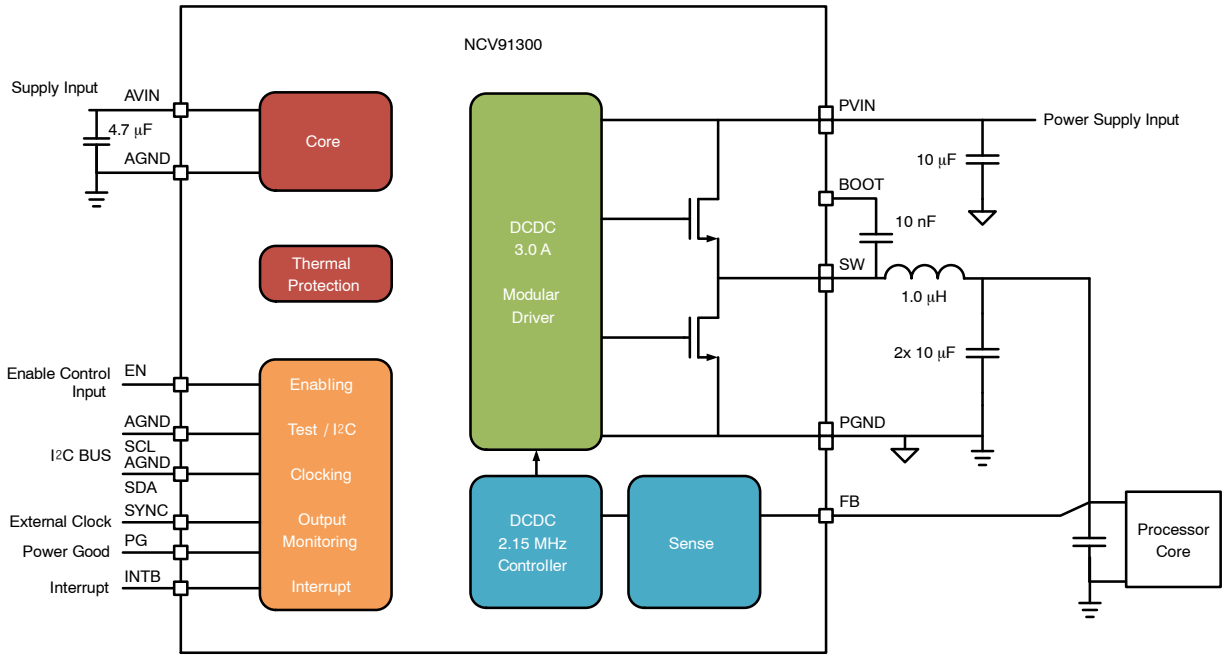


Figure 61. Typical Application Schematic

Output Filter Considerations

The output filter introduces a double pole in the system at a frequency of:

$$f_{LC} = \frac{1}{2 \times \pi \times \sqrt{L \times C}} \quad \text{(eq. 1)}$$

The NCV91300 internal compensation network is optimized for a typical output filter comprising a 1.0 µH inductor and 10 µF capacitor as describes in the basic application schematic in Figure 61.

Voltage Sensing Considerations

In order to regulate the power supply rail, the NCV91300 must sense its output voltage. The IC can support two sensing methods:

- Normal sensing: The FB pin should be connected to the output capacitor positive terminal (voltage to regulate).
- Remote sensing: The power supply rail sense should be made close to the system powered by the NCV91300. The voltage to the system is more accurate, since the PCB line impedance voltage drop is within the regulation loop. In this case, we recommend connecting the FB pin to the system decoupling capacitor positive terminal.

Components Selection

Inductor Selection

The inductance of the inductor is chosen such that the peak−to−peak ripple current I_{L_PP} is approximately 20% to 50% of the maximum output current I_{OUT_MAX}. This provides the best trade−off between transient response and output ripple. The inductance corresponding to a given current ripple is:

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times I_{L\_PP}} \quad \text{(eq. 2)}$$

The selected inductor must have a saturation current rating higher than the maximum peak current which is calculated by:

$$I_{L\_MAX} = I_{OUT\_MAX} + \frac{I_{L\_PP}}{2} \quad \text{(eq. 3)}$$

The inductor must also have a high enough current rating to avoid self−heating. A low DCR is therefore preferred. Refer to Table 21 for recommended inductors.

Table 21. INDUCTOR SELECTION

Supplier	Part #	Value (μH)	Size (L x l x T) (mm)	Saturation Current Max (A)	DCR Max at 25°C (mΩ)
TDK	TFM252012ALMA1R0MTAA	1.0	2.5 x 2.0 x 1.2	4.2	42
Murata	DFE2HCAH1R0MJ0	1.0	2.5 x 2.0 x 2.0	3.8	42
TDK	TFM322512ALMA1R0MTAA	1.0	3.2 x 2.5 x 1.2	4.6	37
Murata	DFE322520D−1R0MP2	1.0	3.2 x 2.5 x 2.0	7.5	21
CoilCraft	XAL4020−102ME	1.0	4.0 x 4.0 x 2.1	8.7	14.6

Output Capacitor Selection

The output capacitor selection is determined by output voltage ripple and load transient response requirement. For high transient load performance a high output capacitor value must be used. For a given peak−to−peak ripple current I_{L_PP} in the inductor of the output filter, the output voltage ripple across the output capacitor is the sum of three components as shown below.

$$V_{OUT\_PP} \approx V_{OUT\_PP(C)} + V_{OUT\_PP(ESR)} + V_{OUT\_PP(ESL)} \quad \text{(eq. 4)}$$

With:

$$V_{OUT\_PP(C)} = \frac{I_{L\_PP}}{8 \times C \times f_{SW}}$$

$$V_{OUT\_PP(ESR)} = I_{L\_PP} \times ESR$$

$$V_{OUT\_PP(ESL)} = \frac{L_{ESL}}{L} \times V_{IN}$$

Where the peak−to−peak ripple current is given by

$$I_{L\_PP} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}$$

In applications with all ceramic output capacitors, the main ripple component of the output ripple is $V_{OUT\_PP(C)}$. The minimum output capacitance can be calculated based on a given output ripple requirement V_{OUT_PP} in PWM operation mode.

$$C_{MIN} = \frac{I_{L\_PP}}{8 \times V_{OUT\_PP} \times f_{SW}} \quad \text{(eq. 5)}$$

Refer to Table 22 for recommended output capacitor.

Table 22. OUTPUT CAPACITOR SELECTION

Supplier	Part #	Value (μF)	Case	Size (L x l x T) (mm)
TDK	CGA4J1X7R0J106K125AC	10.0	0805	2.0 x 1.25 x 1.25
Murata	GCM21BR70J106KE22#	10.0	0805	2.0 x 1.25 x 1.25

Input Capacitor Selection

One of the input capacitor selection requirements is the input voltage ripple. To minimize the input voltage ripple and get better decoupling at the input power supply rail, a ceramic capacitor is recommended due to low ESR and ESL. The minimum input capacitance with respect to the input ripple voltage V_{IN_PP} is

$$C_{IN\_MIN} = \frac{I_{OUT\_MAX} \times (D - D^2)}{V_{IN\_PP} \times f_{SW}} \quad \text{(eq. 6)}$$

Where

$$D = \frac{V_{OUT}}{V_{IN}}$$

In addition, the input capacitor must be able to absorb the input current, which has a RMS value of

$$I_{IN\_RMS} = I_{OUT\_MAX} \times \sqrt{D - D^2} \quad \text{(eq. 7)}$$

The input capacitor also must be sufficient to protect the device from over voltage spikes, and a 10 μF capacitor or greater is required. The input capacitor should be located as close as possible to the IC. All PGND pins must be connected together to the ground terminal of the input cap which then must be connected to the ground plane. All PVIN pins must be connected together to the Vbat terminal of the input cap which then connects to the Vbat plane.

In addition to the proper input capacitor selection, and in order to damp the ringing effects due to the switching activity, an RC snubber network can be placed between the switch node (SW) and the power ground (PGND), which is of particular interest in applications operating at high input voltage levels at P_{VIN}.

Refer to Table 23 for recommended input capacitor.

Table 23. INPUT CAPACITOR SELECTION

Supplier	Part #	Value (µF)	Case	Size (L x l x T) (mm)
TDK	CGA5L1X7R1E106K160AC	10.0	0805	2.0 x 1.25 x 1.60
Murata	GCM31CR71C106KA64#	10.0	0805	2.0 x 1.25 x 1.60
TDK	CGA4J1X7R0J106K125AC	10.0	0805	2.0 x 1.25 x 1.25
Murata	GCM21BR70J106KE22#	10.0	0805	2.0 x 1.25 x 1.25

Power Capability and Thermal consideration

The difference in temperature between the junction (T_J) and ambient (T_A), the NCV91300 junction−to−ambient thermal resistance in the application and the on−chip power dissipation (P_{IC}) drive the NCV91300's power capability.

The on−chip power dissipation P_{IC} can be determined as

$$P_{IC} = P_T - P_L \quad \text{(eq. 8)}$$

with the total power losses P_T being

$$P_T = V_{OUT} \times I_{OUT} \times \left(\frac{1}{\eta} - 1\right)$$

where η is the efficiency and P_L the simplified inductor power losses

$$P_L = I_{LOAD}^2 \times DCR.$$

Now the junction temperature T_J can easily be calculated as

$$T_J = R\theta_{JA} \times P_{IC} + T_A \quad \text{(eq. 9)}$$

To avoid irreversible damage and overheating, the Thermal Shut Down (TSD) of the NCV91300 will stop the power stage switching activity as soon as the die temperature rises up to the 170°C TSD threshold. The dissipation in the power stage mainly depends on the losses in the HSS (High Side Switch) and LSS (Low Side Switch) and is then directly function of the loading current. The NCV91300 specification is guaranteed for a maximum Junction Temperature (T_{J_MAX}) of 150°C. When the junction temperature ranges from 150°C to the TSD threshold, the IC will still operate and will not be damaged, but the specifications are not guaranteed and the parameters value may deviate significantly. It is then important to try to keep the $T_J \leq 150°C$. The THERMAL INFORMATION table provides the thermal parameters ($R_{\theta Jx}$) defined by the JEDEC JESD51−3 as well as some thermal characterization parameters. The thermal characterization parameters are the result of measurements on the standard NCV91300 demo board, while the thermal parameters are the result of simulations in the JESD51 defined environment.

The junction−to−ambient thermal resistance is a function of the PCB layout (number of layers and copper and PCB size) and the environment. For example, the NCV91300 mounted on the EVB has an $R_{\theta JAm}$ about 38°C/W.

Example:

Assuming 3.3 V input voltage and a 1.8 V / 2 A DC output, the efficiency, according to Figure 8, is 82%.

Then the total dissipated power

$$P_T = V_{OUT} \times I_{OUT} \times \left(\frac{1}{\eta} - 1\right) = 790 \text{ mW}.$$

The TDK TFM252012ALMA1R0MTAA inductor DCR is comprised between 35 mΩ (Typical) and 42 mΩ (max), so the power dissipated in the inductor

$$P_L = I_{LOAD}^2 \times DCR$$

is within the 168 mW to 140 mW range, giving about 622 mW to 650 mW dissipated in the NCV91300.

Then, the expected junction temperature for a NCV91300 on its standard demo board placed at 125°C ambient temperature in a natural airflow environment

$$(T_J = R\theta_{JA} \times P_{IC} + T_A)$$

is in the 149°C range.

A thermal simulation of the NCV91300 on the application board in a 125°C ambient temperature and natural airflow shows that the above prediction is accurate (~1% error):

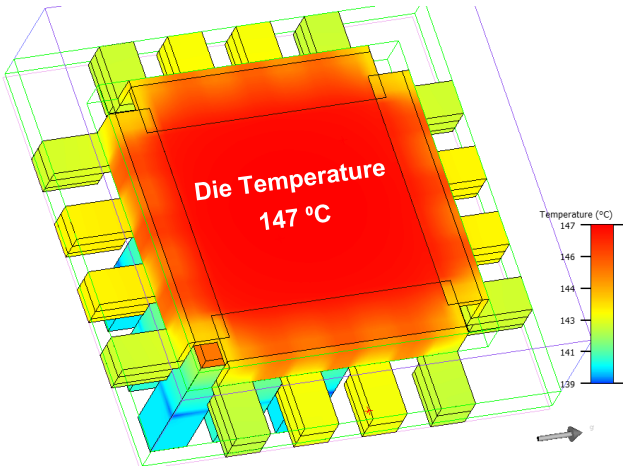


Figure 62. Simulation of the Die Temperature (P_{IC} = 650 mW / ambient T° = 125°C)

Based on this model, a maximum power dissipation versus temperature is given by the Table 24:

Table 24. MAXIMUM POWER DISSIPATION VERSUS EXTERNAL TEMPERATURE

	NCV91300 Internal Dissipation (mW)	500	600	650	700	800	900	1000	1100	1200	1300	1400	1500	2000
Die Temperature (°C)	Ambient Temperature(T_A) 25°C	44.1	47.8	49.6	51.5	55.2	58.8	62.5	66.2	69.8	73.4	77.1	80.7	98.8
	Ambient Temperature(T_A) 105°C	123	126	128	130	133	137	140	143	147	150	154	157	175
	Ambient Temperature(T_A) 125°C	142	146	147	149	153	156	159	163	166	170	173	177	

Layout Considerations

Switching Noise Consideration

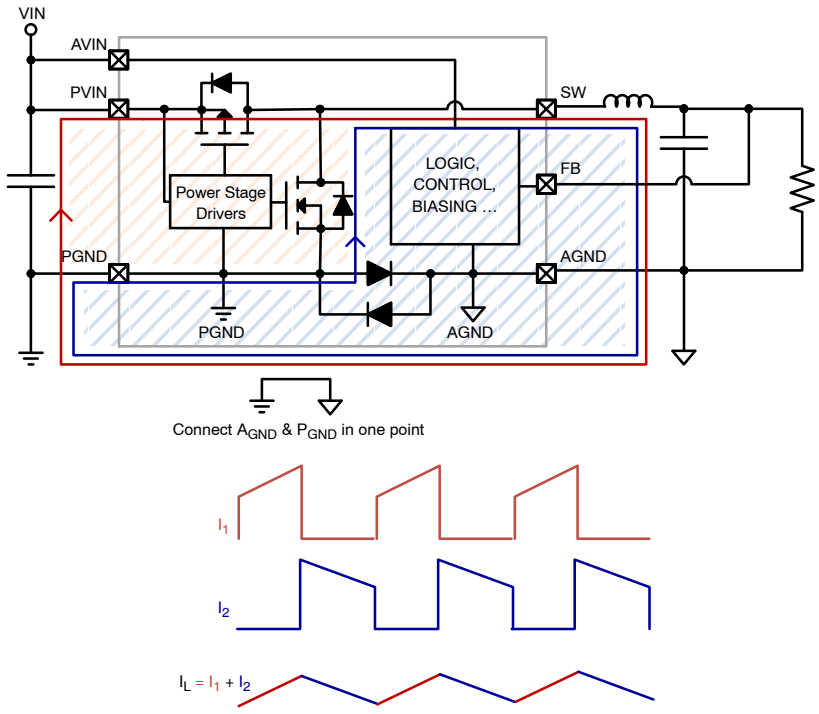


Figure 63. AC Current Flowing Loops

- The DC/DC buck converter has two main loops where high AC currents flow.
- When the High−Side Switch (HSS) is on, the current flows from PVIN via HSS and L to the output capacitor and the load. The current flows back via ground to the input. The AC portion of the current will flow via the input and output capacitors. This current is shown in red color (I1).
- When HSS switches off, the inductor current will keep flowing in the same direction, and the Low−Side Switch (LSS) is switched on. The current flows via LSS, L, load and output capacitor and back via ground to LSS. This loop is shown in blue (I2).
- Both I1 and I2 are discontinuous currents, meaning that they have sharp rising and falling edges at the beginning and end of the active time. These sharp edges have fast rise and fall times (high dI/dt). Therefore they have a lot of high frequency content.
- I1 and I2 share a common path from switch node to inductor to output capacitor to ground back to the source of LSS. The sum of I1 and I2 is a relatively smooth continuous saw−tooth waveform, which has less high frequency content due to the absence of high dI/dt edges.
- From noise point of view, the current loop with the high dI/dt current is the red shaded area. This loop will generate the most high frequencies and should be considered the most critical loop for noise in buck converters. The dI/dt of the current in the blue shaded area is not as high as it is in the other area and generally generates a lot less noise.

Electrical Rules

Good electrical layout is a key to make sure proper operation, high efficiency, and noise reduction. Electrical layout guidelines are:

- Since the red shaded area is the noisiest loop, it is critical to identify it and to place the input cap in such a way that this loop is minimized. It is also important to make sure that the path between the 2 terminals of the input cap and the PVIN & PGND pins is as short as possible and free of any vias to either the VIN or the GND PCB plane. It can also be a good practice to make a local PGND and VIN planes and to keep those planes as solid as possible below and in the input switching loop. Any trace or vias in this area reduces the plane effectiveness and increase the plane impedance. Vias from these planes to the other main planes of the PCB should be placed outside of the critical loop.
- Also, it is important to place the output capacitor ground in an area that does not overlap the input capacitor switching loop : this could generate extra high frequency noise in the output voltage
- Connecting the PGND plane to the main PCB GND plane (to whitch the AGND pin should be connected too) in one point (doing a kind of “star routing”) is also important to isolate the AGND and keep them quiet.
- Use wide and short traces for power paths (such as P_{VIN}, V_{OUT}, SW, and PGND) to reduce parasitic inductance and high−frequency loop area. It is also good for efficiency improvement.
- The device should be well decoupled by input capacitor and input loop area should be as small as possible to reduce parasitic inductance, input voltage spike, and noise emission.
- SW node should be a large copper pour, but compact because it is also a noise source.
- It would be good to have separated local ground planes for PGND and AGND and connect the two planes at one point. Directly connect AGND pin to the exposed pad and then connect to AGND ground plane through vias. Try best to avoid overlap of input ground loop and output ground loop to prevent noise impact on output regulation.
- Arrange a “quiet” path for output voltage sense, and make it surrounded by a ground plane.

Thermal Rules

Good PCB layout improves the thermal performance and thus allows for high power dissipation even with a small IC package. Thermal layout guidelines are:

- A four or more layers PCB board with solid ground planes is preferred for better heat dissipation.
- Use multiple vias around the IC to connect the inner ground layers to reduce thermal impedance.
- Use a large and thick copper area especially in the top layer for good thermal conduction and radiation.
- Use two layers or more for the high current paths (PVIN, PGND, SW) in order to split current into different paths and limit PCB copper self−heating.

Component Placement

- Input capacitor placed as close as possible to the IC.
- PVIN directly connected to Cin input capacitor, and then connected to the Vin plane. Local mini planes used on the top layer and the layer just below the top layer with laser vias.
- AVIN connected to the Vin plane just after the capacitor.
- AGND directly connected to the GND plane.
- PGND directly connected to Cin input capacitor, and then connected to the GND plane: Local mini planes used on the top layer and the layer just below the top layer with laser vias.
- SW connected to the Lout inductor with local mini planes on the top layer and the layer just below the top layer The 2 local mini planes are connected together by laser vias.

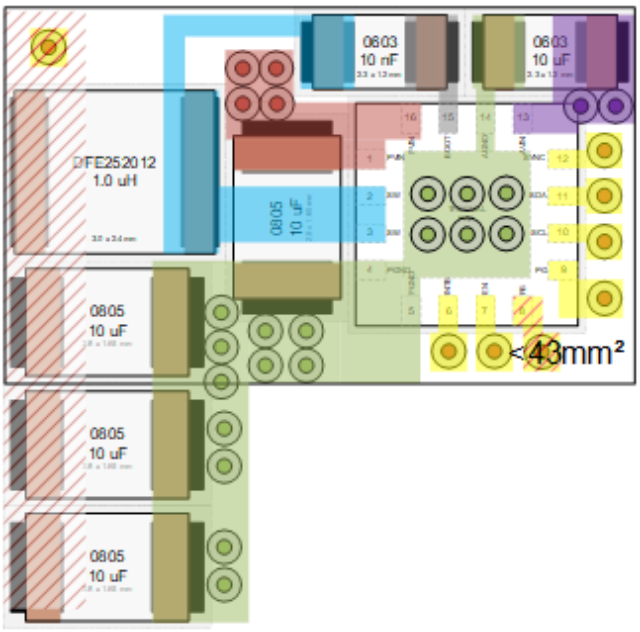


Figure 64. Placement Recommendation

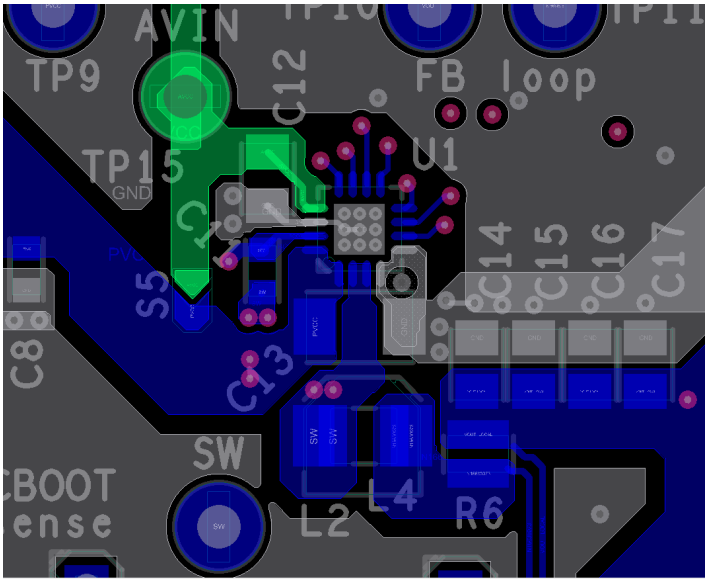


Figure 65. Layout Example

ORDERING INFORMATION

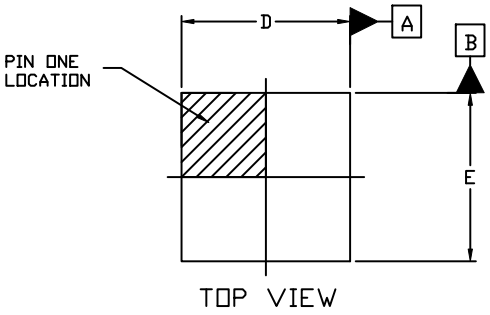
Device Order Number	Specific Device Marking	Default Voltage	Default Max Current	Default Mode	Package Type	Shipping†
NCV91300MNWBTXG	W3	1.1 V	2.5 A	Forced PWM	QFNW16 3x3, 0.5P (Pb−Free)	TBD

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

13. For full details about the configurations, refer to Table 5

PACKAGE DIMENSIONS

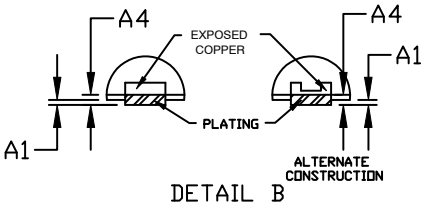
QFNW16 3x3, 0.5P
CASE 484AL
ISSUE A



TOP VIEW

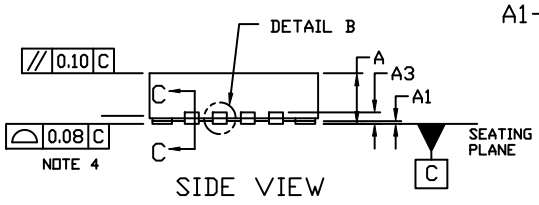
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

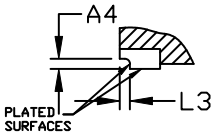


DETAIL B

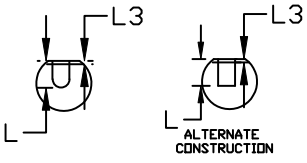
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	---	---	0.05
A3	0.20 REF		
A4	0.10	---	---
b	0.20	0.25	0.30
D	2.90	3.00	3.10
D2	1.70	1.80	1.90
E	2.90	3.00	3.10
E2	1.70	1.80	1.90
e	0.50 BSC		
K	0.20 REF		
L	0.30	0.40	0.50
L3	0.05 REF		



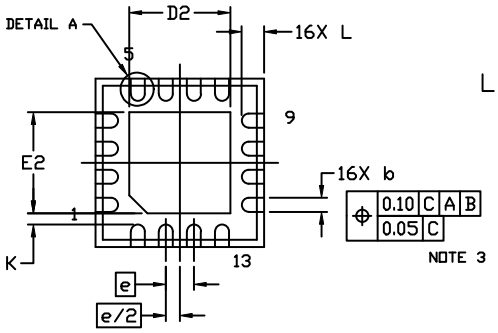
SIDE VIEW



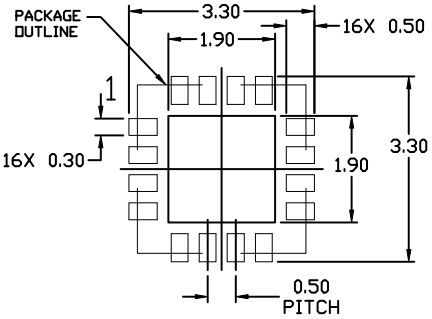
SECTION C-C



DETAIL A



BOTTOM VIEW



RECOMMENDED
MOUNTING FOOTPRINT