AN90045

Nexperia load switch ICs

Rev. 1.0 — 29 June 2023 application note

Document information

Information	Content
Keywords	Load switch, NPS4053, NPS4069, Quick Output Discharge (QOD), True Reverse Current Blocking (TRCB), Auto Retry, Latch Off
Abstract	This application note provides basic information about Nexperia load switch ICs. Explanations are provided on when load switch ICs should be used and how they can be implemented in a power chain. Details of important protection features such as reverse voltage, over-current and over-temperature are included. The key data sheet parameters are described and guidance on PCB layout is provided.

1. Introduction

Nexperia load switch ICs are highly integrated Power Management Integrated Circuits (PMICs) designed to efficiently control power rails within electronic systems. Load switches serve as indispensable components for managing power distribution and enabling the smooth operation of various loads. Fig. 1 shows a Nexperia load switch IC in its simplest form, consisting of a voltage input pin, a voltage output pin, an ON pin (this pin is named EN for some devices) and a ground pin.

When a voltage is applied to the input pin, the load switch IC remains in an off-state until the enable pin is triggered or driven to its enabled state. This means that the load switch pass element (typically a MOSFET) will only activate and allow current to flow to the output once the enable pin is set high or low depending on its active state. Nexperia load switch ICs ensures precise control over power delivery, making them an ideal choice for efficient and reliable power management in electronic systems.

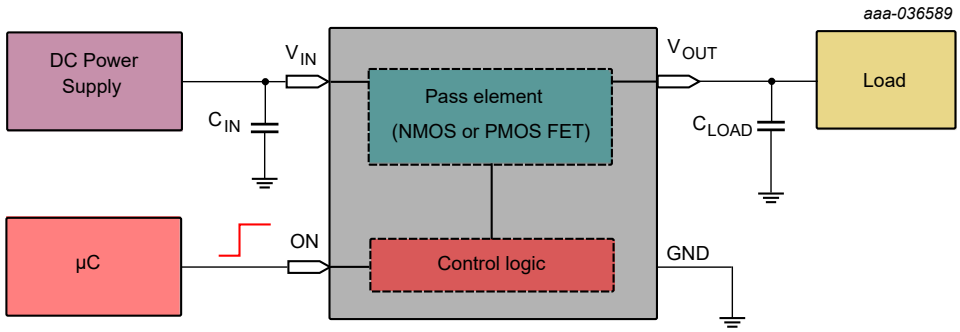

Fig. 1. Basic load switch diagram

1.1. Load switch internal features

A quick look at the internal blocks of a load switch can be helpful in determining how it functions. Fig. 2 shows the Nexperia NPS40xx series load switch block diagram which has additional features such as fault control to determine over current events, True Reverse Current Blocking (TRCB), and Over Temperature Protection (OTP). The product's features are described below.

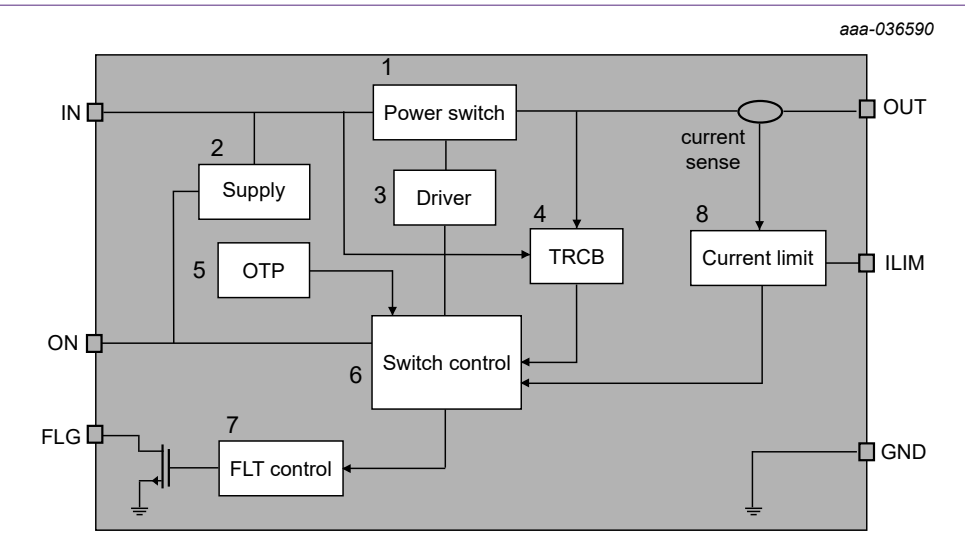

Fig. 2. NPS40xx series load switch block diagram

1. The internal FET acts like a relay to turn-on and turn-off the output voltage corresponding to the state of the EN signal. Each load switch has a characteristic on-resistance that is primarily determined by the FET used in the load switch. This FET can be either P-channel or N-channel

depending on the load switch, and each have their own advantages and disadvantages, see Section 4.2.

2. The supply is the internal block that controls the charge pump (for NFET only), and other control blocks used to drive the gate control in the load switch.
3. This is the gate driver of the internal pass FET. The gate driver controls the on and off time of the FET for a pre-determined rise and fall time of the output voltage.
4. True Reverse Current Blocking is a feature designed to block the current flowing in the reverse direction from the output terminal (OUT) to the input terminal (IN) when output voltage (OUT) > input voltage (IN).
5. The over temperature protection block is used to protect the load switch from thermal events. Once the junction temperature of the device reaches a certain temperature, the device will turn the pass FET off, and assert a fault flag to let the user know there is a thermal event inside the IC.
6. The Switch Control block is controlled by an external logic signal (ON), which controls the pass FET. The internal block protection features, such as OTP, TRCB, and current limit protection are also tied to this block to disable the pass FET when an error condition resulting in a FLG has been met.
7. The NPS40xx series of load switch has internal fault control that allows a signal to be asserted low under the following conditions: overcurrent, over temperature and reverse voltage conditions. This allows the user to know if something is wrong downstream as well as if the load switch itself has any issues.
8. The NPS40xx series of load switch has a constant current limit control built in that limits current at the load when the current through the pass FET has been exceeded. This behaves as an over current protection for downstream devices connected to OUT. When the current threshold has been exceeded, the device will switch into constant current mode, to limit the power to connected loads.

1.2. Data sheet parameters

Understanding the data sheet parameters is an important aspect of implementing any integrated circuits into a system design. Table 1 describes the data sheet parameters commonly specified in load switch IC data sheets.

Table 1. Common load switch data sheet parameters

symbol	name	description
VIN	operating voltage	The maximum voltage that can be applied to the input pins of the load switch, with respect to the ground of the device.
R_{DSon}	static drain-source on-state resistance	The typical resistance between the pins IN and OUT of the device when the device is turned ON. Since the load switch typically connects the input and output (IN and OUT) with a MOSFET, this also take into consideration the resistance of the FET and the packaging. Usually specified at a specific temperature range.
t_r	output rise time	The time interval between one reference point on a waveform and a second reference point on the same waveform (typically 10% and 90%) that is changing from a defined low level to a defined high level.
t_f	output fall time	The time interval between one reference point on a waveform and a second reference point on the same waveform (typically 10% and 90%) that is changing from a defined high level to a defined low level.
VIH	High level input voltage on the ON pin	The minimum voltage required to enable the load switch.
VIL	Low level input voltage on the ON pin	The maximum voltage required to disable the load switch.
I_Q	quiescent current	The amount of current the device consumes in operation.
I_{SD}	shut-down current	The amount of current flowing into the pin “IN” when the device is in a non-active state.

symbol	name	description
I_{ON}	enable pin current	The amount of current that is flowing into the enable (or “ON”) pin when the applied voltage is above the minimum threshold voltage.
I_{limit}	current-limit threshold	The maximum continuous DC current that can safely flow from the output terminal of the device at voltages within the normal operating range.
t_{SHORT}	output short circuit response time	The time taken for the device to recognize a short circuit fault, and turn-off the internal MOSFET.
$T_{shutdown}$	thermal shutdown temperature	The junction temperature at which the device will disable the internal MOSFET.

2. Load switch function in the power chain

Fig. 3 shows a typical power chain. The use of each of the controllers is application dependent and is determined by the designer. Some controllers integrate functions of other controllers into their features which may eliminate the need to use multiple parts.

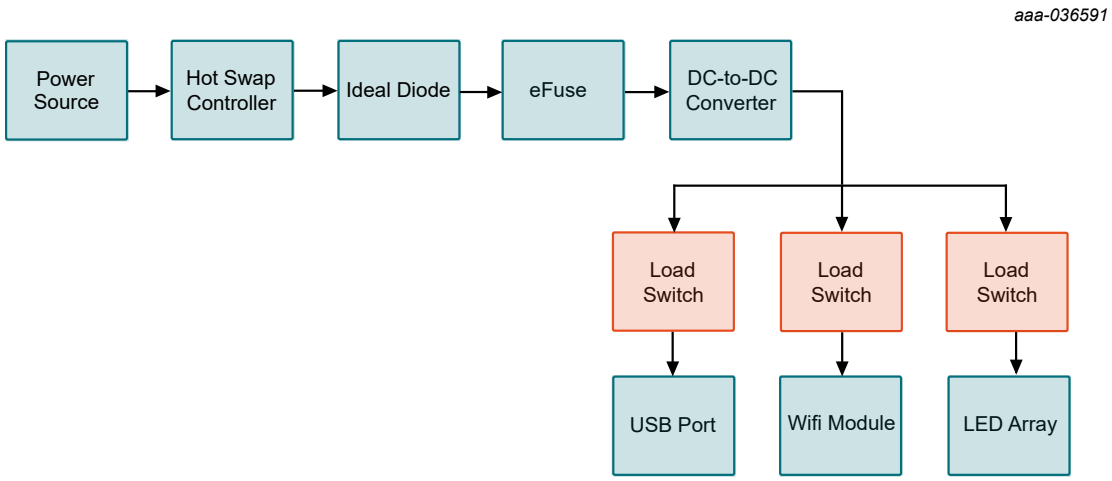

Fig. 3. Typical power chain block diagram

- **Hot Swap Controller** - protects rest of circuit from inrush current during connect/disconnect; may also integrate eFuse and ideal diode function.
- **Ideal Diode** - protects the DC-to-DC converter from reverse polarity; could be part of the eFuse block.
- **eFuse** - protects the DC-to-DC converter from over-current.
- **DC-to-DC converter**; most sensitive and expensive part of the power chain to protect.
- **Load Switch**; nearest the load; load switches are typically used for smaller currents.

The following sections give a brief outline of the function of the Hot-swap controller, Ideal diode and eFuse power chain blocks.

2.1. Hot-swap controller

Hot-swap controllers provide circuit protection from many potential hazards caused by sudden changes in the input supply. Hot-swap controllers limit the inrush current by slowly decreasing the on-state resistance of an external N-channel MOSFET, Fig. 4 shows an example hot-swap controller application.

Hot-swap controllers are integral to protecting the integrity of your system's electronic loads during “hot” plug-ins, which ensures safe operation while maintaining the reliability of the device over time.

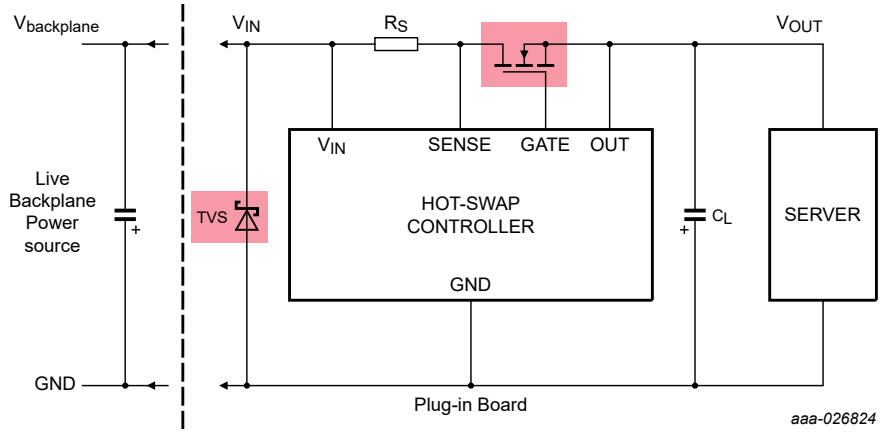

Fig. 4. Hot-swap controller application using Nexperia ASFET and TVS

2.2. eFuse

eFuses are integrated power path protection devices that are used to limit currents and voltages to safe levels during overload conditions. Fig. 5 shows the internal block diagram of Nexperia's eFuse IC NPS3102. An eFuse operates similarly to a standard fuse with the ability of detecting and quickly reacting to over-current and over-voltage conditions. The device can limit the output current to a safe value that is defined by the designer. Some of the advantages include:

- Minimizing IR drop across power path with monitoring features
- Protecting against supply brownout and overshoots
- Enable wide configurability with multiple features to suit different application requirements

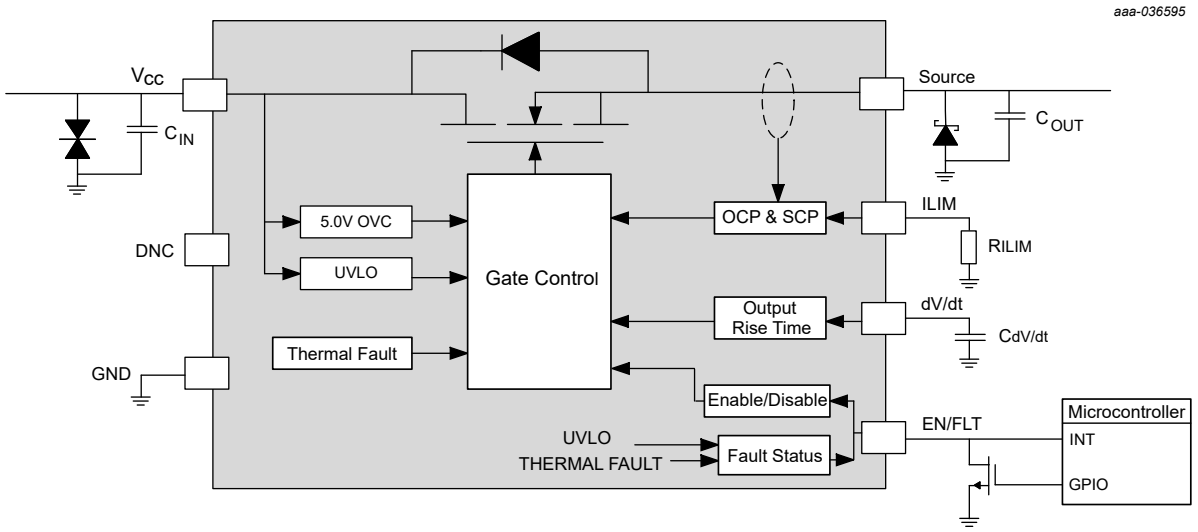

Fig. 5. Block diagram of Nexperia eFUSE IC NPS3102

2.3. Ideal diode (OR-ing controller)

Ideal diode and OR-ing controllers are used in power system designs to provide protection from various input supply fault conditions and to provide system redundancy by paralleling power supplies. Fig. 6 shows the internal blocks of an ideal diode IC. These devices are often used to replace a Schottky diode by delivering on the following benefits:

- Lowers power dissipation
- Lower reverse leakage current
- Higher headroom for downstream device
- Lower forward voltage drop

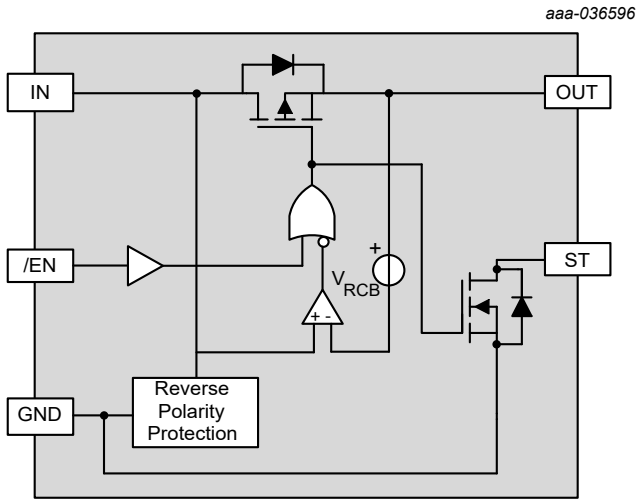

Fig. 6. Example of Nexperia ideal diode internal blocks

3. Benefits of load switch use in power chain design

3.1. Power sequencing and state transition

One of the benefits of using load switches in the power chain is the control of point-of-load power sequencing, see Fig. 7. Controlling the sequencing of the power rails also helps control the amount of inrush current to the load during power-up. This ultimately reduces the stress on the system and prevents any unwanted reverse bias conditions. Many designs, including those that use processors, must adhere to a strict power sequence to properly function, Fig. 8.

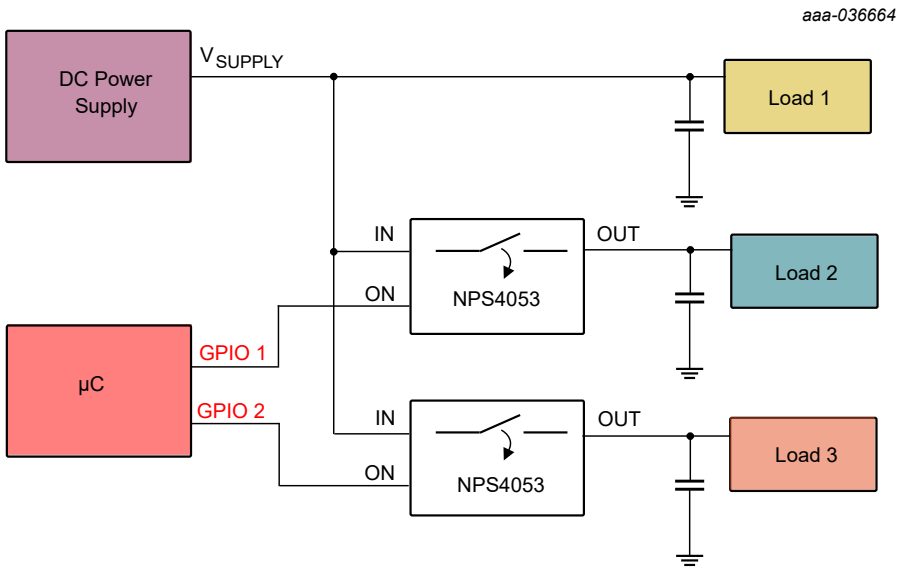

Fig. 7. Example of power sequencing with NPS4053 load switch

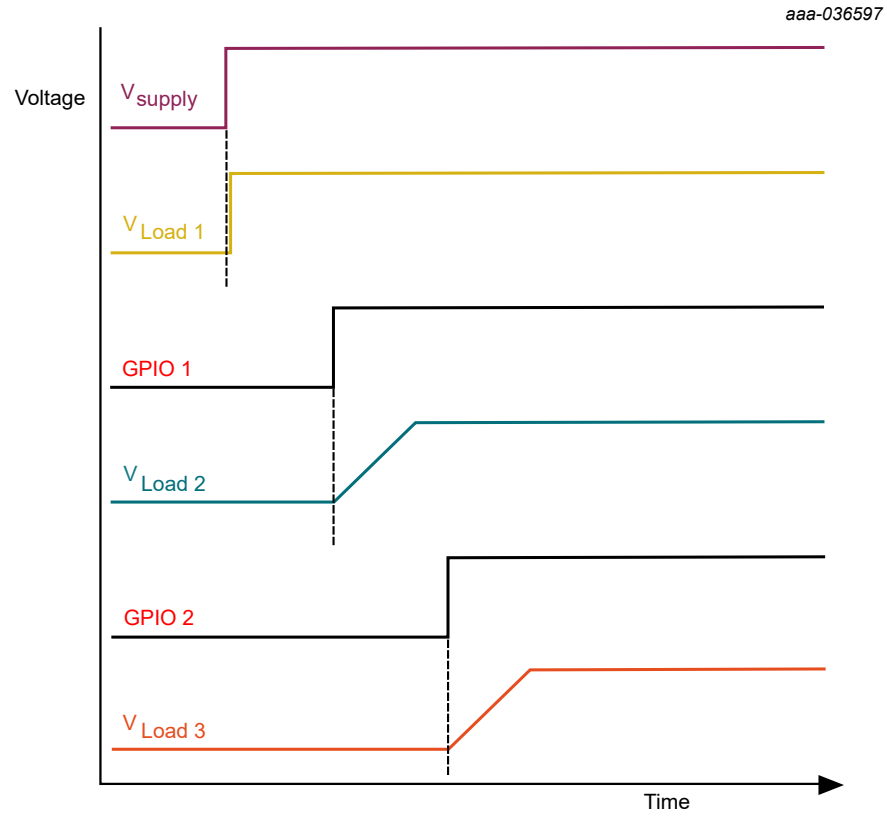

Fig. 8. Power sequencing waveforms

3.2. Leakage current control

In many applications, integrated circuits can be put into a standby mode, which effectively disables the integrated circuit. However although this circuit is in standby, there is a small amount of unwanted leakage current consumed by the system. If the system is battery operated, it is useful to limit the amount of leakage the device consumes in standby mode. Turning off these sub systems

using a load switch reduces power consumption and can increase the durability/longevity of the device.

3.3. Inrush current control

Inrush current is the initial input current drawn by an electrical load at turn-on. This occurs due to the instantaneous currents required to charge the system's discrete components such as capacitors and inductors. When devices are first turned on, the discharged discrete components offer a low impedance path that allows high currents to flow into the circuit. These high initial currents can damage discrete and non-discrete components downstream of the power supply and cause faults to occur in the system.

Load switches and e-fuses can be implemented to solve this issue by controlling the slew rate of the applied system voltage. This can eliminate any sag seen on the input voltage when voltage is first applied to the system. See Section 4.4 for further details.

3.4. Quick output discharge

Quick Output Discharge (QOD) is a feature that will quickly discharge the output when the device is disabled or in an "OFF" state, see Fig. 9. Without this feature, when the load switch IC is disabled the load voltage can be left floating, this can cause downstream circuits to not power down to a defined state. The main benefit of adding QOD functionality is to make sure that V_{OUT} will be at a known "OFF" state when the device is disabled.

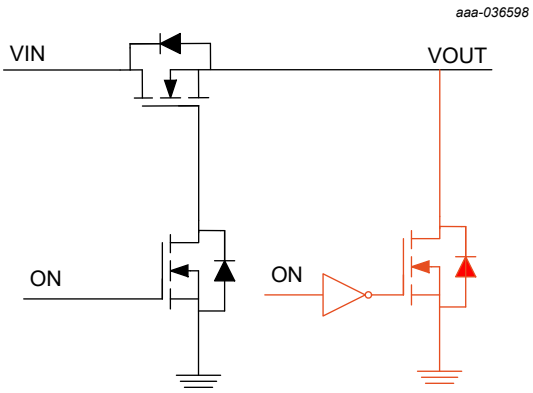

Fig. 9. Quick output discharge circuit

3.5. Fault detection features

Some Nexperia devices utilize the benefits of fault detection to tell the user if there are any thermal or electrical issues with the connected circuits. These fault detection features include: reverse voltage protection, over-current protection, output short circuit protection and over-temperature protection. These features are typically integrated into the load switch to reduce BOM costs and solution sizes.

- **Reverse voltage protection** will turn-off the internal MOSFET whenever the output voltage exceeds the input voltage by a given threshold. This prevents a reversal of current flow out of the input pin.
- **Current limiting** will limit the amount of current that is able to be applied to the load. The current limit is typically set by an external resistor or capacitor in many load switch ICs. When the load current exceeds current limit threshold set by the external resistor, the device enters constant current mode by limiting the output current to the current limit threshold until the over current condition is removed.
- **Output short circuit protection** allows the device to avoid any damage to circuits downstream by putting the device into constant current mode and limiting the amount of current flowing through the device. The device will limit the output current to I_{SC} (short circuit current limit) until the short circuit condition is removed.
- **Latch off** some load switches and e-fuses latch off when the current limit threshold is exceeded. There are also e-fuses that have an auto retry function in case of fault situations.
- **Over-temperature protection** to avoid any damage to circuit from thermal events, some load switches and E-Fuses offer over-temperature protection. When the device junction temperature exceeds the thermal shutdown threshold, the internal MOSFET will turn-off until the device cools down to a lower steady state temperature (typically 10 °C less than the threshold temperature). Some devices will restart after the steady state temperature has been reached, and others must be re-enabled via the “ON” pin.

3.6. Advantages over discrete solutions

An advantage of integrated load switches over discrete solutions is that they combine multiple functions into a single device, including the switch itself, driver circuitry, protection features, and diagnostic capability. This integration eliminates the need for external components, such as MOSFETs and resistors, which simplifies the design process and reduces overall system cost. Additionally, integrated load switches offer better thermal performance, higher switching speeds, and smaller form factors than discrete components. They also provide more reliable and consistent performance due to the tight integration of components and better control over manufacturing processes.

Overall, the use of integrated load switches can lead to significant improvements in system performance, cost-effectiveness, and space utilization. Fig. 10 shows the size comparison of a discrete load switch solution vs the Nexperia NPS4053.

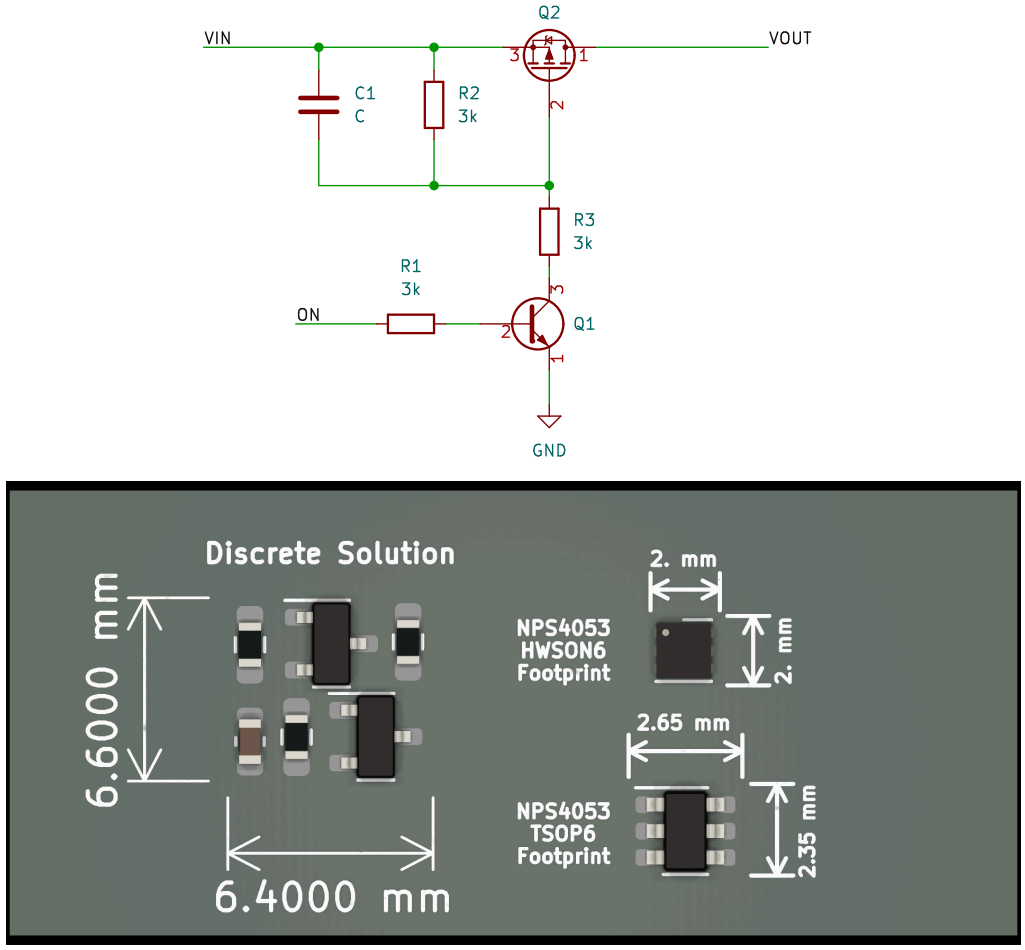

Fig. 10. Discrete load switch schematic and PCB area in comparison with integrated load switch

4. Design considerations: part selection

4.1. Package size

Selecting the correct package size for a load switch IC in a circuit is of great importance in ensuring the overall functionality and performance of the system. The package size directly influences the thermal management, electrical characteristics, and mechanical reliability of the load switch. A well-matched package size ensures efficient heat dissipation, preventing overheating and potential damage to the switch and surrounding components. It also contributes to optimizing the electrical performance, such as minimizing parasitic inductance and resistance, which can affect switching speed and power efficiency. Furthermore, the package size plays a crucial role in reliability, as it determines the physical footprint and compatibility with other components, aiding in the overall design and layout of the circuit. Therefore, careful consideration of the package size when selecting a load switch is essential for achieving reliable, high-performance, and space-efficient circuit designs.

Nexperia offers a wide array of packages that include TSOP-5, TSOP-6, TSSOP-6, HWSON6, and HWSON8 for current and next generation load switches. Each package has unique characteristics that cater to different circuit requirements. Nexperia's TSOP-5 and TSOP-6 offer enhanced thermal performance due to its larger size and pin pitch. This larger size allows for improved heat transfer and improved overall reliability. The TSSOP-6 package is designed to be compact and offers a smaller footprint compared to the TSOP-6 and TSOP-5 packages. This smaller size makes it ideal for applications with limited space on the circuit board. The TSSOP-6 package typically has a thinner body and narrower lead pitch, allowing for higher component density and more efficient

use of board space. Nexperia's HWSON6 and HWSON8 packages combine a small footprint with high power handling capability, making it an ideal choice for applications demanding both space efficiency and robustness.

4.2. NMOS vs PMOS

The selection of a P-channel or N-channel load switch depends on the requirements of the system application. P-channel and N-channel MOSFETs both have advantages and disadvantages. N-channel MOSFETs have a few strengths over P-channel MOSFETs. For example, N-channel MOSFETs typically have lower R_{DSON} and gate capacitance for the same die area. This makes the N-channel MOSFET preferable for higher current applications.

N-channel MOSFETs typically connect the drain to the input voltage and the source to the output pin. In order for the NMOS to turn on, the gate-to-source voltage must be greater than the threshold voltage of the NMOS. Since the input rail operates independently of the NMOS turn on, the NMOS can operate at very low input voltages, as well as higher input voltages as long as the gate-to-source threshold voltage requirement is met. Commonly, the gate is controlled via a charge pump.

P-channel MOSFETs typically connect the source to the input voltage and the drain to the output. Inversely to NMOS, PMOS devices turn on when the source-to-gate voltage is greater than the threshold voltage. Assuming the gate voltage is 0 V at turn on, the input rail must be greater than the threshold voltage of the PMOS. PMOS devices have a much simpler on/off control block compared to NMOS devices. NMOS devices require an additional voltage at the gate to turn on, whereas PMOS devices do not.

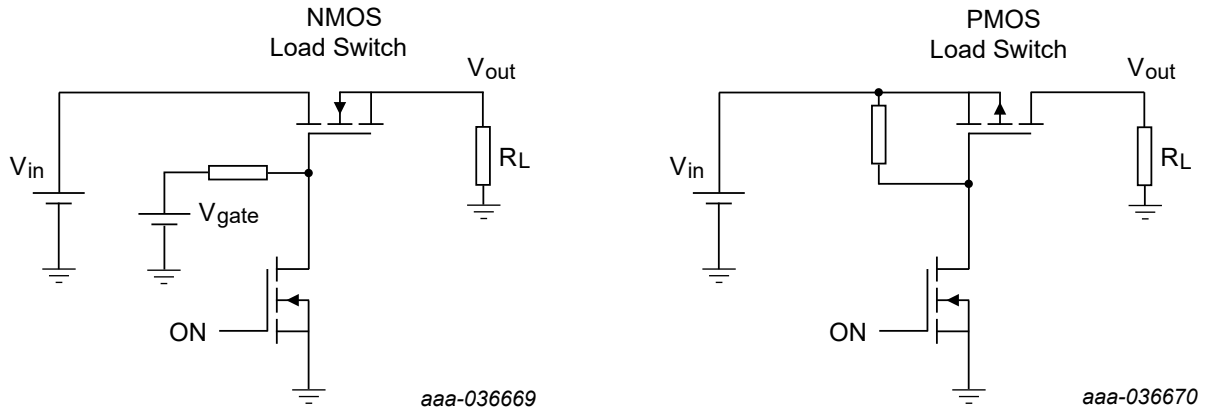

Fig. 11. NMOS vs PMOS discrete load switches

4.3. Gate-to-source voltage

The efficiency of the circuit is directly related to the applied gate-to-source voltage of the pass transistor (MOSFET). This is because R_{DSON} is inversely proportional to the applied gate-to-source voltage. Operating too close to the gate-to-source threshold can result in higher conduction losses, and any small change in V_{GS} can result in a change to R_{DSON}.

4.4. Inrush Current

Inrush occurs when the load switch is first turned on and connected to a load. The load could be anything from a DC-to-DC converter, charge circuit for a battery, or any other sub-circuit. The turn-on speed of the MOSFET directly influences the amount of inrush current on the input side of the load switch. A sudden inrush of current can cause a dip in the input supply voltage which can impact the rest of the system downstream, reducing the reliability of the system overtime and damaging circuit components.

Some devices have inrush current control. By means of an external capacitor, the output voltage ramp can be controlled. Consideration should be given to the device dissipation during this ramp. Dissipation is defined as the voltage across the pass transistor times the current. During inrush

control the pass FET will be in the linear region having a high voltage across it. When multiplying this with the load current, one can easily trigger the thermal protection of the device.

A typical circuit with connected load, is shown Fig. 12.

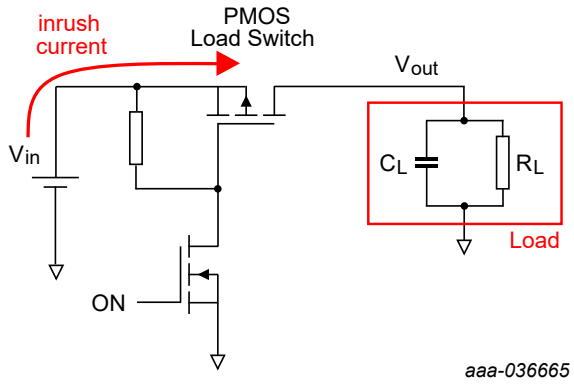

Fig. 12. PMOS load switch inrush current

The inrush current can be approximated as:

$$I_{inrush} = C_{LOAD} \times \frac{dV_{LOAD}}{dt} \quad (1)$$

4.5. Efficiency

Efficiency is important when power management is crucial for a design application. Some designs need to be running at optimal efficiency to eliminate any power losses in the form of heat. Power loss can be defined as:

$$P_{LOSS} = I_{LOAD}^{2} \times R_{DSon} \quad (2)$$

The R_{DSON} of the MOSFET causes a voltage drop between the input and output voltages when the device is turned on. For designs that require high load currents, this voltage drop becomes important. The voltage drop will increase as the load current increases, and the voltage drop at maximum load current must be considered when selecting a part.

$$V_{OUT} = V_{IN} - I_{LOAD} \times R_{DSon} \quad (3)$$

4.6. Voltage and current ratings

Before selecting a load switch for a design application, it is important to consider the voltage and current required by the design. The load switch must be able to support the DC voltage and current, typically with some margin, that the circuit will be exposed to during operation. It is also important to consider the transient and peak currents and voltages that the circuit might see during operation.

4.7. Shutdown and quiescent currents

Shutdown current is the amount of current the device consumes when it is powered off. The shutdown current directly affects the amount of power that is consumed when the device is in a shutdown state. If the design has critical power needs (e.g. battery operated systems), the shutdown current should be considered so as to eliminate any unwanted power consumption when the load switch is off.

Quiescent current is the current that is consumed when the load switch is powered on. This current along with I^2R losses will determine the amount of power that is consumed when the load switch is powered on.

4.8. Rise and input transition times

Rise time can vary depending on the input voltage and the system load. If applicable, it is also important to consider the downstream system's input rise transition times when selecting a load switch as these rise times can affect functionality. Some ICs have an initial turn-on slew rate that they need to adhere to.

4.9. Auto-retry function

During a flag condition in a load switch with auto-retry functionality, the part is momentarily disabled, and re-enables after a pre-set amount of time. The auto-retry functionality can be implemented with a resistor and capacitor on the /FLG pin, see Fig. 13.

During an over current flag, the /FLG pin pulls low, and disables the part. This in turn, pulls the ON pin low, and the /FLG pin goes into a Hi-Z state allowing C_{AR} to begin charging. The part re-enables when the voltage on the ON pin reaches its turn-on threshold. The time interval after which auto-retry turns on the device again, is determined by the RC time constant. The device continues to cycle in this manner until the flag condition is removed.

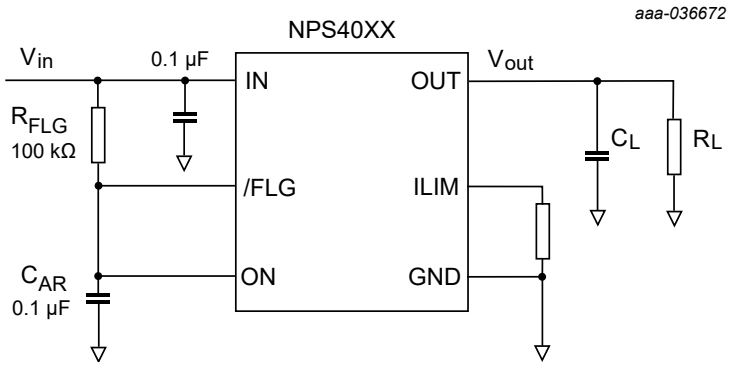

Fig. 13. NPS40XX with auto-retry functionality

4.10. Latch-off function

Latch off devices behave slightly different when the FLG pin is asserted. During a flag condition, the latch-off devices assert the /FLG after the deglitch period and immediately turn off the device. The device remains off regardless of whether the overload condition is removed from the output. To resume normal operation, the ON pin must be toggled, or power must be cycled to the device.

5. Equations

5.1. Inrush current

The inrush current for the device can be calculated as:

$$I_{inrush} = C_{LOAD} \times \frac{dV_{LOAD}}{dt} \quad (1)$$

dV_{LOAD} is the change in voltage across the load over time.

C_{LOAD} is the load capacitance.

5.2. Maximum allowable power dissipation

Under normal operating conditions the maximum IC junction temperature should be restricted to 125 °C. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, the equation shown below can be used:

$$P_{D(max)} = \frac{T_{j(max)} - T_A}{\theta_{j\text{-}A}} \quad (4)$$

$P_{D(max}$ = maximum allowable power dissipation.

$T_{j(max)}$ = maximum allowable junction temperature (125 °C for the NPS40XX devices).

T_A = ambient temperature of the device.

$\theta_{J\text{-}A}$ = junction to air thermal impedance; this parameter is highly dependent on the PCB layout.

5.3. Voltage drop

To determine the voltage drop across the load switch, (which must be kept to acceptable level), it is important to know how to calculate the $R_{ON(max)}$. The following equation can be used to calculate the V_{IN} to V_{OUT} voltage drop:

$$R_{ON(max)} = \frac{\Delta V_{max}}{I_{LOAD}} \quad (5)$$

$\Delta V_{(max)}$ = maximum voltage drop from V_{IN} to V_{OUT}.

I_{LOAD} = load current.

$R_{ON(max)}$ = maximum on-resistance of the device.

5.4. Power dissipation

The power dissipated in the load switch can be determined by:

$$P_{LOSS} = V_{IN} \times I_Q + I_{LOAD}^2 \times R_{DSon} \quad (6)$$

V_{IN} = input voltage.

I_Q = quiescent current of the load switch, (for large load currents, I_Q may be negligible when compared to the losses due to R_{DSon}, hence I_Q can be ignored.).

I_{LOAD} = load current of the load switch.

R_{DSon} = on-state resistance of the load switch.

6. Common PCB layout considerations

For PCB layout considerations, the NPS40XX series load switch in TSOP-6 package will be used as an example to show common design practices.

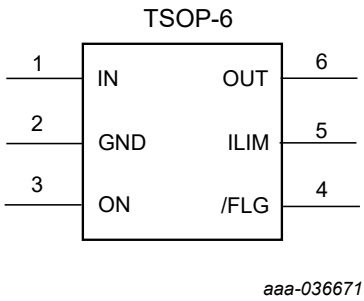

Fig. 14. Pin configuration of NPS40XX (TSOP-6 package)

6.1. PCB layout guidelines

Nexperia has provided an example basic schematic, Fig. 15 and PCB layout for a load switch IC application using the NPS4053, PCB layouts should take account of the following reccomendations:

- Place a 100 nF bypass capacitor near the IN and GND pins and make the connections using a low-inductance trace to pin 1 (IN). This capacitor should be placed near pin 1 (IN). Vias to ground are placed close to the ground connection of the device to keep the ground loop as short as possible.
- If large transients are expected, an additional 10 µF capacitor can be placed near the IN and GND pins with the connection made using a low-inductance trace at pin 1 (IN). Vias to ground should be placed close to the ground connection of the device in order to keep the ground loop as short as possible.
- Place a 100 nF capacitor and a 150 µF bypass capacitor on the output pin when large transient currents are expected on the output. Vias to ground are placed close to the ground connection of the device to keep the ground loop as short as possible.
- If the load switch IC has a pin for R_{LIM}, keep the R_{LIM} trace as short as possible to eliminate any parasitic effects on the current limiting accuracy.

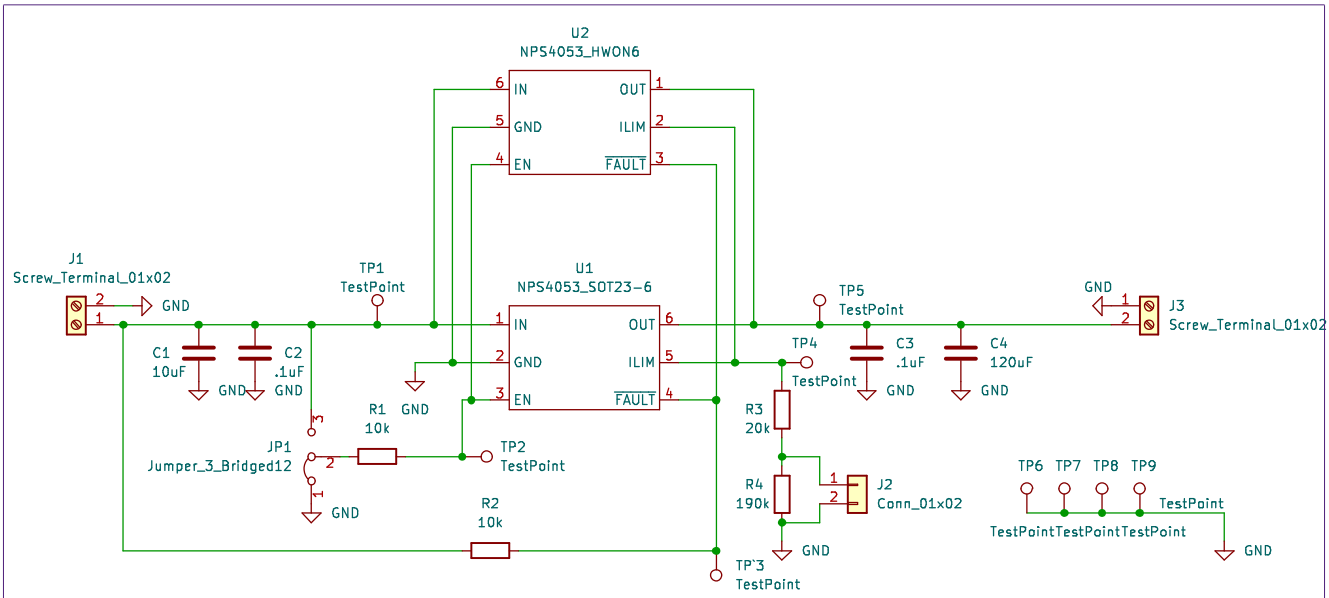

Fig. 15. NPS4053 series load switch application schematic

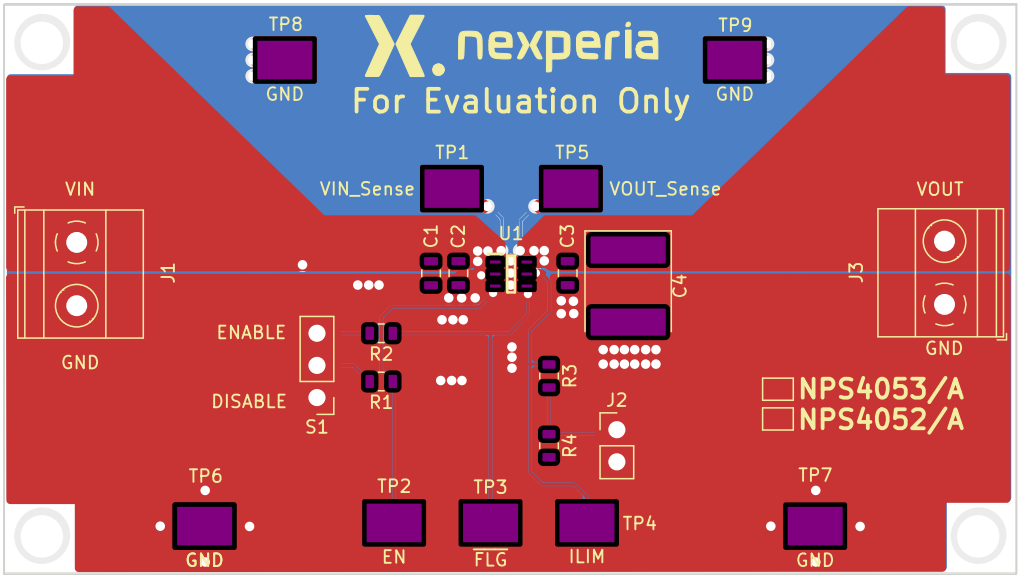

Fig. 16. NPS40xx evaluation board PCB

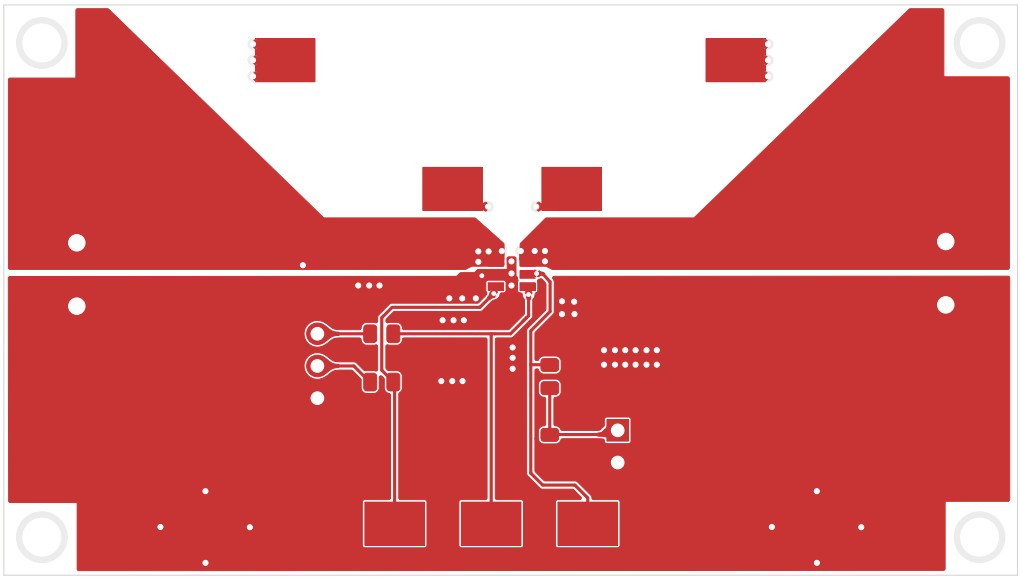

Fig. 17. NPS40xx evaluation board PCB top layer

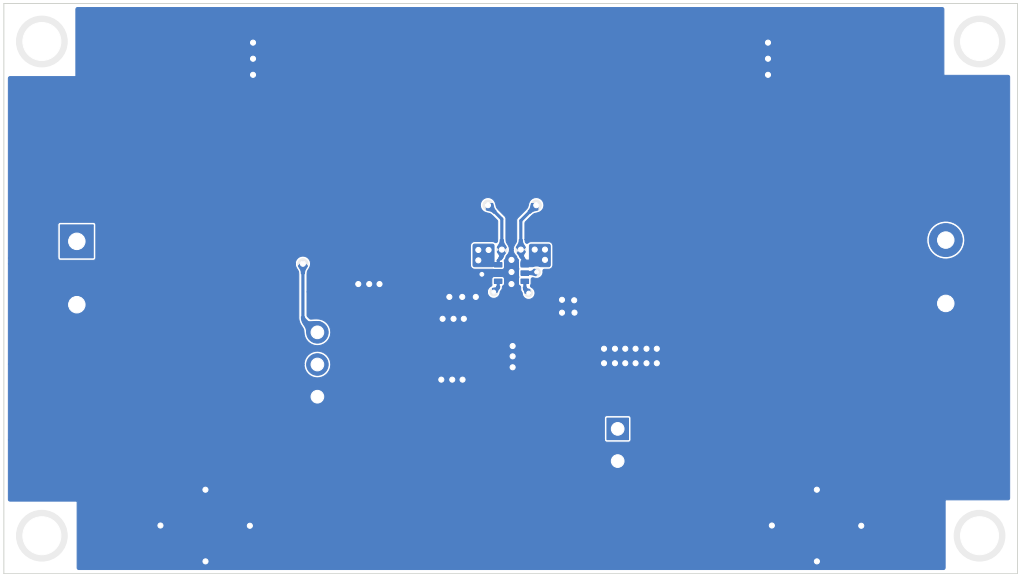

Fig. 18. NPS40xx evaluation board PCB bottom layer

7. Revision history

Table 2. Revision history

Revision number	Date	Description
1.0	2023-06-29	Initial version.

8. Legal information

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