UM90011

NEVB21-USBC1 evaluation board

Rev. 1 — 9 March 2022 user manual

Document information

Information	Content
Keywords	USB Type-C, ESD Protection, TrEOS, USB3.2, HDMI 2.1, low capacitance, signal integrity
Abstract	This user manual gives guidance on how to use the NEVB21-USBC1 evaluation board

nexperia

1. Introduction

When looking for the 'ideal' ESD protection solution for high-speed lines, there are three main challenges - signal integrity, system-level ESD robustness and footprint. Addressing signal integrity, we need an ESD protection device with low capacitance but also low inductance, which is quite often overlooked. From a system-level ESD robustness perspective, a low clamping voltage is becoming more important than robustness of the ESD protection device itself. Surge robustness of the protection device has become important due to potential fault conditions, where data lines might be shorted with supply lines.

Nexperia's new DFN0603-3 package provides two protection devices in one housing, keeping the benefits of TrEOS technology, very low capacitance, very low clamping and very high robustness, and also showing outstanding RF performance on very fast data lines. The DFN0603-3 series offers capacitance down to 0.2 pF, surge robustness up to 11 A and a clamping voltage of 4.4 V for a 8 A 8/20 µs surge. The benefit of this 2-in-1 solution is shown in Fig. 1.

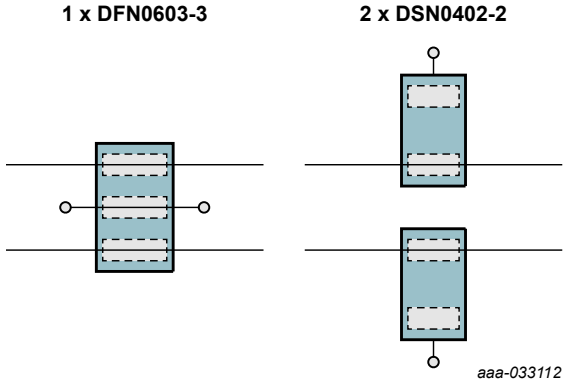


Fig. 1. Scheme showing advantage of DFN0603-3 against typical single line protection

Since it is crucial for the end application to pass performance and compliance testing according to IEC61000, a well-designed platform is needed in advance. Nexperia's evaluation board **NEVB21-USBC1** is the perfect test vehicle for direct benchmarking of a complete USB Type-C interface. Beside super speed data line protection it features protection of all the other relevant data, control and supply lines in USB Type-C. A complete overview is given in Fig. 2.

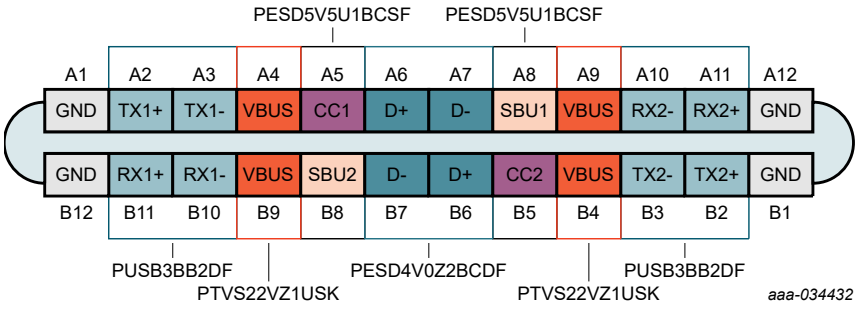


Fig. 2. USB Type-C interface protection with Nexperia's ESD protection

This user manual provides guidance on how utilize the NEVB21-USBC1.

2. Evaluation board description

Nexperia's **NEVB21-USBC1** is designed to demonstrate the USB Type-C functionality as a plug and play solution. To offer good RF performance the board is designed to keep parasitics to an absolute minimum allowing the super speed lines (TX/RX) to have maximum bandwidth. For this reason additional USB Type-C breakout boards are needed if surge or burst tests (according to IEC61000) are conducted. Top side and bottom side are designed symmetrically. The top view is shown in Fig. 3.

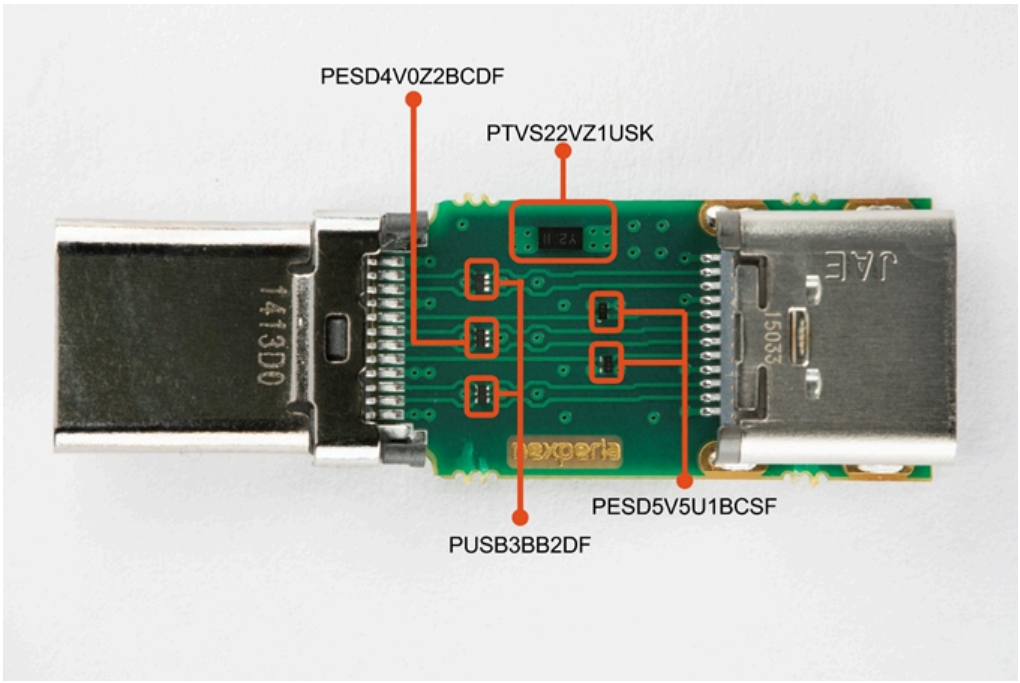


Fig. 3. NEVB21-USBC1 top view

The evaluation board features the **PUSB3BB2DF** which is a symmetrical bidirectional ESD protection diode array with 3 ESD protection diodes in a single DFN0603-3 package. As mentioned in the beginning it comes in the DFN0603-3 footprint where 2 ESD protection diodes are realized in one package. It is specially designed to comply with Thunderbolt, USB 3.2 (data rates >5 Gbps) and HDMI 2.1 data line requirements to provide full signal integrity and at the same time best in class protection. To protect all RX/TX lines four **PUSB3BB2D** are needed. For the D+ and D- lines (USB 2.0 lines) the **PESD4V0Z2BCDF** is chosen. Since it comes in the DFN0603-3 package as well and supports latest USB and HDMI standards. Two of **PESD4V0Z2BCDF** are needed for the D+/D- lines in the USB Type-C interface. It should be highlighted at this point that the middle pin must be connected to signal ground as is shown in Fig. 4.

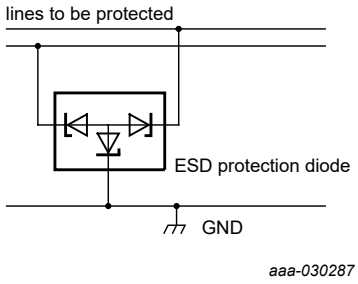


Fig. 4. Recommended use of the ESD protection devices in DFN0603-3

For the CC lines (used to establish and manage the Source-to-Sink connection e.g. cable orientation, Type-C current modes, Power delivery etc.) and the SBU lines (used for Alternate mode especially for lower speed side band signals) the **PESD5V5U1BCSF** is used as bidirectional

protection device. These device are suitable for very sensitive single interface line as they come with ultra-low leakage current (<1 nA). Since there are two SBU and two CC lines in an interface four **PESD5V5U1BCSF** are needed for full protection.

For the BUS supply line VBUS a transient voltage suppressor diode which supports 60 W power supply (all 4 VBUS pins combined) is needed. For protecting VBUS **PTVS22VZ1USK** is chosen. It comes with a rated peak pulse power of 200 W (10/1000 µs pulse) in robust and compact housing (DSN1608-2).

3. Setup and results

For quick start just place the NEVB21-USBC1 between a Host device (e.g. computer) and a Client device (e.g. storage device supporting USB3.2) as shown in Fig. 5. The easiest way is to stream or copy a large file like a 4k video directly on or to the host device from the storage device.

Fig. 5. Typical test setup for the NEVB21-USBC1

In Fig. 6 and Fig. 7, the eye diagram of a transmission on the super speed lines with a data rate 10 Gbps (USB3.2) is shown. Fig. 7 shown the transmission without the protection device and Fig. 6 with the **PUSB3BB2DF**. The eye opening height in both cases is nearly equal. This emphasizes an outstanding RF performance of the **PUSB3BB2DF.**

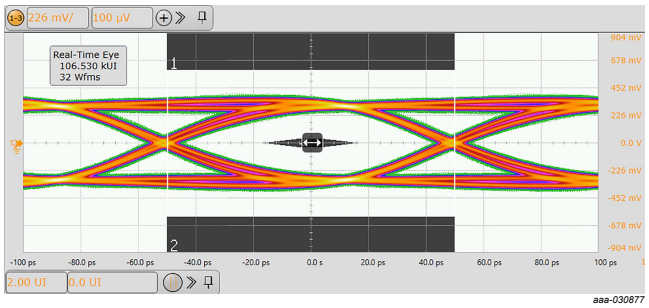


Fig. 6. USB3.2 eye diagram, PCB with PUSB3BB2DF; data rate: 10 Gbit/s, GND on pin 2

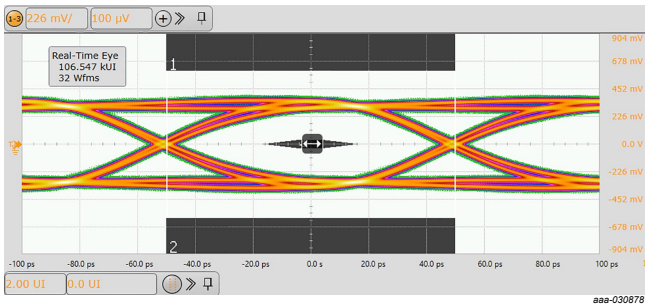


Fig. 7. USB3.2 eye diagram, only PCB; data rate: 10 Gbit/s, GND on pin 2

To evaluate the ESD contact discharge performance of the **PUSB3BB2DF** the ESD pulse transient response test according to IEC6100-4-2 was performed. In Fig. 8 the transient response for contact discharge of ±15 kV is shown. Here the outstanding fast reaction can be clearly seen. After 100 ns the transient pulse is completely attenuated.

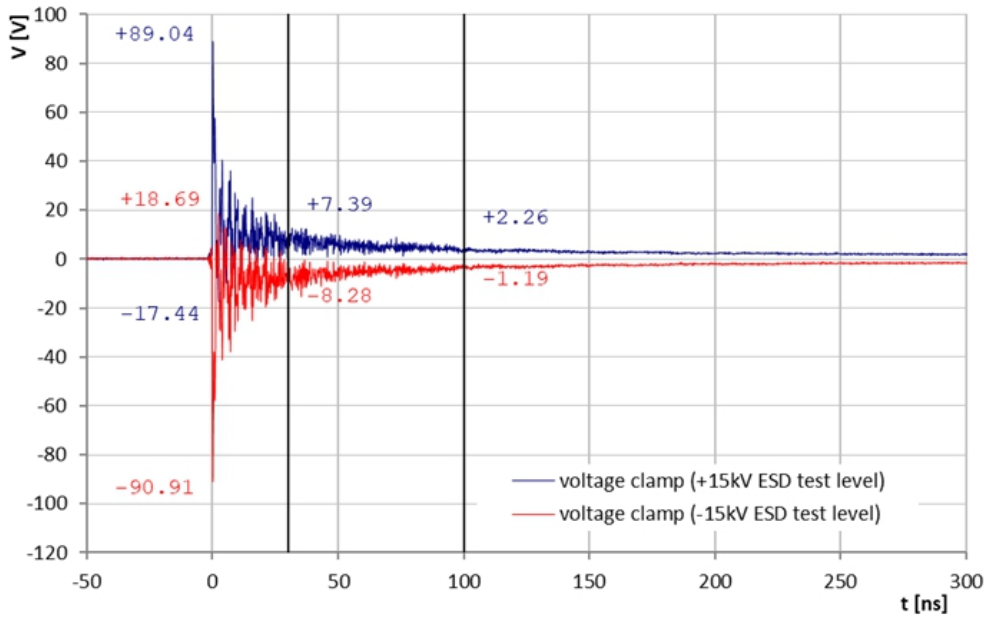
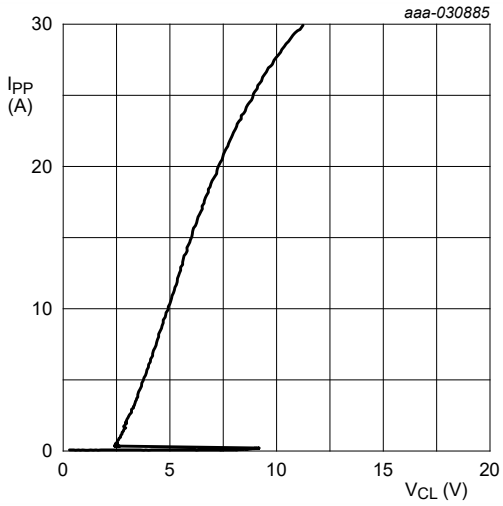


Fig. 8. ESD pulse transient response of the DUT (contact discharge of ±15 kV) according to IEC 61000-4-2

In Fig. 9 the dynamic resistance is shown. Transmission Line Pulse measurement, shot TLP, is used to record the data. The **PUSB3BB2DF** features a low trigger voltage and a deep snap back behavior of the device. This way best in class protection can obtained.



t_r = 1 ns

t_p = 100 ns; Transmission Line Pulse (TLP)

Fig. 9. Dynamic resistance with positive clamping; typical values

4. Schematic

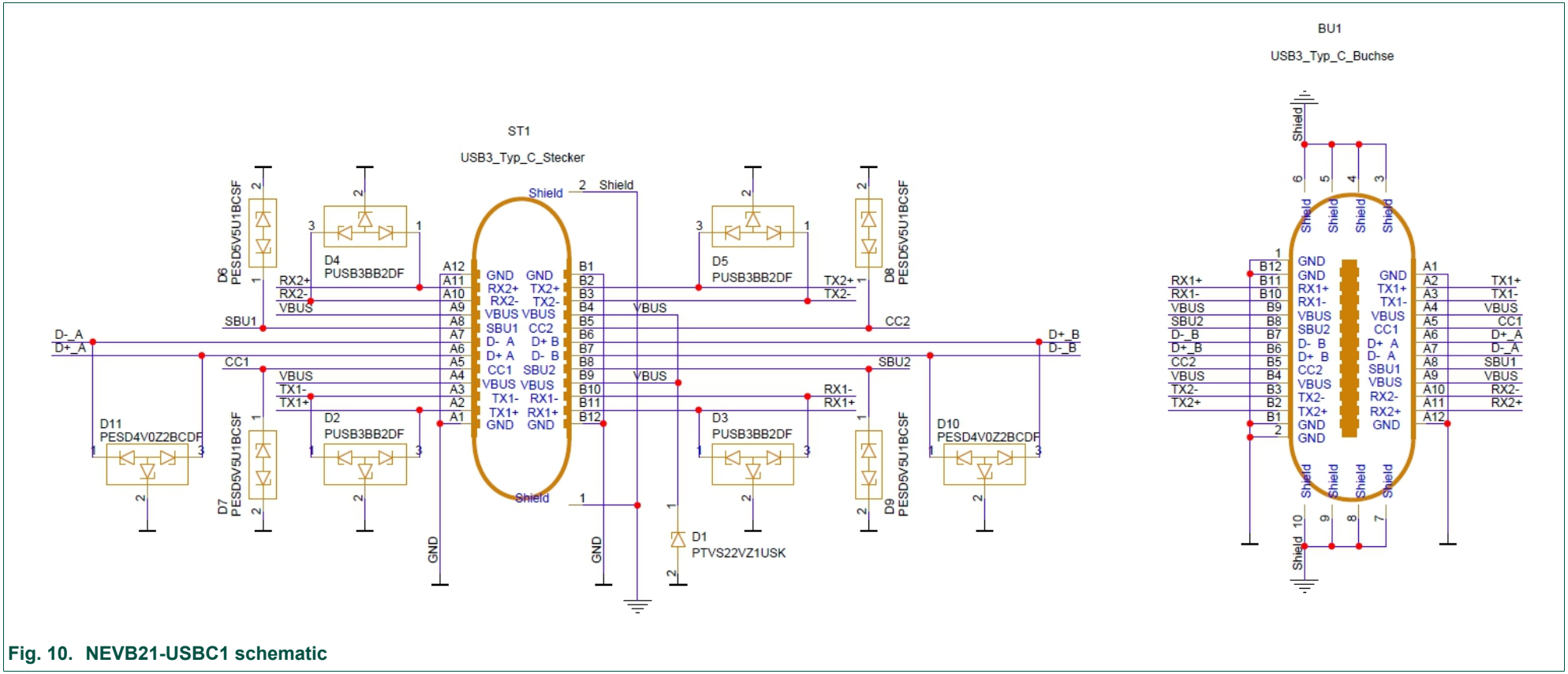


Fig. 10. NEVB21-USBC1 schematic

5. Layout

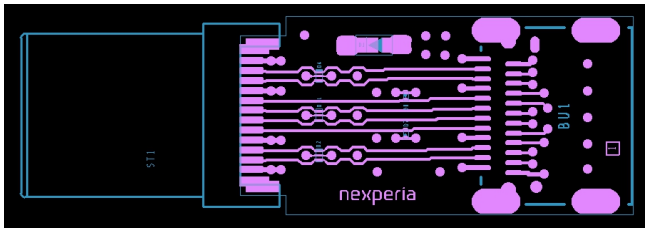


Fig. 11. 11th Top layer with Top silkscreen

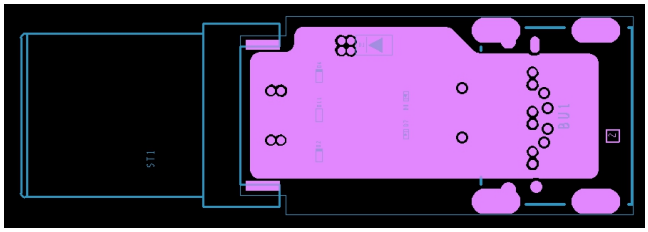


Fig. 12. Layer 2

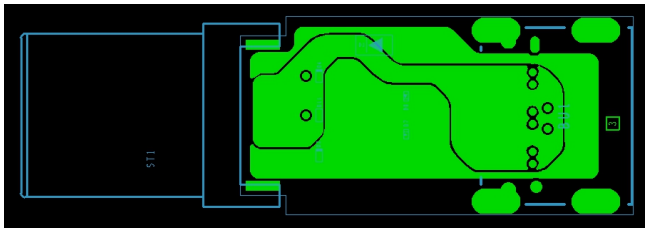


Fig. 13. Layer 3

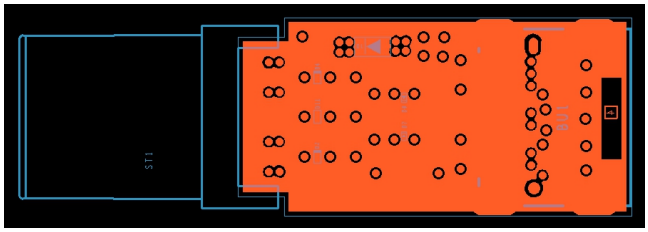


Fig. 14. Layer 4

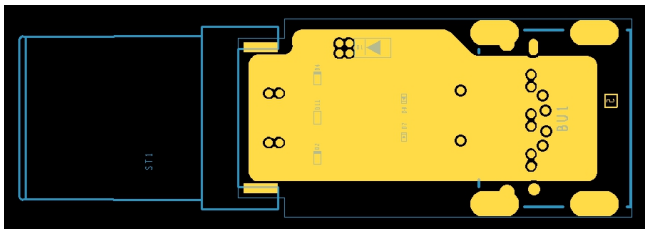


Fig. 15. Layer 5

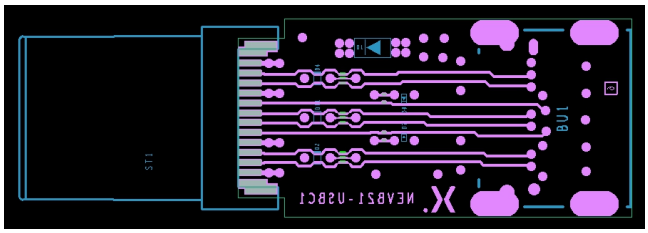


Fig. 16. Bottom layer with bottom silkscreen

6. Revision history

Table 1. Revision history

Revision number	Date	Description
UM90011 v.1	20220309	Initial version

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