NIS5112

Electronic Fuse

The NIS5112 is an integrated switch utilizing a high side N−channel FET driven by an internal charge pump. This switch features a MOSFET which allows for current sensing using inexpensive chip resistors instead of expensive, low impedance current shunts.

It is designed to operate in 12 V systems and includes a robust thermal protection circuit.

Features

- Integrated Power Device
- Power Device Thermally Protected
- No External Current Shunt Required
- Enable/Timer Pin
- Adjustable Slew Rate for Output Voltage
- 9 V to 18 V Input Range
- 30 mΩ Typical
- Internal Charge Pump
- ESD Ratings: Human Body Model (HBM); 4000 V
- These are Pb−Free Devices

Typical Applications

- Hard Drives

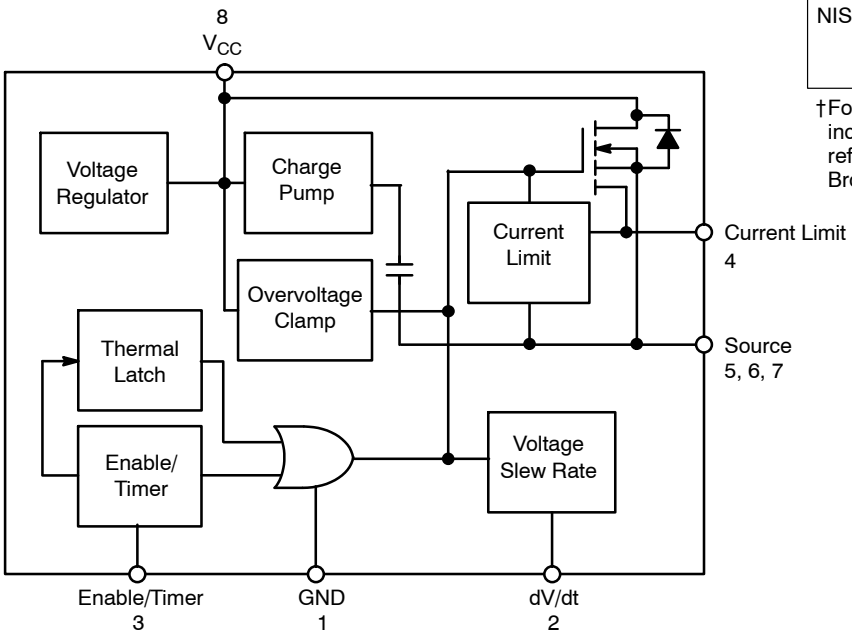

Figure 1. Block Diagram

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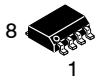
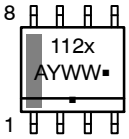
MARKING DIAGRAM



SOIC−8 NB
CASE 751



x = L for thermal latch off
= H for thermal auto−retry
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NIS5112D1R2G	SOIC−8 Latch Off (Pb−Free)	2500 Tape & Reel
NIS5112D2R2G	SOIC−8 Auto−Retry (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Table 1. FUNCTIONAL PIN DESCRIPTION

Pin	Function	Description
3	Enable/Timer	A high level signal on this pin allows the device to begin operation. Connection of a capacitor will delay turn on for timing purposes. A low input signal inhibits the operation.
1	Ground	Negative input voltage to the device. This is used as the internal reference for the IC.
4	I_{Limit}	A resistor between this pin and the source pin sets the current limit level.
5,6,7	Source	Source of power FET, which is also the switching node for the load.
2	dV/dt	A capacitor from this pin to ground programs the slew rate of the output at turn on. This capacitor is discharged by an internal discharge circuit when the device is disabled via the enable pin.
8	V_{CC}	Positive input voltage to the device.

Table 2. MAXIMUM RATINGS (Maximum ratings are those, that, if exceeded, may cause damage to the device. Electrical characteristics are not guaranteed over this range)

Rating		Symbol	Value	Unit
Input Voltage, Operating,	Steady−State (Input+ to Input−) Transient (Conditions 1 ms)	V_{in}	−0.3 to 18 −0.3 to 25	V
Drain Voltage, Operating,	Steady−State (Drain to Input−) Transient (Conditions 1 ms)	V_{DD}	−0.3 to 18 −0.3 to 25	V
Drain Current, Peak (Internally Clamped)		I_{Dpk}	25	A
Drain Current, Continuous (T_A=25°C), (Note 2)		I_{Davg}	5.3	A
Thermal Resistance, Junction−to−Air 0.5 in^2 Copper 1.0 in^2 Copper		Q_{JA}	 120 110	 °C/W °C/W
Thermal Resistance, Junction−to−Lead (Pin 8)		Q_{JL}	27	°C/W
Power Dissipation (T_A = 25°C) (Note 1)		P_{max}	1.0	W
Operating Temperature Range (Note 2)		T_J	−40 to 175	°C
Nonoperating Temperature Range		T_J	−55 to 175	°C
Lead Temperature, Soldering (10 Sec)		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Mounted on FR−4 board, 1 in sq pad, 1 oz coverage.
2. Actual maximum junction temperature is limited by an internal protection circuit and will not reach the absolute maximum temperature as specified.

Table 3. ELECTRICAL CHARACTERISTICS (Unless otherwise noted: V_{CC} = 12 V, R_{LIMIT} = 56 Ω T_J = 25°C)

Characteristics	Symbol	Min	Typ	Max	Unit
POWER FET					
Delay Time (Enabling of Chip to Beginning of Conduction (10% of IPK))	T_{dly}	–	5.0	–	ms
Charging Time (Beginning of Conduction to 90% of V_{out}) $C_{dV/dt}$ = 1 μF, C_{load} = 1000 μF	t_{chg}	–	64	–	ms
ON Resistance (I_D = 2 A, T_J = −20°C) (Note 3) (I_D = 2 A, T_J = 25°C) (I_D = 2 A, T_J = 100°C) (Note 3)	R_{DSon}	– 	 23.5 28 37	 27.5 32 43.5	mΩ
Off State Output Voltage (V_{in} = 12 V_{dc}, Enable Low, V_{dc}, T_J = −20°C) (Note 3) (V_{in} = 12 V_{dc}, Enable Low, T_J = 25°C) (V_{in} = 12 V_{dc}, Enable Low, T_J = 100°C) (Note 3)	V_{off}	 – – –	 – – –	 120 120 200	mV
Output Capacitance (V_{DS} = 12 V_{dc}, V_{GS} = 0 V_{dc}, f = 10 kHz)		–	396	–	pF
THERMAL LATCH					
Shutdown Temperature (Note 3)	T_{SD}	125	135	145	°C
Thermal Hysteresis (Auto Retry Only) (Note 3)	T_{hyst}	–	40	–	°C
ENABLE/TIMER					
Enable Voltage (Turn−on) (R_{load} = 2 K, T_J = −20°C) (Note 3) (R_{load} = 2 K, T_J = 25°C) (R_{load} = 2 K, T_J = 100°C) (Note 3)	V_{ENon}	 2.45 2.5 2.7	 – – –	 – – –	V
Enable Voltage (Turn−off) (R_{load} = 2 K, T_J = −20°C) (Note 3) (R_{load} = 2 K, T_J = 25°C) (R_{load} = 2 K, T_J = 100°C) (Note 3)	V_{ENoff}	 – – –	 – – –	 1.8 1.9 2.0	V
Charging Current (Current Sourced into Timing Cap) (T_J = −20°C) (Note 3) (T_J = 25°C) (T_J = 100°C) (Note 3)	I_{Charge}	 67 70 71	 80 83 84	 90 92 96	μA
OVERVOLTAGE CLAMP					
Output Clamping Voltage (V_{CC} = 18 V, T_J = −20°C) (Note 3) (V_{CC} = 18 V, T_J = 25°C) (V_{CC} = 18 V, T_J = 100°C) (Note 3)	V_{Clamp}	 14 14 13	 15.5 15 14.5	 17 16.2 16	V
CURRENT LIMIT					
Short Circuit Current Limit, ($R_{extILimit}$ = 56 Ω, T_J = −20°C) (Note 3) ($R_{extILimit}$ = 56 Ω, T_J = 25°C) ($R_{extILimit}$ = 56 Ω, T_J = 100°C) (Note 3)	I_{Lim-SS}	 2.05 2.0 1.7	 2.7 2.5 2.3	 3.2 3.0 2.7	A
Overload Current Limit, (Note 3) ($R_{extILimit}$ = 56 Ω, T_J = −20°C) ($R_{extILimit}$ = 56 Ω, T_J = 25°C) ($R_{extILimit}$ = 56 Ω, T_J = 100°C)	I_{Lim-OL}	 3.7 3.5 3.4	 4.6 4.4 4.3	 5.5 5.3 5.2	A
dV/dt CIRCUIT					
Slew Rate ($C_{dV/dt}$ = 1 μf)	dV/dt	 0.130	 0.15	 0.170	V/ms
Charging Current (Current Sourced into dV/dt Cap) (T_J = −20°C) (Note 3) (T_J = 25°C) (T_J = 100°C) (Note 3)	$I_{dV/dt}$	 67 70 71	 80 83 84	 90 92 96	μA
Max Capacitor Voltage	V_{max}	–	–	V_{CC}	V
TOTAL DEVICE					
Bias Current (Device Operational, Load Open, V_{in} = 12 V)	I_{Bias}	–	1.45	2.0	mA
Minimum Operating Voltage	V_{min}	–	–	9.0	V

3. Verified by design.

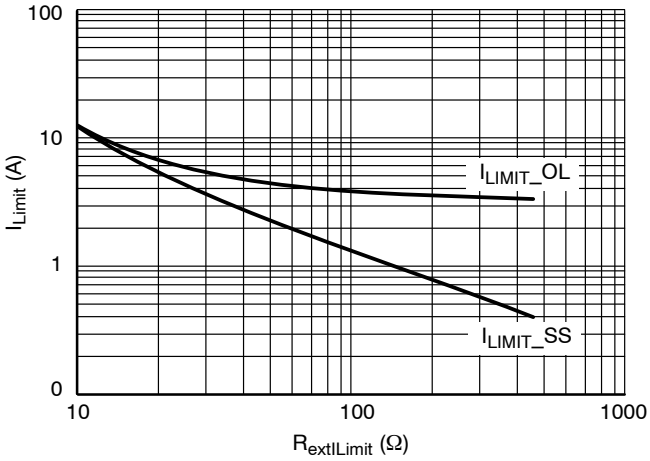


Figure 2. Current Limit Adjustment

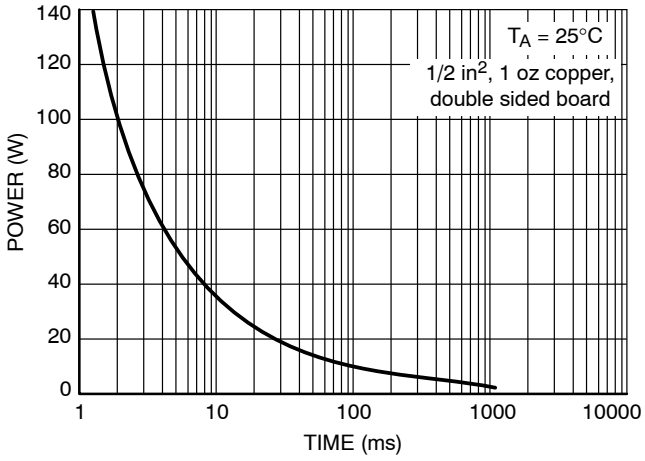
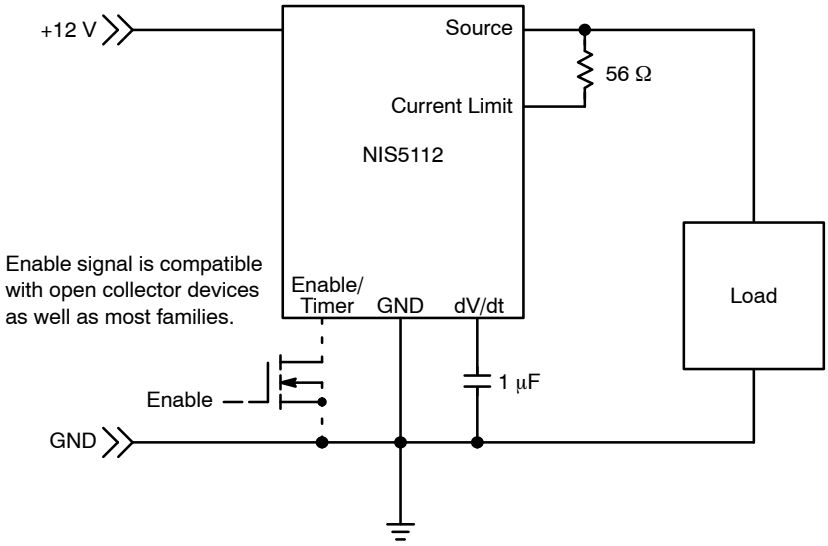


Figure 3. Overload vs. Shutdown Time



(Typical operating conditions: V_{in} = 12 V, R_{ILimit} = 56 Ω, $C_{dV/dt}$ = 1 μF)

Figure 4. Typical Application Circuit

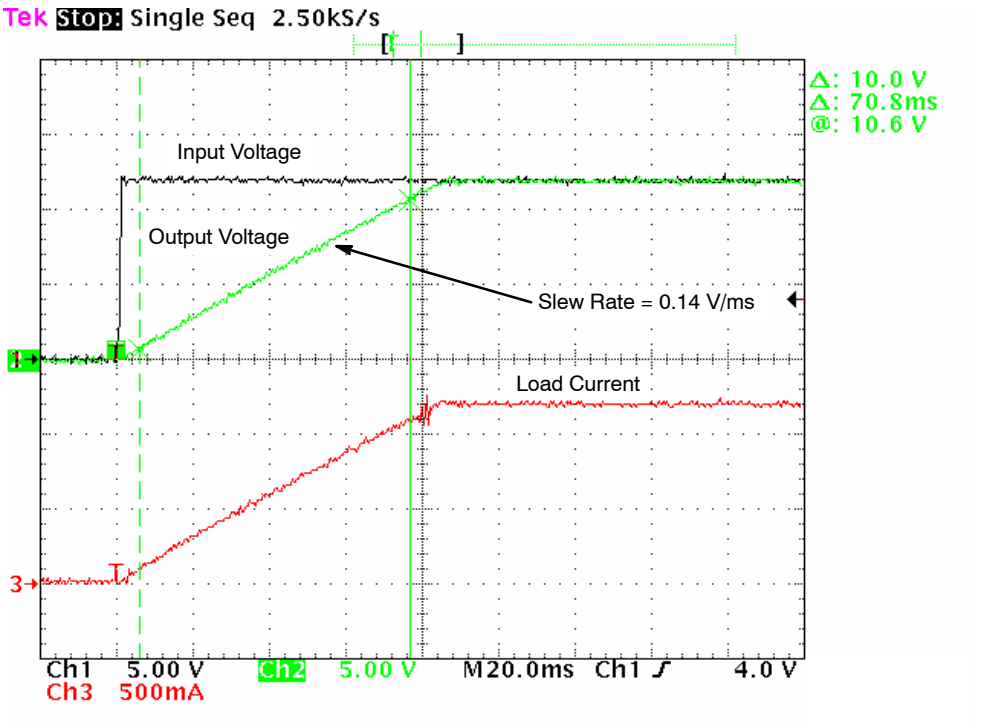


Figure 5. Turn−on Waveforms for a Resistive Load of 10 Ω ($C_{dV/dt}$ = 1 μf)

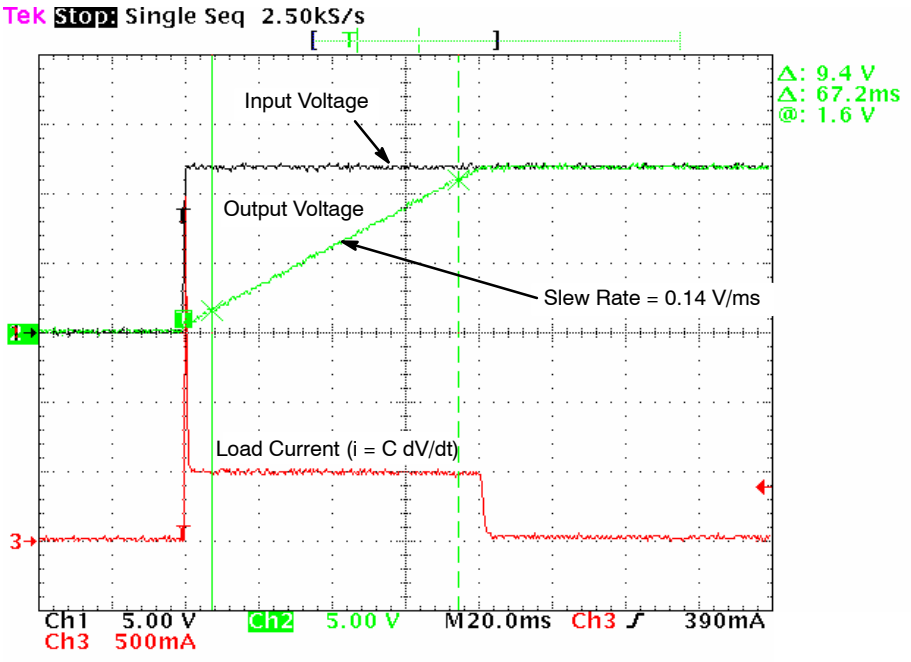


Figure 6. Turn−on Waveforms for a Load Capacitance of 3,300 μf ($C_{dV/dt}$ = 1 μf)

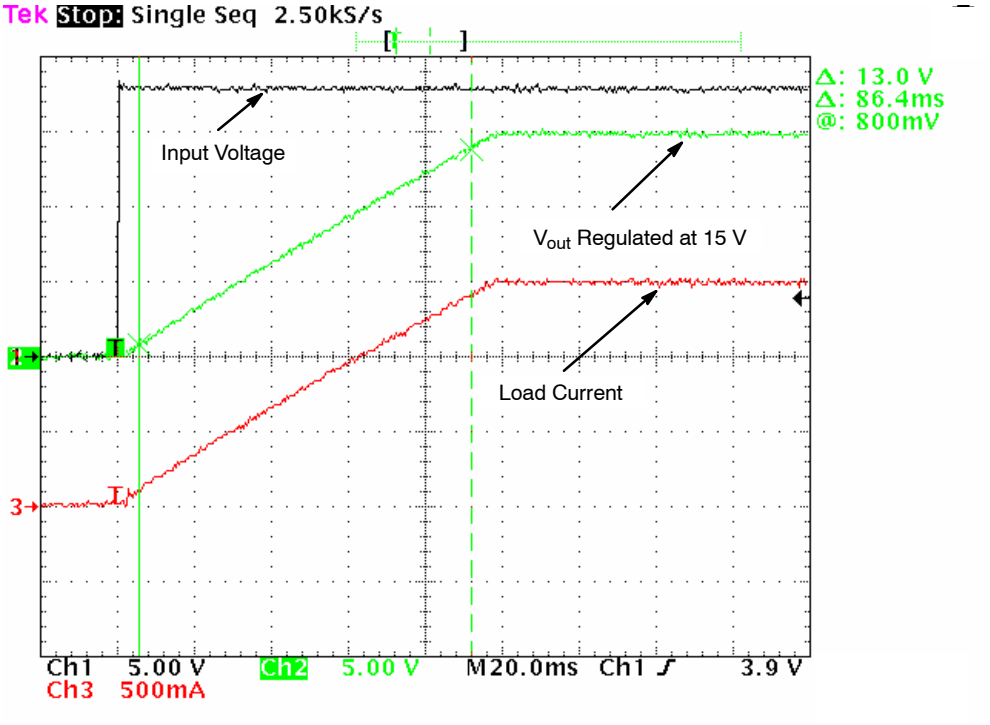


Figure 7. Turn−on Waveforms for an Overvoltage Condition (10 Ω Resistive Load)

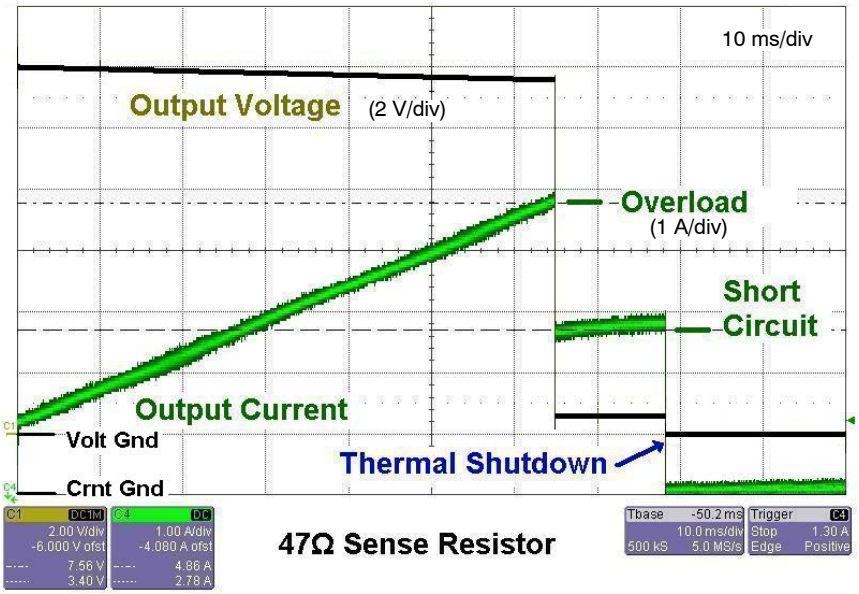


Figure 8. Current Waveforms for Overload, Short Circuit and Thermal Shutdown

DEVICE OPERATION

Basic Operation

This device is a self−protected, resettable, electronic fuse. It contains circuits to monitor the input voltage, output current, die temperature, turn−on di/dt and turn−on dV/dt, as well as an enable/timer function.

On application of the input voltage, the device will apply the input voltage to the load based on the restrictions of the controlling circuits. The dV/dt of the output voltage can be programmed by the addition of a capacitor to the dV/dt pin, or if left open, the output current will be limited by the internally controlled di/dt.

The device will remain on as long as the temperature does not exceed the 135°C limit that is programmed into the chip. The current limit circuit does not shut down the part but will reduce the conductivity of the FET to maintain a constant current as long as it remains at the set level. The input overvoltage clamp also does not shut down the part, but will limit the output voltage to 15 V in the event that the input exceeds that level.

The device can be turned on and off by the enable/timer function, which can also be used to reset the device after a thermal fault if the thermal latch version is chosen.

An internal charge pump provides bias for the gate voltage of the internal N−channel power FET and also for the current limit circuit. The remainder of the control circuitry operates between the input voltage (V_{CC}) and ground.

dV/dt

This circuit is comprised of an operational amplifier and current source as shown in Figure 9. The enable circuit controls a FET that keeps the slew−rate capacitor discharged any time the device is disabled. When the enable pin is released (low−to−high transition) or when power is applied with the enable pin in a high state, the dV/dt capacitor begins to charge due to the 80 μA in the current source. The amplifier controls the output voltage and tracks the voltage on the dV/dt cap scaled by a factor of 2. The output voltage will continue to ramp higher until it reaches the input voltage, or until the 15 V clamp limits it.

The equation for the output slew rate is
$dV/dt = (I/C_{dV/dt}) \times 2$.
Where:
I – is 80 μA (internal current source)
$C_{dV/dt}$ – is the desired dV/dt capacitor value.

The dV/dt ramp begins with a small step of about 200 mV. This step causes a current surge into the output load capacitance which can be seen in Figure 6. The peak level of this surge will be limited to the overload level of the current limit.

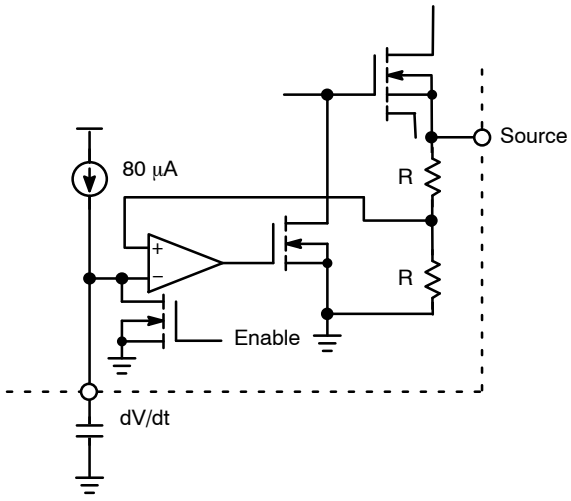


Figure 9. dV/dt Circuit

Overvoltage Clamp

The overvoltage clamp consists of an amplifier and reference. It monitors the output voltage and if the output voltage exceeds 15 V, the gate drive of the main FET is reduced to limit the output. This is intended to allow operation through transients while protecting the load. If an overvoltage condition exists for many seconds, the device may overheat due to the voltage drop across the FET combined with the load current. In this event, the thermal protection circuit would shut down the device.

Enable/Timer

The enable/timer pin can function either as a direct enable pin, or as a time delay. In the enable mode, an open collector device is connected to this pin. When the device is in its low impedance mode, this pin is low and the operation of the chip is disabled. If a time delay is required, a capacitor is added to this pin.

If a capacitor is added without an open collector device, the turn on will be delayed from the time at which the UVLO voltage is reached. If an open collector device is also used, the delay will start from the time that it goes into its high impedance state. The capacitor is charged by an internal current source of 80 μA (typical).

The nominal trip voltage of the comparator is 2.5 V and was designed to be compatible with most logic families. In general, logic gates can be tied directly to this pin, but it is recommended that this be tested.

There is an inherent delay in the turn on of the electronic fuse, due to the method of gate drive used. The gate of the power FET is charged through a high impedance resistor, and from the time that the gate starts charging until the time that it reaches its threshold voltage, there will be no conduction. Once the gate reaches its threshold voltage, the output current will begin a controlled ramp up phase.

This delay will be added to any timing delay due to the enable/timer circuit. Figure 10 shows a simplified diagram of the enable/timer circuit.

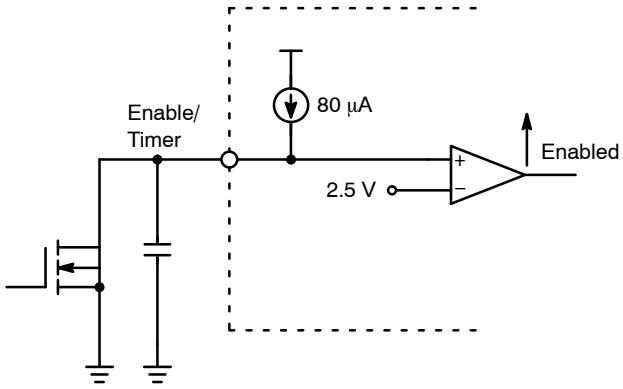


Figure 10. Simplified Schematic Diagram of the Enable/Timer Circuit

Thermal Protection Circuit

The temperature limit circuit senses the temperature of the Power FET and removes the gate drive if the maximum level is exceeded. The NIS5112 device has two different thermal limit versions, auto−retry and latch off.

Auto−Retry Version

The device will shut down when the thermal limit threshold is reached (T_J = 135°C, typical) and will not turn back on until the die temperature reduces down to 95°C (40°C hysteresis, typical). It will keep auto−retrying until the fault condition is removed or power is turned−off.

Latch−Off Version

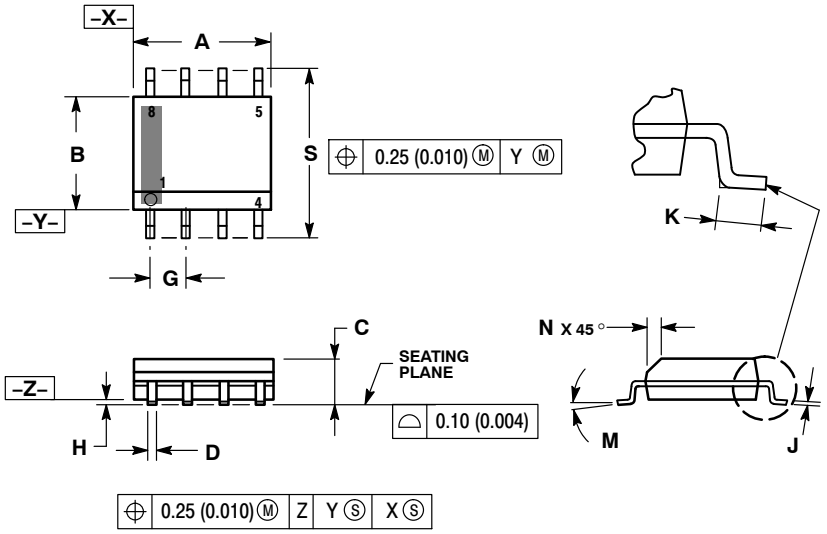
For the latch−off version, the device will shut down when the thermal limit threshold is reached (T_J = 135°C, typical) and will remain off until power is reset.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

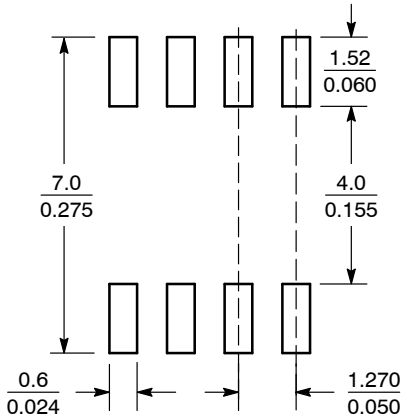
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

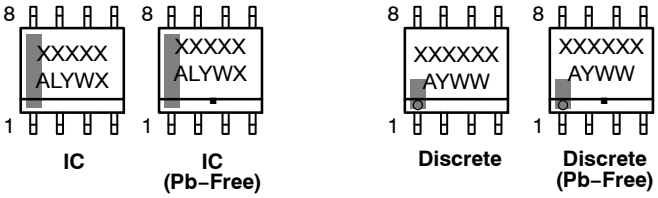
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOIC−8 NB**	**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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