

MJD44E3, NJVMJD44E3T4G

Darlington Power Transistor DPAK For Surface Mount Applications

Designed for general purpose power and switching output or driver stages in applications such as switching regulators, converters, and power amplifiers.

Features

- Electrically Similar to Popular D44E3 Device
- High DC Gain – 1000 Min @ 5.0 Adc
- Low Sat. Voltage – 1.5 V @ 5.0 Adc
- Compatible With Existing Automatic Pick and Place Equipment
- Epoxy Meets UL 94 V-0 @ 0.125 in
- ESD Ratings:
 - ◆ Human Body Model, 3B > 8000 V
 - ◆ Machine Model, C > 400 V
- NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These are Pb-Free Packages*

MAXIMUM RATINGS

| Rating | Symbol | Max | Unit |
|---|----------------|---------------|--------------------------|
| Collector-Emitter Voltage | V_{CEO} | 80 | Vdc |
| Emitter-Base Voltage | V_{EB} | 7 | Vdc |
| Collector Current – Continuous | I_C | 10 | Adc |
| Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C | P_D | 20 0.16 | W W/ $^\circ\text{C}$ |
| Total Power Dissipation (Note 1) @ $T_A = 25^\circ\text{C}$ Derate above 25°C | P_D | 1.75 0.014 | W W/ $^\circ\text{C}$ |
| Operating and Storage Junction Temperature Range | T_J, T_{stg} | -55 to +150 | $^\circ\text{C}$ |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



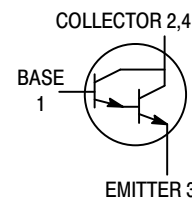
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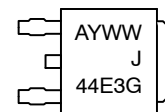
NPN DARLINGTON SILICON POWER TRANSISTORS 10 AMPERES 80 VOLTS, 20 WATTS



DPAK
CASE 369C
STYLE 1



MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- WW = Work Week
- J44E3 = Device Code
- G = Pb-Free Package

ORDERING INFORMATION

| Device | Package | Shipping† |
|---------------|-------------------|------------------------|
| MJD44E3T4G | DPAK (Pb-Free) | 2,500 / Tape & Reel |
| NJVMJD44E3T4G | DPAK (Pb-Free) | 2,500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MJD44E3, NJVMJD44E3T4G

THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|--|-----------------|------|---------------|
| Thermal Resistance, Junction-to-Case | $R_{\theta JC}$ | 6.25 | $^{\circ}C/W$ |
| Thermal Resistance, Junction-to-Ambient (Note 2) | $R_{\theta JA}$ | 71.4 | $^{\circ}C/W$ |
| Lead Temperature for Soldering | T_L | 260 | $^{\circ}C$ |

2. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}C$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

OFF CHARACTERISTICS

| | | | | | |
|--|-----------|---|---|----|---------|
| Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEO}, V_{BE} = 0$) | I_{CES} | - | - | 10 | μA |
| Emitter Cutoff Current ($V_{EB} = 7 \text{ Vdc}$) | I_{EBO} | - | - | 1 | μA |

ON CHARACTERISTICS

| | | | | | |
|---|---------------|------|---|----------|-----|
| Collector-Emitter Saturation Voltage ($I_C = 5 \text{ Adc}, I_B = 10 \text{ mAdc}$) ($I_C = 10 \text{ Adc}, I_B = 20 \text{ mAdc}$) | $V_{CE(sat)}$ | - | - | 1.5 2 | Vdc |
| Base-Emitter Saturation Voltage ($I_C = 5 \text{ Adc}, I_B = 10 \text{ mAdc}$) | $V_{BE(sat)}$ | - | - | 2.5 | Vdc |
| DC Current Gain ($V_{CE} = 5 \text{ Vdc}, I_C = 5 \text{ Adc}$) | h_{FE} | 1000 | - | - | - |

DYNAMIC CHARACTERISTICS

| | | | | | |
|--|----------|---|---|-----|----|
| Collector Capacitance ($V_{CB} = 10 \text{ Vdc}, f_{test} = 1 \text{ MHz}$) | C_{cb} | - | - | 130 | pF |
|--|----------|---|---|-----|----|

SWITCHING TIMES

| | | | | | |
|---|-------------|---|-----|---|---------|
| Delay and Rise Times ($I_C = 10 \text{ Adc}, I_{B1} = 20 \text{ mAdc}$) | $t_d + t_r$ | - | 0.6 | - | μs |
| Storage Time ($I_C = 10 \text{ Adc}, I_{B1} = I_{B2} = 20 \text{ mAdc}$) | t_s | - | 2 | - | μs |
| Fall Time ($I_C = 10 \text{ Adc}, I_{B1} = I_{B2} = 20 \text{ mAdc}$) | t_f | - | 0.5 | - | μs |

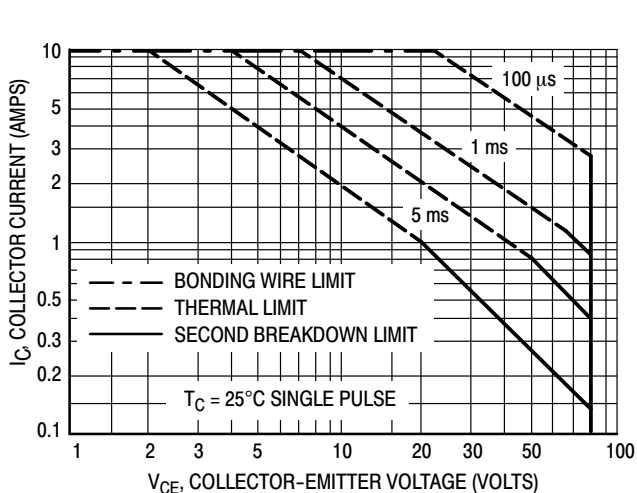


Figure 1. Maximum Forward Bias Safe Operating Area

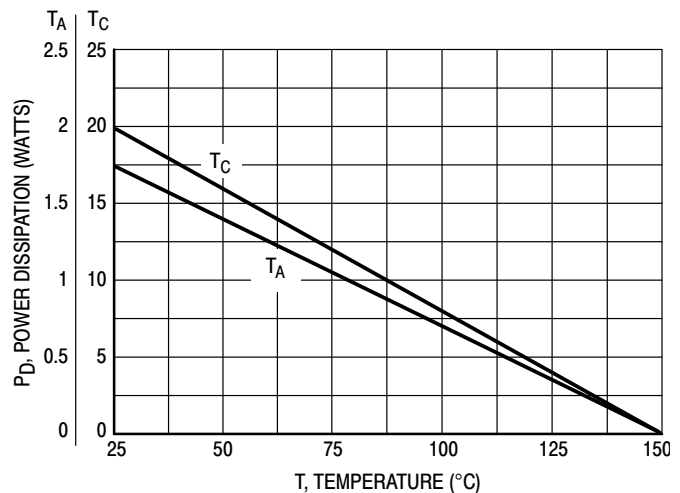
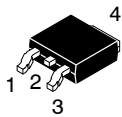


Figure 2. Power Derating

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

DPAK (SINGLE GAUGE)

CASE 369C

ISSUE F

DATE 21 JUL 2015

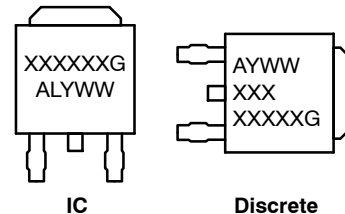


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.086 | 0.094 | 2.18 | 2.38 |
| A1 | 0.000 | 0.005 | 0.00 | 0.13 |
| b | 0.025 | 0.035 | 0.63 | 0.89 |
| b2 | 0.028 | 0.045 | 0.72 | 1.14 |
| b3 | 0.180 | 0.215 | 4.57 | 5.46 |
| c | 0.018 | 0.024 | 0.46 | 0.61 |
| c2 | 0.018 | 0.024 | 0.46 | 0.61 |
| D | 0.235 | 0.245 | 5.97 | 6.22 |
| E | 0.250 | 0.265 | 6.35 | 6.73 |
| e | 0.090 BSC | | 2.29 BSC | |
| H | 0.370 | 0.410 | 9.40 | 10.41 |
| L | 0.055 | 0.070 | 1.40 | 1.78 |
| L1 | 0.114 REF | | 2.90 REF | |
| L2 | 0.020 BSC | | 0.51 BSC | |
| L3 | 0.035 | 0.050 | 0.89 | 1.27 |
| L4 | --- | 0.040 | --- | 1.01 |
| Z | 0.155 | --- | 3.93 | --- |

GENERIC MARKING DIAGRAM*

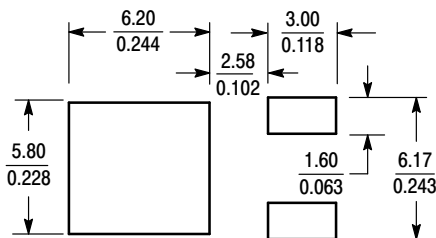


- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

- | | | | | |
|--|--|---|---|--|
| <p>STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR</p> | <p>STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN</p> | <p>STYLE 3: PIN 1. ANODE 2. CATHODE 3. ANODE 4. CATHODE</p> | <p>STYLE 4: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE</p> | <p>STYLE 5: PIN 1. GATE 2. ANODE 3. CATHODE 4. ANODE</p> |
| <p>STYLE 6: PIN 1. MT1 2. MT2 3. GATE 4. MT2</p> | <p>STYLE 7: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR</p> | <p>STYLE 8: PIN 1. N/C 2. CATHODE 3. ANODE 4. CATHODE</p> | <p>STYLE 9: PIN 1. ANODE 2. CATHODE 3. RESISTOR ADJUST 4. CATHODE</p> | <p>STYLE 10: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. ANODE</p> |

SOLDERING FOOTPRINT*



SCALE 3:1 (mm / inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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| DESCRIPTION: | DPAK (SINGLE GAUGE) | PAGE 1 OF 1 |

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