# NLSX4373

# 2-Bit 20 Mb/s Dual-Supply Level Translator

The NLSX4373 is a 2−bit configurable dual−supply bidirectional auto sensing translator that does not require a directional control pin. The $V_{CC}$ I/O and $V_L$ I/O ports are designed to track two different power supply rails, $V_{CC}$ and $V_L$ respectively. The $V_{CC}$ supply rail is configurable from 1.5 V to 5.5 V while $V_L$ supply rail is configurable to 1.5 V to 5.5 V. This allows voltage logic signals on the $V_L$ side to be translated into lower, higher or equal value voltage logic signals on the $V_{CC}$ side, and vice−versa.

The NLSX4373 translator has open−drain outputs with integrated 10 kΩ pullup resistors on the I/O lines. The integrated pullup resistors are used to pullup the I/O lines to either $V_L$ or $V_{CC}$. The NLSX4373 is an excellent match for open−drain applications such as the $I^2C$ communication bus.

### Features

- $V_L$ can be Less than, Greater than or Equal to $V_{CC}$
- Wide $V_{CC}$ Operating Range: 1.5 V to 5.5 V
  Wide $V_L$ Operating Range: 1.5 V to 5.5 V
- High−Speed with 20 Mb/s Guaranteed Date Rate
- Low Bit−to−Bit Skew
- Enable Input and I/O Lines have Overvoltage Tolerant (OVT) to 5.5 V
- Nonpreferential Powerup Sequencing
- Integrated 10 kΩ Pullup Resistors
- Small packaging: UDFN8, SO−8, Micro8
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable*
- This is a Pb−Free Device

### Typical Applications

- $I^2C$, SMBus, PMBus
- Low Voltage ASIC Level Translation
- Mobile Phones, PDAs, Cameras

### Important Information

- ESD Protection for All Pins
  − Human Body Model (HBM) > 7000 V

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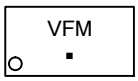
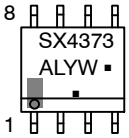
**MARKING DIAGRAMS**


**UDFN8**
**MU SUFFIX**
**CASE 517AJ**

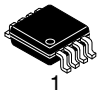



VF = Specific Device Code
M = Date Code
▪ = Pb−Free Package

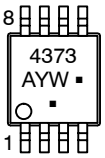

**SO−8**
**D SUFFIX**
**CASE 751**




A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package




**Micro8™**
**DM SUFFIX**
**CASE 846A**



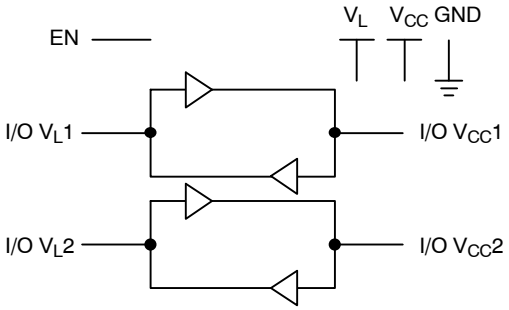

A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

**ORDERING INFORMATION**

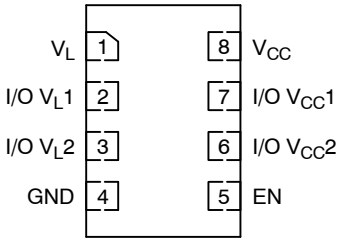
| Device | Package | Shipping† |
|---|---|---|
| NLSX4373MUTAG | UDFN8 (Pb−Free) | 3000/Tape & Reel |
| NLVSX4373MUTAG* | UDFN8 (Pb−Free) | 3000/Tape & Reel |
| NLSX4373DR2G | SO−8 (Pb−Free) | 2500/Tape & Reel |
| NLVSX4373DR2G* | SO−8 (Pb−Free) | 2500/Tape & Reel |
| NLSX4373DMR2G | Micro8 (Pb−Free) | 4000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

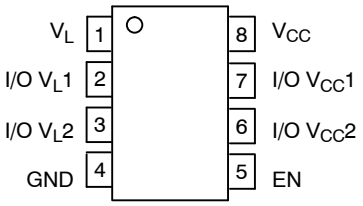
## LOGIC DIAGRAM



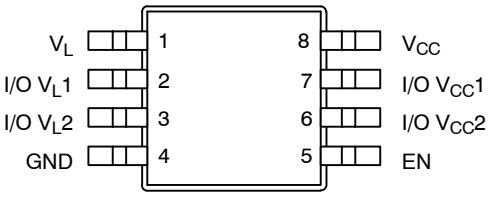

## PIN ASSIGNMENTS




UDFN8
(Top View)




SOIC−8
(Top View)




Micro8
(Top View)

### PIN ASSIGNMENT

| Pins | Description |
|---|---|
| $V_{CC}$ | $V_{CC}$ Input Voltage |
| $V_L$ | $V_L$ Input Voltage |
| GND | Ground |
| EN | Output Enable |
| I/O $V_{CC}$n | $V_{CC}$ I/O Port, Referenced to $V_{CC}$ |
| I/O $V_L$n | $V_L$ I/O Port, Referenced to $V_L$ |

### FUNCTION TABLE

| EN | Operating Mode |
|---|---|
| L | Hi−Z |
| H | I/O Buses Connected |

## MAXIMUM RATINGS

| Symbol | Parameter | Value | Condition | Unit |
|---|---|---|---|---|
| $V_{CC}$ | High−side DC Supply Voltage | −0.3 to +7.0 | | V |
| $V_L$ | High−side DC Supply Voltage | −0.3 to +7.0 | | V |
| I/O $V_{CC}$ | $V_{CC}$−Referenced DC Input/Output Voltage | −0.3 to ($V_{CC}$ + 0.3) | | V |
| I/O $V_L$ | $V_L$−Referenced DC Input/Output Voltage | −0.3 to ($V_L$ + 0.3) | | V |
| $V_{EN}$ | Enable Control Pin DC Input Voltage | −0.3 to +7.0 | | V |
| $I_{I/O\_SC}$ | Short−Circuit Duration (I/O $V_L$ and I/O $V_{CC}$ to GND) | 40 | Continuous | mA |
| $T_{STG}$ | Storage Temperature | −65 to +150 | | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | High−side Positive DC Supply Voltage | 1.5 | 5.5 | V |
| $V_L$ | High−side Positive DC Supply Voltage | 1.5 | 5.5 | V |
| $V_{EN}$ | Enable Control Pin Voltage | GND | 5.5 | V |
| $V_{IO}$ | Enable Control Pin Voltage | GND | 5.5 | V |
| $T_A$ | Operating Temperature Range | −40 | +85 | °C |

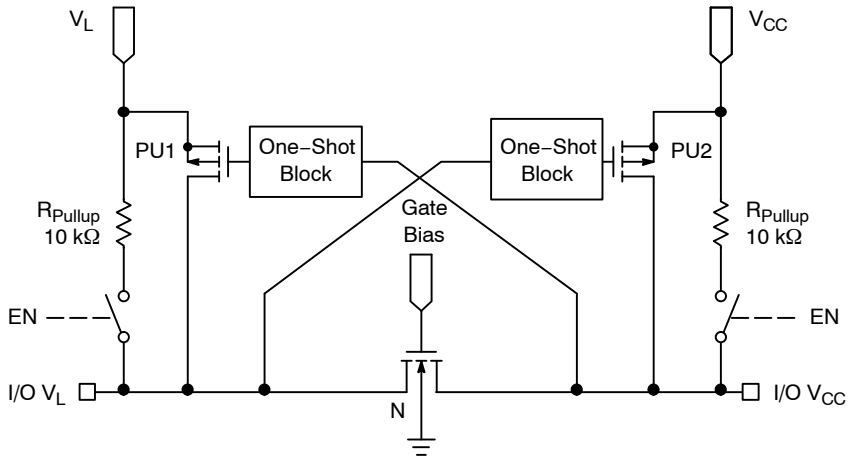



**Figure 1. Block Diagram (1 I/O Line)**

**DC ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 1.5 V to 5.5 V and $V_L$ = 1.5 V to 5.5 V, unless otherwise specified)

| Symbol | Parameter | Test Conditions | −40°C to +85°C | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ (Notes 1, 2) | Max | |
| $V_{IHC}$ | I/O $V_{CC}$ Input HIGH Voltage | | $V_{CC}$ − 0.4 | − | − | V |
| $V_{ILC}$ | I/O $V_{CC}$ Input LOW Voltage | | − | − | 0.15 | V |
| $V_{IHL}$ | I/O $V_L$ Input HIGH Voltage | | $V_L$ − 0.2 | − | − | V |
| $V_{ILL}$ | I/O $V_L$ Input LOW Voltage | | − | − | 0.15 | V |
| $V_{IH}$ | Control Pin Input HIGH Voltage | | $V_L$ − 0.2 | − | − | V |
| $V_{IL}$ | Control Pin Input LOW Voltage | | − | − | 0.15 | V |
| $V_{OHC}$ | I/O $V_{CC}$ Output HIGH Voltage | I/O $V_{CC}$ Source Current = 20 μA | 2/3 * $V_{CC}$ | − | − | V |
| $V_{OLC}$ | I/O $V_{CC}$ Output LOW Voltage | I/O $V_{CC}$ Sink Current = 20 μA | − | − | 1/3 * $V_{CC}$ | V |
| $V_{OHL}$ | I/O $V_L$ Output HIGH Voltage | I/O $V_L$ Source Current = 20 μA | 2/3 * $V_L$ | − | − | V |
| $V_{OLL}$ | I/O $V_L$ Output LOW Voltage | I/O $V_L$ Sink Current = 20 μA | − | − | 1/3 * $V_L$ | V |
| $I_{QVCC}$ | $V_{CC}$ Supply Current | I/O $V_{CC}$ and I/O $V_L$ Unconnected, $V_{EN}$ = $V_L$ | − | 0.5 | 2.0 | μA |
| $I_{QVL}$ | $V_L$ Supply Current | I/O $V_{CC}$ and I/O $V_L$ Unconnected, $V_{EN}$ = $V_L$ | − | 0.3 | 1.5 | μA |
| $I_{TS-VCC}$ | $V_{CC}$ Tristate Output Mode Supply Current | I/O $V_{CC}$ and I/O $V_L$ Unconnected, $V_{EN}$ = GND | − | 0.1 | 1.0 | μA |
| $I_{TS-VL}$ | $V_L$ Tristate Output Mode Supply Current | I/O $V_{CC}$ and I/O $V_L$ Unconnected, $V_{EN}$ = GND | − | 0.1 | 1.0 | μA |
| $I_{OZ}$ | I/O Tristate Output Mode Leakage Current | $T_A$ = +25°C | − | 0.1 | 1.0 | μA |
| $R_{PU}$ | Pullup Resistor I/O $V_L$ and $V_{CC}$ | $T_A$ = +25°C | − | 10 | − | kΩ |

1. Typical values are for $V_{CC}$ = +2.8 V, $V_L$ = +1.8 V and $T_A$ = +25°C.
2. All units are production tested at $T_A$ = +25°C. Limits over the operating temperature range are guaranteed by design.

## TIMING CHARACTERISTICS – RAIL–TO–RAIL DRIVING CONFIGURATIONS

(I/O test circuit of Figures 2 and 3, $C_{LOAD}$ = 15 pF, driver output impedance ≤ 50 Ω, $R_{LOAD}$ = 1 MΩ)

| Symbol | Parameter | Test Conditions | –40°C to +85°C (Notes 3 and 4) | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| **$V_L$ = 1.5 V, $V_{CC}$ = 5.5 V** | | | | | | |
| $t_{RVCC}$ | I/O $V_{CC}$ Risetime | | | | 15 | ns |
| $t_{FVCC}$ | I/O $V_{CC}$ Falltime | | | | 20 | ns |
| $t_{RVL}$ | I/O $V_L$ Risetime | | | | 30 | ns |
| $t_{FVL}$ | I/O $V_L$ Falltime | | | | 10 | ns |
| $t_{PDVL–VCC}$ | Propagation Delay (Driving I/O $V_L$) | | | | 20 | ns |
| $t_{PDVCC–VL}$ | Propagation Delay (Driving I/O $V_{CC}$) | | | | 20 | ns |
| $t_{PPSKEW}$ | Part–to–Part Skew | | | | 5 | nS |
| | Maximum Data Rate | | 20 | | | Mb/s |
| **$V_L$ = 1.8 V, $V_{CC}$ = 2.8 V** | | | | | | |
| $t_{RVCC}$ | I/O $V_{CC}$ Risetime | | | | 15 | ns |
| $t_{FVCC}$ | I/O $V_{CC}$ Falltime | | | | 15 | ns |
| $t_{RVL}$ | I/O $V_L$ Risetime | | | | 25 | ns |
| $t_{FVL}$ | I/O $V_L$ Falltime | | | | 10 | ns |
| $t_{PDVL–VCC}$ | Propagation Delay (Driving I/O $V_L$) | | | | 15 | ns |
| $t_{PDVCC–VL}$ | Propagation Delay (Driving I/O $V_{CC}$) | | | | 15 | ns |
| $t_{PPSKEW}$ | Part–to–Part Skew | | | | 5 | nS |
| | Maximum Data Rate | | 20 | | | Mb/s |
| **$V_L$ = 2.5 V, $V_{CC}$ = 3.6 V** | | | | | | |
| $t_{RVCC}$ | I/O $V_{CC}$ Risetime | | | | 15 | ns |
| $t_{FVCC}$ | I/O $V_{CC}$ Falltime | | | | 10 | ns |
| $t_{RVL}$ | I/O $V_L$ Risetime | | | | 15 | ns |
| $t_{FVL}$ | I/O $V_L$ Falltime | | | | 10 | ns |
| $t_{PDVL–VCC}$ | Propagation Delay (Driving I/O $V_L$) | | | | 15 | ns |
| $t_{PDVCC–VL}$ | Propagation Delay (Driving I/O $V_{CC}$) | | | | 15 | ns |
| $t_{PPSKEW}$ | Part–to–Part Skew | | | | 5 | nS |
| | Maximum Data Rate | | 20 | | | Mb/s |
| **$V_L$ = 2.8 V, $V_{CC}$ = 1.8 V** | | | | | | |
| $t_{RVCC}$ | I/O $V_{CC}$ Risetime | | | | 25 | ns |
| $t_{FVCC}$ | I/O $V_{CC}$ Falltime | | | | 10 | ns |
| $t_{RVL}$ | I/O $V_L$ Risetime | | | | 20 | ns |
| $t_{FVL}$ | I/O $V_L$ Falltime | | | | 15 | ns |
| $t_{PDVL–VCC}$ | Propagation Delay (Driving I/O $V_L$) | | | | 15 | ns |
| $t_{PDVCC–VL}$ | Propagation Delay (Driving I/O $V_{CC}$) | | | | 15 | ns |
| $t_{PPSKEW}$ | Part–to–Part Skew | | | | 5 | nS |
| | Maximum Data Rate | | 20 | | | Mb/s |

3. Typical values are for $V_{CC}$ = +3.3 V, $V_L$ = +1.8 V and $T_A$ = +25°C.
4. All units are production tested at $T_A$ = +25°C. Limits over the operating temperature range are guaranteed by design.

## TIMING CHARACTERISTICS – RAIL–TO–RAIL DRIVING CONFIGURATIONS

(I/O test circuit of Figures 2 and 3, $C_{LOAD}$ = 15 pF, driver output impedance ≤ 50 Ω, $R_{LOAD}$ = 1 MΩ)

| Symbol | Parameter | Test Conditions | –40°C to +85°C (Notes 3 and 4) | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| **$V_L$ = 3.6 V, $V_{CC}$ = 2.5 V** | | | | | | |
| $t_{RVCC}$ | I/O $V_{CC}$ Risetime | | | | 15 | ns |
| $t_{FVCC}$ | I/O $V_{CC}$ Falltime | | | | 10 | ns |
| $t_{RVL}$ | I/O $V_L$ Risetime | | | | 15 | ns |
| $t_{FVL}$ | I/O $V_L$ Falltime | | | | 15 | ns |
| $t_{PDVL–VCC}$ | Propagation Delay (Driving I/O $V_L$) | | | | 15 | ns |
| $t_{PDVCC–VL}$ | Propagation Delay (Driving I/O $V_{CC}$) | | | | 15 | ns |
| $t_{PPSKEW}$ | Part–to–Part Skew | | | | 5 | nS |
| | Maximum Data Rate | | 20 | | | Mb/s |
| **$V_L$ = 5.5 V, $V_{CC}$ = 1.5 V** | | | | | | |
| $t_{RVCC}$ | I/O $V_{CC}$ Risetime | | | | 30 | ns |
| $t_{FVCC}$ | I/O $V_{CC}$ Falltime | | | | 10 | ns |
| $t_{RVL}$ | I/O $V_L$ Risetime | | | | 15 | ns |
| $t_{FVL}$ | I/O $V_L$ Falltime | | | | 20 | ns |
| $t_{PDVL–VCC}$ | Propagation Delay (Driving I/O $V_L$) | | | | 20 | ns |
| $t_{PDVCC–VL}$ | Propagation Delay (Driving I/O $V_{CC}$) | | | | 20 | ns |
| $t_{PPSKEW}$ | Part–to–Part Skew | | | | 5 | nS |
| | Maximum Data Rate | | 20 | | | Mb/s |

3. Typical values are for $V_{CC}$ = +3.3 V, $V_L$ = +1.8 V and $T_A$ = +25°C.
4. All units are production tested at $T_A$ = +25°C. Limits over the operating temperature range are guaranteed by design.

## TIMING CHARACTERISTICS – OPEN DRAIN DRIVING CONFIGURATIONS

(I/O test circuit of Figures 4 and 5, $C_{LOAD}$ = 15 pF, driver output impedance ≤ 50 Ω, $R_{LOAD}$ = 1 MΩ)

| Symbol | Parameter | Test Conditions | –40°C to +85°C (Notes 5 and 6) | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| **+1.5 ≤ $V_L$ ≤ $V_{CC}$ ≤ +5.5 V** | | | | | | |
| $t_{RVCC}$ | I/O $V_{CC}$ Risetime | | | | 400 | ns |
| $t_{FVCC}$ | I/O $V_{CC}$ Falltime | | | | 50 | ns |
| $t_{RVL}$ | I/O $V_L$ Risetime | | | | 400 | ns |
| $t_{FVL}$ | I/O $V_L$ Falltime | | | | 60 | ns |
| $t_{PDVL–VCC}$ | Propagation Delay (Driving I/O $V_L$) | | | | 1000 | ns |
| $t_{PDVCC–VL}$ | Propagation Delay (Driving I/O $V_{CC}$) | | | | 1000 | ns |
| $t_{PPSKEW}$ | Part–to–Part Skew | | | | 50 | nS |
| MDR | Maximum Data Rate | | 2 | | | Mb/s |

5. Typical values are for $V_{CC}$ = +3.3 V, $V_L$ = +1.8 V and $T_A$ = +25°C.
6. All units are production tested at $T_A$ = +25°C. Limits over the operating temperature range are guaranteed by design.

## TEST SETUPS

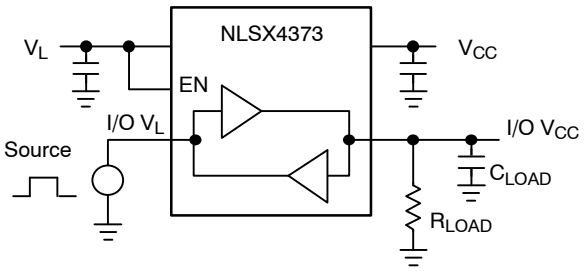



**Figure 2. Rail−to−Rail Driving I/O $V_L$**

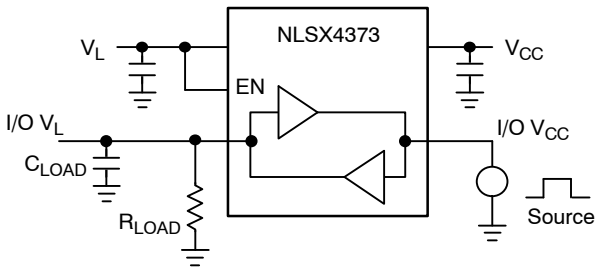



**Figure 3. Rail−to−Rail Driving I/O $V_{CC}$**

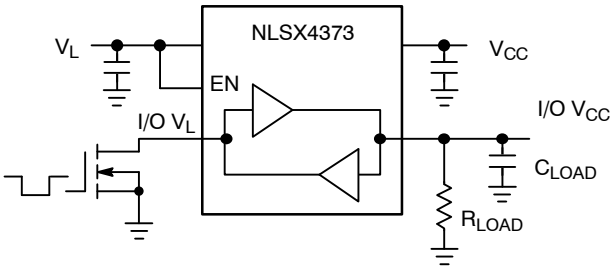



**Figure 4. Open−Drain Driving I/O $V_L$**

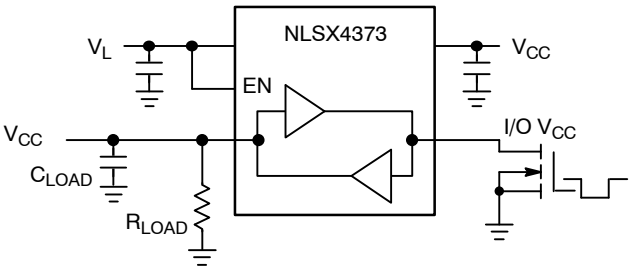



**Figure 5. Open−Drain Driving I/O $V_{CC}$**

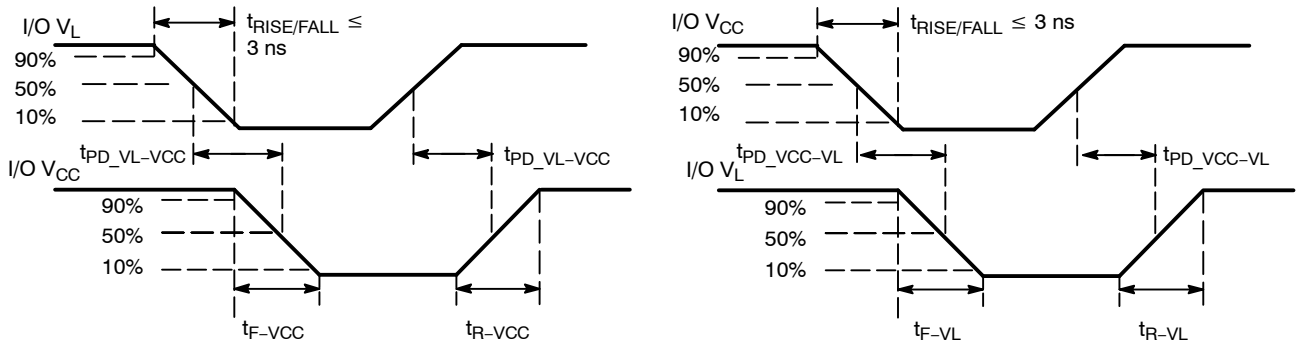
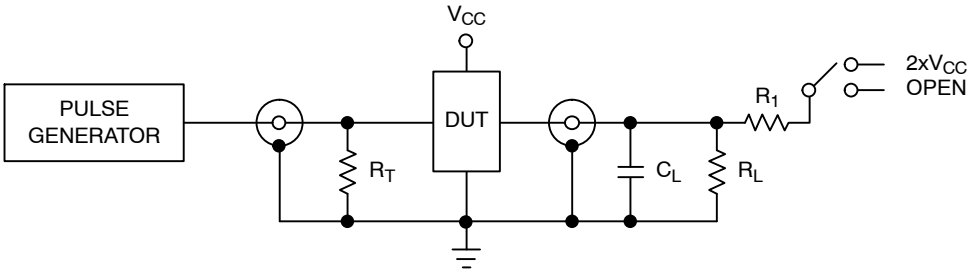



**Figure 6. Definition of Timing Specification Parameters**




| Test | Switch |
|---|---|
| $t_{PZH}$, $t_{PHZ}$ | Open |
| $t_{PZL}$, $t_{PLZ}$ | 2 x $V_{CC}$ |

$C_L$ = 15 pF or equivalent (Includes jig and probe capacitance)
$R_L$ = $R_1$ = 50 kΩ or equivalent
$R_T$ = $Z_{OUT}$ of pulse generator (typically 50 Ω)

**Figure 7. Test Circuit for Enable/Disable Time Measurement**

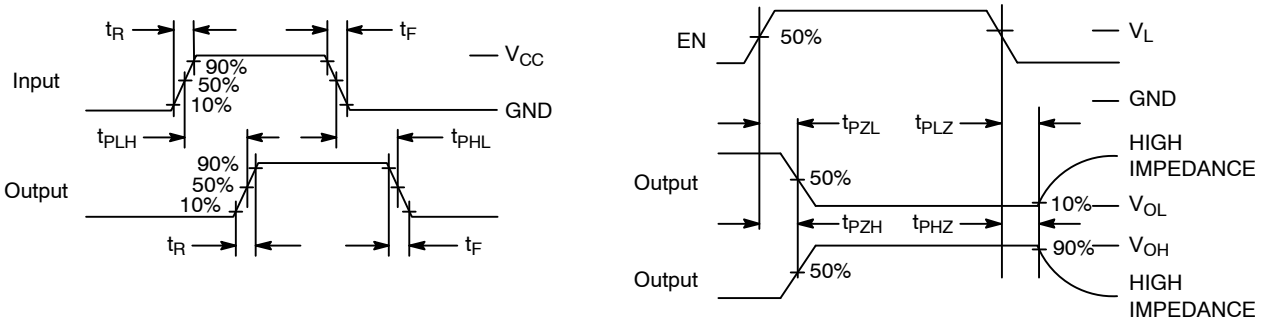



**Figure 8. Timing Definitions for Propagation Delays and Enable/Disable Measurement**

## APPLICATIONS INFORMATION

### Level Translator Architecture

The NLSX4373 auto sense translator provides bi−directional voltage level shifting to transfer data in multiple supply voltage systems. This device has two supply voltages, $V_L$ and $V_{CC}$, which set the logic levels on the input and output sides of the translator. When used to transfer data from the $V_L$ to the $V_{CC}$ ports, input signals referenced to the $V_L$ supply are translated to output signals with a logic level matched to $V_{CC}$. In a similar manner, the $V_{CC}$ to $V_L$ translation shifts input signals with a logic level compatible to $V_{CC}$ to an output signal matched to $V_L$.

The NLSX4373 consists of two bi−directional channels that independently determine the direction of the data flow without requiring a directional pin. The one−shot circuits are used to detect the rising or falling input signals. In addition, the one shots decrease the rise and fall time of the output signal for high−to−low and low−to−high transitions.

Each input/output channel has an internal 10 kΩ pull. The magnitude of the pullup resistors can be reduced by connecting external resistors in parallel to the internal 10 kΩ resistors.

### Input Driver Requirements

The rise ($t_R$) and fall ($t_F$) timing parameters of the open drain outputs depend on the magnitude of the pull−up resistors. In addition, the propagation times ($t_{PD}$), skew ($t_{PSKEW}$) and maximum data rate depend on the impedance of the device that is connected to the translator. The timing parameters listed in the data sheet assume that the output impedance of the drivers connected to the translator is less than 50 kΩ.

### Enable Input (EN)

The NLSX4373 has an Enable pin (EN) that provides tri−state operation at the I/O pins. Driving the Enable pin to a low logic level minimizes the power consumption of the device and drives the I/O $V_{CC}$ and I/O $V_L$ pins to a high impedance state. Normal translation operation occurs when the EN pin is equal to a logic high signal. The EN pin is referenced to the $V_L$ supply and has Overvoltage Tolerant (OVT) protection.

### Power Supply Guidelines

During normal operation, supply voltage $V_L$ can be greater than, less than or equal to $V_{CC}$. The sequencing of the power supplies will not damage the device during the power up operation.

For optimal performance, 0.01 μF to 0.1 μF decoupling capacitors should be used on the $V_L$ and $V_{CC}$ power supply pins. Ceramic capacitors are a good design choice to filter and bypass any noise signals on the voltage lines to the ground plane of the PCB. The noise immunity will be maximized by placing the capacitors as close as possible to the supply and ground pins, along with minimizing the PCB connection traces.

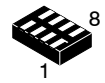
Micro8 is a trademark of International Rectifier.

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

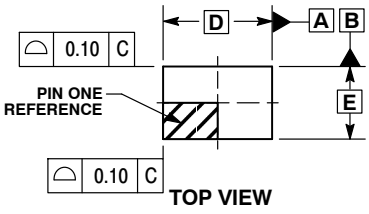
ON Semiconductor®

**UDFN8 1.8x1.2, 0.4P**
CASE 517AJ−01
ISSUE O

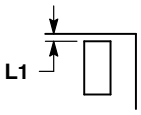
DATE 08 NOV 2006



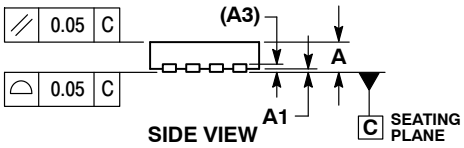

**SCALE 4:1**



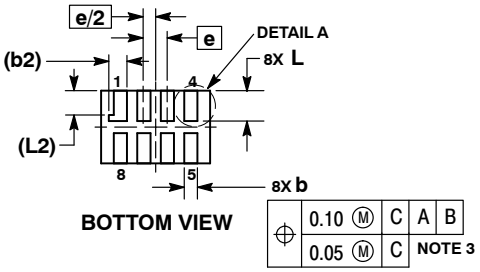

**TOP VIEW**




**DETAIL A**
**NOTE 5**




**SIDE VIEW**




**BOTTOM VIEW**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP.
4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH MAY NOT EXCEED 0.03 ONTO BOTTOM SURFACE OF TERMINALS.
5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

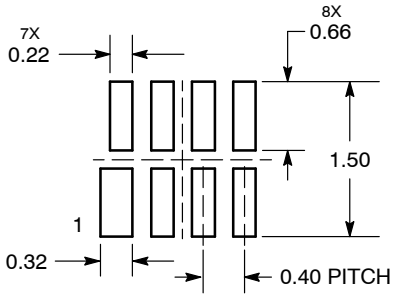
| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.45 | 0.55 |
| A1 | 0.00 | 0.05 |
| A3 | 0.127 REF | |
| b | 0.15 | 0.25 |
| b2 | 0.30 REF | |
| D | 1.80 BSC | |
| E | 1.20 BSC | |
| e | 0.40 BSC | |
| L | 0.45 | 0.55 |
| L1 | 0.00 | 0.03 |
| L2 | 0.40 REF | |

### GENERIC MARKING DIAGRAM*


XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

### MOUNTING FOOTPRINT SOLDERMASK DEFINED




DIMENSIONS: MILLIMETERS

| | | | |
|---|---|---|---|
| **DOCUMENT NUMBER:** | **98AON23417D** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. | |
| **DESCRIPTION:** | **UDFN8 1.8X1.2, 0.4P** | | **PAGE 1 OF 1** |

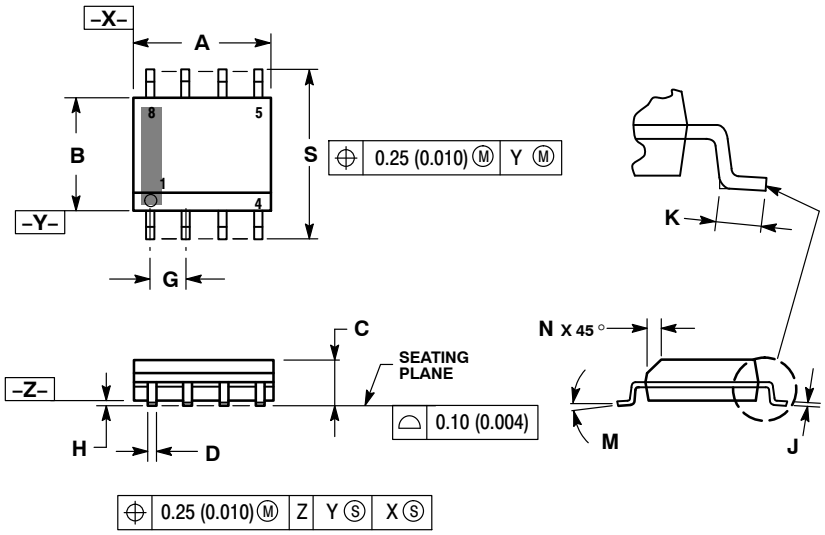
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

ON Semiconductor®

**SCALE 1:1**

**SOIC−8 NB**
CASE 751−07
ISSUE AK

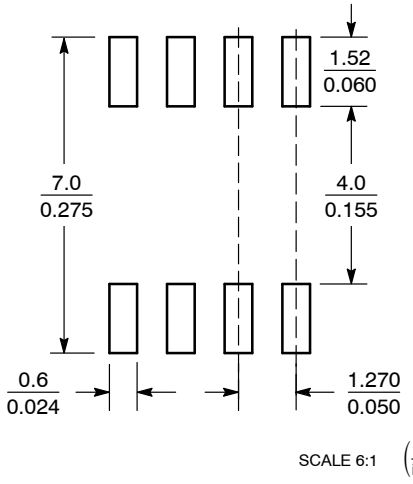
DATE 16 FEB 2011




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

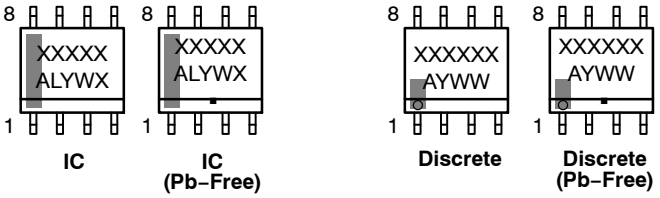
| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

### SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**STYLES ON PAGE 2**

| | | | |
|---|---|---|---|
| **DOCUMENT NUMBER:** | **98ASB42564B** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. | |
| **DESCRIPTION:** | **SOIC−8 NB** | | **PAGE 1 OF 2** |

**SOIC−8 NB**
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

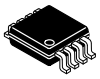
STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

| | | | |
|---|---|---|---|
| **DOCUMENT NUMBER:** | **98ASB42564B** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. | |
| **DESCRIPTION:** | **SOIC−8 NB** | | **PAGE 2 OF 2** |

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

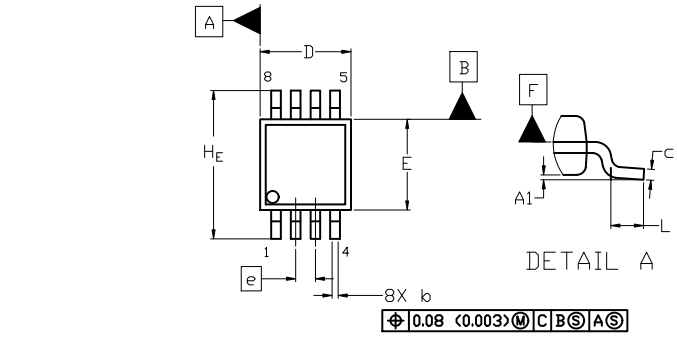
ON Semiconductor®

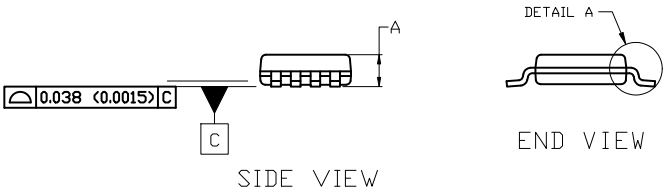


**SCALE 2:1**

**Micro8**
CASE 846A−02
ISSUE K

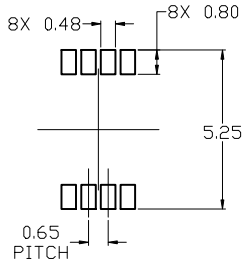
DATE 16 JUL 2020




NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

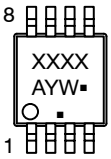



RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | --- | --- | 1.10 |
| A1 | 0.05 | 0.08 | 0.15 |
| b | 0.25 | 0.33 | 0.40 |
| c | 0.13 | 0.18 | 0.23 |
| D | 2.90 | 3.00 | 3.10 |
| E | 2.90 | 3.00 | 3.10 |
| e | 0.65 BSC | | |
| $H_E$ | 4.75 | 4.90 | 5.05 |
| L | 0.40 | 0.55 | 0.70 |

### GENERIC MARKING DIAGRAM*




XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:
PIN 1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98ASB14087C** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
| **DESCRIPTION:** | **MICRO8** | **PAGE 1 OF 1** |