MC14569B

Programmable Divide-By-N Dual 4-Bit Binary/BCD Down Counter

The MC14569B is a programmable divide−by−N dual 4−bit binary or BCD down counter constructed with MOS P−Channel and N−Channel enhancement mode devices (complementary MOS) in a monolithic structure.

This device has been designed for use with the MC14568B phase comparator/counter in frequency synthesizers, phase−locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

Features

- Speed−up Circuitry for Zero Detection
- Each 4−Bit Counter Can Divide Independently in BCD or Binary Mode
- Can be Cascaded With MC14526B for Frequency Synthesizer Applications
- All Outputs are Buffered
- Schmitt Triggered Clock Conditioning
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- This Device is Pb−Free and is RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Temperature Derating: "D/DW" Package: −7.0 mW/°C From 65°C To 125°C
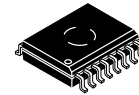
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.
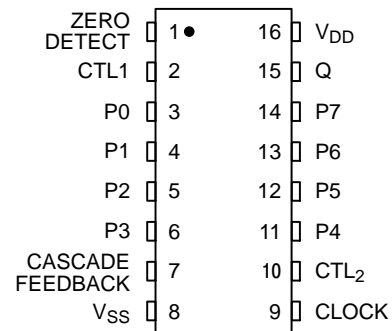
ON Semiconductor®

SOIC−16 WB
DW SUFFIX
CASE 751G

PIN ASSIGNMENT

ZERO DETECT	1●	16	V_{DD}
CTL1	2	15	Q
P0	3	14	P7
P1	4	13	P6
P2	5	12	P5
P3	6	11	P4
CASCADE FEEDBACK	7	10	CTL_2
V_{SS}	8	9	CLOCK

MARKING DIAGRAM

```
16
14569B
AWLYYWWG
1
```
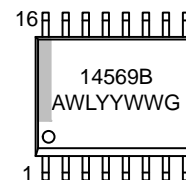
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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BLOCK DIAGRAM

CTL = Low for Binary Count
CTL = High for BCD Count

P0 P1 P2 P3   CTL$_1$ CTL$_2$ P4 P5 P6 P7

3 4 5 6   2   10   11 12 13 14

V_{DD} = PIN 16
V_{SS} = PIN 8

CLOCK ⊶ 9 →

| BINARY/BCD COUNTER #1 | CLOCK
LOAD | BINARY/BCD COUNTER #2 |

15 ⊸ Q

CASCADE FEEDBACK ⊶ 7 →

ZERO DETECT ENCODER

1 ZERO DETECT
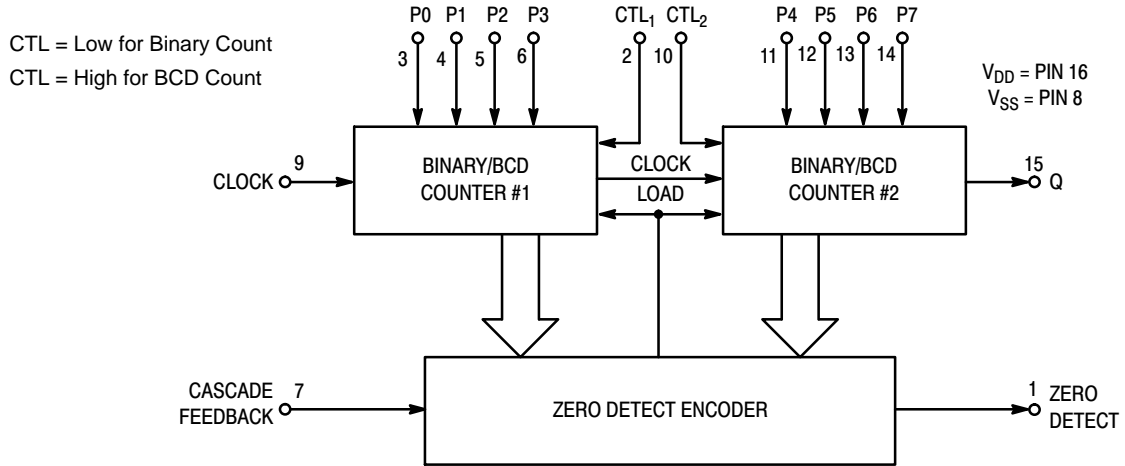
ORDERING INFORMATION

Device	Package	Shipping†
MC14569BDWG	SOIC–16 WB (Pb–Free)	47 Units / Rail
MC14569BDWR2G	SOIC–16 WB (Pb–Free)	1000 Units / Tape & Reel
NLV14569BDWR2G*	SOIC–16 WB (Pb–Free)	1000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable.

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V$_{SS}$)

Characteristic		Symbol	V$_{DD}$ Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ (Note 2)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V$_{in}$ = V$_{DD}$ or 0		V$_{OL}$	5.0 10 15	− − −	0.05 0.05 0.05	− − −	0 0 0	0.05 0.05 0.05	− − −	0.05 0.05 0.05	Vdc
V$_{in}$ = 0 or V$_{DD}$ "1" Level		V$_{OH}$	5.0 10 15	4.95 9.95 14.95	− − −	4.95 9.95 14.95	5.0 10 15	− − −	4.95 9.95 14.95	− − −	Vdc
Input Voltage "0" Level (V$_O$ = 4.5 or 0.5 Vdc) (V$_O$ = 9.0 or 1.0 Vdc) (V$_O$ = 13.5 or 1.5 Vdc)		V$_{IL}$	5.0 10 15	− − −	1.5 3.0 4.0	− − −	2.25 4.50 6.75	1.5 3.0 4.0	− − −	1.5 3.0 4.0	Vdc
(V$_O$ = 0.5 or 4.5 Vdc) "1" Level (V$_O$ = 1.0 or 9.0 Vdc) (V$_O$ = 1.5 or 13.5 Vdc)		V$_{IH}$	5.0 10 15	3.5 7.0 11	− − −	3.5 7.0 11	2.75 5.50 8.25	− − −	3.5 7.0 11	− − −	Vdc
Output Drive Current (V$_{OH}$ = 2.5 Vdc) Source (V$_{OH}$ = 4.6 Vdc) (V$_{OH}$ = 9.5 Vdc) (V$_{OH}$ = 13.5 Vdc)		I$_{OH}$	5.0 5.0 10 15	−3.0 −0.64 −1.6 −4.2	− − − −	−2.4 −0.51 −1.3 −3.4	−4.2 −0.88 −2.25 −8.8	− − − −	−1.7 −0.36 −0.9 −2.4	− − − −	mAdc
(V$_{OL}$ = 0.4 Vdc) Sink (V$_{OL}$ = 0.5 Vdc) (V$_{OL}$ = 1.5 Vdc)		I$_{OL}$	5.0 10 15	0.64 1.6 4.2	− − −	0.51 1.3 3.4	0.88 2.25 8.8	− − −	0.36 0.9 2.4	− − −	mAdc
Input Current		I$_{in}$	15	−	±0.1	−	±0.00001	±0.1	−	±1.0	μAdc
Input Capacitance (V$_{in}$ = 0)		C$_{in}$	−	−	−	−	5.0	7.5	−	−	pF
Quiescent Current (Per Package)		I$_{DD}$	5.0 10 15	− − −	5.0 10 20	− − −	0.005 0.010 0.015	5.0 10 20	− − −	150 300 600	μAdc
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) (C$_L$ = 50 pF on all outputs, all buffers switching)		I$_T$	5.0 10 15	I$_T$ = (0.58 μA/kHz) f + I$_{DD}$ I$_T$ = (1.20 μA/kHz) f + I$_{DD}$ I$_T$ = (1.95 μA/kHz) f + I$_{DD}$							μAdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L − 50) \text{ Vfk}$$

where: I$_T$ is in μA (per package), C$_L$ in pF, V = (V$_{DD}$ − V$_{SS}$) in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

| Characteristic | Symbol | V_{DD} Vdc | All Types | | | Unit |
			Min	Typ (Note 5)	Max	
Output Rise Time	t_{TLH}	5.0	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Output Fall Time	t_{THL}	5.0	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Turn–On Delay Time	t_{PLH}					ns
Zero Detect Output		5.0	–	420	700	
		10	–	175	300	
		15	–	125	250	
Q Output		5.0	–	675	1200	ns
		10	–	285	500	
		15	–	200	400	
Turn–Off Delay Time	t_{PHL}					ns
Zero Detect Output		5.0	–	380	600	
		10	–	150	300	
		15	–	100	200	
Q Output		5.0	–	530	1000	ns
		10	–	225	400	
		15	–	155	300	
Clock Pulse Width	t_{WH}	5.0	300	100	–	ns
		10	150	45	–	
		15	115	30	–	
Clock Pulse Frequency	f_{cl}	5.0	–	3.5	2.1	MHz
		10	–	9.5	5.1	
		15	–	13.0	7.8	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	NO LIMIT			μs
		10				
		15				

5. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
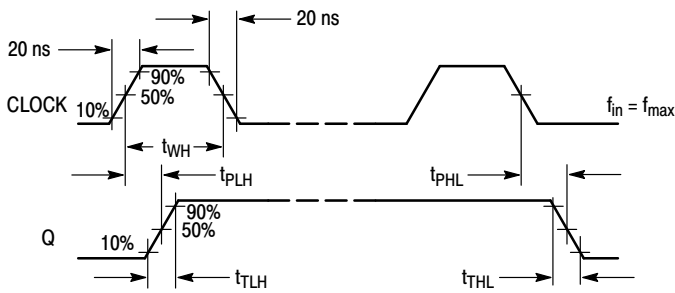
SWITCHING WAVEFORMS
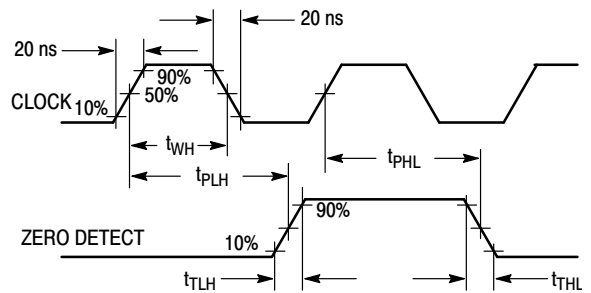

Figure 1.

Figure 2.

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PIN DESCRIPTIONS

INPUTS

P0, P1, P2, P3 (Pins 3, 4, 5, 6) – Preset Inputs. Programmable inputs for the least significant counter. May be binary or BCD depending on the control input.

P4, P5, P6, P7 (Pins 11, 12, 13, 14) – Preset Inputs. Programmable inputs for the most significant counter. May be binary or BCD depending on the control input.

Clock (Pin 9) – Preset data is decremented by one on each positive transition of this signal.

OUTPUTS

Zero Detect (Pin 1) – This output is normally low and goes high for one clock cycle when the counter has decremented to zero.

Q (Pin 15) – Output of the last stage of the most significant counter. This output will be inactive unless the preset input P7 has been set high.

CONTROLS

Cascade Feedback (Pin 7) – This pin is normally set high. When low, loading of the preset inputs (P0 through P7) is inhibited, i.e., P0 through P7 are "don't cares." Refer to Table 1 for output characteristics.

CTL_1 (Pin 2) – This pin controls the counting mode of the least significant counter. When set high, counting mode is BCD. When set low, counting mode is binary.

CTL_2 (Pin 10) – This pin controls the counting mode of the most significant counter. When set high, counting mode is BCD. When set low, counting mode is binary.

SUPPLY PINS

V_{SS} (Pin 18) – Negative Supply Voltage. This pin is usually connected to ground.

V_{DD} (Pin 16) – Positive Supply Voltage. This pin is connected to a positive supply voltage ranging from 3.0 V to 18 V.

OPERATING CHARACTERISTICS

The MC14569B is a programmable divide–by–N dual 4–bit down counter. This counter may be programmed (i.e., preset) in BCD or binary code through inputs P0 to P7. For each counter, the counting sequence may be chosen independently by applying a high (for BCD count) or a low (for binary count) to the control inputs CTL_1 and CTL_2.

The divide ratio N (N being the value programmed on the preset inputs P0 to P7) is automatically loaded into the counter as soon as the count 1 is detected. Therefore, a division ratio of one is not possible. After N clock cycles, one pulse appears on the Zero Detect output. (See Timing Diagram.) The Q output is the output of the last stage of the most significant counter (See Tables 1 through 5, Mode Controls.)

When cascading the MC14569B to the MC14526B, the Cascade Feedback input, Q, and Zero Detect outputs must be respectively connected to "0", Clock, and Load of the following counter. If the MC14569B is used alone, Cascade Feedback must be connected to V_{DD}.
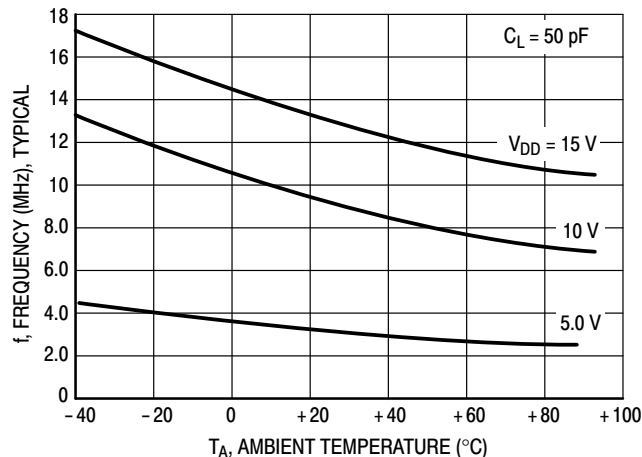
Table 1Mode Controls (Cascade Feedback = Low)

Counter Control Values		Divide Ratio	
CTL_1	CTL_2	Zero Detect	Q
0	0	256	256
0	1	160	160
1	0	160	160
1	1	100	100

NOTE: Data Preset Inputs (P0–P7) are "Don't Cares" while Cascade Feedback is Low.

Table 2Mode Controls (CTL_1 = Low, CTL_2 = Low, Cascade Feedback = High)

Preset Inputs								Divide Ratio		
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q	Comments
0	0	0	0	0	0	0	0	256	256	Max Count
0	0	0	0	0	0	0	1	X	X	Illegal State
0	0	0	0	0	0	1	0	2	X	Min Count
0	0	0	0	0	0	1	1	3	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	0	1	1	1	1	15	X	
0	0	0	1	0	0	0	0	16	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	1	0	0	0	0	0	32	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	0	0	0	0	0	0	64	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	1	1	1	1	1	1	127	X	
1	0	0	0	0	0	0	0	128	128	Q Output Active
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	0	1	0	0	0	136	136	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	1	1	1	1	1	1	1	255	255	↓
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0			
128	64	32	16	8	4	2	1			Bit Value
Counter #2 Binary				Counter #1 Binary						Counting Sequence

X = No Output (Always Low)

Table 3Mode Controls (CTL$_1$ = High, CTL$_2$ = Low, Cascade Feedback = High)

P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q	Comments
Preset Inputs								Divide Ratio		
0	0	0	0	0	0	0	0	160	160	Max Count
0	0	0	0	0	0	0	1	X	X	Illegal State
0	0	0	0	0	0	1	0	2	X	Min Count
0	0	0	0	0	0	1	1	3	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	0	1	0	0	1	9	X	
0	0	0	1	0	0	0	0	10	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	1	1	0	0	1	19	X	
0	0	1	0	0	0	0	0	20	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	1	1	0	0	0	0	30	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	0	0	0	0	0	0	40	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	0	1	0	0	0	0	50	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	1	0	0	0	0	0	60	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	1	1	0	0	0	0	70	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
1	0	0	0	0	0	0	0	80	80	Q Output Active
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	1	0	0	0	0	90	90	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	1	1	1	0	0	0	0	150	150	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	1	1	1	1	0	0	1	159	159	
80	40	20	10	8	4	2	1			Bit Value
Counter #2 Binary				Counter #1 BCD						Counting Sequence

X = No Output (Always Low)

Table 4Mode Controls (CTL$_1$ = Low, CTL$_2$ = High, Cascade Feedback = High)

P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q	Comments
\multicolumn{8}{c}{**Preset Values**}			\multicolumn{2}{c}{**Divide Ratio**}		
0	0	0	0	0	0	0	0	160	160	Max Count
0	0	0	0	0	0	0	1	X	X	Illegal State
0	0	0	0	0	0	1	0	2	X	Min Count
0	0	0	0	0	0	1	1	3	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	0	1	1	1	1	15	X	
0	0	0	1	0	0	0	0	16	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	1	1	1	1	1	31	X	
0	0	1	0	0	0	0	0	32	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	1	1	0	0	0	0	48	X	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
0	1	0	0	0	0	0	0	64	X	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
0	1	0	1	0	0	0	0	80	X	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
0	1	1	1	0	0	0	0	112	X	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	0	0	0	0	0	128	128	Q Output Active
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	1	0	0	0	0	144	144	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	1	1	1	1	1	159	159	
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0			
128	64	32	16	8	4	2	1			Bit Value
\multicolumn{4}{c}{Counter #2 BCD}				\multicolumn{4}{c}{Counter #1 Binary}					Counting Sequence

X = No Output (Always Low)

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Table 5Mode Controls (CTL$_1$ = High, CTL$_2$ = High, Cascade Feedback = High)

Preset Values								Divide Ratio		
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q	Comments
0	0	0	0	0	0	0	0	100	100	Max Count
0	0	0	0	0	0	0	1	X	X	illegal state
0	0	0	0	0	0	1	0	2	X	Min Count
0	0	0	0	0	0	1	1	3	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	0	1	0	0	1	9	X	
0	0	0	1	0	0	0	0	10	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	1	1	0	0	0	0	30	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	0	0	0	0	0	0	40	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	0	1	0	0	0	0	50	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	1	1	0	0	0	0	70	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
1	0	0	0	0	0	0	0	80	80	Q Output Active
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	1	0	0	0	0	90	90	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	1	1	0	0	1	99	99	↓
80	40	20	10	8	4	2	1			Bit Value
Counter #2 BCD				Counter #1 BCD						Counting Sequence

X = No Output (Always Low)

TIMING DIAGRAM MC14569B
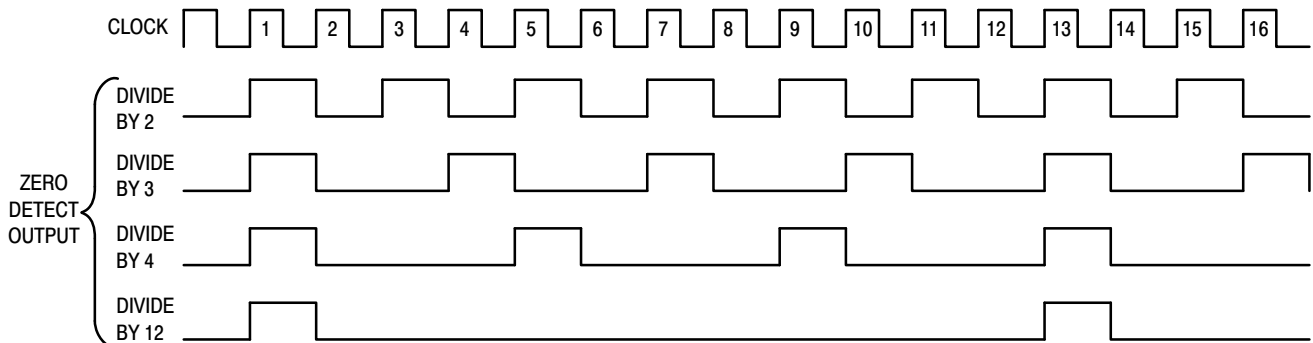
MC14569B

LOGIC DIAGRAM
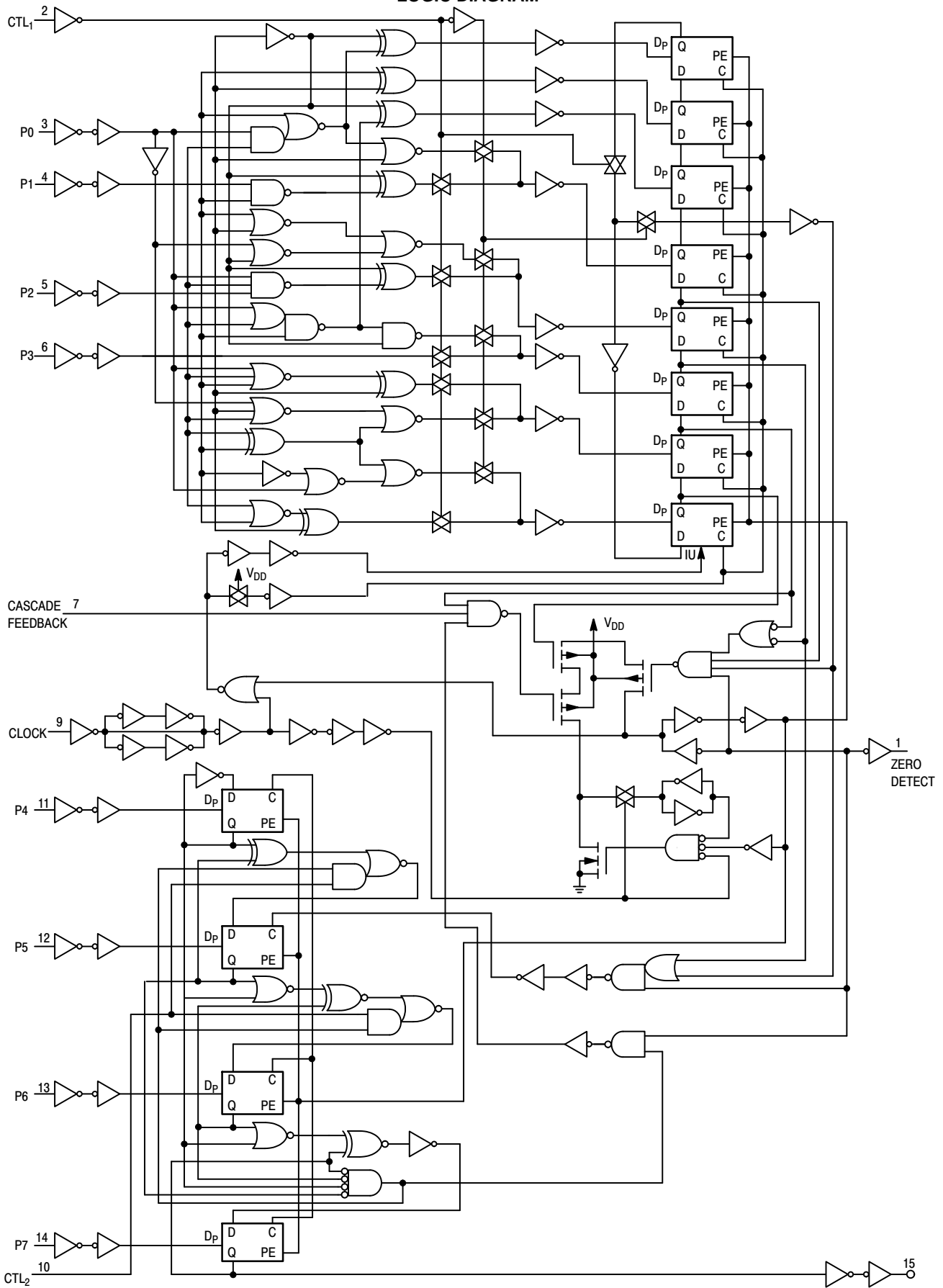
MC14569B
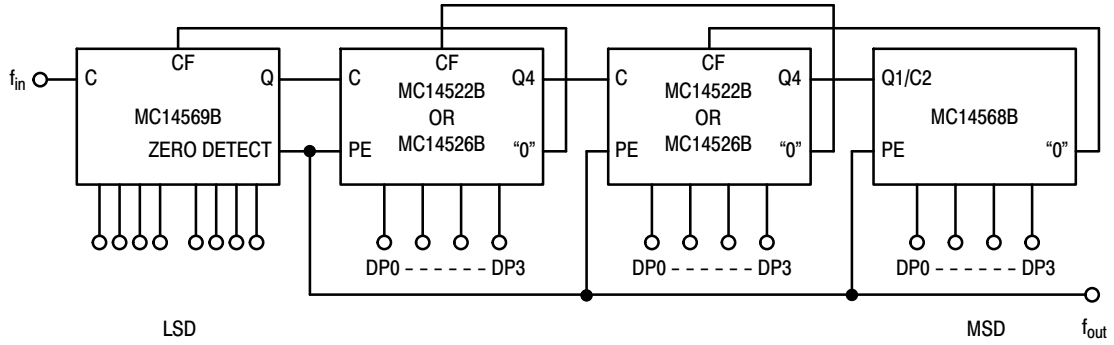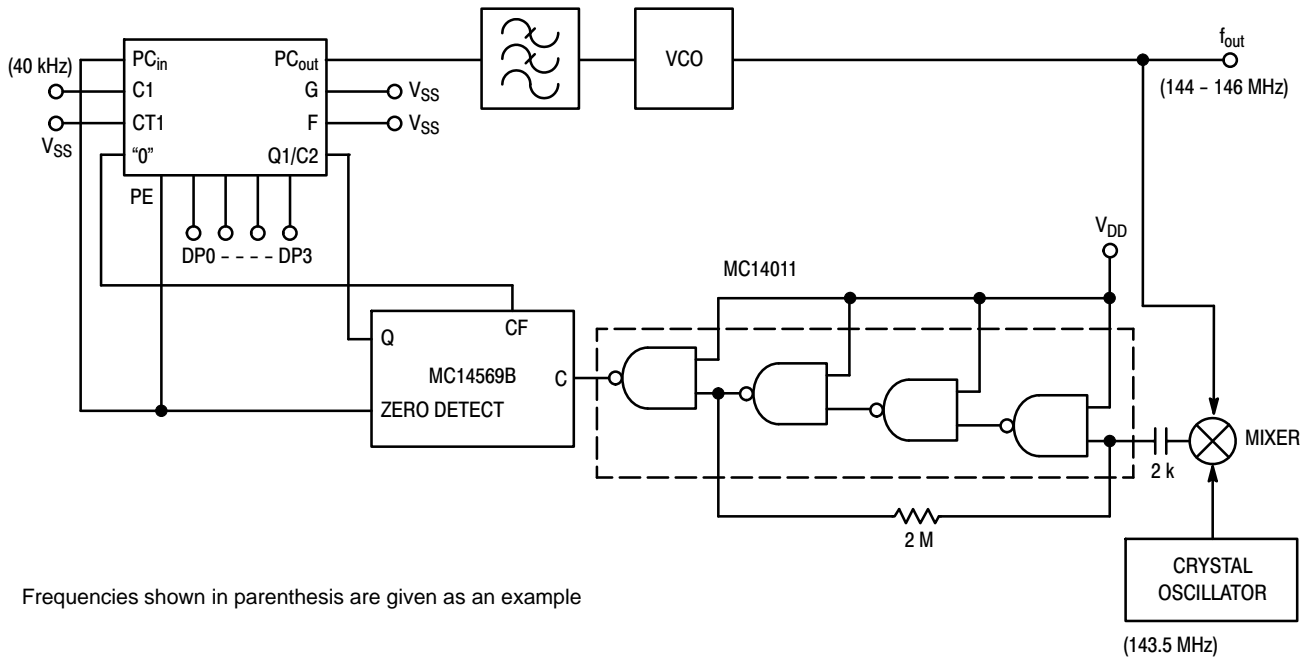
TYPICAL APPLICATIONS

Figure 3. Cascading MC14568B and MC14522B or MC14526B with MC14569B

Frequencies shown in parenthesis are given as an example

Figure 4. Frequency Synthesizer with MC14568B and MC14569B Using a Mixer
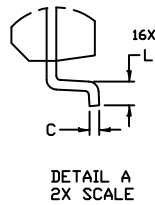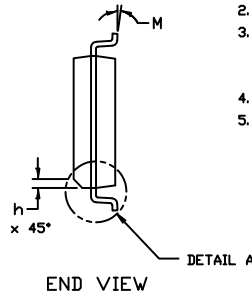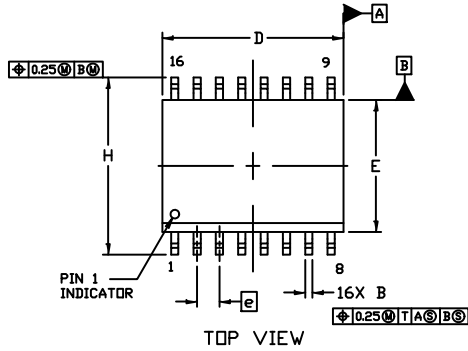**(Channel Spacing 10 kHz)**

onsemi

SOIC−16 WB
CASE 751G
ISSUE E

DATE 08 OCT 2021

1

SCALE 1:1

⊕ 0.25 Ⓜ B Ⓜ

Ⓐ

B

D

16   9

H

E

PIN 1
INDICATOR

1   8

e   16X B

⊕ 0.25 Ⓜ T A Ⓢ B Ⓢ

TOP VIEW

M

h
× 45°

DETAIL A

END VIEW

A1   A

SEATING
PLANE   T

SIDE VIEW

16X

L

C

DETAIL A
2X SCALE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
   ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS
   OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION OR FLASH TO BE 0.15 PER SIDE.

DIM	MILLIMETERS	
	MIN.	MAX.
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.53 REF	
L	0.50	0.90
M	0°	7°

16X 0.58

11.00

16X 1.62   1

1.27
PITCH

RECOMMENDED
MOUNTING FOOTPRINT

GENERIC
MARKING DIAGRAM*

16

XXXXXXXXXXX
XXXXXXXXXXX
AWLYYWWG

1
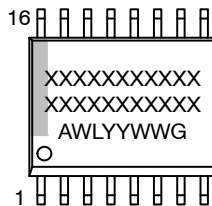
XXXXX = Specific Device Code
A   = Assembly Location
WL   = Wafer Lot
YY   = Year
WW   = Work Week
G   = Pb−Free Package

*This information is generic. Please refer to
device data sheet for actual part marking.
Pb−Free indicator, "G" or microdot "▪", may
or may not be present. Some products may
not follow the Generic Marking.