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# NLX1G332

# 3-Input OR Gate

The NLX1G332 is an advanced high−speed 3−input CMOS OR gate in ultra−small footprint.

The NLX1G332 input structures provide protection when voltages up to 7.0 V are applied, regardless of the supply voltage.

### Features

- High Speed: $t_{PD}$ = 2.4 ns (Typ) @ $V_{CC}$ = 5.0 V
- Designed for 1.65 V to 5.5 V $V_{CC}$ Operation
- Low Power Dissipation: $I_{CC}$ = 1 μA (Max) at $T_A$ = 25°C
- 24 mA Balanced Output Source and Sink Capability
- Balanced Propagation Delays
- Overvoltage Tolerant (OVT) Input Pins
- Ultra−Small Packages
- These are Pb−Free Devices

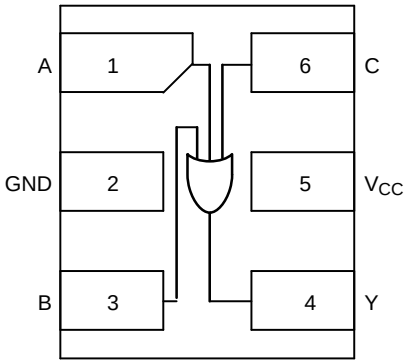


**Figure 1. Pinout** (Top View)

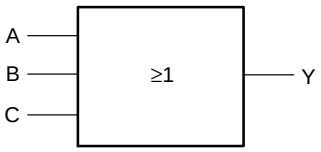


**Figure 2. Logic Symbol**

**PIN ASSIGNMENT**

| Pin | Function |
|---|---|
| 1 | A |
| 2 | GND |
| 3 | B |
| 4 | Y |
| 5 | $V_{CC}$ |
| 6 | C |

**FUNCTION TABLE**

| Input | | | Output |
|---|---|---|---|
| **A** | **B** | **C** | **Y** |
| H | X | X | H |
| X | H | X | H |
| X | X | H | H |
| L | L | L | L |

H − HIGH Logic Level
L − LOW Logic Level
X = Either LOW or HIGH Logic Level

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**MARKING DIAGRAMS**

1

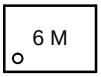
**UDFN6**
**1.0 x 1.0**
**CASE 517BX**


1

**UDFN6**
**1.2 x 1.0**
**CASE 517AA**


1

**UDFN6**
**1.45 x 1.0**
**CASE 517AQ**




X = Device Marking
M = Date Code
▪ = Pb−Free Package

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

## MAXIMUM RATINGS

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | | −0.5 to +7.0 | V |
| $V_{IN}$ | DC Input Voltage | | −0.5 to +7.0 | V |
| $V_{OUT}$ | DC Output Voltage | | −0.5 to +7.0 | V |
| $I_{IK}$ | DC Input Diode Current | $V_{IN}$ < GND | −50 | mA |
| $I_{OK}$ | DC Output Diode Current | $V_{OUT}$ < GND | −50 | mA |
| $I_O$ | DC Output Source/Sink Current | | ±50 | mA |
| $I_{CC}$ | DC Supply Current Per Supply Pin | | ±100 | mA |
| $I_{GND}$ | DC Ground Current per Ground Pin | | ±100 | mA |
| $T_{STG}$ | Storage Temperature Range | | −65 to +150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds | | 260 | °C |
| $T_J$ | Junction Temperature Under Bias | | 150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Note 1) | | 496 | °C/W |
| $P_D$ | Power Dissipation in Still Air @ 85°C | | 252 | mW |
| MSL | Moisture Sensitivity | | Level 1 | |
| $F_R$ | Flammability Rating Oxygen | Index: 28 to 34 | UL 94 V−0 @ 0.125 in | |
| $V_{ESD}$ | ESD Withstand Voltage | Human Body Model (Note 2)<br>Machine Model (Note 3)<br>Charged Device Model (Note 4) | >2000<br>>200<br>N/A | V |
| $I_{LATCHUP}$ | Latchup Performance Above $V_{CC}$ and Below GND at 125 °C (Note 5) | | ±500 | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2 ounce copper trace no air flow.
2. Tested to EIA/JESD22−A114−A.
3. Tested to EIA/JESD22−A115−A.
4. Tested to JESD22−C101−A.
5. Tested to EIA / JESD78.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Positive DC Supply Voltage | Operating<br>Data Retention Only | 1.65<br>1.5 | 5.5<br>5.5 | V |
| $V_{IN}$ | Digital Input Voltage (Note 6) | | 0 | 5.5 | V |
| $V_{OUT}$ | Output Voltage | | 0 | 5.5 | V |
| $T_A$ | Operating Free−Air Temperature | | −55 | +125 | °C |
| $\Delta t/\Delta V$ | Input Transition Rise or Fall Rate | $V_{CC}$ = 1.8 V ± 0.15 V<br>$V_{CC}$ = 2.5 V ± 0.2 V<br>$V_{CC}$ = 3.3 V ± 0.3 V<br>$V_{CC}$ = 5.0 V ± 0.5 V | 0<br>0<br>0<br>0 | 20<br>20<br>10<br>5 | ns/V |

6. Unused inputs may not be left open. All inputs must be tied to a high or low−logic input voltage level.

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

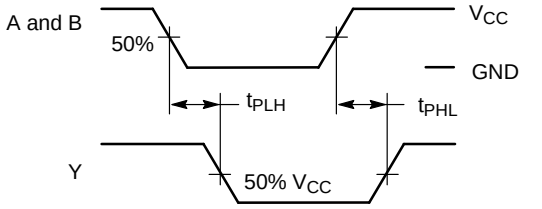
| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A$ = 25 °C | | | $T_A$ = −55°C to +125°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | |
| $V_{IH}$ | Low−Level Input Voltage | | 1.65 | 0.75 x $V_{CC}$ | | | 0.75 x $V_{CC}$ | | V |
| | | | 2.3 to 5.5 | 0.70 x $V_{CC}$ | | | 0.70 x $V_{CC}$ | | |
| $V_{IL}$ | Low−Level Input Voltage | | 1.65 | | | 0.25 x $V_{CC}$ | | 0.25 x $V_{CC}$ | V |
| | | | 2.3 − 5.5 | | | 0.30 x $V_{CC}$ | | 0.30 x $V_{CC}$ | |
| $V_{OH}$ | High−Level Output Voltage | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OH}$ = −100 μA | 1.65 − 5.5 | $V_{CC}$−0.1 | $V_{CC}$ | | $V_{CC}$−0.1 | | V |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OH}$ = −4 mA<br>$I_{OH}$ = −8 mA<br>$I_{OH}$ = −12 mA<br>$I_{OH}$ = −16 mA<br>$I_{OH}$ = −24 mA<br>$I_{OH}$ = −32 mA | 1.65<br>2.3<br>2.7<br>3.0<br>3.0<br>4.5 | 1.29<br>1.9<br>2.2<br>2.4<br>2.3<br>3.8 | 1.52<br>2.15<br>2.4<br>2.8<br>2.68<br>4.2 | | 1.29<br>1.9<br>2.2<br>2.4<br>2.3<br>3.8 | | |
| $V_{OL}$ | Low−Level Output Voltage | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OL}$ = 100 μA | 1.65 − 5.5 | | | 0.1 | | 0.1 | V |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OH}$ = 4 mA<br>$I_{OH}$ = 8 mA<br>$I_{OH}$ = 12 mA<br>$I_{OH}$ = 16 mA<br>$I_{OH}$ = 24 mA<br>$I_{OH}$ = 32 mA | 1.65<br>2.3<br>2.7<br>3.0<br>3.0<br>4.5 | | 0.08<br>0.1<br>0.12<br>0.15<br>0.22<br>0.22 | 0.24<br>0.3<br>0.4<br>0.4<br>0.55<br>0.55 | | 0.24<br>0.3<br>0.4<br>0.4<br>0.55<br>0.55 | |
| $I_{IN}$ | Input Leakage Current | 0 ≤ $V_{IN}$ ≤ 5.5V | 0 to 5.5 | | | ±0.1 | | ±1.0 | μA |
| $I_{OFF}$ | Power−Off Output Leakage Current | $V_{IN}$ or $V_{OUT}$ = 5.5 V | 0 | | | 1.0 | | 10 | μA |
| $I_{CC}$ | Quiescent Supply Current | 0 ≤ $V_{IN}$ ≤ $V_{CC}$ | 5.5 | | | 1.0 | | 10 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## AC ELECTRICAL CHARACTERISTICS (Input $t_r$ = $t_f$ = 2.5 nS)

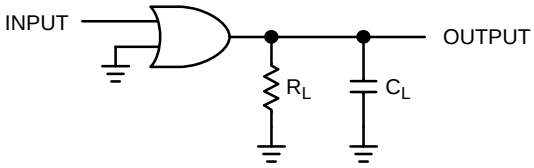
| Symbol | Parameter | $V_{CC}$ (V) | Test Condition | $T_A$ = 25 °C | | | $T_A$ = −55°C to +125°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay, Input to Output | 1.65−1.95 | $R_L$ = 1 MΩ, $C_L$ = 15 pF | 2.0 | 5.5 | 18.5 | 2.0 | 19 | ns |
| | | 2.3−2.7 | $R_L$ = 1 MΩ, $C_L$ = 15 pF | 0.8 | 3.0 | 11 | 0.8 | 11.5 | |
| | | 3.0−3.6 | $R_L$ = 1 MΩ, $C_L$ = 15 pF | 0.5 | 2.6 | 7.5 | 0.5 | 8.0 | |
| | | | $R_L$ = 500 Ω, $C_L$ = 50 pF | 1.5 | 3.0 | 8.5 | 1.5 | 9.0 | |
| | | 4.5−5.5 | $R_L$ = 1 MΩ, $C_L$ = 15 pF | 0.5 | 2.2 | 5.5 | 0.5 | 6.0 | |
| | | | $R_L$ = 500 Ω, $C_L$ = 50 pF | 0.8 | 2.4 | 7.0 | 0.8 | 7.5 | |
| $C_{IN}$ | Input Capacitance | 5.5 | $V_{IN}$ = 0 V or $V_{CC}$ | | 4.0 | | | | pF |
| $C_{PD}$ | Power Dissipation Capacitance (Note 7) | 3.3<br>5.5 | 10 MHz<br>$V_{IN}$ = 0 V or $V_{CC}$ | | 20<br>26 | | | | pF |

7. $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)}$ = $C_{PD}$ • $V_{CC}$ • $f_{in}$ + $I_{CC}$. $C_{PD}$ is used to determine the no−load dynamic power consumption: $P_D$ = $C_{PD}$ • $V_{CC}^2$ • $f_{in}$ + $I_{CC}$ • $V_{CC}$.




$t_R = t_F$ = 2.5 ns, 10% to 90%, f = 1 MHz, $t_W$ = 500 ns

**Figure 3. Switching Waveforms**




A 1 MHz square input wave is recommended for propagation delay tests

**Figure 4. Test Circuit**

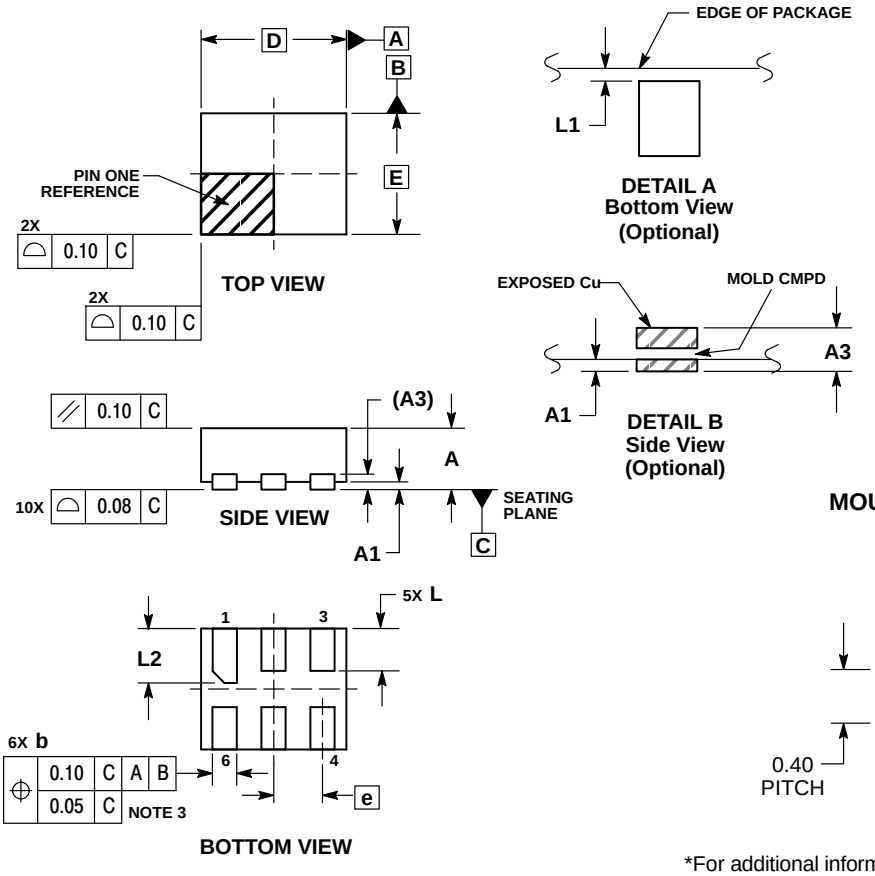
## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NLX1G332MUTCG<br>In Development | UDFN6, 1.2 x 1.0, 0.4P<br>(Pb−Free) | 3000 / Tape & Reel |
| NLX1G332AMUTCG | UDFN6, 1.45 x 1.0, 0.5P<br>(Pb−Free) | 3000 / Tape & Reel |
| NLX1G332CMUTCG | UDFN6, 1.0 x 1.0, 0.35P<br>(Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## PACKAGE DIMENSIONS

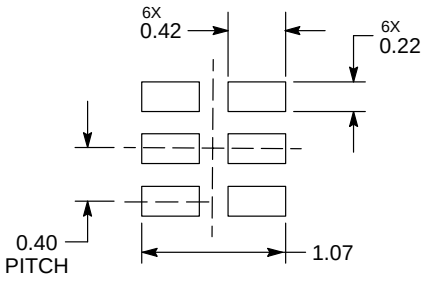
**UDFN6, 1.2x1.0, 0.4P**
CASE 517AA−01
ISSUE D




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.45 | 0.55 |
| A1 | 0.00 | 0.05 |
| A3 | 0.127 REF | |
| b | 0.15 | 0.25 |
| D | 1.20 BSC | |
| E | 1.00 BSC | |
| e | 0.40 BSC | |
| L | 0.30 | 0.40 |
| L1 | 0.00 | 0.15 |
| L2 | 0.40 | 0.50 |

**MOUNTING FOOTPRINT***

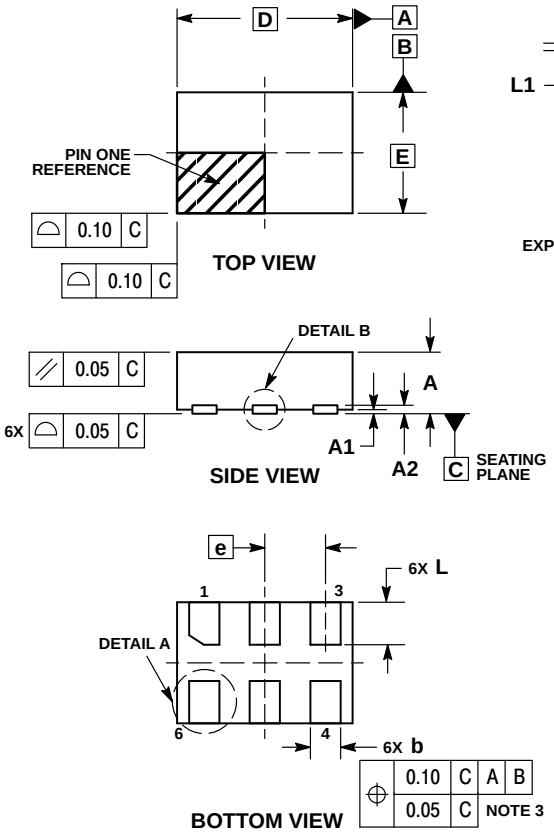


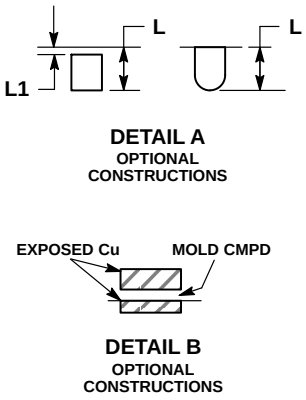

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

**UDFN6 1.45x1.0, 0.5P**
CASE 517AQ
ISSUE O

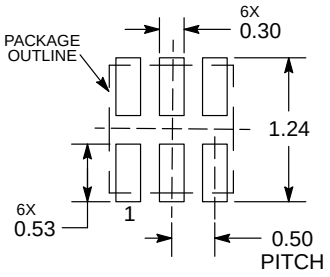



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.45 | 0.55 |
| A1 | 0.00 | 0.05 |
| A2 | 0.07 REF | |
| b | 0.20 | 0.30 |
| D | 1.45 BSC | |
| E | 1.00 BSC | |
| e | 0.50 BSC | |
| L | 0.30 | 0.40 |
| L1 | ––– | 0.15 |

### MOUNTING FOOTPRINT




DIMENSIONS: MILLIMETERS

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