NPT2018

12.5 W GaN Wideband Transistor
DC - 3.5 GHz

Rev. V3

Features

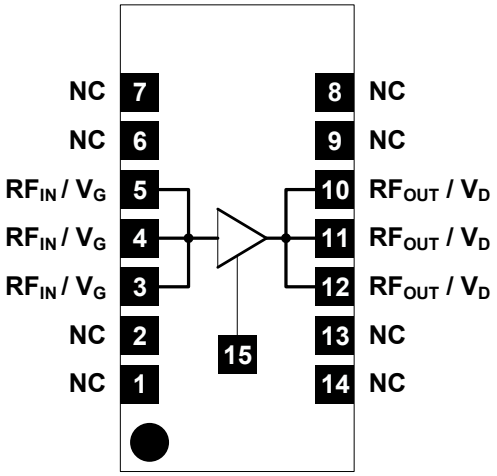
- GaN on Si HEMT D-Mode Transistor
- Suitable for Linear and Saturated Applications
- Tunable from DC - 3.5 GHz
- 50 V Power Operation
- 16 dB Gain @ 2.5 GHz
- 56% Drain Efficiency @ 2.5 GHz
- 100% RF Tested
- Lead-Free 3 x 6 mm 14-Lead PDFN Package
- RoHS* Compliant

Description

The NPT2018 GaN HEMT is a wideband transistor optimized for DC - 3.5 GHz operation. This device supports CW, pulsed, and linear operation with output power levels to 12.5 W (41 dBm) in an industry standard surface mount plastic package.

The NPT2018 is ideally suited for defense communications, land mobile radio, avionics, wireless infrastructure, ISM applications and VHF/ UHF/L/S-band radar.

Functional Schematic



Ordering Information[1]

Part Number	Package
NPT2018	Bulk
NPT2018-TR500	500 piece reel
NPT2018-TR100	100 piece reel
NPT2018-SMB	Sample Board

1. Reference Application Note M513 for reel size information.

Pin Configuration

Pin #	Pin Name	Function
1-2, 6-9, 13-14	NC	No Connection
3-5	RF_{IN} / V_G	RF Input / Gate
10-12	RF_{OUT} / V_D	RF Output / Drain
15	Paddle[2]	Ground / Source

2. The exposed pad centered on the package bottom must be connected to RF and DC ground. This path must also provide a low thermal resistance heat path.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

RF Electrical Specifications: T_A = 25°C, V_{DS} = 50 V, I_{DQ} = 75 mA

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Units
Small Signal Gain	CW, 2.5 GHz	G_{SS}	-	19	-	dB
Output Power	CW, 2.5 GHz, P_{IN} = 25 dBm	P_{SAT}	41.0	42.5	-	dBm
Power Gain	CW, 2.5 GHz, P_{IN} = 25 dBm	G_P	14.5	17.0	-	dB
Drain Efficiency	CW, 2.5 GHz, P_{IN} = 25 dBm	η	48.0	59.0	-	%
Ruggedness: Output Mismatch	All phase angles	Y	VSWR = 10:1, No Device Damage			

DC Electrical Characteristics: T_A = 25°C

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Units
Drain-Source Leakage Current	V_{GS} = -8 V, V_{DS} = 160 V	I_{DLK}	-	-	3.15	mA
Gate Threshold Voltage	V_{DS} = 50 V, I_D = 3 mA	V_T	-2.5	-1.5	-0.5	V
Gate Quiescent Voltage	V_{DS} = 50 V, I_D = 75 mA	V_{GSQ}	-2.1	-1.2	-0.3	V
On Resistance	V_{DS} = 2 V, I_D = 22 mA	R_{ON}	-	1.6	-	Ω
Maximum Drain Current	V_{DS} = 7 V pulsed, pulse width 300 µs	$I_{D,MAX}$	-	1.75	-	A

Thermal Characteristics[3,4]

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Units
Thermal Resistance	V_{DS} = 50 V, P_D = 11.5 W, T_C = 85°C, T_{CN} = 85°C	$R_{\theta JC}$	-	9.9	-	°C/W

3. Junction temperature (T_{CN}) measured using IR Microscopy. Case temperature measured using thermocouple embedded in heat-sink.
4. The thermal resistance of the mounting configuration must be added to the device $R_{\theta JC}$, for proper T_{CN} calculation during operation. The recommended via pattern, shown on page 5, on a 20 mil thick, 1 oz. plated copper, PCB adds an additional 3.4°C/W to the typical value.

Absolute Maximum Ratings[5,6,7]

Parameter	Absolute Maximum
Drain Source Voltage, V_{DS}	160 V
Gate Source Voltage, V_{GS}	-10 to 3 V
Gate Current, I_G	3.2 mA
Channel Temperature, T_{CN}	+225°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C

5. Exceeding any one or combination of these limits may cause permanent damage to this device.
6. MACOM does not recommend sustained operation near these survivability limits.
7. Operating at nominal conditions with $T_{CN} \leq 200°C$ will ensure MTTF > 1 x 10^6 hours.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Nitride Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A and CDM Class 2CA devices.

Bias Sequencing

Turning the device ON

1. Set V_{GS} to the pinch-off (V_P), typically -5 V.
2. Turn on V_{DS} to nominal voltage (50 V).
3. Increase V_{GS} until the I_{DS} current is reached.
4. Apply RF power to desired level.

Turning the device OFF

1. Turn the RF power off.
2. Decrease V_{GS} down to V_P.
3. Decrease V_{DS} down to 0 V.
4. Turn off V_{GS}.

12.5 W GaN Wideband Transistor
DC - 3.5 GHz

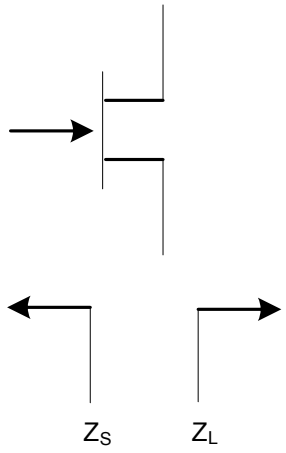
Rev. V3

Load-Pull Performance: V_{DS} = 50 V, I_{DQ} = 75 mA, T_C = 25°C

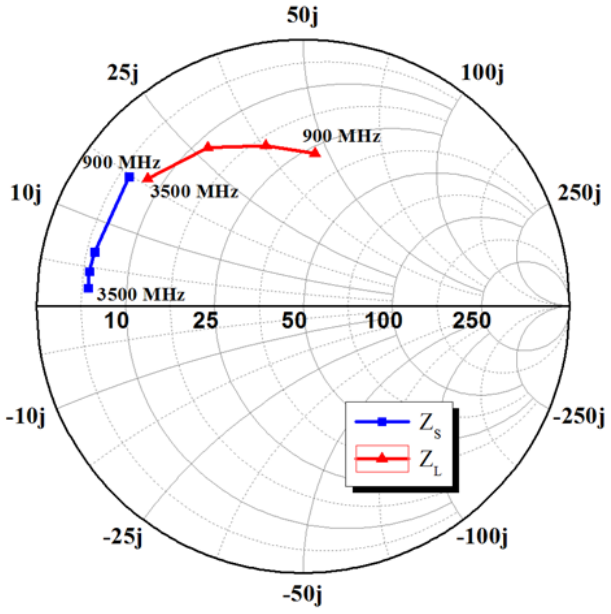
Reference Plane at Device Leads, CW Drain Efficiency and Output Power Tradeoff Impedance

Frequency (MHz)	Z_S (Ω)	Z_L (Ω)	P_{SAT} (W)	G_{SS} (dB)	Drain Efficiency at P_{SAT} (%)
900	5.7 + j16.4	27 + j46.2	14.5	29.0	62
1800	5.4 + j6.3	18.6 + j36.2	14.2	22.0	59
2500	5.2 + j4	11.8 + j27.1	14.0	19.0	57
3500	5.3 + j2.1	7.9 + j17.5	13.0	16.5	55

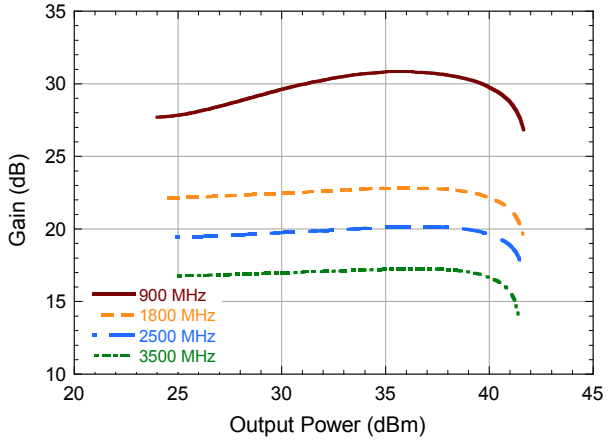
Impedance Reference



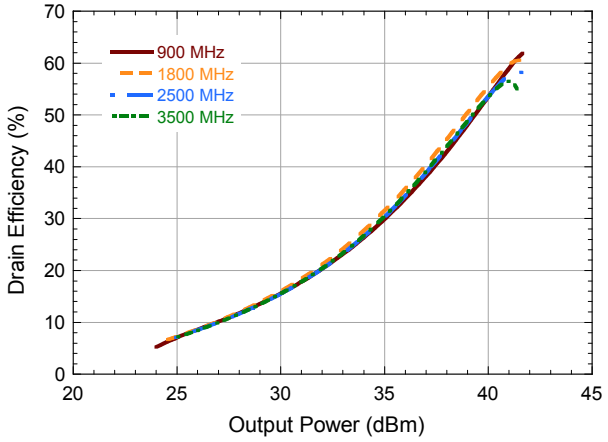
Z_S and Z_L vs. Frequency



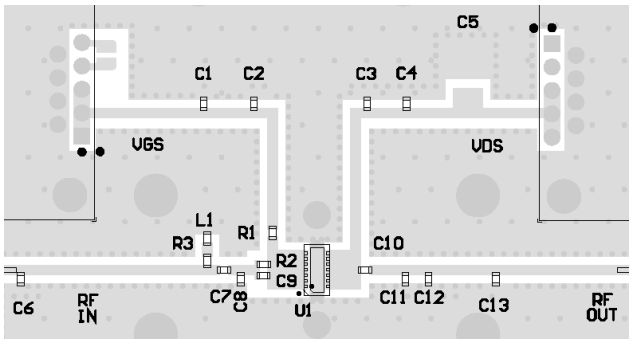
Gain vs. Output Power



Drain Efficiency vs. Output Power



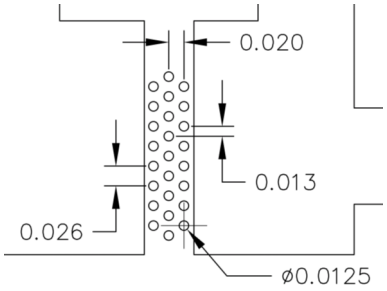
2.5 GHz Sample Board



Parts are tested in a narrowband 2.5 GHz sample board (20-mil thick RO4350). Electrical and thermal grounding is provided using a standard-plated densely packed via hole array (see recommended via pattern).

Matching is provided using a combination of lumped elements and transmission lines as shown in the layout to the left. Recommended tuning solution component placement, transmission lines, and details are shown below.

Recommended Via Pattern



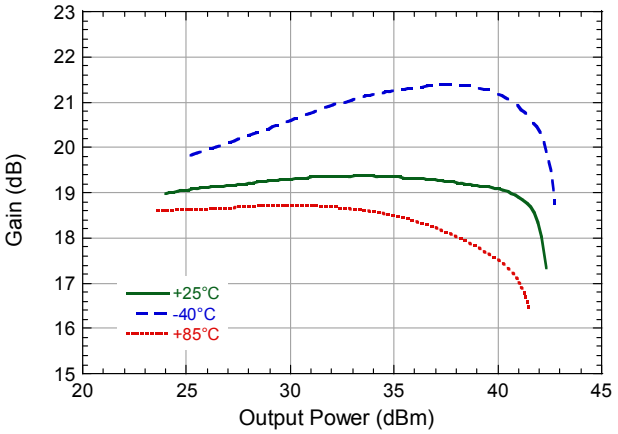
Dimensions in inches.

Parts List

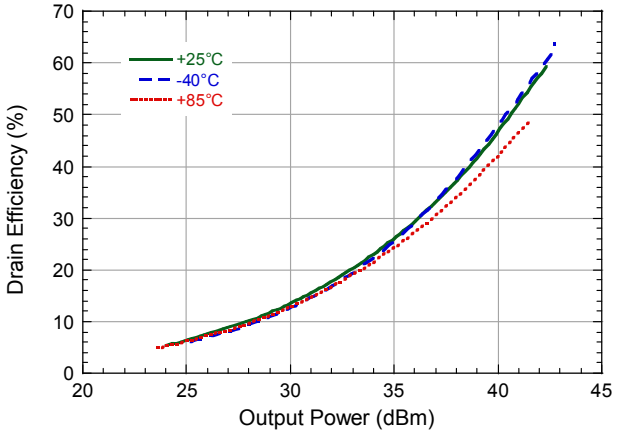
Ref. Designator	Value	Tolerance	Manufacturer	Mfg. Part Number
C1	1 µF	10%	TDK	C1608X6S1H105K080AC
C2, C3, C10	10 pF	2%	Passive Plus	0603N100GW251
C4	10 nF	10%	Murata	GCM188R72A103KA37D
C5	Not Used			
C6	0.6 pF	±0.05 pF	Passive Plus	0603N0R6AW251
C7	1.8 pF	±0.05 pF	Passive Plus	0603N1R8AW251
C8	2.7 pF	±0.05 pF	Passive Plus	0603N2R7AW251
C9	4.7 pF	±0.1 pF	Passive Plus	0603N4R7BW251
C11	3.0 pF	±0.05 pF	Passive Plus	0603N3R0AW251
C12	0.4 pF	±0.05 pF	Passive Plus	0603N0R4AW251
C13	0.9 pF	±0.05 pF	Passive Plus	0603N0R9AW251
L1	10 nH	±5%		
R1	300 Ω	5%	Panasonic	ERJ-3GEYJ301V
R2	100 Ω	5%	Panasonic	ERJ-3GEYJ101V
R3	43 Ω	5%	Panasonic	ERJ-3GEYJ430V

Typical Performance as Measured in the 2.5 GHz Sample Board: CW, V_{DS} = 50 V, I_{DQ} = 75 mA (Unless Noted)

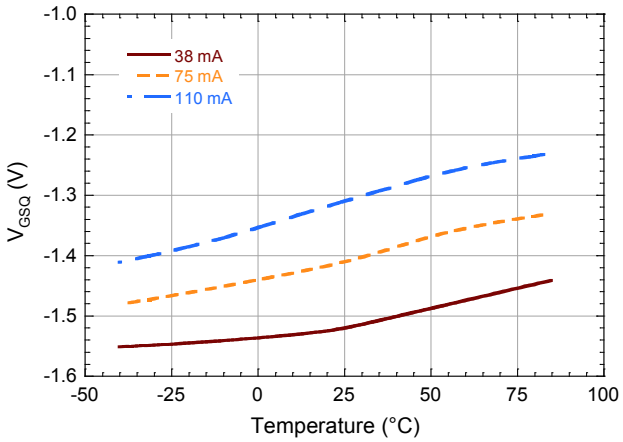
Gain vs. Output Power Over Temperature



Drain Efficiency vs. Output Power Over Temperature

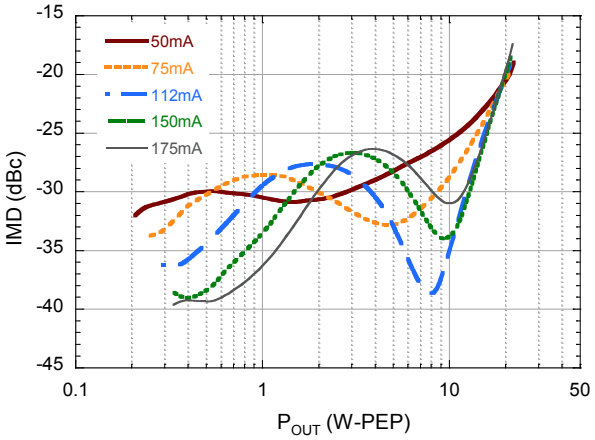


Quiescent V_{GS} vs. Temperature

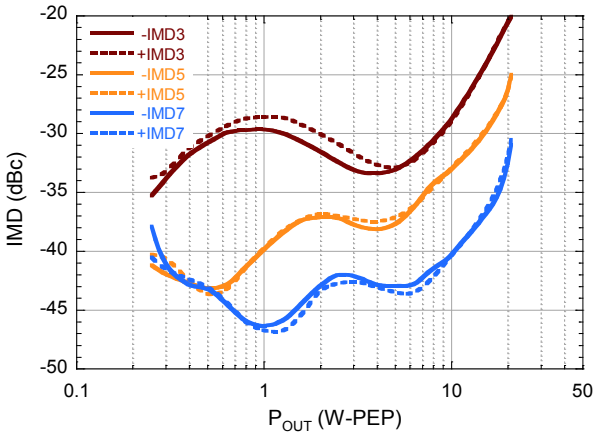


Typical 2-Tone Performance as Measured in the 2.5 GHz Sample Board: 1 MHz Tone Spacing, V_{DS} = 50 V, I_{DQ} = 75 mA, T_C = 25°C (Unless Noted)

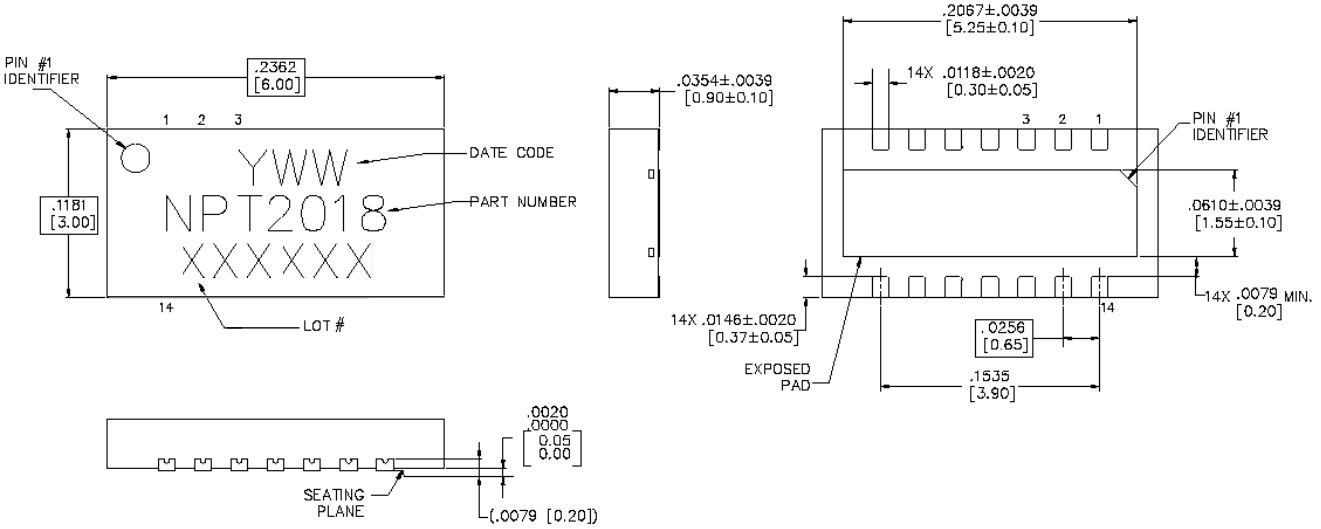
2-Tone IMD3 vs. Output Power vs. Quiescent Current



2-Tone IMD vs. Output Power



3 x 6 mm 14-Lead DFN Plastic Package†



All dimensions shown as in [mm]

† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 3 requirements.
Plating is Ni / Pd / Au.