BCP69T1G, NSVBCP69T1G

PNP Silicon Epitaxial Transistor

This PNP Silicon Epitaxial Transistor is designed for use in low voltage, high current applications. The device is housed in the SOT−223 package, which is designed for medium power surface mount applications.

Features

- High Current: I_C = −1.0 A
- The SOT−223 Package Can Be Soldered Using Wave or Reflow.
- SOT−223 package ensures level mounting, resulting in improved thermal conduction, and allows visual inspection of soldered joints. The formed leads absorb thermal stress during soldering, eliminating the possibility of damage to the die.
- NPN Complement is BCP68
- AEC−Q101 Qualified and PPAP Capable
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	−20	Vdc
Collector−Base Voltage	V_{CBO}	−25	Vdc
Emitter−Base Voltage	V_{EBO}	−5.0	Vdc
Collector Current	I_C	−1.0	Adc
Total Power Dissipation @ T_A = 25°C (Note 1) Derate above 25°C	P_D	1.5 12	W mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance − Junction−to−Ambient (Surface Mounted)	$R_{\theta JA}$	83.3	°C/W
Lead Temperature for Soldering, 0.0625 in from case Time in Solder Bath	T_L	260 10	°C s

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Device mounted on a glass epoxy printed circuit board 1.575 in. x 1.575 in. x 0.059 in.; mounting pad for the collector lead min. 0.93 sq. in.

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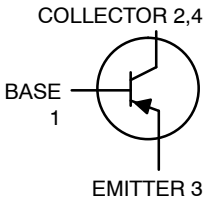
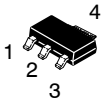
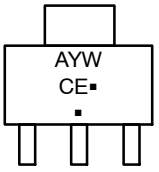
MEDIUM POWER PNP SILICON HIGH CURRENT TRANSISTOR SURFACE MOUNT





SOT−223 (TO−261)
CASE 318E
STYLE 1

MARKING DIAGRAM



CE = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(*Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
BCP69T1G	SOT−223 (Pb−Free)	1000 / Tape & Reel
NSVBCP69T1G	SOT−223 (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Breakdown Voltage (I_C = −100 μAdc, I_E = 0)	$V_{(BR)CES}$	−25	−	−	Vdc
Collector−Emitter Breakdown Voltage (I_C = −1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	−20	−	−	Vdc
Emitter−Base Breakdown Voltage (I_E = −10 μAdc, I_C = 0)	$V_{(BR)EBO}$	−5.0	−	−	Vdc
Collector−Base Cutoff Current (V_{CB} = −25 Vdc, I_E = 0)	I_{CBO}	−	−	−10	μAdc
Emitter−Base Cutoff Current (V_{EB} = −5.0 Vdc, I_C = 0)	I_{EBO}	−	−	−10	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = −5.0 mAdc, V_{CE} = −10 Vdc) (I_C = −500 mAdc, V_{CE} = −1.0 Vdc) (I_C = −1.0 Adc, V_{CE} = −1.0 Vdc)	h_{FE}	 50 85 60	 − − −	 − 375 −	−
Collector−Emitter Saturation Voltage (I_C = −1.0 Adc, I_B = −100 mAdc)	$V_{CE(sat)}$	−	−	−0.5	Vdc
Base−Emitter On Voltage (I_C = −1.0 Adc, V_{CE} = −1.0 Vdc)	$V_{BE(on)}$	−	−	−1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current−Gain − Bandwidth Product (I_C = −10 mAdc, V_{CE} = −5.0 Vdc)	f_T	−	60	−	MHz

TYPICAL ELECTRICAL CHARACTERISTICS

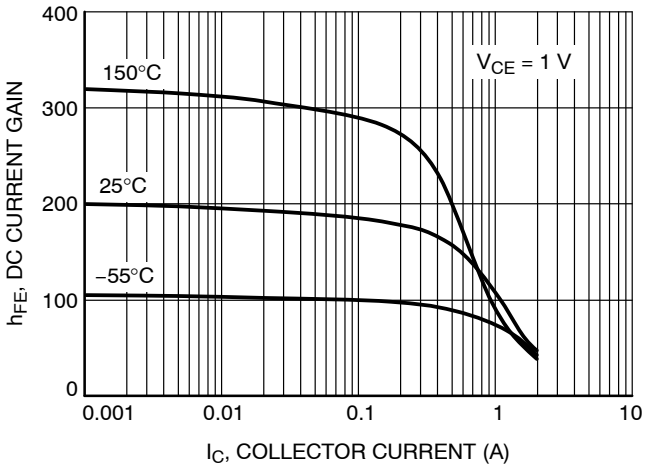


Figure 1. DC Current Gain

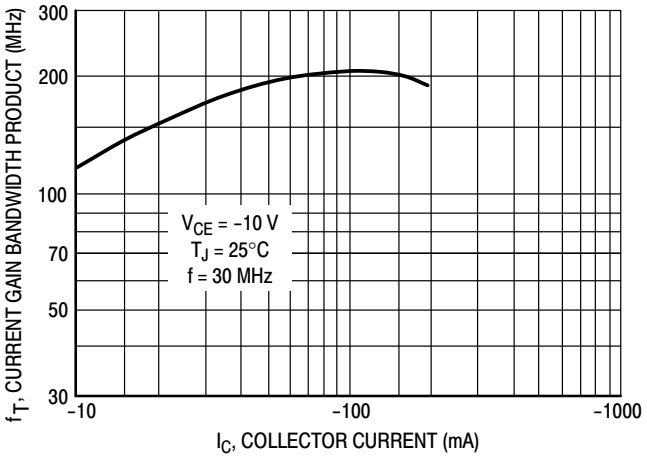


Figure 2. Current Gain Bandwidth Product

TYPICAL ELECTRICAL CHARACTERISTICS

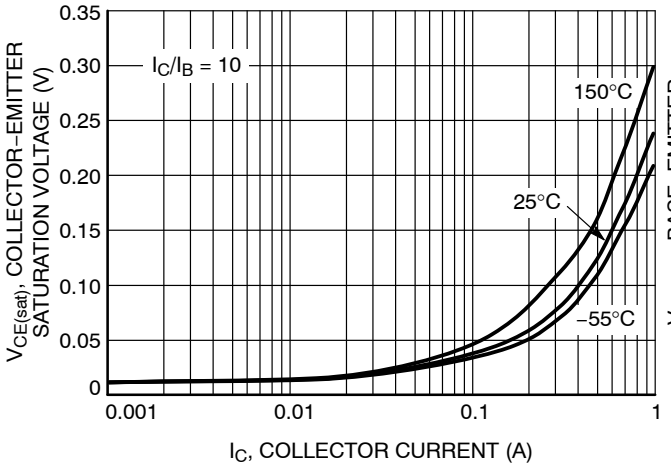


Figure 3. Collector Emitter Saturation Voltage vs. Collector Current

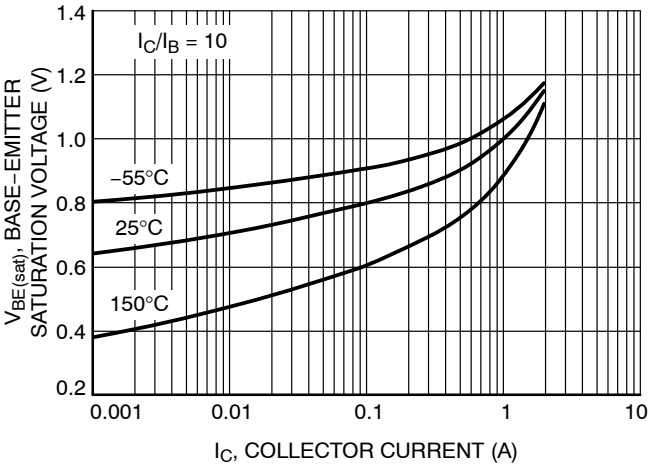


Figure 4. Base Emitter Saturation Voltage vs. Collector Current

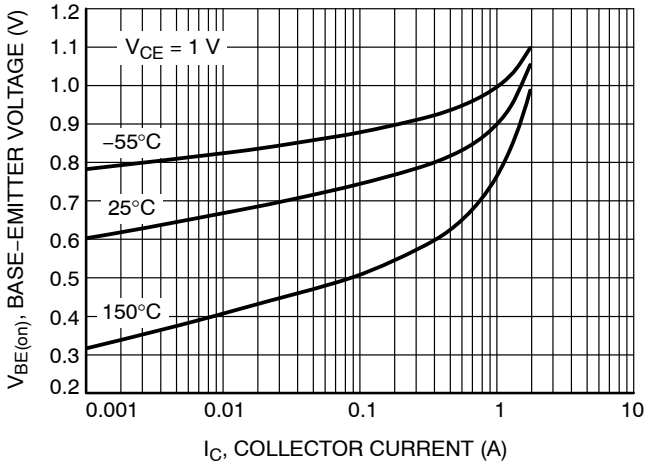


Figure 5. Base Emitter Voltage vs. Collector Current

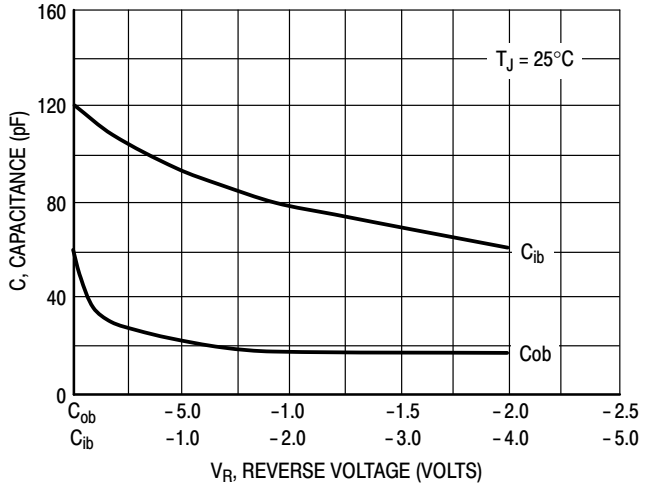


Figure 6. Capacitances

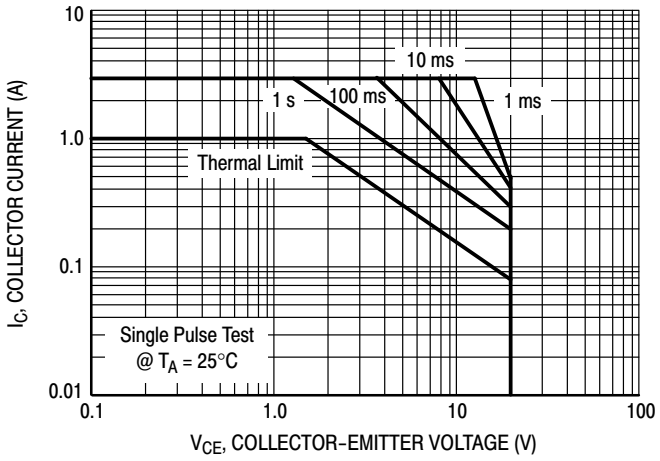
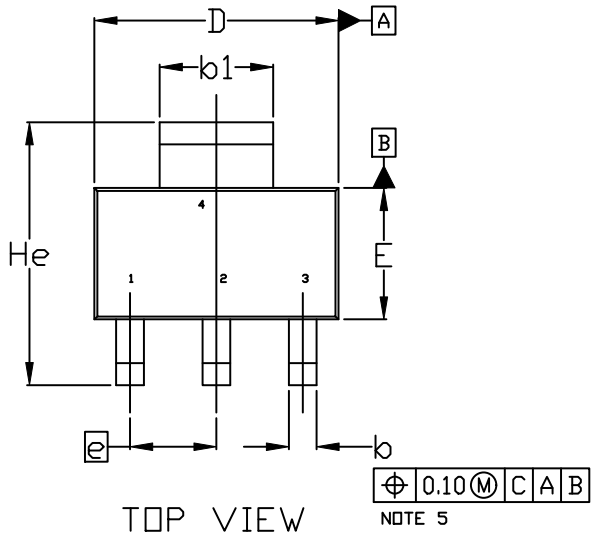


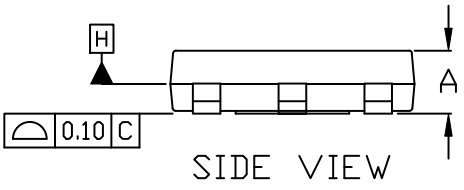
Figure 7. Safe Operating Area

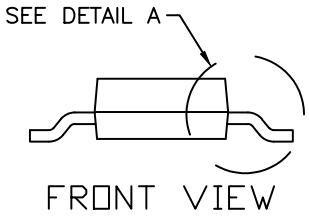
SCALE 1:1

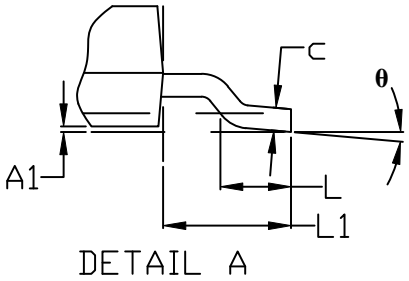
SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018



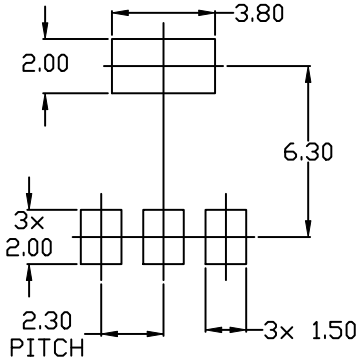






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN

STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE

STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT

STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND

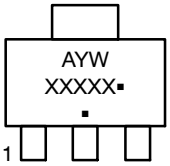
STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT

STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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