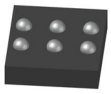
# 256 Kb I²C CMOS Serial EEPROM in WLCSP Package

# NV24C256C6PTG



**WLCSP6**
**C6PTG SUFFIX**
**CASE 567ZZ**

## Description

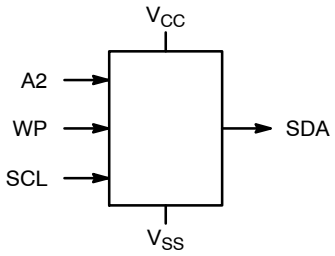
The NV24C256C6PTG is a 256 Kb Serial CMOS EEPROM, internally organized as 32768 words of 8 bits each.

They feature a 64-byte page write buffer and support both the Standard (100 kHz), Fast (400 kHz) and Fast-Plus (1 MHz) I²C protocol.

The Write Protect input allows hardware protection for the memory array. The A2 input allows two NV24C256C6PTG devices to be connected to the same bus.

## Features

- Supports Standard, Fast and Fast-Plus I²C Protocol
- Two Selectable I²C Device Addresses
- 1.7 V to 5.5 V Supply Voltage Range
- 64-byte Page Write Buffer
- Schmitt Triggers and Noise Suppression Filters on I²C Bus Inputs (SCL and SDA)
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Automotive Temperature Range: −40°C to +105°C
- Ultra-thin 6-ball WLCSP Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant*

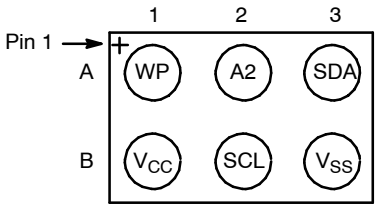



**NV24C256C6PTG**

**Figure 1. Functional Symbol**

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PIN CONFIGURATION

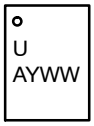



(Top View)

## PIN FUNCTION

| Pin Name | Function |
|---|---|
| SDA | Serial Data Input/Output |
| SCL | Serial Clock Input |
| $V_{CC}$ | Power Supply |
| $V_{SS}$ | Ground |
| WP | Hardware Write Protect |
| A2 | Address Pin |

## MARKING DIAGRAM




U = Specific Device Code
A = Assembly Location
Y = Production Year
WW = Production Week

## ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 8 of this data sheet.

**Table 1. ABSOLUTE MAXIMUM RATINGS**

| Parameter | Rating | Unit |
|---|---|---|
| Storage Temperature | −65 to +150 | °C |
| Voltage on Any Pin with Respect to Ground (Note 1) | −0.5 to +6.5 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The DC input voltage on any pin should not be lower than −0.5 V or higher than $V_{CC}$ + 1.0 V. During transitions, the voltage on any pin may undershoot to no less than −1.5 V or overshoot to no more than $V_{CC}$ + 1.5 V, for periods of less than 20 ns.

**Table 2. RELIABILITY CHARACTERISTICS** (Note 2)

| Symbol | Parameter | Min | Unit |
|---|---|---|---|
| $N_{END}$ (Note 3) | Endurance | 1,000,000 | Program/Erase Cycles |
| $T_{DR}$ (Note 4) | Data Retention | 100 | Years |

2. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
3. Page Mode, $V_{CC}$ = 5 V, 25°C
4. $T_A$ = 55°C

**Table 3. DC AND AC OPERATING CONDITIONS**

| Supply Voltage / Temperature Range | Operation |
|---|---|
| $V_{CC}$ = 1.7 V to 5.5 V / $T_A$ = −40°C to +105°C | READ / WRITE |
| $V_{CC}$ = 1.6 V to 5.5 V / $T_A$ = −40°C to +105°C | READ |
| $V_{CC}$ = 1.6 V to 5.5 V / $T_A$ = 0°C to +105°C | WRITE |

**Table 4. D.C. OPERATING CHARACTERISTICS**

| Symbol | Parameter | Test Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{CCR}$ | Read Current | Read, $f_{SCL}$ = 400 kHz/1 MHz | | | 1 | mA |
| $I_{CCW}$ | Write Current | | | | 2 | mA |
| $I_{SB}$ | Standby Current | All I/O Pins at GND or $V_{CC}$ | $V_{CC}$ < 2.5 V | | 1 | μA |
| | | | $V_{CC}$ > 2.5 V | | 2 | |
| $I_L$ | I/O Pin Leakage | Pin at GND or $V_{CC}$ | | | 2 | μA |
| $V_{IL1}$ | Input Low Voltage | $V_{CC} \geq$ 2.5 V | | −0.5 | 0.3 $V_{CC}$ | V |
| $V_{IL2}$ | Input Low Voltage | $V_{CC}$ < 2.5 V | | −0.5 | 0.25 $V_{CC}$ | V |
| $V_{IH1}$ | Input High Voltage | $V_{CC} \geq$ 2.5 V | | 0.7 $V_{CC}$ | $V_{CC}$ + 1 | V |
| $V_{IH2}$ | Input High Voltage | $V_{CC}$ < 2.5 V | | 0.75 $V_{CC}$ | $V_{CC}$ + 1 | V |
| $V_{OL1}$ | Output Low Voltage | $V_{CC} \geq$ 2.5 V, $I_{OL}$ = 3.0 mA | | | 0.4 | V |
| $V_{OL2}$ | Output Low Voltage | $V_{CC}$ < 2.5 V, $I_{OL}$ = 1.0 mA | | | 0.2 | V |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**Table 5. PIN IMPEDANCE CHARACTERISTICS**

| Symbol | Parameter | Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ (Note 5) | SDA I/O Pin Capacitance | $V_{IN}$ = 0 V | 8 | pF |
| $C_{IN}$ (Note 5) | Input Capacitance (other pins) | $V_{IN}$ = 0 V | 6 | pF |

5. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.

**Table 6. A.C. CHARACTERISTICS** (Note 6)

| Symbol | Parameter | Standard $V_{CC}$ = 1.7 to 5.5 $T_A$ = −40 to 105°C | | Fast $V_{CC}$ = 1.7 to 5.5 $T_A$ = −40 to 105°C | | Fast−Plus $V_{CC}$ = 1.7 to 5.5 $T_A$ = −40 to 105°C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $F_{SCL}$ | Clock Frequency | | 100 | | 400 | | 1,000 | kHz |
| $t_{HD:STA}$ | START Condition Hold Time | 4 | | 0.6 | | 0.25 | | μs |
| $t_{LOW}$ | Low Period of SCL Clock | 4.7 | | 1.3 | | 0.45 | | μs |
| $t_{HIGH}$ | High Period of SCL Clock | 4 | | 0.6 | | 0.40 | | μs |
| $t_{SU:STA}$ | START Condition Setup Time | 4.7 | | 0.6 | | 0.25 | | μs |
| $t_{HD:DAT}$ | Data In Hold Time | 0 | | 0 | | 0 | | μs |
| $t_{SU:DAT}$ | Data In Setup Time | 250 | | 100 | | 50 | | ns |
| $t_R$ (Note 7) | SDA and SCL Rise Time | | 1,000 | 20 | 300 | | 100 | ns |
| $t_F$ (Note 7) | SDA and SCL Fall Time | | 300 | 20 | 300 | | 100 | ns |
| $t_{SU:STO}$ | STOP Condition Setup Time | 4 | | 0.6 | | 0.25 | | μs |
| $t_{BUF}$ | Bus Free Time Between STOP and START | 4.7 | | 1.3 | | 0.5 | | μs |
| $t_{AA}$ | SCL Low to Data Out Valid | | 3.5 | | 0.9 | | 0.40 | μs |
| $t_{DH}$ | Data Out Hold Time | 100 | | 100 | | 50 | | ns |
| $T_i$ (Note 7) | Noise Pulse Filtered at SCL and SDA Inputs | | 100 | | 50 | | 50 | ns |
| $t_{WR}$ | Write Cycle Time | | 5 | | 5 | | 5 | ms |
| $T_{PU}$ (Notes 7, 8) | Power-up to Ready Mode | | 0.35 | | 0.35 | | 0.35 | ms |

6. Test conditions according to “A.C. Test Conditions” table.
7. Tested initially and after a design or process change that affects this parameter.
8. $t_{PU}$ is the delay between the time $V_{CC}$ is stable and the device is ready to accept commands.

**Table 7. A.C. TEST CONDITIONS**

| Parameter | Condition |
|---|---|
| Input Levels | $0.2 \times V_{CC}$ to $0.8 \times V_{CC}$ |
| Input Rise and Fall Times | ≤ 50 ns |
| Input Reference Levels | $0.3 \times V_{CC}$, $0.7 \times V_{CC}$ |
| Output Reference Levels | $0.5 \times V_{CC}$ |
| Output Load | Current Source: $I_{OL}$ = 3 mA ($V_{CC} \geq$ 2.5 V); $I_{OL}$ = 1 mA ($V_{CC}$ < 2.5 V); $C_L$ = 100 pF |

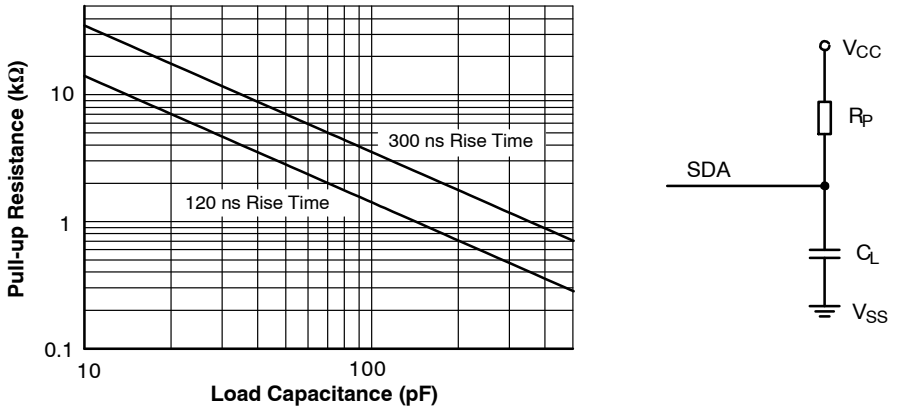



**Figure 2. Maximum Pull-up Resistance vs. Load Capacitance**

### Power-On Reset (POR)

The NV24C256C6PTG incorporates Power-On Reset (POR) circuitry which protects the device against powering up in the wrong state.

The NV24C256C6PTG will power up into Standby mode after $V_{CC}$ exceeds the POR trigger level and will power down into Reset mode when $V_{CC}$ drops below the POR trigger level. This bi-directional POR feature protects the device against 'brown-out' failure following a temporary loss of power.

### Pin Description

- SCL: The Serial Clock input pin accepts the Serial Clock generated by the Master.
- SDA: The Serial Data I/O pin receives input data and transmits data stored in EEPROM. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.
- WP: WP is the Write Protect pin. While the WP pin is connected to the power supply, the entire array becomes Write Protected (i.e. the device becomes Read only). When WP is tied to Ground or left floating, the normal write operations are allowed.
- A2: The A2 pin is a device address input. If A2 is left floating, the input defaults to zero. When A2 is set to logic−0 the device address is 0xA1/0xA0 for read/write. When A2 is set to logic−1 the device address is 0xA9/0xA8 for read/write.

### Functional Description

The NV24C256C6PTG supports the Inter-Integrated Circuit ($I^2C$) Bus data transmission protocol, which defines a device that sends data to the bus as a transmitter and a device receiving data as a receiver. Data flow is controlled by a Master device, which generates the serial clock and all START and STOP conditions. The NV24C256C6PTG acts as a Slave device. Master and Slave alternate as either transmitter or receiver.

### $I^2C$ Bus Protocol

The $I^2C$ bus consists of two 'wires', SCL and SDA. The two wires are connected to the $V_{CC}$ supply via pull-up resistors. Master and Slave devices connect to the 2-wire bus via their respective SCL and SDA pins. The transmitting device pulls down the SDA line to 'transmit' a '0' and releases it to 'transmit' a '1'.

Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics).

During data transfer, the SDA line must remain stable while the SCL line is HIGH. An SDA transition while SCL is HIGH will be interpreted as a START or STOP condition (Figure 3). The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a 'wake-up' call to all receivers. Absent a START, a Slave will not respond to commands. The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH.

#### Device Addressing

The Master initiates data transfer by creating a START condition on the bus. The Master then broadcasts an 8-bit serial Slave address. The first 4 bits of the Slave address are set to 1010. The next 3 bits must match the logic state of A2, 0 and 0. The last bit, R/W, specifies whether a Read (1) or Write (0) operation is to be performed.

#### Acknowledge

After processing the Slave address, the Slave responds with an acknowledge (ACK) by pulling down the SDA line during the $9^{th}$ clock cycle (Figure 5). The Slave will also acknowledge all address bytes and every data byte presented in Write mode if the addressed location is not write protected. In Read mode the Slave shifts out a data byte, and then releases the SDA line during the $9^{th}$ clock cycle. As long as the Master acknowledges the data, the Slave will continue transmitting. The Master terminates the session by not acknowledging the last data byte (NoACK) and by issuing a STOP condition. Bus timing is illustrated in Figure 6.

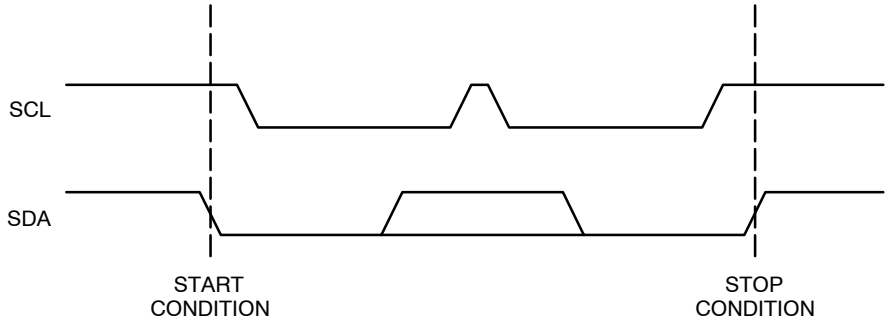



**Figure 3. START/STOP Conditions**

| Memory Array Access | 1 | 0 | 1 | 0 | A2 | 0 | 0 | R/W |
|---|---|---|---|---|---|---|---|---|

**Figure 4. Slave Address Bits**

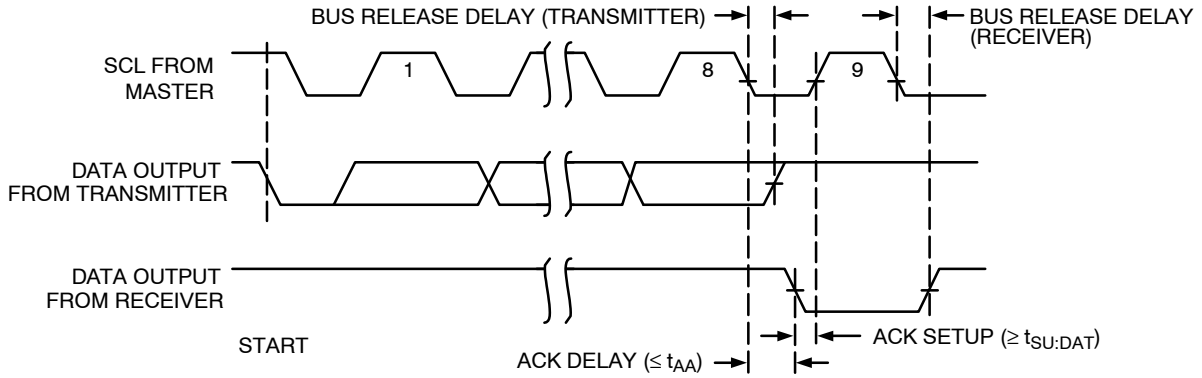



**Figure 5. Acknowledge Timing**

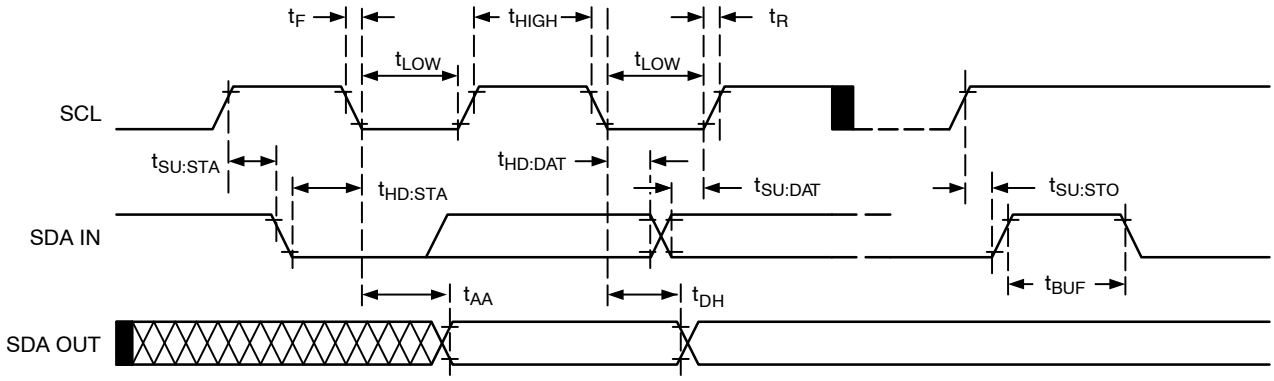



**Figure 6. Bus Timing**

## Write Operations

### Byte Write

In Byte Write mode the Master sends a START, followed by Slave address, two byte address and data to be written (Figure 7). The Slave, NV24C256C6PTG acknowledges all 4 bytes, and the Master then follows up with a STOP, which in turn starts the internal Write operation (Figure 8). During the internal Write cycle ($t_{WR}$), the NV24C256C6PTG will not acknowledge any Read or Write request from the Master.

### Page Write

The NV24C256C6PTG contains 32,768 bytes of data, arranged in 512 pages of 64 bytes each. A two byte address word, following the Slave address, points to the first byte to be written into the memory array. The most significant 9 bits from the address active bits (a14 to a6) identify the page and the last 6 bits (a5 to a0) identify the byte within the page. Up to 64 bytes can be written in one Write cycle (Figure 9). The internal byte address counter is automatically incremented after each data byte is loaded. If the Master transmits more than 64 data bytes, then earlier bytes will be overwritten by later bytes in a 'wrap-around' fashion (within the selected page). The internal Write cycle starts immediately following the STOP.

### Acknowledge Polling

The ready/busy status of the NV24C256C6PTG can be ascertained by sending Read or Write requests immediately following the STOP condition that initiated the internal Write cycle. As long as internal Write is in progress, the NV24C256C6PTG will not acknowledge the Slave address.

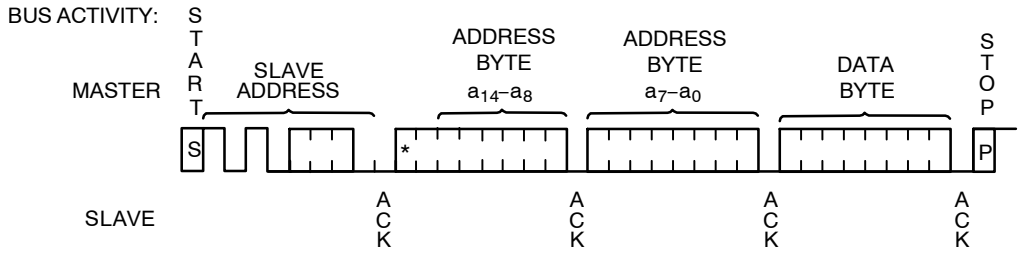



**Figure 7. Byte Write Sequence**

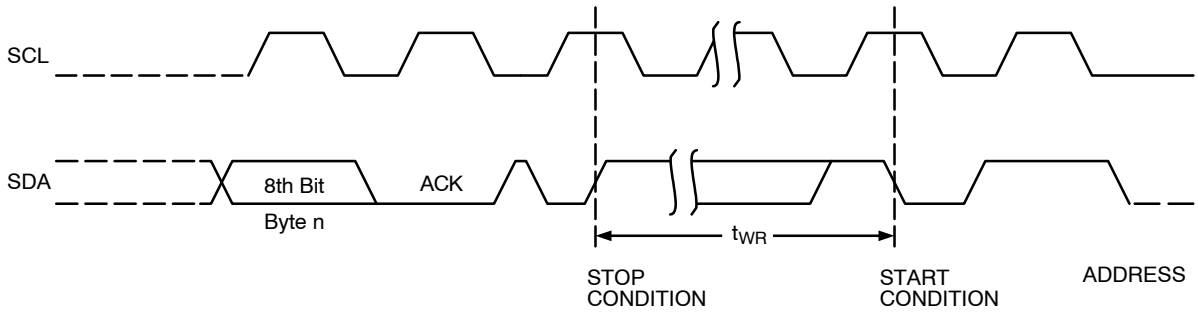



**Figure 8. Write Cycle Timing**

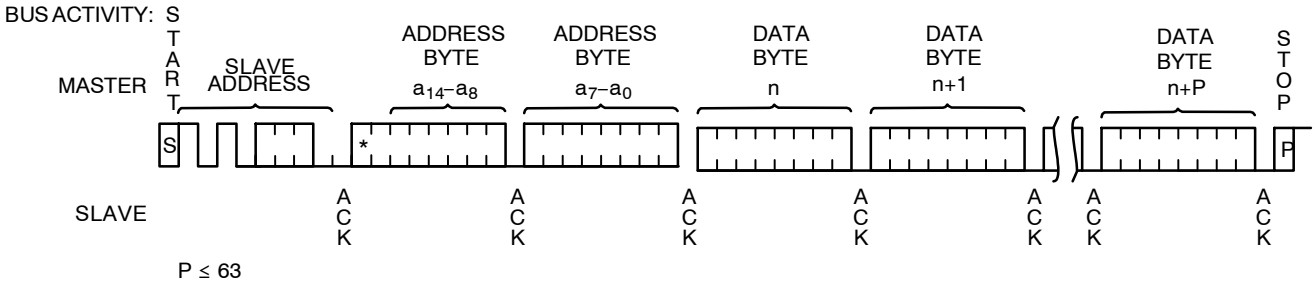



**Figure 9. Page Write Sequence**

## Read Operations

### Immediate Read

Upon receiving a Slave address with the R/$\overline{W}$ bit set to '1', the NV24C256C6PTG will interpret this as a request for data residing at the current byte address in memory. The NV24C256C6PTG will acknowledge the Slave address, will immediately shift out the data residing at the current address, and will then wait for the Master to respond. If the Master does not acknowledge the data (NoACK) and then follows up with a STOP condition (Figure 10), the NV24C256C6PTG returns to Standby mode.

### Selective Read

To read data residing at a specific location, the internal address counter must first be initialized as described under Byte Write. If rather than following up the two address bytes with data, the Master instead follows up with an Immediate Read sequence, then the NV24C256C6PTG will use the 15 active address bits to initialize the internal address counter and will shift out data residing at the corresponding location. If the Master does not acknowledge the data (NoACK) and then follows up with a STOP condition (Figure 11), the NV24C256C6PTG returns to Standby mode.

### Sequential Read

If during a Read session the Master acknowledges the 1st data byte, then the NV24C256C6PTG will continue transmitting data residing at subsequent locations until the Master responds with a NoACK, followed by a STOP (Figure 12). In contrast to Page Write, during Sequential Read the address count will automatically increment to and then wrap-around at end of memory (rather than end of page).

### Delivery State

The NV24C256C6PTG is shipped erased, i.e., all memory array bytes are FFh.

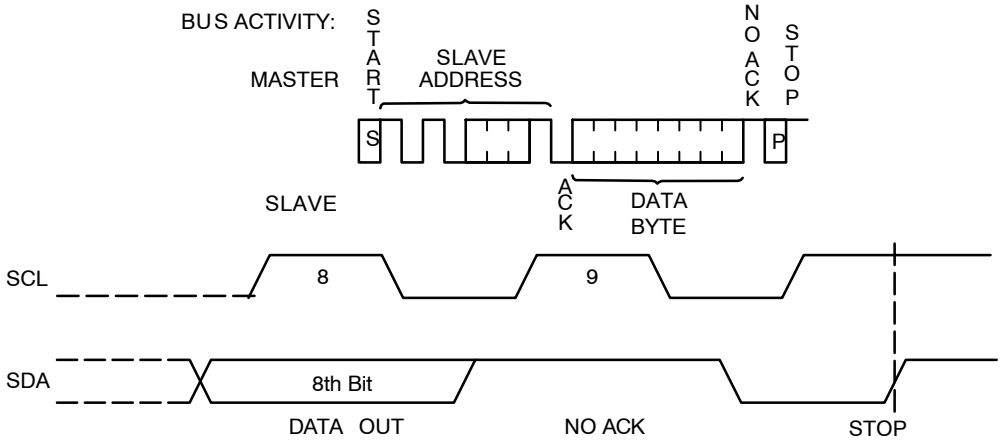



**Figure 10. Immediate Read Sequence and Timing**

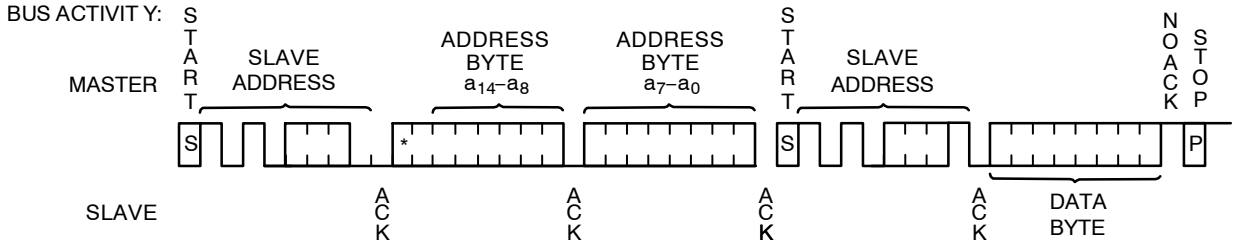



**Figure 11. Selective Read Sequence**

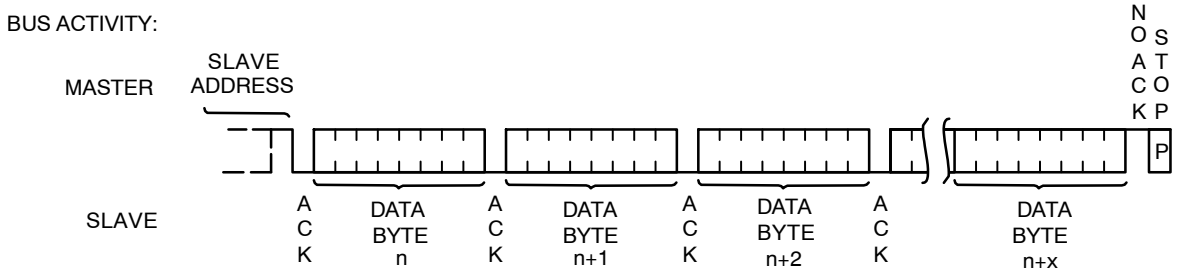



**Figure 12. Sequential Read Sequence**

**Table 8. ORDERING INFORMATION** (Notes 9 thru 11)

| Device Order Number | Specific Device Marking | Package Type | Temperature Range | Bump Composition | Shipping† |
|---|---|---|---|---|---|
| NV24C256C6PTG | U | WLCSP 6-ball | Automotive (−40°C to +105°C) | CuNiSnAg | 5,000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

9. All packages are RoHS-compliant (Lead-free, Halogen-free).
10. For detailed information and a breakdown of device nomenclature and numbering systems, please see the **onsemi** Device Nomenclature document, TND310/D, available at www.onsemi.com
11. **Caution:** The EEPROM devices delivered in WLCSP must never be exposed to ultraviolet light. When exposed to ultraviolet light the EEPROM cells lose their stored data.