# NVT2001; NVT2002

## Bidirectional voltage level translator for open-drain and push-pull applications

Rev. 4.3 — 6 October 2022 Product data sheet

## 1 General description

The NVT2001/02 are bidirectional voltage level translators operational from 1.0 V to 3.6 V ($V_{ref(A)}$) and 1.8 V to 5.5 V ($V_{ref(B)}$), which allow bidirectional voltage translations between 1.0 V and 5 V without the need for a direction pin in open-drain or push-pull applications. Bit widths ranging from 1-bit or 2-bit are offered for level translation application with transmission speeds < 33 MHz for an open-drain system with a 50 pF capacitance and a pull-up of 197 Ω.

When the An or Bn port is LOW, the clamp is in the ON-state and a low resistance connection exists between the An and Bn ports. The low ON-state resistance ($R_{on}$) of the switch allows connections to be made with minimal propagation delay. Assuming the higher voltage is on the Bn port when the Bn port is HIGH, the voltage on the An port is limited to the voltage set by VREFA. When the An port is HIGH, the Bn port is pulled to the drain pull-up supply voltage ($V_{pu(D)}$) by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user without the need for directional control.

When EN is HIGH, the translator switch is on, and the An I/O are connected to the Bn I/O, respectively, allowing bidirectional data flow between ports. When EN is LOW, the translator switch is off, and a high-impedance state exists between ports. The EN input circuit is designed to be supplied by $V_{ref(B)}$. To ensure the high-impedance state during power-up or power-down, EN must be LOW.

All channels have the same electrical characteristics and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the switch is symmetrical. The translator provides excellent ESD protection to lower voltage devices, and at the same time protects less ESD-resistant devices.

## 2 Features and benefits

- Provides bidirectional voltage translation with no direction pin
- Less than 1.5 ns maximum propagation delay
- Allows voltage level translation between:
  - 1.0 V $V_{ref(A)}$ and 1.8 V, 2.5 V, 3.3 V or 5 V $V_{ref(B)}$
  - 1.2 V $V_{ref(A)}$ and 1.8 V, 2.5 V, 3.3 V or 5 V $V_{ref(B)}$
  - 1.8 V $V_{ref(A)}$ and 3.3 V or 5 V $V_{ref(B)}$
  - 2.5 V $V_{ref(A)}$ and 5 V $V_{ref(B)}$
  - 3.3 V $V_{ref(A)}$ and 5 V $V_{ref(B)}$
- Low 3.5 Ω ON-state connection between input and output ports provides less signal distortion
- 5 V tolerant I/O ports to support mixed-mode signal operation
- High-impedance An and Bn pins for EN = LOW

- Lock-up free operation
- Flow through pinout for ease of printed-circuit board trace routing
- ESD protection exceeds 4 kV HBM per JESD22-A114 and 1000 V CDM per JESD22-C101

# 3 Ordering information

**Table 1. Ordering information**

*$T_{amb}$ = -40 °C to +105 °C.*

| Type number | Topside marking | Number of bits | Package | | |
|---|---|---|---|---|---|
| | | | Name | Description | Version |
| NVT2002DP[1] | N2002 | 2 | TSSOP8 | plastic thin shrink small outline package; 8 leads; body width 3 mm | SOT505-1 |
| NVT2002GD | N02 | 2 | XSON8U | plastic extremely thin small outline package; no leads; 8 terminals; UTLP based; body 3 × 2 × 0.5 mm | SOT996-2 |
| NVT2002TL | tT2 | 2 | XSON8 | plastic extremely thin small outline package; no leads; 8 terminals; body 3 × 2 × 0.5 mm | SOT1052-2 |
| NVT2001GM | T1 | 1 | XSON6 | plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm; requires SSB | SOT886 |

[1] GTL2002DP = NVT2002DP.

## 3.1 Ordering options

**Table 2. Ordering options**

| Type number | Orderable part number | Package | Packing method [1] | Minimum order quantity | Temperature |
|---|---|---|---|---|---|
| NVT2002DP | NVT2002DP,118 | TSSOP8 | Reel 13" Q1/T1 *Standard mark SMD | 2500 | $T_{amb}$ = -40 °C to +105 °C |
| NVT2002GD | NVT2002GD,125 [2] | XSON8U | Reel 7" Q3/T4 *Standard mark | 3000 | $T_{amb}$ = -40 °C to +105 °C |
| NVT2002TL | NVT2002TLH | XSON8 | Reel 7" Q3/T4 NDP | 4000 | $T_{amb}$ = -40 °C to +105 °C |
| NVT2001GM | NVT2001GMZ | XSON6 | Reel 7" Q1/T1 *Standard mark SMD SSB [3] | 5000 | $T_{amb}$ = -40 °C to +105 °C |

[1] Standard packing quantities and other packaging data are available at www.nxp.com/packages/.

[2] Discontinuation Notice 202111012DN; drop in replacement is NVT2002TLH.

The TL package has a center pad vs no center pad for the GD package. The TL package pad is not electrically connected to the silicon and is not required to connect to the PCB so it can drop onto the GD package PCB layout. If the existing GD package has a trace underneath the risk is low since the TL package center pad is not connected to the silicon. If there are multiple traces there could be EMI and cross talk. In both cases the customer needs to evaluate risk.

Note: The length and width are reversed between the "GD" and "TL" package drawings but the shorter edge contains the pins and is 2.0 mm in both cases.

[3] This packing method uses a Static Shielding Bag (SSB) solution. Material is to be kept in the sealed bag between uses.

# 4 Functional diagram

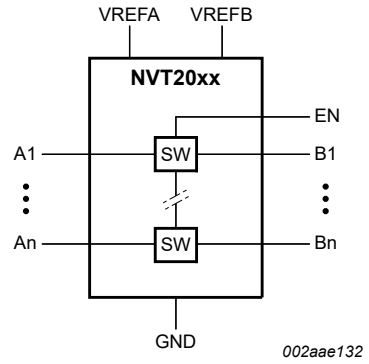
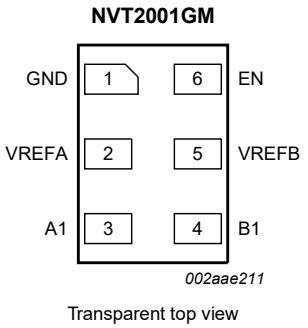



**Figure 1. Logic diagram of NVT2001; NVT2002 (positive logic)**

# 5 Pinning information

## 5.1 Pinning

### 5.1.1 1-bit in XSON6 package




Transparent top view

**Figure 2. Pin configuration for XSON6**

### 5.1.2 2-bit in TSSOP8 and XSON8U packages

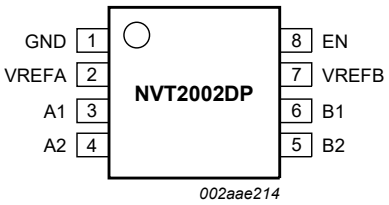
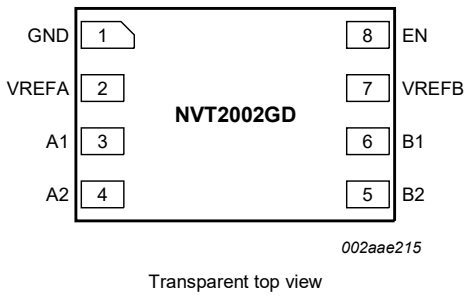



**Figure 3. Pin configuration for TSSOP8**




Transparent top view

**Figure 4. Pin configuration for XSON8U**

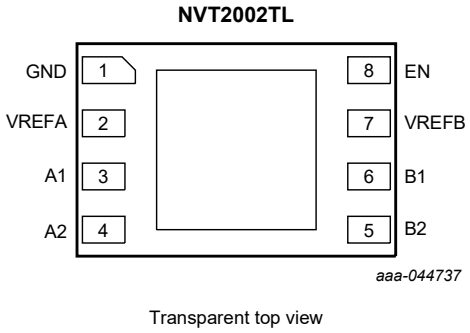



**Figure 5. Pin configuration SOT1052-2 (XSON8)**

## 5.2 Pin description

**Table 3. Pin description**

| Symbol | Pin | | Description |
|---|---|---|---|
| | NVT2001[1] | NVT2002[2] | |
| GND | 1 | 1 | ground (0 V) |
| VREFA | 2 | 2 | low-voltage side reference supply voltage for An |
| A1 | 3 | 3 | low-voltage side; connect to VREFA through a pull-up resistor |
| A2 | - | 4 | |
| B1 | 4 | 6 | high-voltage side; connect to VREFB through a pull-up resistor |
| B2 | - | 5 | |
| VREFB | 5 | 7 | high-voltage side reference supply voltage for Bn |
| EN | 6 | 8 | switch enable input; connect to VREFB and pull-up through a high resistor |

[1] 1-bit NVT2001 available in XSON6 package.
[2] 2-bit NVT2002 available in TSSOP8, XSON8 and XSON8U packages.

# 6 Functional description

Refer to Figure 1.

## 6.1 Function table

**Table 4. Function selection (example)**
*H = HIGH level; L = LOW level.*

| Input EN[1] | Function |
|---|---|
| H | An = Bn |
| L | disconnect |

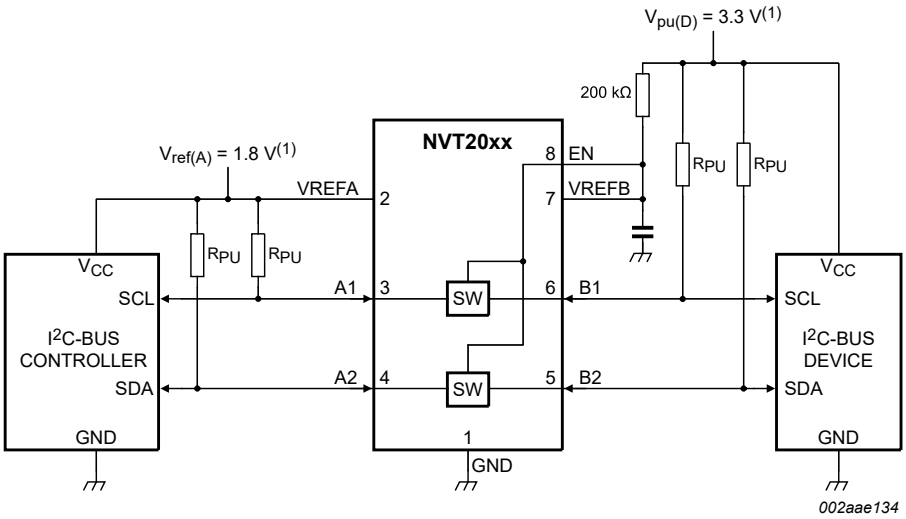
[1] EN is controlled by the $V_{ref(B)}$ logic levels and should be at least 1 V higher than $V_{ref(A)}$ for best translator operation.

# 7 Application design-in information

The NVT2001/02 can be used in level translation applications for interfacing devices or systems operating at different interface voltages with one another. The NVT2001/02 is ideal for use in applications where an open-drain driver is connected to the data I/Os. The NVT2001/02 can also be used in applications where a push-pull driver is connected to the data I/Os.

## 7.1 Enable and disable

The NVT20xx has an EN input that is used to disable the device by setting EN LOW, which places all I/Os in the high-impedance state.




1. The applied voltages at $V_{ref(A)}$ and $V_{pu(D)}$ should be such that $V_{ref(B)}$ is at least 1 V higher than $V_{ref(A)}$ for best translator operation.

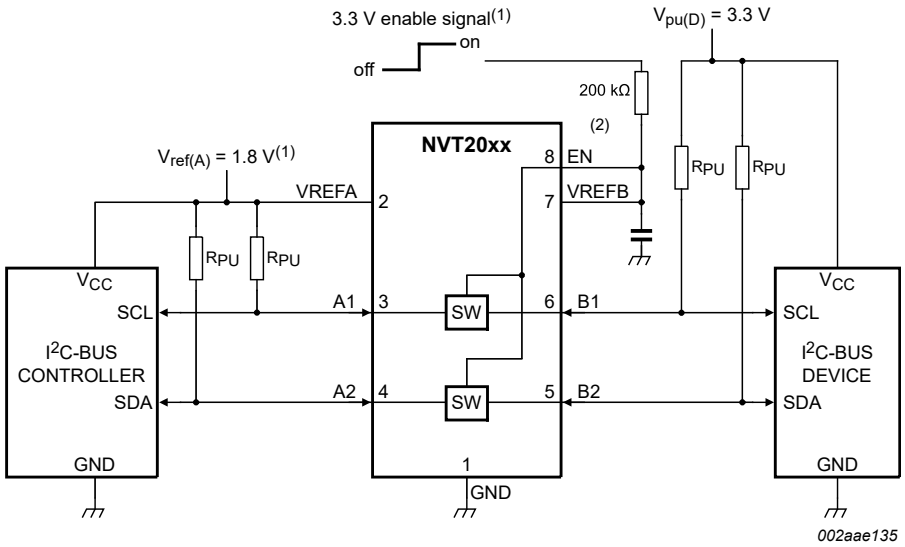
**Figure 6. Typical application circuit (switch always enabled)**

**Table 5. Application operating conditions**

*Refer to Figure 6.*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{ref(B)}$ | reference voltage (B) | | | $V_{ref(A)}$ + 0.6 | 2.1 | 5 | V |
| $V_{I(EN)}$ | input voltage on pin EN | | | $V_{ref(A)}$ + 0.6 | 2.1 | 5 | V |
| $V_{ref(A)}$ | reference voltage (A) | | | 0 | 1.5 | 4.4 | V |
| $I_{sw(pass)}$ | pass switch current | | | - | 14 | - | mA |
| $I_{ref}$ | reference current | transistor | | - | 5 | - | µA |
| $T_{amb}$ | ambient temperature | operating in free-air | | -40 | - | +105 | °C |

[1] All typical values are at $T_{amb}$ = 25 °C.




1. In the Enabled mode, the applied enable voltage $V_{I(EN)}$ and the applied voltage at $V_{ref(A)}$ should be such that $V_{ref(B)}$ is at least 1 V higher than $V_{ref(A)}$ for best translator operation.
2. Note that the enable time and the disable time are essentially controlled by the RC time constant of the capacitor and the 200 kΩ resistor on the EN pin.

**Figure 7. Typical application circuit (switch enable control)**

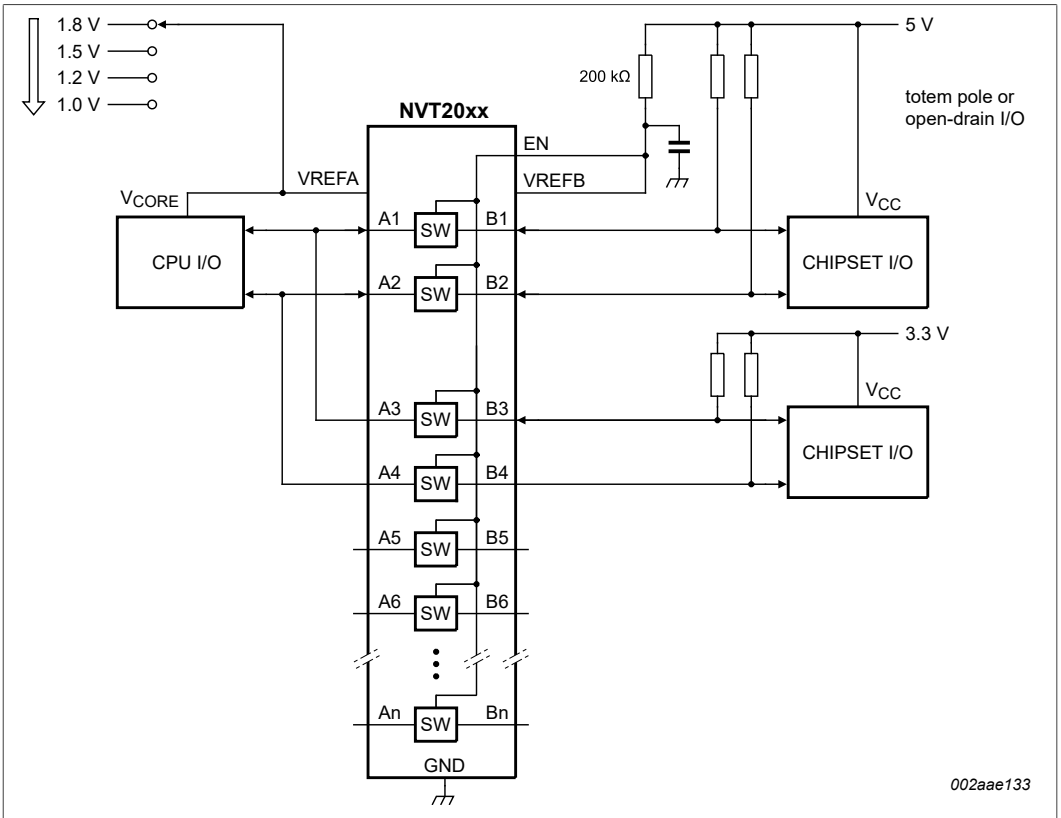



**Figure 8. Bidirectional translation to multiple higher voltage levels**

## 7.2 Bidirectional translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to VREFB and both pins pulled to HIGH side $V_{pu(D)}$ through a pull-up resistor (typically 200 kΩ). This allows VREFB to regulate the EN input. A filter capacitor on VREFB is recommended. The master output driver can be totem pole or open-drain (pull-up resistors may be required) and the slave device output can be totem pole or open-drain (pull-up resistors are required to pull the Bn outputs to $V_{pu(D)}$). However, if either output is totem-pole, data must be unidirectional or the outputs must be 3-stateable and be controlled by some direction-control mechanism to prevent HIGH-to-LOW contentions in either direction. If both outputs are open-drain, no direction control is needed.

The reference supply voltage ($V_{ref(A)}$) is connected to the processor core power supply voltage. When VREFB is connected through a 200 kΩ resistor to a 3.3 V to 5.5 V $V_{pu(D)}$ power supply, and $V_{ref(A)}$ is set between 1.0 V and ($V_{pu(D)}$ - 1 V), the output of each An has a maximum output voltage equal to VREFA, and the output of each Bn has a maximum output voltage equal to $V_{pu(D)}$.

## 7.3 How to size pull-up resistor value

Sizing the pull-up resistor on an open-drain bus is specific to the individual application and is dependent on the following driver characteristics:

- The driver sink current
- The $V_{OL}$ of driver
- The $V_{IL}$ of the driver
- Frequency of operation

The following tables can be used to estimate the pull-up resistor value in different use cases so that the minimum resistance for the pull-up resistor can be found.

Table 6, Table 7 and Table 8 contain suggested minimum values of pull-up resistors for the PCA9306 and NVT20xx devices with typical voltage translation levels and drive currents. The calculated values assume that both drive currents are the same. $V_{OL}$ = $V_{IL}$ = 0.1 × $V_{CC}$ and accounts for a ±5 % $V_{CC}$ tolerance of the supplies, ±1 % resistor values. It should be noted that the resistor chosen in the final application should be equal to or larger than the values shown in Table 6, Table 7 and Table 8 to ensure that the pass voltage is less than 10 % of the $V_{CC}$ voltage, and the external driver should be able to sink the total current from both pull-up resistors. When selecting the minimum resistor value in Table 6, Table 7 or Table 8, the drive current strength that should be chosen should be the lowest drive current seen in the application and account for any drive strength current scaling with output voltage. For the GTL devices, the resistance table should be recalculated to account for the difference in ON resistance and bias voltage limitations between $V_{CC(B)}$ and $V_{CC(A)}$.

**Table 6. Pull-up resistor minimum values, 3 mA driver sink current for PCA9306 and NVT20xx**

| A-side | B-side | | | | | |
|---|---|---|---|---|---|---|
| | 1.2 V | 1.5 V | 1.8 V | 2.5 V | 3.3 V | 5.0 V |
| **1.0 V** | $R_{pu(A)}$ = 750 Ω<br>$R_{pu(B)}$ = 750 Ω | $R_{pu(A)}$ = 845 Ω<br>$R_{pu(B)}$ = 845 Ω | $R_{pu(A)}$ = 976 Ω<br>$R_{pu(B)}$ = 976 Ω | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 887 Ω | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 1.18 kΩ | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 1.82 kΩ |
| **1.2 V** | | $R_{pu(A)}$ = 931 Ω<br>$R_{pu(B)}$ = 931 Ω | $R_{pu(A)}$ = 1.02 kΩ<br>$R_{pu(B)}$ = 1.02 kΩ | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 887 Ω | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 1.18 kΩ | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 1.82 kΩ |

**Table 6. Pull-up resistor minimum values, 3 mA driver sink current for PCA9306 and NVT20xx*...continued***

| A-side | B-side | | | | | |
|---|---|---|---|---|---|---|
| | 1.2 V | 1.5 V | 1.8 V | 2.5 V | 3.3 V | 5.0 V |
| 1.5 V | | | $R_{pu(A)}$ = 1.1 kΩ<br>$R_{pu(B)}$ = 1.1 kΩ | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 866 Ω | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 1.18 kΩ | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 1.78 kΩ |
| 1.8 V | | | | $R_{pu(A)}$ = 1.47 kΩ<br>$R_{pu(B)}$ = 1.47 kΩ | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 1.15 kΩ | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 1.78 kΩ |
| 2.5 V | | | | | $R_{pu(A)}$ = 1.96 kΩ<br>$R_{pu(B)}$ = 1.96 kΩ | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 1.78 kΩ |
| 3.3 V | | | | | | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 1.74 kΩ |

**Table 7. Pull-up resistor minimum values, 10 mA driver sink current for PCA9306 and NVT20xx**

| A-side | B-side | | | | | |
|---|---|---|---|---|---|---|
| | 1.2 V | 1.5 V | 1.8 V | 2.5 V | 3.3 V | 5.0 V |
| 1.0 V | $R_{pu(A)}$ = 221 Ω<br>$R_{pu(B)}$ = 221 Ω | $R_{pu(A)}$ = 255 Ω<br>$R_{pu(B)}$ = 255 Ω | $R_{pu(A)}$ = 287 Ω<br>$R_{pu(B)}$ = 287 Ω | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 267 Ω | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 357 Ω | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 549 Ω |
| 1.2 V | | $R_{pu(A)}$ = 274 Ω<br>$R_{pu(B)}$ = 274 Ω | $R_{pu(A)}$ = 309 Ω<br>$R_{pu(B)}$ = 309 Ω | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 267 Ω | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 357 Ω | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 549 Ω |
| 1.5 V | | | $R_{pu(A)}$ = 332 Ω<br>$R_{pu(B)}$ = 332 Ω | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 261 Ω | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 348 Ω | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 536 Ω |
| 1.8 V | | | | $R_{pu(A)}$ = 442 Ω<br>$R_{pu(B)}$ = 442 Ω | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 348 Ω | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 536 Ω |
| 2.5 V | | | | | $R_{pu(A)}$ = 590 Ω<br>$R_{pu(B)}$ = 590 Ω | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 523 Ω |
| 3.3 V | | | | | | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 523 Ω |

**Table 8. Pull-up resistor minimum values, 15 mA driver sink current for PCA9306 and NVT20xx**

| A-side | B-side | | | | | |
|---|---|---|---|---|---|---|
| | 1.2 V | 1.5 V | 1.8 V | 2.5 V | 3.3 V | 5.0 V |
| 1.0 V | $R_{pu(A)}$ = 147 Ω<br>$R_{pu(B)}$ = 147 Ω | $R_{pu(A)}$ = 169 Ω<br>$R_{pu(B)}$ = 169 Ω | $R_{pu(A)}$ = 191 Ω<br>$R_{pu(B)}$ = 191 Ω | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 178 Ω | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 237 Ω | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 365 Ω |
| 1.2 V | | $R_{pu(A)}$ = 182 Ω<br>$R_{pu(B)}$ = 182 Ω | $R_{pu(A)}$ = 205 Ω<br>$R_{pu(B)}$ = 205 Ω | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 178 Ω | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 237 Ω | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 365 Ω |
| 1.5 V | | | $R_{pu(A)}$ = 221 Ω<br>$R_{pu(B)}$ = 221 Ω | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 174 Ω | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 232 Ω | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 357 Ω |
| 1.8 V | | | | $R_{pu(A)}$ = 294 Ω<br>$R_{pu(B)}$ = 294 Ω | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 232 Ω | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 357 Ω |
| 2.5 V | | | | | $R_{pu(A)}$ = 392 Ω<br>$R_{pu(B)}$ = 392 Ω | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 357 Ω |

**Table 8. Pull-up resistor minimum values, 15 mA driver sink current for PCA9306 and NVT20xx*...continued***

| A-side | B-side | | | | | |
|---|---|---|---|---|---|---|
| | 1.2 V | 1.5 V | 1.8 V | 2.5 V | 3.3 V | 5.0 V |
| **3.3 V** | | | | | | $R_{pu(A)}$ = none<br>$R_{pu(B)}$ = 348 Ω |

## 7.4 How to design for maximum frequency operation

The maximum frequency is limited by the minimum pulse width LOW and HIGH as well as rise time and fall time. See Equation 1 as an example of the maximum frequency. The rise and fall times are shown in Figure 9.

$$f_{max} = \frac{1}{t_{LOW(min)} + t_{HIGH(min)} + t_{r(actual)} + t_{f(actual)}} \quad (1)$$

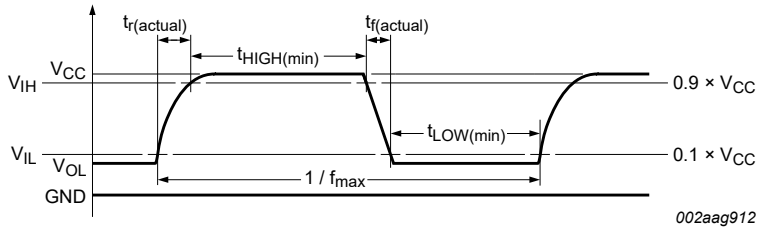



**Figure 9. An example waveform for maximum frequency**

The rise and fall times are dependent upon translation voltages, the drive strength, the total node capacitance ($C_{L(tot)}$) and the pull-up resistors ($R_{PU}$) that are present on the bus. The node capacitance is the addition of the PCB trace capacitance and the device capacitance that exists on the bus. Because of the dependency of the external components, PCB layout and the different device operating states the calculation of rise and fall times is complex and has several inflection points along the curve.

The main component of the rise and fall times is the RC time constant of the bus line when the device is in its two primary operating states: when device is in the ON state and it is low-impedance, the other is when the device is OFF isolating the A-side from the B-side.

A description of the fall time applied to either An or Bn output going from HIGH to LOW is as follows. Whichever side is asserted first, the B-side down must discharge to the $V_{CC(A)}$ voltage. The time is determined by the pull-up resistor, pull-down driver strength and the capacitance. As the level moves below the $V_{CC(A)}$ voltage, the channel resistance drops so that both A and B sides equal. The capacitance on both sides is connected to form the total capacitance and the pull-up resistors on both sides combine to the parallel equivalent resistance. The $R_{on}$ of the device is small compared to the pull-up resistor values, so its effect on the pull-up resistance can be neglected and the fall is determined by the driver pulling the combined capacitance and pull-up resistor currents. An estimation of the actual fall time seen by the device is equal to the time it takes for the B-side to fall to the $V_{CC(A)}$ voltage and the time it takes for both sides to fall from the $V_{CC(A)}$ voltage to the $V_{IL}$ level.

A description of the rise time applied to either An or Bn output going from LOW to HIGH is as follows. When the signal level is LOW, the $R_{on}$ is at its minimum, so the A and B sides are essentially one node. They will rise together with an RC time constant that is the sum of all the capacitance from both sides and the parallel of the resistance from both sides. As the signal approaches the $V_{CC(A)}$ voltage, the channel resistance goes up

and the waveforms separate, with the B side finishing its rise with the RC time constant of the B side. The rise to $V_{CC(A)}$ is essentially the same for both sides.

There are some basic guidelines to follow that will help maximize the performance of the device:

- Keep trace length to a minimum by placing the NVT device close to the processor.
- The signal round trip time on trace should be shorter than the rise or fall time of signal to reduce reflections.
- The faster the edge of the signal, the higher the chance for ringing.
- The higher drive strength controlled by the pull-up resistor (up to 15 mA), the higher the frequency the device can use.

The system designer must design the pull-up resistor value based on external current drive strength and limit the node capacitance (minimize the wire, stub, connector and trace length) to get the desired operation frequency result.

### 7.5 GD package vs TL package

Due to differences in package construction the TL package has a center pad vs no center pad for the GD package. The following section provides guidance in replacement vs new applications.

- **No trace under GD package**
  1. Replacement of GD package: The pad is not electrically connected to the silicon (no wire bond and epoxy is not conductive) and can be left floating. It is not required to be connected to the PCB. Simply place the TL package on the same PCB traces as the existing GD package.
  2. New use of the TL package: Place PCB trace for soldering of the center pad based on PCB layout recommendations for better mechanical connection and thermal conductivity. The PCB center pad can be connect to GND or left floating.
- **Trace under the GD package**
  1. Replacement of GD package: It is not best practice to have center pad over the trace but since the TL package center pad is not connected to the silicon the risk is low. If there are multiple traces there could be EMI and cross talk. In both cases the customer needs to evaluate risk.
  2. New use of the TL package: Do not route traces under the package

## 8 Limiting values

**Table 9. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*
*Over operating free-air temperature range.*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{ref(A)}$ | reference voltage (A) | | | -0.5 | +6 | V |
| $V_{ref(B)}$ | reference voltage (B) | | | -0.5 | +6 | V |
| $V_I$ | input voltage | | | -0.5[1] | +6 | V |
| $V_{I/O}$ | voltage on an input/output pin | | | -0.5[1] | +6 | V |
| $I_{ch}$ | channel current (DC) | | | - | 128 | mA |
| $I_{IK}$ | input clamping current | $V_I$ < 0 V | | -50 | - | mA |

**Table 9. Limiting values**...*continued*

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

*Over operating free-air temperature range.*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{OK}$ | output clamping current | | [2] | -50 | +50 | mA |
| $T_{stg}$ | storage temperature | | | -65 | +150 | °C |

[1] The input and input/output negative voltage ratings may be exceeded if the input and input/output clamp current ratings are observed.
[2] Low duty cycle pulses, not DC because of heating.

# 9 Recommended operating conditions

**Table 10. Operating conditions**

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{I/O}$ | voltage on an input/output pin | An, Bn | | 0 | 5.5 | V |
| $V_{ref(A)}$ | reference voltage (A) | VREFA | [1] | 0 | 5.4 | V |
| $V_{ref(B)}$ | reference voltage (B) | VREFB | [1] | 0 | 5.5 | V |
| $V_{I(EN)}$ | input voltage on pin EN | | | 0 | 5.5 | V |
| $I_{sw(pass)}$ | pass switch current | | | - | 64 | mA |
| $T_{amb}$ | ambient temperature | operating in free-air | | -40 | +105 | °C |

[1] $V_{ref(A)} \leq V_{ref(B)}$ - 1 V for best results in level shifting applications.

# 10 Static characteristics

**Table 11. Static characteristics**

*$T_{amb}$ = -40 °C to +105 °C, unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | input clamping voltage | $I_I$ = -18 mA; $V_{I(EN)}$ = 0 V | | - | - | -1.2 | V |
| $I_{IH}$ | HIGH-level input current | $V_I$ = 5 V; $V_{I(EN)}$ = 0 V | | - | - | 5 | µA |
| $C_{i(EN)}$ | input capacitance on pin EN | $V_I$ = 3 V or 0 V | | - | 7.1 | - | pF |
| $C_{io(off)}$ | off-state input/output capacitance | An, Bn; $V_O$ = 3 V or 0 V; $V_{I(EN)}$ = 0 V | | - | 4 | 6 | pF |
| $C_{io(on)}$ | on-state input/output capacitance | An, Bn; $V_O$ = 3 V or 0 V; $V_{I(EN)}$ = 3 V | | - | 9.3 | 12.5[2] | pF |
| $R_{on}$ | ON-state resistance | An, Bn; $V_I$ = 0 V; $I_O$ = 64 mA; $V_{I(EN)}$ = 4.5 V | [3][4][5] | 1 | 2.4 | 5.0 | Ω |
| | | $V_I$ = 2.4 V; $I_O$ = 15 mA; $V_{I(EN)}$ = 4.5 V | [3][4] | - | 4.8 | 7.5 | Ω |

[1] All typical values are at $T_{amb}$ = 25 °C.
[2] Not production tested, maximum value based on characterization data of typical parts.
[3] Measured by the voltage drop between the An and Bn terminals at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two terminals.
[4] See curves in Figure 10 for typical temperature and $V_{I(EN)}$ behavior.
[5] Guaranteed by design.

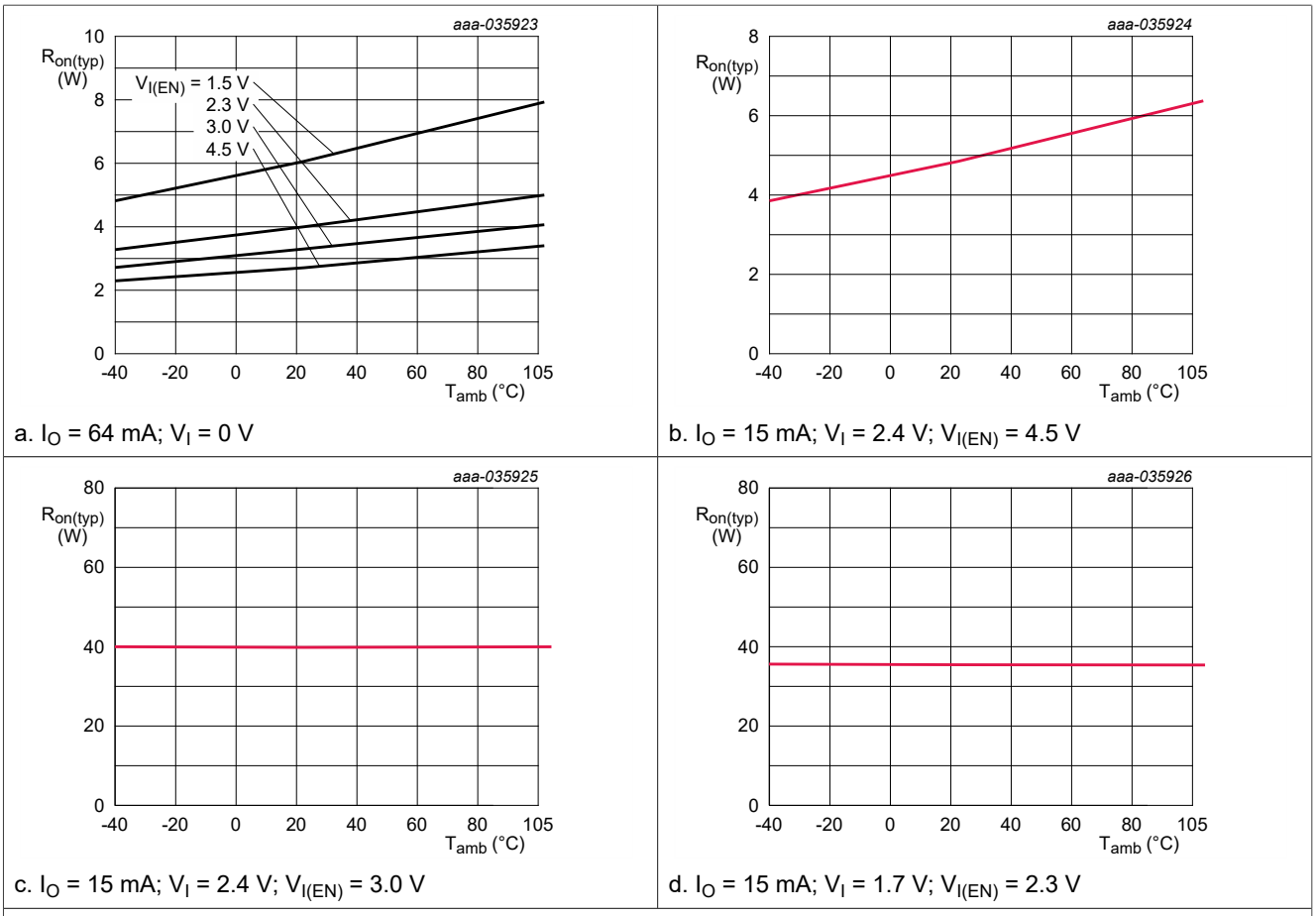



**Figure 10. Typical ON-state resistance versus ambient temperature**

# 11 Dynamic characteristics

## 11.1 Open-drain drivers

**Table 12. Dynamic characteristics for open-drain drivers**

*$T_{amb}$ = -40 °C to +105 °C; $V_{I(EN)}$ = $V_{ref(B)}$; $R_{bias(ext)}$ = 200 kΩ; $C_{VREFB}$ = 0.1 µF; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Refer to Figure 13** | | | | | | | |
| $t_{PLH}$ | LOW to HIGH propagation delay | from (input) Bn to (output) An | [1] | | $R_{on} \times (C_L + C_{io(on)})$ | | ns |
| $t_{PHL}$ | HIGH to LOW propagation delay | from (input) Bn to (output) An | | | $R_{on} \times (C_L + C_{io(on)})$ | | ns |

[1] See graphs based on $R_{on}$ typical and $C_{io(on)} + C_L$ = 50 pF.

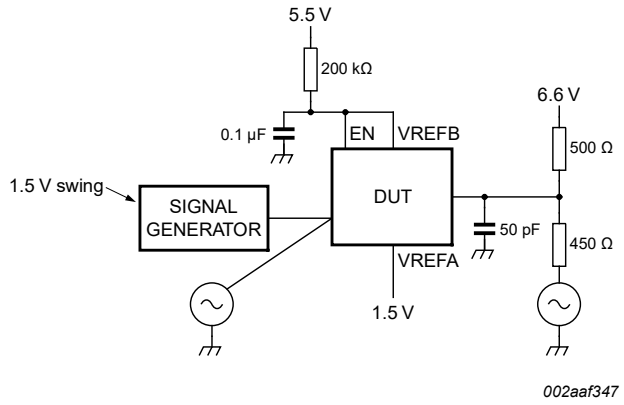



**Figure 11. AC test setup**

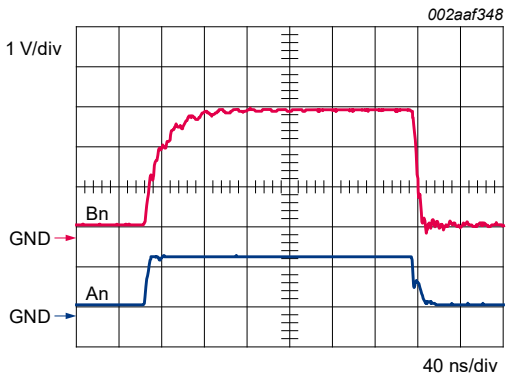
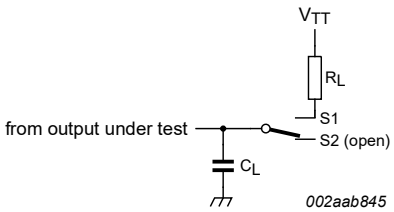
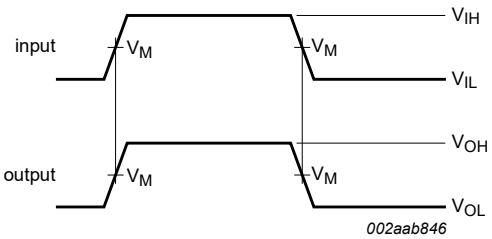



**Figure 12. Example of typical AC waveform**




a. Load circuit




b. Timing diagram; high-impedance scope probe used

S2 = translating down, and same voltage.

$C_L$ includes probe and jig capacitance.

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; $Z_o$ = 50 Ω; $t_r$ ≤ 2 ns; $t_f$ ≤ 2 ns.

The outputs are measured one at a time, with one transition per measurement.

**Figure 13. Load circuit for outputs**

## 12 Performance curves

$t_{PLH}$ up-translation is typically dominated by the RC time constant, i.e., $C_{L(tot)} \times R_{PU}$ = 50 pF × 197 Ω = 9.85 ns, but the $R_{on} \times C_{L(tot)}$ = 50 pF × 5 Ω = 0.250 ns.

$t_{PHL}$ is typically dominated by the external pull-down driver + $R_{on}$, which is typically small compared to the $t_{PLH}$ in an up-translation case.

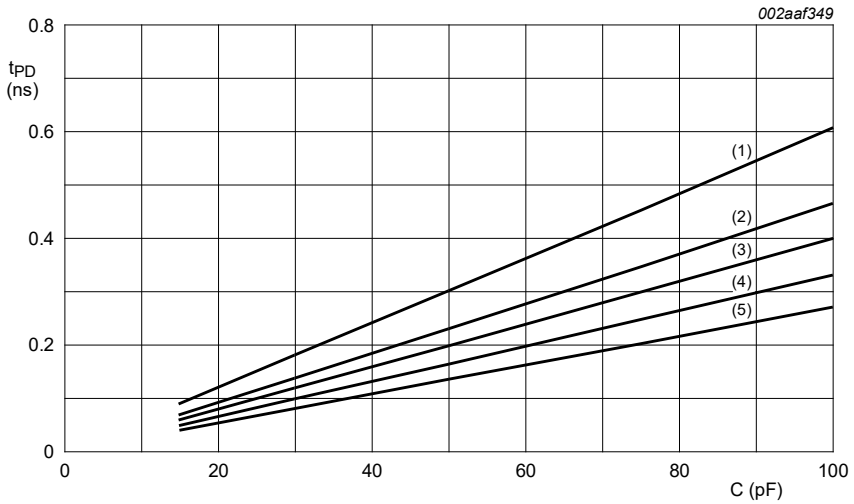
Enable/disable times are dominated by the RC time constant on the EN pin since the transistor turn off is on the order of ns, but the enable RC is on the order of ms.

Fall time is dominated by the external pull-down driver with only a slight $R_{on}$ addition.

Rise time is dominated by the $R_{PU} \times C_L$.

Skew time within the part is virtually non-existent, dominated by the difference in bond wire lengths, which is typically small compared to the board-level routing differences.

Maximum data rate is dominated by the system capacitance and pull-up resistors.

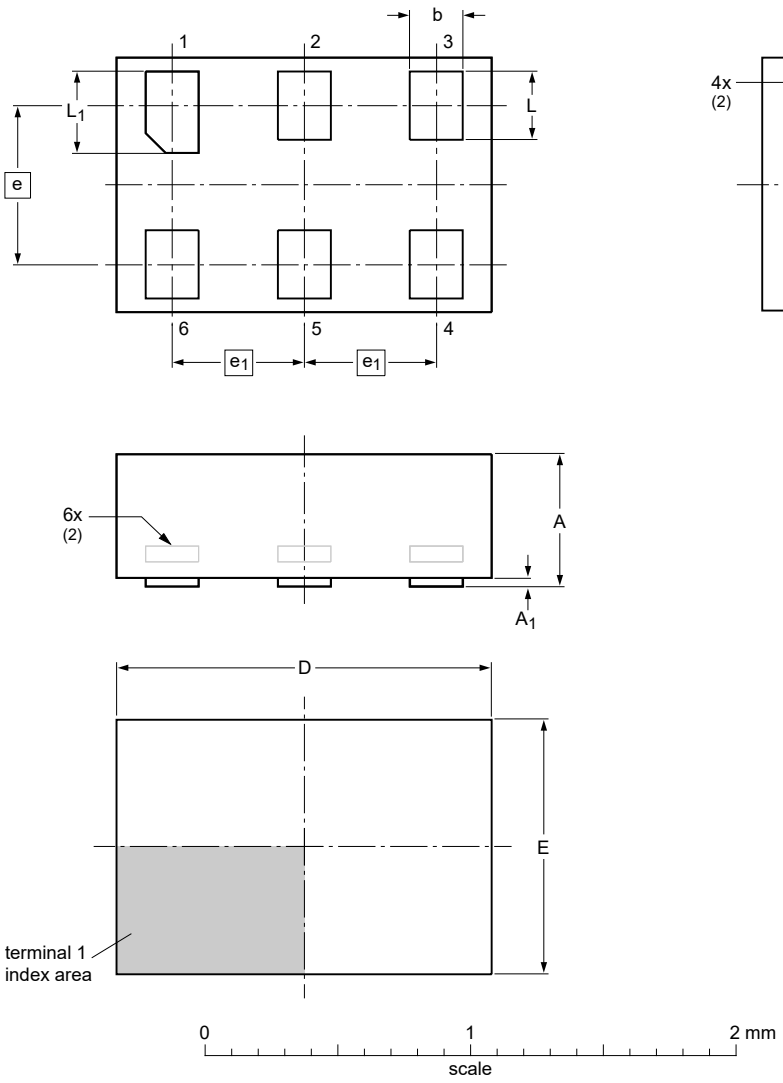



1. $V_{I(EN)}$ = 1.5 V; $I_O$ = 64 mA; $V_I$ = 0 V.
2. $V_{I(EN)}$ = 4.5 V; $I_O$ = 15 mA; $V_I$ = 2.4 V.
3. $V_{I(EN)}$ = 2.3 V; $I_O$ = 64 mA; $V_I$ = 0 V.
4. $V_{I(EN)}$ = 3.0 V; $I_O$ = 64 mA; $V_I$ = 0 V.
5. $V_{I(EN)}$ = 4.5 V; $I_O$ = 64 mA; $V_I$ = 0 V.

**Figure 14. Typical capacitance versus propagation delay**

## 13 Package outline

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm — SOT886




Dimensions (mm are the original dimensions)

| Unit | | $A^{(1)}$ | $A_1$ | b | D | E | e | $e_1$ | L | $L_1$ |
|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 0.5 | 0.04 | 0.25 | 1.50 | 1.05 | | | 0.35 | 0.40 |
| | nom | | | 0.20 | 1.45 | 1.00 | 0.6 | 0.5 | 0.30 | 0.35 |
| | min | | | 0.17 | 1.40 | 0.95 | | | 0.27 | 0.32 |

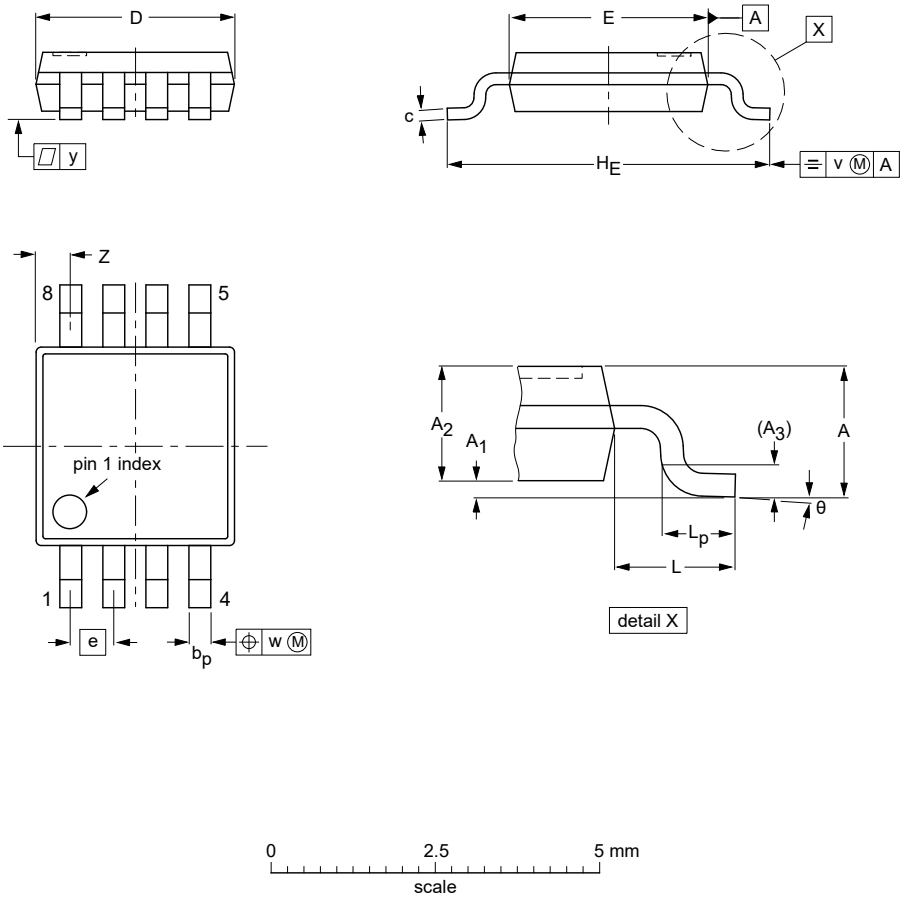
Notes
1. Including plating thickness.
2. Can be visible in some manufacturing processes.

*sot886_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT886 | | MO-252 | | | | ~~04-07-22~~ 12-01-05 |

**Figure 15. Package outline SOT886 (XSON6)**

**TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm** **SOT505-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.45<br>0.25 | 0.28<br>0.15 | 3.1<br>2.9 | 3.1<br>2.9 | 0.65 | 5.1<br>4.7 | 0.94 | 0.7<br>0.4 | 0.1 | 0.1 | 0.1 | 0.70<br>0.35 | 6°<br>0° |

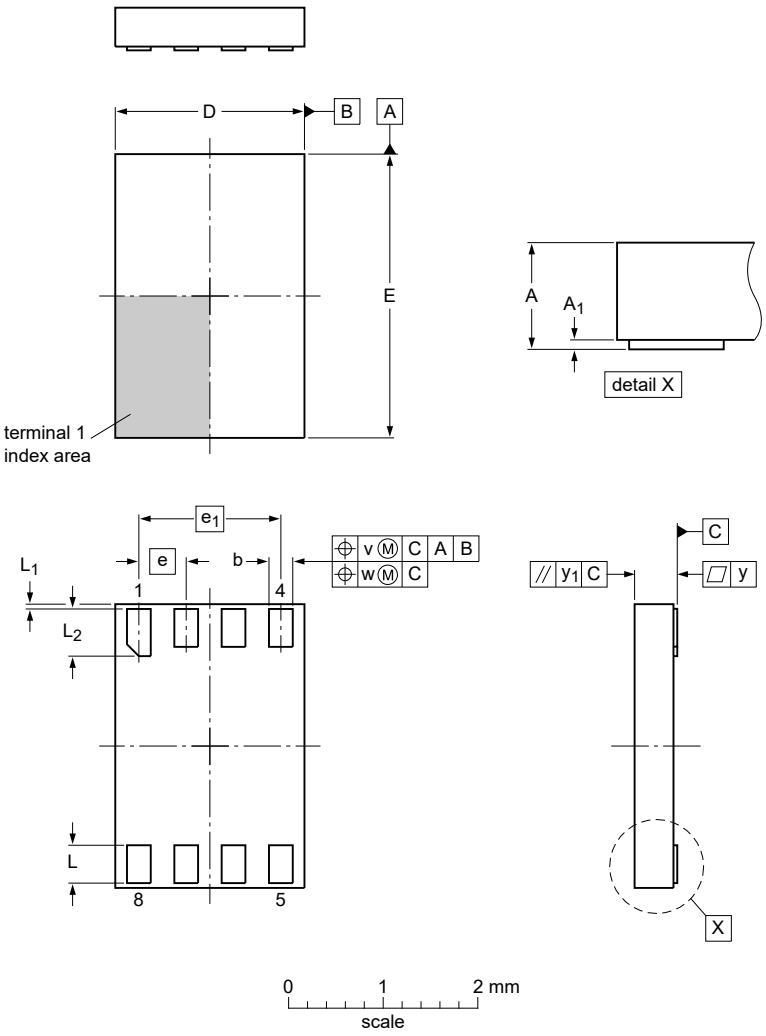
**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT505-1 | | | | | | ~~99-04-09~~<br>03-02-18 |

**Figure 16. Package outline SOT505-1 (TSSOP8)**

**XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 3 x 2 x 0.5 mm** **SOT996-2**




Dimensions (mm are the original dimensions)

| Unit(1) | | A | $A_1$ | b | D | E | e | $e_1$ | L | $L_1$ | $L_2$ | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 0.5 | 0.05 | 0.35 | 2.1 | 3.1 | 0.5 | 1.5 | 0.5 | 0.15 | 0.6 | 0.1 | 0.05 | 0.05 | 0.1 |
| | nom | | | | | | | | | | | | | | |
| | min | | 0.00 | 0.15 | 1.9 | 2.9 | | | 0.3 | 0.05 | 0.4 | | | | |

*sot996-2_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT996-2 | | | | | | ~~07-12-21~~ 12-11-20 |

**Figure 17. Package outline SOT996-2 (XSON8U)**

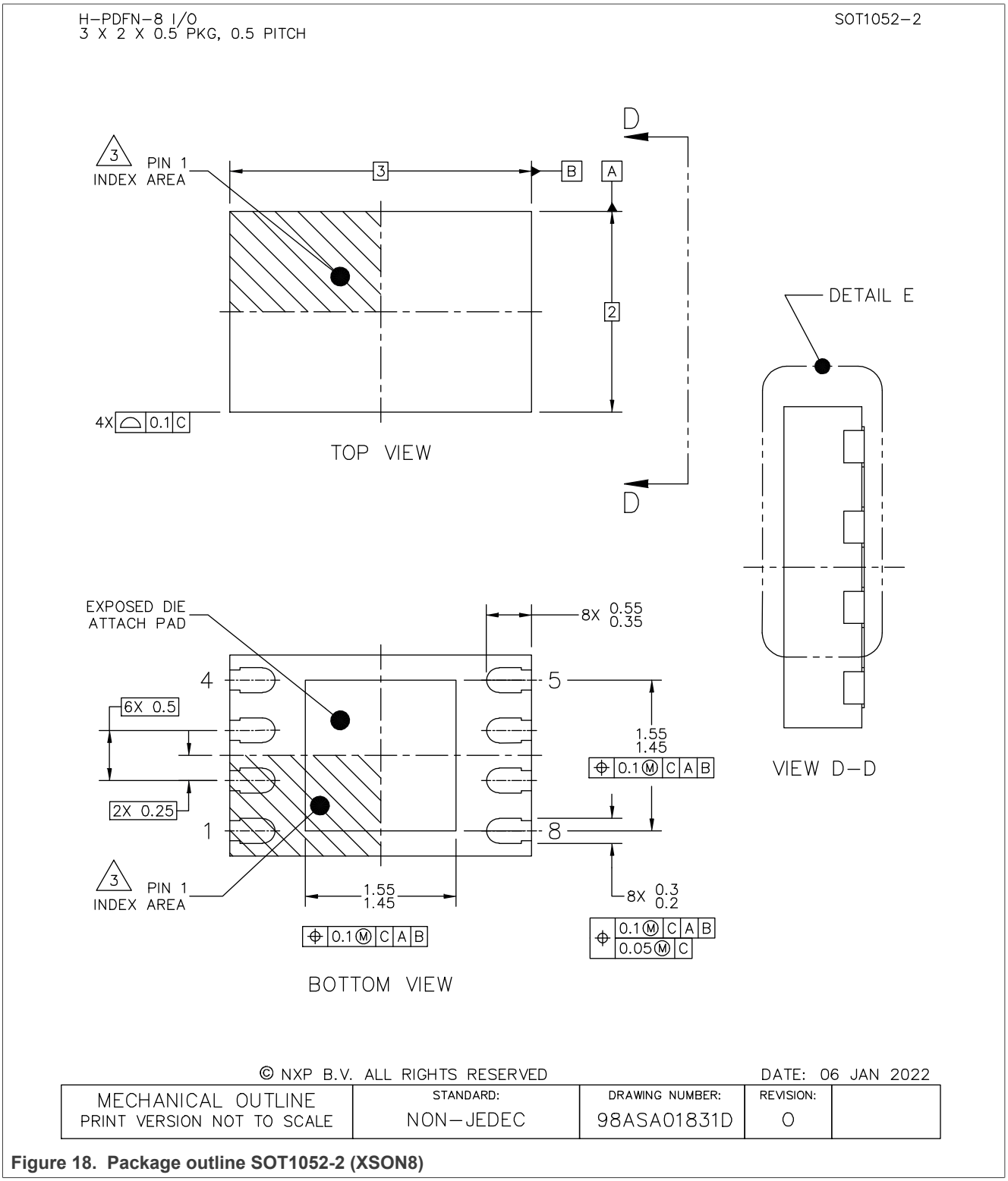



**Figure 18. Package outline SOT1052-2 (XSON8)**

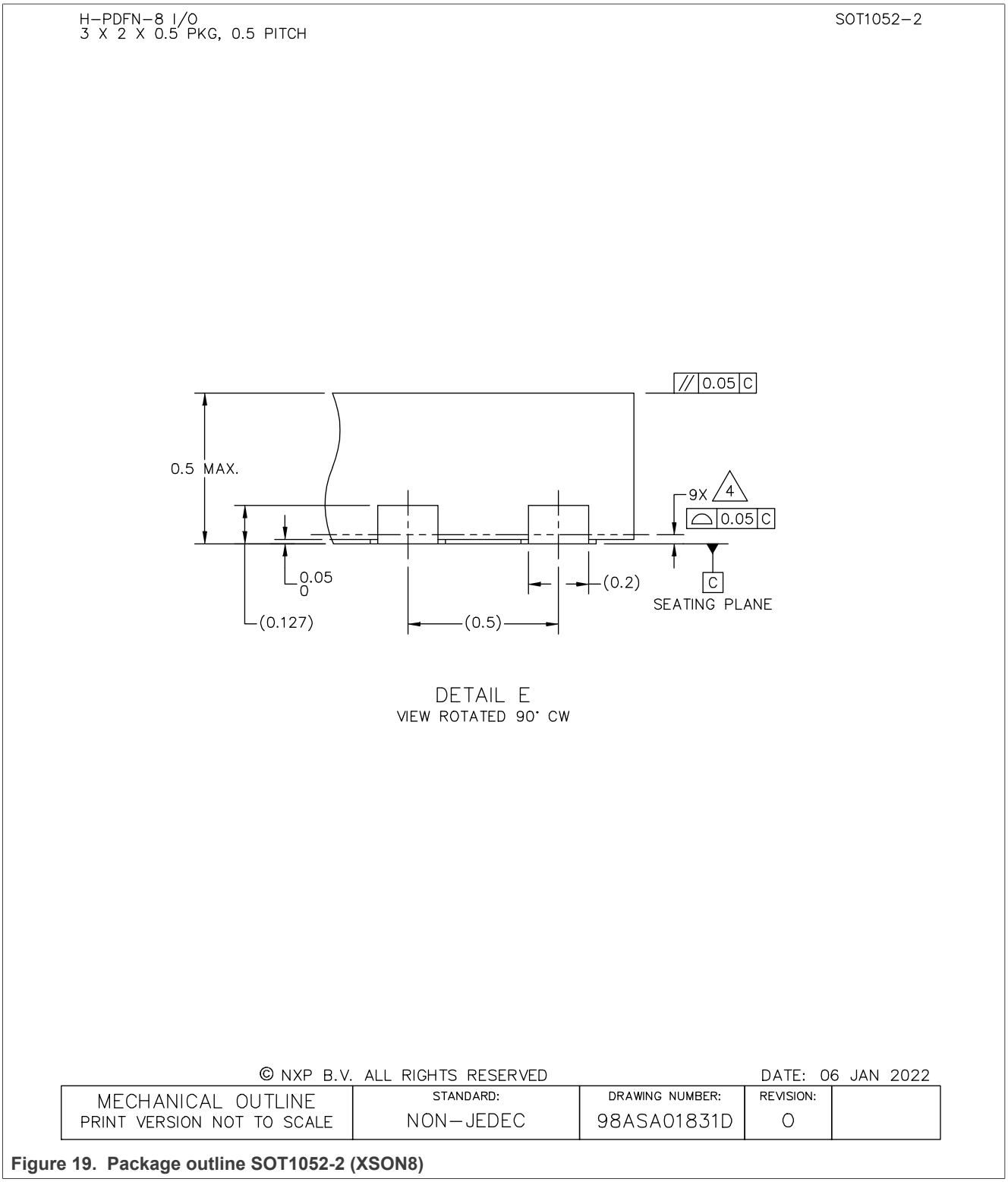



**Figure 19. Package outline SOT1052-2 (XSON8)**

# 14 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

## 14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

## 14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

## 14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 20) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 13 and Table 14

**Table 13. SnPb eutectic process (from J-STD-020D)**

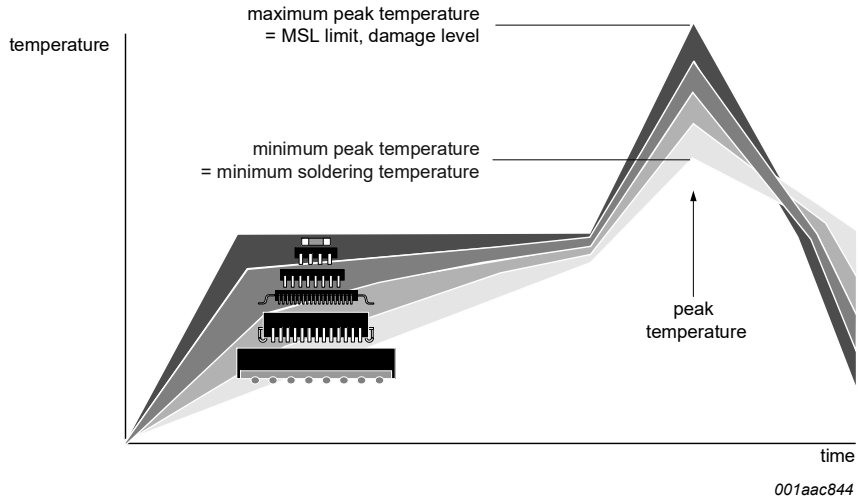
| Package thickness (mm) | Package reflow temperature (°C) | |
|---|---|---|
| | Volume (mm³) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

**Table 14. Lead-free process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) | | |
|---|---|---|---|
| | Volume (mm³) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 20.




MSL: Moisture Sensitivity Level

**Figure 20. Temperature profiles for large and small components**

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

## 15 Soldering: PCB footprints

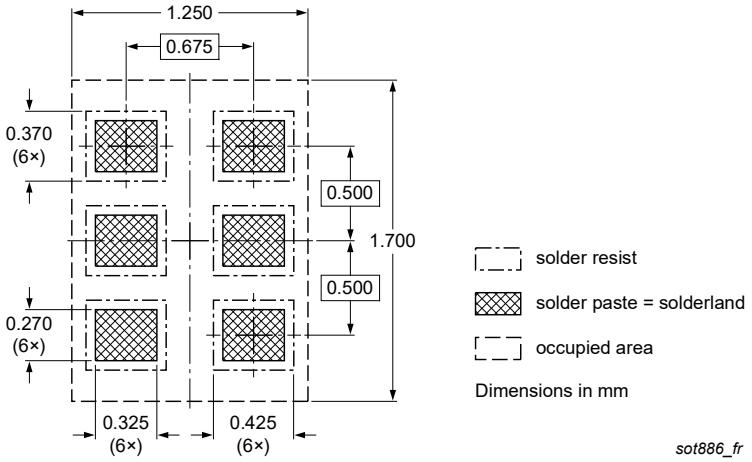



**Figure 21. PCB footprint for SOT886 (XSON6); reflow soldering**

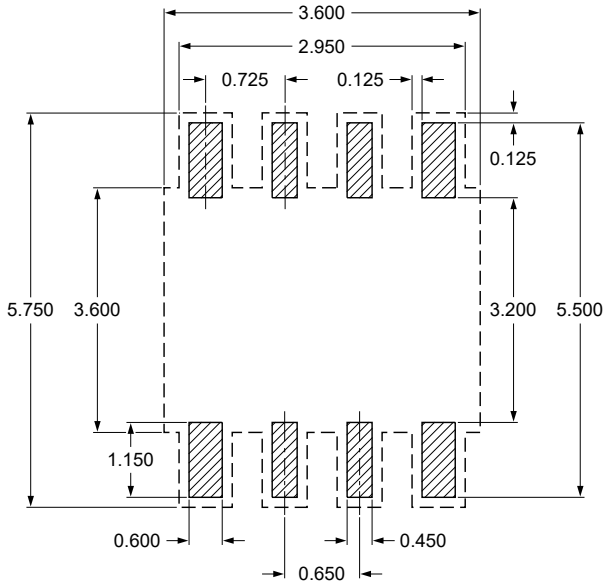



**Figure 22. PCB footprint for SOT505-1 (TSSOP8); reflow soldering**

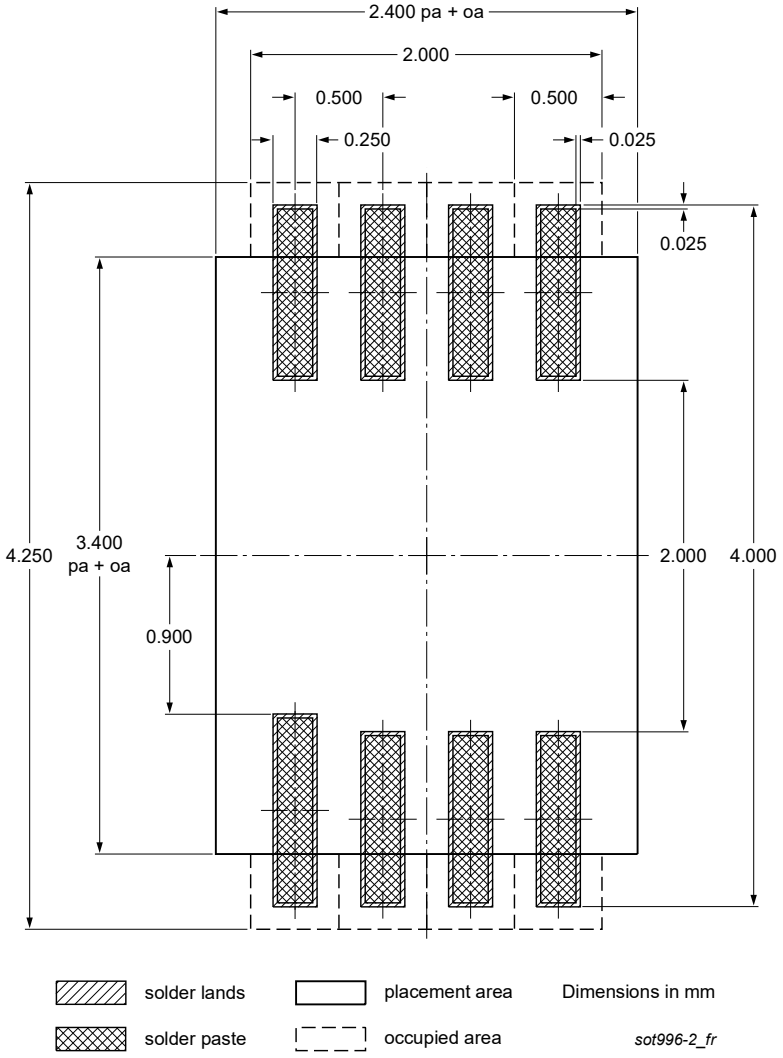
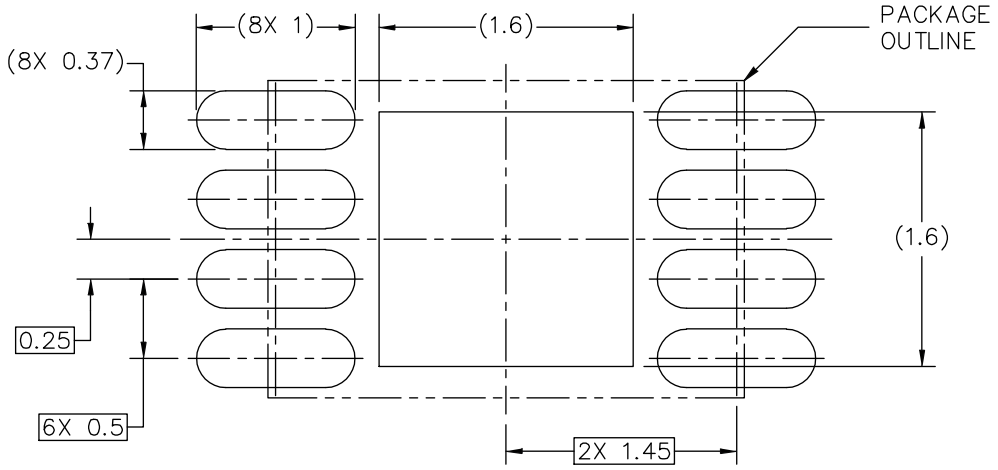



**Figure 23. PCB footprint for SOT996-2 (XSON8U); reflow soldering**

H–PDFN–8 I/O
3 X 2 X 0.5 PKG, 0.5 PITCH

SOT1052–2




PCB DESIGN GUIDELINES
RECOMMENDED SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.



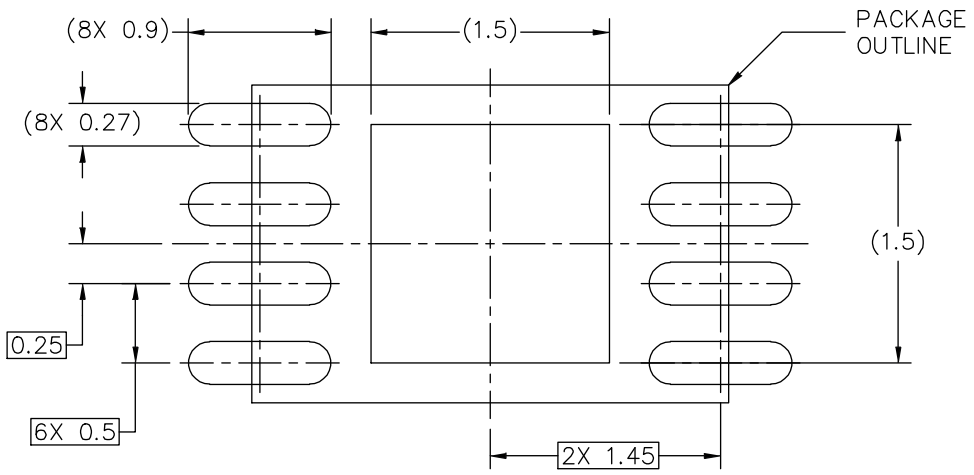
DATE: 06 JAN 2022

| MECHANICAL OUTLINE<br>PRINT VERSION NOT TO SCALE | STANDARD:<br>NON–JEDEC | DRAWING NUMBER:<br>98ASA01831D | REVISION:<br>O | |
|---|---|---|---|---|

**Figure 24. PCB footprint for SOT1052-2 (XSON8); recommended solder mask opening pattern**

H–PDFN–8 I/O
3 X 2 X 0.5 PKG, 0.5 PITCH

SOT1052–2




PCB DESIGN GUIDELINES
RECOMMENDED I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.



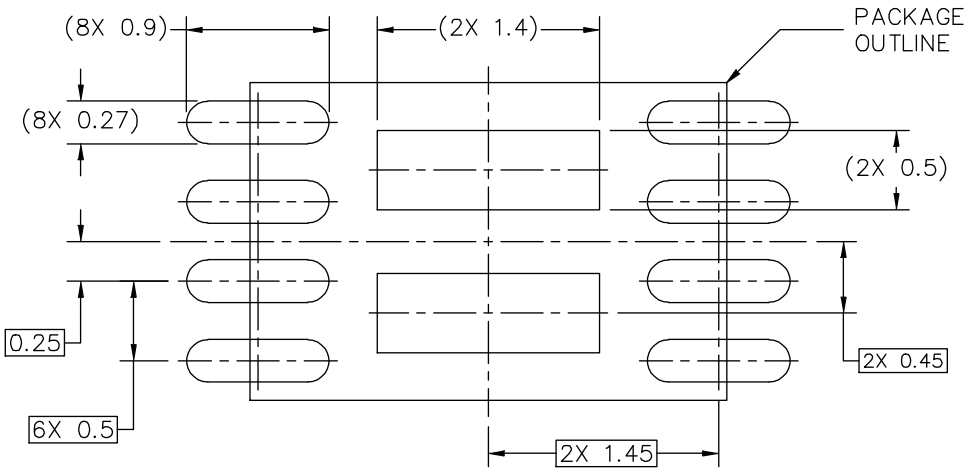
DATE: 06 JAN 2022

| MECHANICAL OUTLINE<br>PRINT VERSION NOT TO SCALE | STANDARD:<br>NON–JEDEC | DRAWING NUMBER:<br>98ASA01831D | REVISION:<br>O | |
|---|---|---|---|---|

**Figure 25. PCB footprint for SOT1052-2 (XSON8); recommended I/O pads and solderable area**

H−PDFN−8 I/O
3 X 2 X 0.5 PKG, 0.5 PITCH

SOT1052−2




RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES − RECOMMENDED SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.



DATE: 06 JAN 2022

| MECHANICAL OUTLINE<br>PRINT VERSION NOT TO SCALE | STANDARD:<br>NON−JEDEC | DRAWING NUMBER:<br>98ASA01831D | REVISION:<br>O | |
|---|---|---|---|---|

**Figure 26. PCB footprint for SOT1052-2 (XSON8); recommended solder paste stencil**

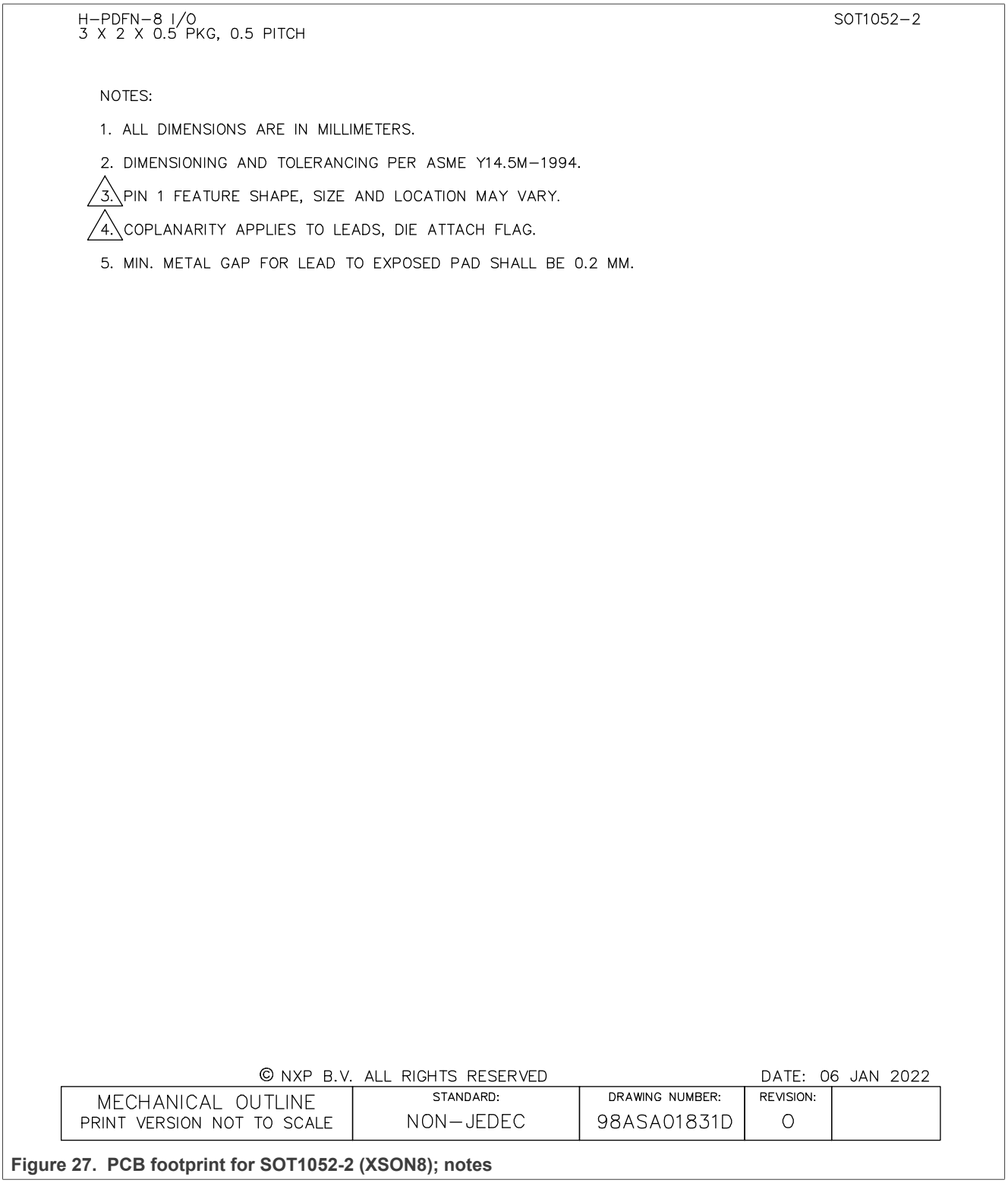



**Figure 27. PCB footprint for SOT1052-2 (XSON8); notes**

# 16 Abbreviations

**Table 15. Abbreviations**

| Acronym | Description |
|---|---|
| CDM | Charged Device Model |
| ESD | ElectroStatic Discharge |
| GTL | Gunning Transceiver Logic |
| HBM | Human Body Model |
| $I^2C$-bus | Inter-Integrated Circuit bus |
| I/O | Input/Output |
| LVTTL | Low Voltage Transistor-Transistor Logic |
| PRR | Pulse Repetition Rate |
| RC | Resistor-Capacitor network |

# 17 Revision history

**Table 16. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| NVT2001_NVT2002 v.4.3 | 20221006 | Product data sheet | 202210008I | NVT2001_NVT2002 v.4.2 |
| Modifications: | • Section 3: NVT2002TL Minimum Order Quantity corrected to 4Ku per reel | | | |
| NVT2001_NVT2002 v.4.2 | 20220207 | Product data sheet | - | NVT2001_NVT2002 v.4.1 |
| NVT2001_NVT2002 v.4.1 | 20191206 | Product data sheet | 201909001A, 201912004I | NVT2001_NVT2002 v.4 |
| Modifications: | • Package SOT886 requiring SSB added. Refer to PCN number 201909001A XSON6 (SOT886) Assembly/Test Transfer from ATGD and ATSN to ATBK.<br>• Corrected NVT2001GM topside mark N1X to N1. Only two characters allowed in Line 1 and there is no revolving date code.<br>• Improved temperature range from "-40 °C to +85 °C" to "-40 °C to +105 °C" | | | |
| NVT2001_NVT2002 v.4 | 20140127 | Product data sheet | - | NVT2001_NVT2002 v.3 |
| NVT2001_NVT2002 v.3 | 20120426 | Product data sheet | - | NVT2001_NVT2002 v.2 |
| NVT2001_NVT2002 v.2 | 20111026 | Product data sheet | - | NVT2001_NVT2002 v.1 |
| NVT2001_NVT2002 v.1 | 20100830 | Product data sheet | - | - |

# 18 Legal information

## 18.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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## Tables



## Figures