NVT4557

SIM card interface level translator with EMI filter and ESD protection

Rev. 2.1 — 12 November 2021 Product data sheet

1 General description

The NVT4557 device is built for interfacing a SIM card with a single low-voltage 1.08 V to 1.98 V host side interface. The NVT4557 contains three 1.62 V to 3.6 V level translators to convert the data, RSTn and CLKn signals between a SIM card and a host microcontroller.

The NVT4557 is compliant with all ETSI, IMT-2000 and ISO-7816 SIM/Smart card interface requirements.

2 Features and benefits

- Supports clock speed up to 10 MHz clock
- Compliant with all ETSI, IMT-2000 and ISO-7816 SIM/Smart card interface requirements
- Support SIM card supply voltages with range of 1.62 V to 3.6 V
- Host microcontroller operating voltage range: 1.08 V to 1.98 V
- Automatic level translation of I/O, RSTn and CLKn between SIM card and host side interface with capacitance isolation
- Incorporates shutdown feature for the SIM card signals according to ISO-7816-3
- Automatic enable and disable through V_{CCB} (Enable pin on NVT4557HK 10 pin package only)
- Integrated pull-up and pull-down resistors: no external resistors required
- Integrated EMI filters suppress higher harmonics of digital I/Os
- Integrated 8 kV ESD protection according to IEC 61000-4-2, level 4 on V_{CCB} or any of the card side pins. External ESD diodes are not required.
- Level shifting buffers keep ESD stress away from the host (zero-clamping concept)
- Pb-free, Restriction of Hazardous Substances (RoHS) compliant and free of halogen and antimony (Dark Green compliant)
- Available in 9-pin WLCSP package in 0.3 mm pitch and 10-pin XQFN10 package with 0.4 mm pitch

3 Applications

- NVT4557 can be used with a range of SIM card attached devices including:
  - Mobile and personal phones
  - Wireless modems
  - SIM card terminals

4 Ordering information

Table 1. Ordering information

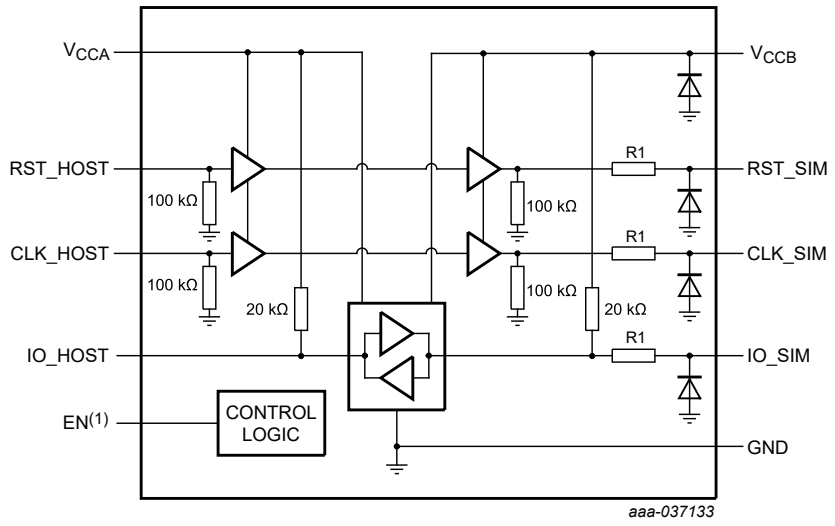
Type number	Topside mark	Package		
		Name	Description	Version
NVT4557UK	7	WLCSP9	wafer level CSP package; 9 bumps (3 x 3); body 0.92 mm × 0.92 mm × 0.525 mm with 0.3 mm pitch	SOT2042-2
NVT4557HK	57	XQFN10	plastic, extremely thin quad flat package; no leads; 10 terminals; body 1.40 x 1.80 x 0.50 mm	SOT1160-1

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
NVT4557UK	NVT4557UKAZ	WLCSP9	Reel 13" Q1/T1 DP[1]	20000	T_{amb} = -40 °C to +85 °C
NVT4557HK	NVT4557HKX	XQFN10	Reel 7" Q1/T1 NDP[2]	4000	T_{amb} = -40 °C to +85 °C

[1] Find packing information - www.nxp.com/docs/en/packing/SOT2042-2_118.pdf
[2] Find packing information - www.nxp.com/docs/en/packing/SOT1160-1_115.pdf

5 Functional diagram



1. 10-pin version only

Figure 1. Functional diagram

6 Pinning information

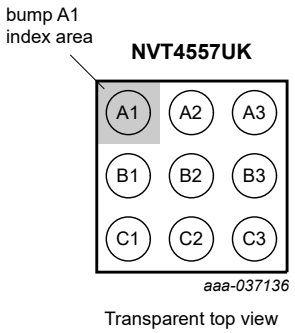


Figure 2. Bump configuration for WLCSP9

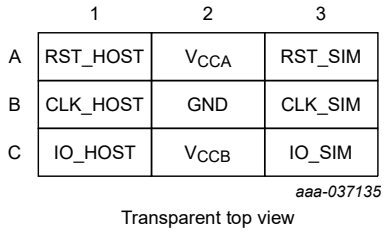


Figure 3. Bump mapping for WLCSP9

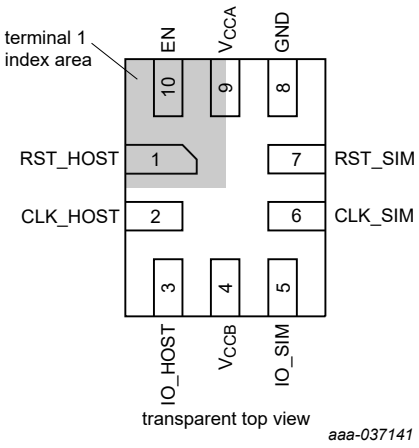


Figure 4. Pin configuration for XQFN10

6.1 Pin description

Table 3. Pin description

Symbol	Pinning for WLCSP9	Pinning for XQFN10	Type	Description
RST_HOST	A1	1	I	Reset input from host controller.
V_{CCA}	A2	9	supply	Supply voltage for the host controller side input/output pins (CLK_HOST, RST_HOST, IO_HOST). This pin should be bypassed with a 0.1 µF ceramic capacitor close to the pin.
RST_SIM	A3	7	O	Reset output pin for the SIM card.
CLK_HOST	B1	2	I	Clock input from host controller.
GND	B2	8	ground	Ground for the SIM card and host controller. Proper grounding and bypassing are required to meet ESD specifications.
CLK_SIM	B3	6	O	Clock output pin for the SIM card.
IO_HOST	C1	3	I/O	Host controller bidirectional data input/output. The host output must be on an open-drain driver.

Table 3. Pin description...*continued*

Symbol	Pinning for WLCSP9	Pinning for XQFN10	Type	Description
V_{CCB}	C2	4	supply	SIM card supply voltage. When V_{CCB} is below the $V_{CCBdisable}$, the device is disabled. This pin should be bypassed with a 0.1 µF ceramic capacitor close to the pin.
IO_SIM	C3	5	I/O	SIM card bidirectional data input/output. The SIM card output must be on an open-drain driver.
EN	—	10	I	Host controller driven enable pin. This pin should be HIGH (V_{CCA}) for normal operation, and LOW to help avoid race conditions specifically during the shutdown sequence. (Only on 10 pin version - for 9 pin version EN is pulled to V_{CCA}.)

7 Functional description

Table 4. Function table

Supply Voltage		Input	Input/Out		Operational Mode
V_{CCA}	V_{CCB}	EN [1] [2]	Host	SIM Card	
1.08 V to 1.98 V	1.62 V to 3.6 V	H	HOST = SIM Card	SIM Card = HOST	Active
1.08 V to 1.98 V	1.62 V to 3.6 V	L	See Table 5, Condition B		Shutdown Mode
GND	1.62 V to 3.6 V	X	See Table 5, Condition B		Shutdown Mode
1.08 V to 1.98 V	GND	X	See Table 5, Condition A		Shutdown Mode
GND	GND	X	See Table 5, Condition A		Shutdown Mode

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.
[2] V_{IL} and V_{IH} are referenced to V_{CCA}. The EN can be controlled by an external device limit of V_{CCA} + 0.3 V.

Table 5. Pin condition

Pin condition	Condition A	Condition B
RST_HOST	100 kΩ pull low	100 kΩ pull low
CLK_HOST	100 kΩ pull low	100 kΩ pull low
IO_HOST	20 kΩ pull to V_{CCA}	20 kΩ pull to V_{CCA}
RST_SIM	100 kΩ pull low	400 Ω pull low
CLK_SIM	100 kΩ pull low	400 Ω pull low
IO_SIM	High Z	400 Ω pull low

Refer to Figure 1.

7.1 Shutdown sequence of NVT4557 (10-pin version only)

The ISO 7816-3 specification specifies the shutdown sequence for the SIM card signals to ensure that the card is properly disabled for power savings. Also during hot swap, the orderly shutdown of these signals helps to avoid any improper write and corruption of data.

When the enable, EN, is asserted LOW, the shutdown sequence is initiated by powering down the RST_SIM channel. Once the RST_SIM channel is powered down, CLK_SIM and IO_SIM are powered down sequentially one-by-one. An internal pull-down resistor on the SIM pins is used to pull these channels LOW. The shutdown sequence is completed in a few microseconds. It is important that EN is pulled LOW before V_{CCA} and V_{CCB} supplies go LOW to ensure that the shutdown sequence is properly initiated.

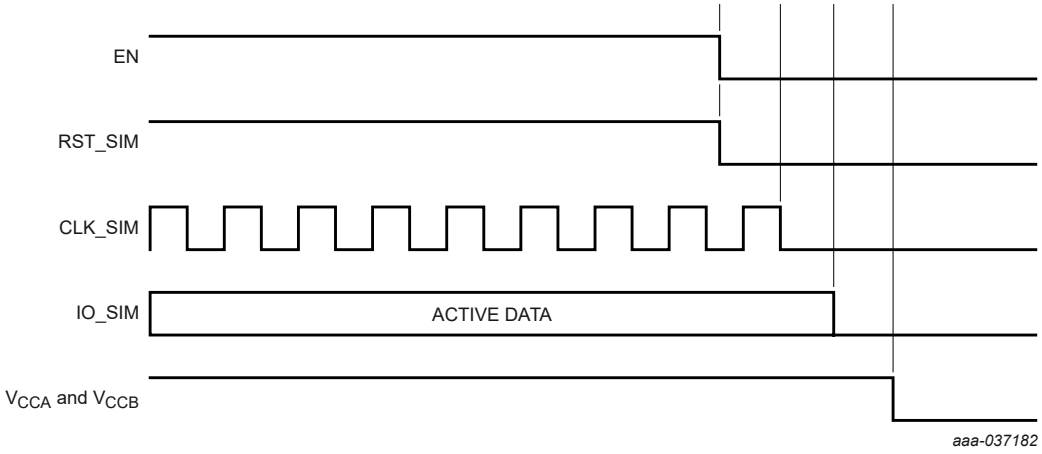
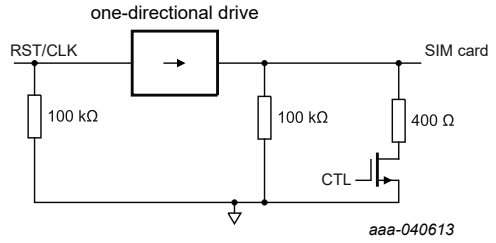


Figure 5. Shutdown sequence for RST_SIM, CLK_SIM, IO_SIM and V_{CCA}/V_{CCB} of NVT4557 SIM card translator

7.2 Embedded Enable - 9 pin and 10 pin if Enable is tied to V_{CCA}

The device contains an auto-enable feature. If V_{CCB} rises above V_{CCB_EN}, the level translator logic is enabled automatically. As soon as V_{CCB} drops below the V_{CCB_DIS}, the SIM card side drivers and the level translator logic is disabled. Host side IO pin is configured as input with a 20 kΩ resistor pulled up to V_{CCA}.

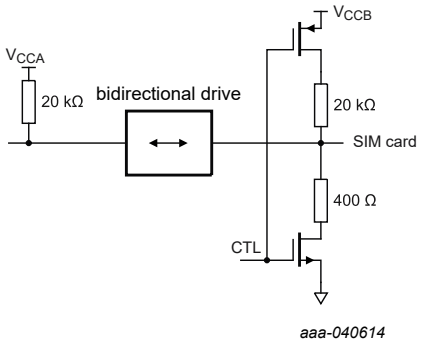
When the V_{CCB} drops below V_{CCB} disable voltage but is still higher than a MOS threshold (e.g., 0.8 V) the pulldown NMOS in the one-directional drive will be off and NMOS controlled by CTL will be on, and the 400 Ω resistor will keep the card side CLK/RST/IO low. Additionally the CLK/RST pins on both the Host and Card side have a 100 kΩ pull down resistor. The 400 Ω resistor is used for discharge at power off and the 100 kΩ resister is used for keep RST_SIM/CLK_SIM low when V_{CCB} below vth.



When V_{CCB_EN} = 0 then CTL = V_{CCB} and line is high-Z.

When V_{CCB_EN} = 1 then CTL = GND and line is active.

Figure 6. RST/CLK voltage level translation architecture



When V_{CCB_EN} = 0 then CTL = V_{CCB} and line is high-Z.

When V_{CCB_EN} = 1 then CTL = GND and line is active.

Figure 7. IO voltage level translation architecture

7.3 EMI filter

All input/output driver stages are equipped with EMI filters to reduce interferences towards sensitive mobile communication.

7.4 ESD protection

The device has robust ESD protections on all SIM card pins as well as on the V_{CCB} pin. The architecture prevents any stress for the host: the voltage translator discharges any stress to supply ground.

8 Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CCA}	host supply voltage			GND – 0.5	2.4	V
V_{CCB}	SIM supply voltage			GND – 0.5	4.0	V
$V_{I(CLK\_HOST)}$	input voltage on pin CLK_HOST	input signal voltage, HOST side		GND – 0.5	V_{CCA} + 0.3	V
$V_{I(RST\_HOST)}$	input voltage on pin RST_HOST	input signal voltage, HOST side		GND – 0.5	V_{CCA} + 0.3	V
$V_{I(IO\_HOST)}$	input voltage on pin IO_HOST	input signal voltage, HOST side		GND – 0.5	V_{CCA} + 0.3	V
$V_{I(CLK\_SIM)}$	input voltage on pin CLK_SIM	input signal voltage, SIM side		GND – 0.5	V_{CCB} + 0.3	V
$V_{I(RST\_SIM)}$	input voltage on pin RST_SIM	input signal voltage, SIM side		GND – 0.5	V_{CCB} + 0.3	V
$V_{I(IO\_SIM)}$	input voltage on pin IO_SIM	input signal voltage, SIM side		GND – 0.5	V_{CCB} + 0.3	V
T_{stg}	storage temperature			–55	+125	°C
T_{amb}	ambient temperature			–40	+85	°C

Table 6. Limiting values...*continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4, all memory card-side pins, V_{CCB} and GND	[1]			
		contact discharge		–8	+8	kV
		air discharge	[2]	–15	+15	kV
		Human Body Model (HBM) JEDEC JESD22-A114F; all pins		–2000	+2000	V
		Charge Device Model (CDM) JEDEC JESD22-C101E; all pins		–500	+500	V
$I_{lu(IO)}$	input/output latch-up current	JESD 78B: $-0.5 \times V_{CC} < V_I < 1.5 \times V_{CC}$; $T_j < 125$ °C		–100	+100	mA

[1] All system level tests are performed with the application-specific capacitors connected to the supply pins V_{SUPPLY}, V_{LDO} and V_{CCA}.

[2] The IEC 61000-4-2 standards are defined so that each level is considered equivalent – a Level 4 contact discharge of 8 kV is considered equivalent to a 15 kV air discharge. Air discharge is provided for information only and was not tested. Per IEC61000-4-2: Contact discharge is the preferred test method, air discharges shall be used where contact discharge cannot be applied. Please refer to AN10897: A guide to designing for ESD and EMC and AN11267: EMC and system level ESD design guidelines for LCD drivers for more information on ESD testing and ESD design techniques.

9 Characteristics

Table 7. Supplies

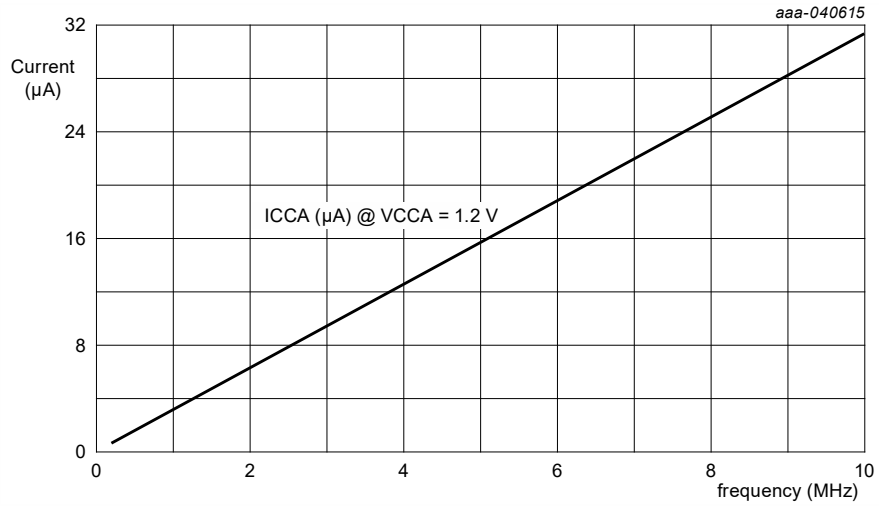
$1.62 V \le V_{CCB} \le 3.6 V$; $1.08 V \le V_{CCA} \le 1.98 V$; $T_{amb} = -40$ °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
V_{CCA}	supply voltage			1.08	—	1.98	V
I_{CCA}	supply current	operating mode; f_{CLK_HOST} = 1 MHz, EN = V_{CCA}		—	5	10	µA
		Quiescent current; EN = V_{CCA}, IO_HOST = V_{CCA} and CLK_HOST = GND		—	0.01	1	µA
		shutdown mode; EN = GND	[2]	—	—	1	µA
V_{CCB}	SIM supply voltage			1.62	—	3.6	V
I_{CCB}	SIM supply current	operating mode; f_{CLK_HOST} = 1 MHz, EN = V_{CCA}, C_l = 50 pF V_{CCB} = 3.6 V		—	300	350	µA
		Quiescent current; EN = V_{CCA}, IO_HOST and CLK_HOST = GND		—	3.7	10	µA
		shutdown mode; EN = GND	[2]	—	—	1	µA
V_I	input voltage	host side	[3]	–0.3	—	V_{CCA} + 0.3	V
		sim card side		–0.3	—	V_{CCB} + 0.3	V

[1] Typical values measured at 25 °C.

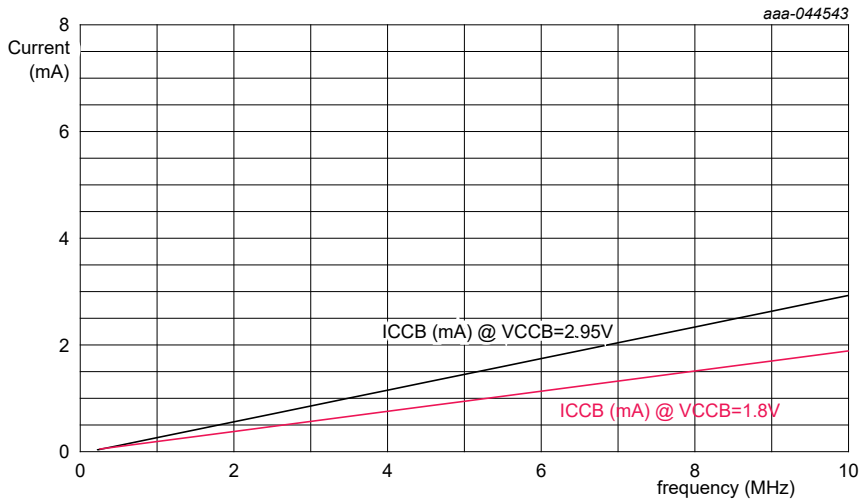
[2] EN pin not featured on 9 pin version and is pulled internally to V_{CCA}

[3] The voltage must not exceed 1.98 V steady state.



V_{CCA} = 1.2 V and V_{CCB} = 1.8 V or 2.95 V; C_I = 50 pF

Figure 8. Operating Mode Current over Frequency- Host side



V_{CCA} = 1.2 V and V_{CCB} = 1.8 V or 2.95 V; C_I = 50 pF

Figure 9. Operating Mode Current over Frequency - Card side

Table 8. Static characteristics

1.62 V ≤ V_{CCB} ≤ 3.6 V; 1.08 V ≤ V_{CCA} ≤ 1.98 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
Automatic enable feature: V_{CCB}							
V_{CCB_EN}	device enable voltage level	V_{CCA} ≥ 1.0 V, V_{CCB} rising edge		1.62	—	—	V
V_{CCB_DIS}	device disable voltage level	V_{CCA} ≥ 1.0 V, V_{CCB} falling edge		—	—	0.8	V
Hardware enable pin							
V_{IH}	HIGH-level input voltage	EN pin		0.7 × V_{CCA}	—	—	V
V_{IL}	LOW-level input voltage	EN pin		—	—	0.3 × V_{CCA}	V
Level shifter							
V_{IH}	HIGH-level input voltage	IO_HOST, RST_HOST, CLK_HOST					
		1.08 V ≤ V_{CCA} < 1.98 V	[2]	0.7 × V_{CCA}	—	—	V
		IO_SIM	[2]	0.7 × V_{CCB}	—	—	V
V_{IL}	LOW-level input voltage	IO_HOST, RST_HOST, CLK_HOST	[2]	—	—	0.3 × V_{CCA}	V
		IO_SIM	[2]	—	—	0.3 × V_{CCB}	V
R_{PU}	pull-up resistance	IO_SIM connected to V_{CCB}	[3]	14	20	26	kΩ
		IO_HOST connected to V_{CCA}	[3]	14	20	26	kΩ
V_{OH}	HIGH-level output voltage	RST_SIM, CLK_SIM; I_{OH} = –1 mA	[2]	0.8 × V_{CCB}	—	V_{CCB}	V
		IO_SIM; I_{OH} = –10 µA	[2]	0.8 × V_{CCB}	—	V_{CCB}	V
		IO_HOST; I_{OH} = –8 µA	[2]	0.8 × V_{CCA}	—	V_{CCA}	V
V_{OL}	LOW-level output voltage	RST_SIM, CLK_SIM; I_{OL} = 1 mA	[2]	0	—	0.125 × V_{CCB}	mV
		IO_SIM; I_{OL} = 1 mA	[2]	0	—	0.125 × V_{CCB}	mV
		IO_HOST; I_{OL} = 1 mA	[2]	0	—	0.25 × V_{CCA}	mV
R_{pd}	pull-down resistance	CLK_HOST/SIM, RST_HOST/SIM	[4]	70	100	130	kΩ
EMI filter							
R_s	series resistance	IO_SIM; R1 tolerance ± 30 % [5]	[2]	—	30	—	Ω
		RST_SIM; R1 tolerance ± 30 % [5]		—	30	—	Ω
		CLK_SIM; R1 tolerance ± 30 % [5]	[2]	—	30	—	Ω
C_{io}	input/output capacitance	IO_SIM	[2]	—	8.5	—	pF
		RST_SIM		—	8.5	—	pF
		CLK_SIM	[2]	—	8.5	—	pF

[1] Typical values measured at 25 °C.
[2] V_{IL}, V_{IH} depend on the individual supply voltage per interface.
[3] See Figure 12 for details.
[4] EN pin not featured on 9 pin version and is pulled internally to V_{CCA}
[5] Guaranteed by design

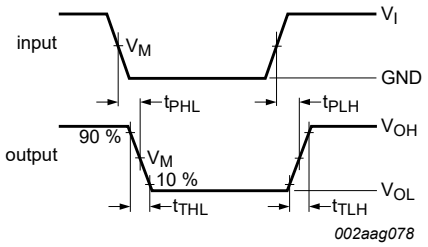
Table 9. Dynamic characteristics

1.62 V ≤ V_{CCB} ≤ 3.6 V; 1.08 V ≤ V_{CCA} ≤ 1.98 V; f_{clk} = f_{io} = 1 MHz; T_{amb} = −40 °C to +85 °C; unless otherwise specified. Refer to Figure 10.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CCA} = 1.8 V; V_{CCB} = 3.0 V; SIM card C_L ≤ 30 pF; host C_L ≤ 10 pF							
t_{PD}	propagation delay	I/O channel; SIM card side to host side		—	8	15	ns
		all channels; host side to SIM card side		—	8	15	ns
t_t	transition time			—	—	10	ns
$t_{sk(o)}$	output skew time	between channels; IO_SIM and CLK_SIM	[1]	—	2	—	ns
f_{clk}	clock frequency	CLK_SIM [2]		—	—	10	MHz
V_{CCA} = 1.2 V; V_{CCB} = 1.8 V; SIM card C_L ≤ 30 pF; host C_L ≤ 10 pF							
t_{PD}	propagation delay	I/O channel; SIM card side to host side		—	15	25	ns
		all channels; host side to SIM card side		—	15	25	ns
t_t	transition time			—	—	10	ns
$t_{sk(o)}$	output skew time	between channels; IO_SIM and CLK_SIM	[1]	—	2	—	ns
f_{clk}	clock frequency	CLK_SIM [2]		—	—	10	MHz

[1] Skew between any two outputs of the same package switching in the same direction with the same C_L.
[2] Guaranteed by design

9.1 Waveforms



Measurement points are given in Table 9.

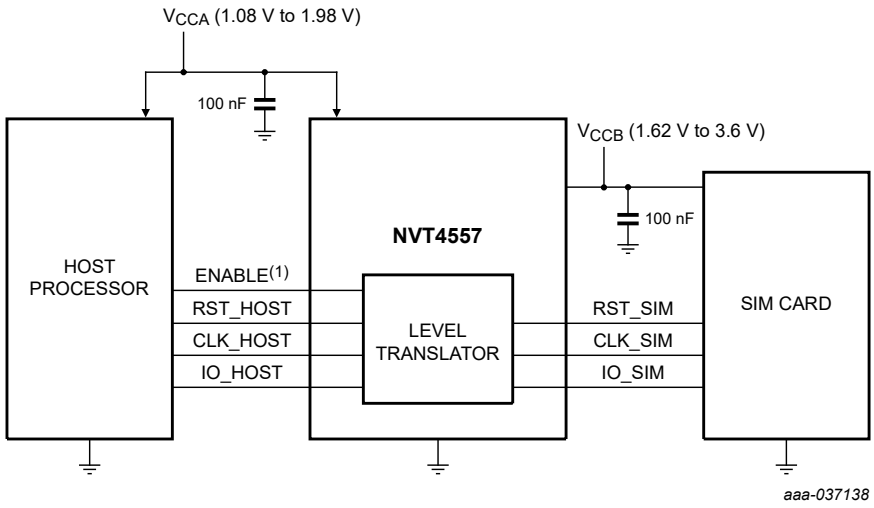
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

t_{PHL} and t_{PLH} are t_{PD} propagation delay; t_{THL} and t_{TLH} are the transition time.

Figure 10. Data input to data output propagation delay times

10 Application information

The application circuit for the NVT4557, which shows the typical interface with a SIM card, is shown in Figure 11.



1. 10-pin XQFN only

Figure 11. NVT4557 application circuit interfacing with typical SIM card

10.1 Input/output capacitor considerations

It is recommended that a 1 µF and 100 nF capacitors having low Equivalent Series Resistance (ESR) are used respectively at V_{CCA} and V_{CCB} input terminals of the device. X5R and X7R type multi-layer ceramic capacitors (MLCC) are preferred because they have minimal variation in value and ESR over temperature. The maximum ESR should be < 500 mΩ (50 mΩ typical).

10.2 Layout consideration

The capacitors should be placed directly at the terminals and ground plane. It is recommended to design the PCB so that the V_{CCA} and V_{CCB} pins are bypassed with a capacitor with each ground returning to a common node at the GND pin of the device such that ground loops are minimized.

Additional information can be found in AN13158 NVT4858/NVT4557 voltage-level translator layout guideline.

10.3 Level translator stage

The architecture of the device I/O channel is shown in Figure 12. The device does not require an extra input signal to control the direction of data flow from host to SIM or from SIM to host. As a change of driving direction is just possible when both sides are in HIGH state, the control logic is recognizing the first falling edge granting it control about the other signal side. During a rising edge signal, the non-driving output is driven by a one-shot circuit to accelerate the rising edge. In case of a communication error or some other unforeseen incident that would drive both connected sides to be drivers at the same time, the internal logic automatically prevents stuck-at situation, so both I/Os will return to HIGH level once released from being driven LOW.

The channels RST and CLK just contain single direction drivers without the holding mechanism of the I/O channel, as these are just driven from the host to the card side.

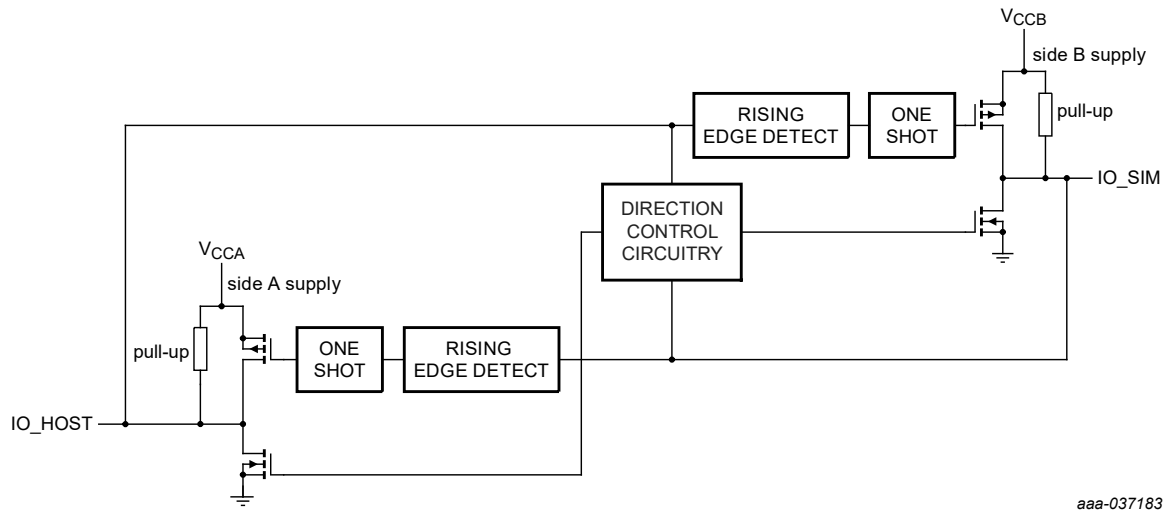


Figure 12. Automatic direction control level translator for HIGH-level direction change interfaces

11 Package outline

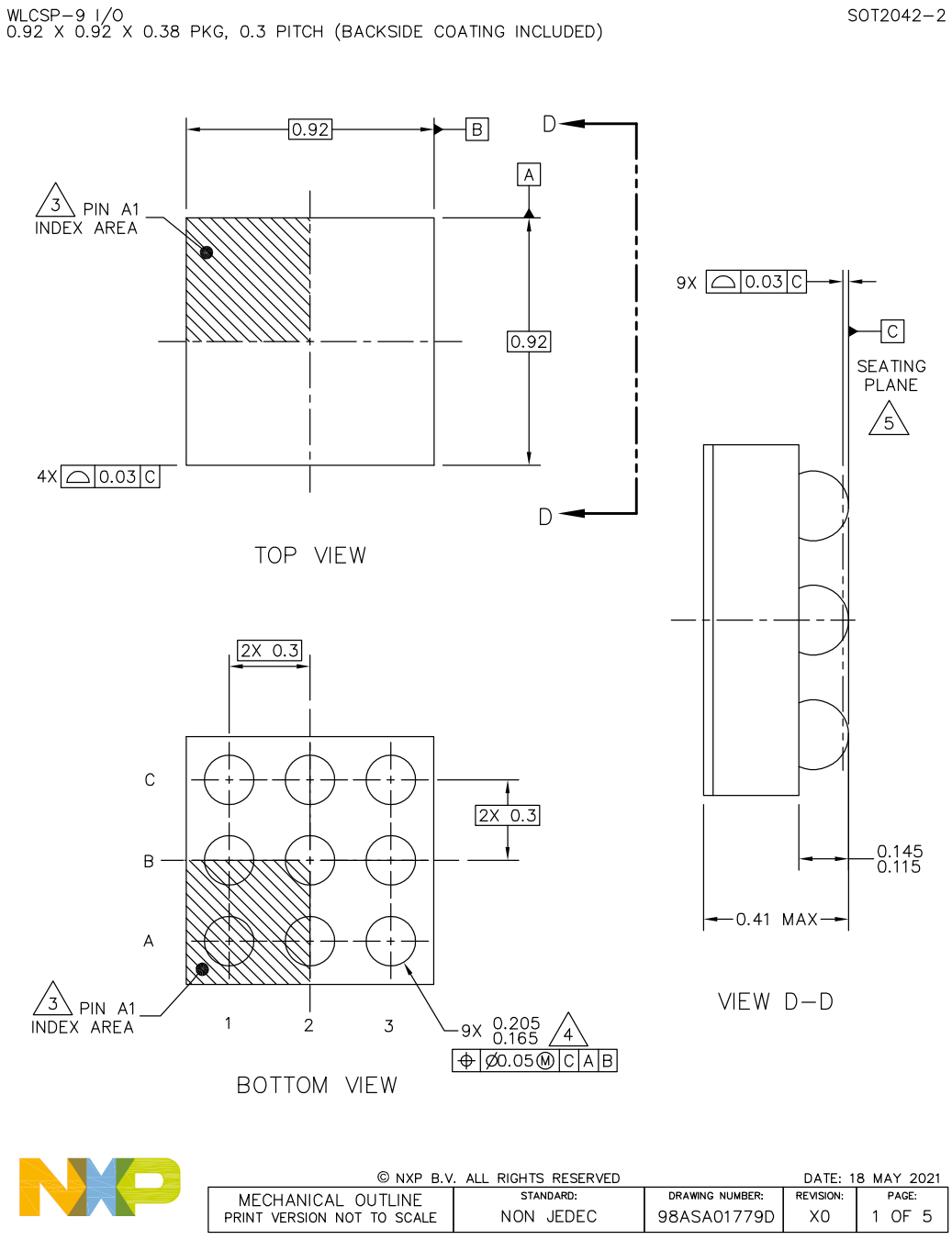


Figure 13. Package outline WLCSP9 (SOT2042-2)

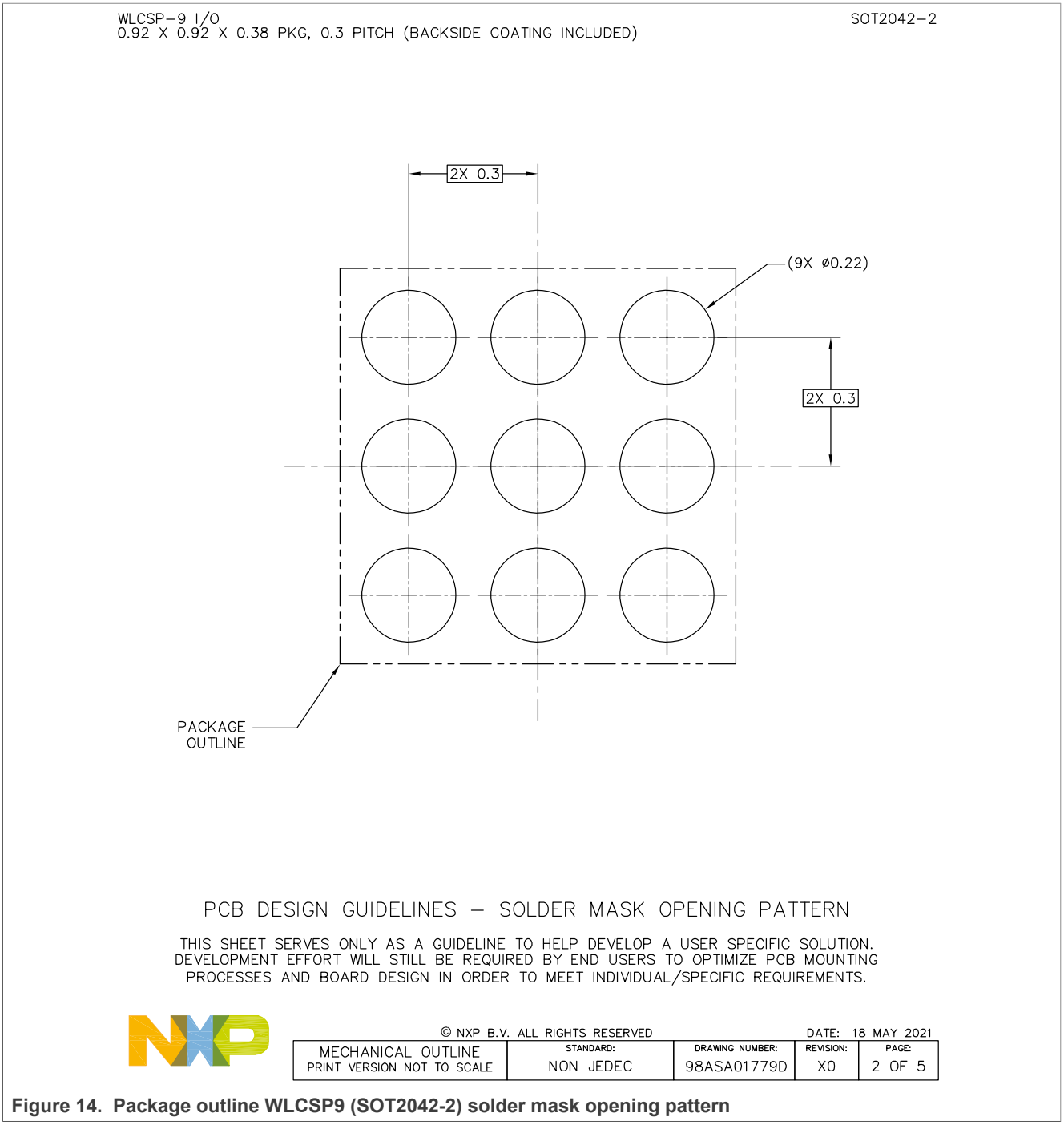


Figure 14. Package outline WLCSP9 (SOT2042-2) solder mask opening pattern

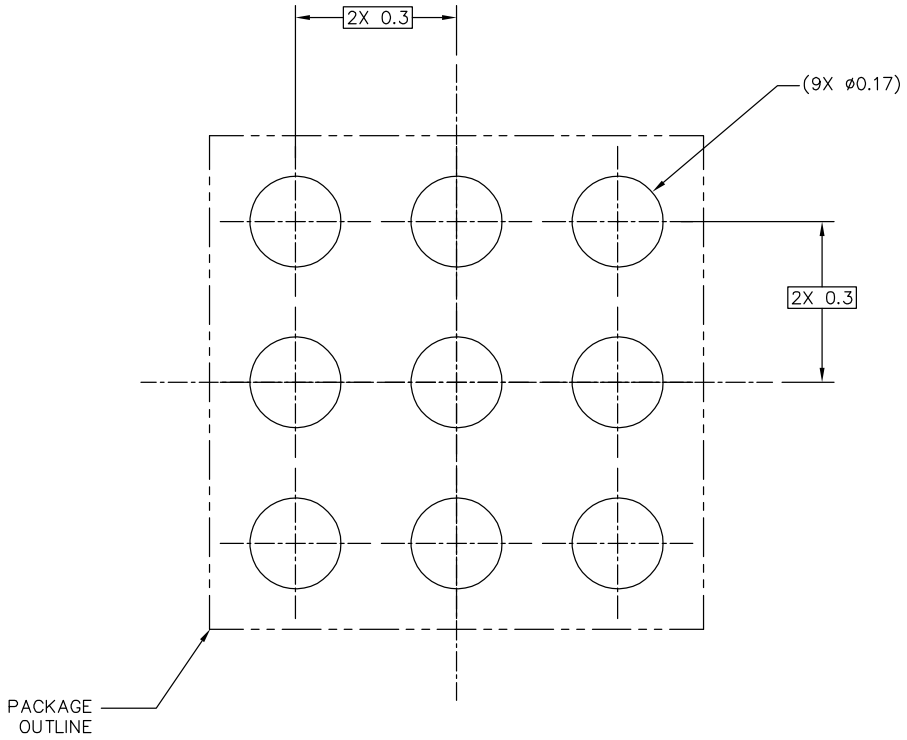


Figure 15. Package outline WLCSP9 (SOT2042-2) I/O pads and solderable area

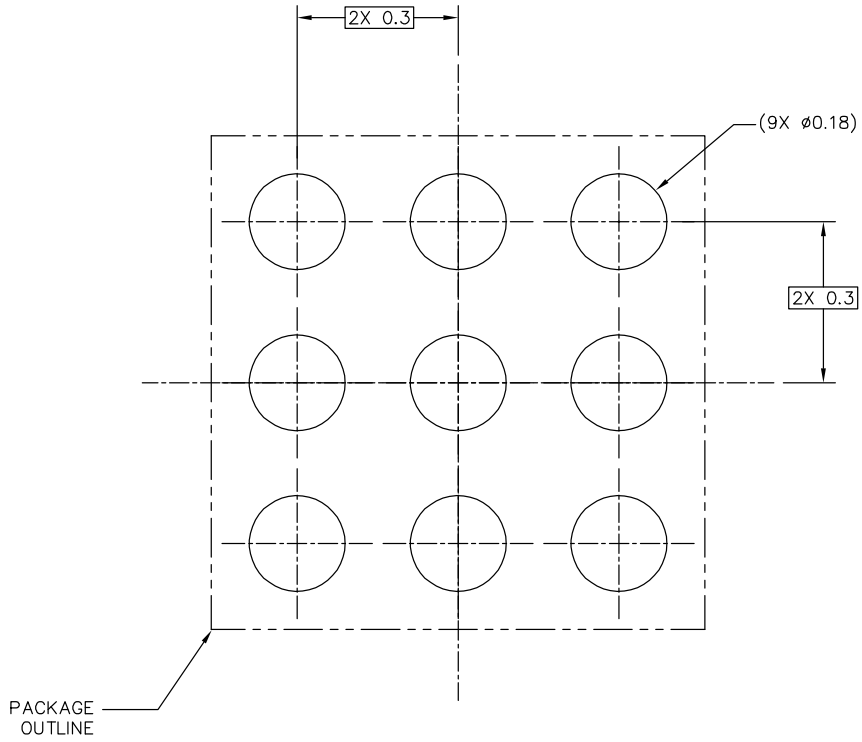


Figure 16. Package outline WLCSP9 (SOT2042-2) solder paste stencil

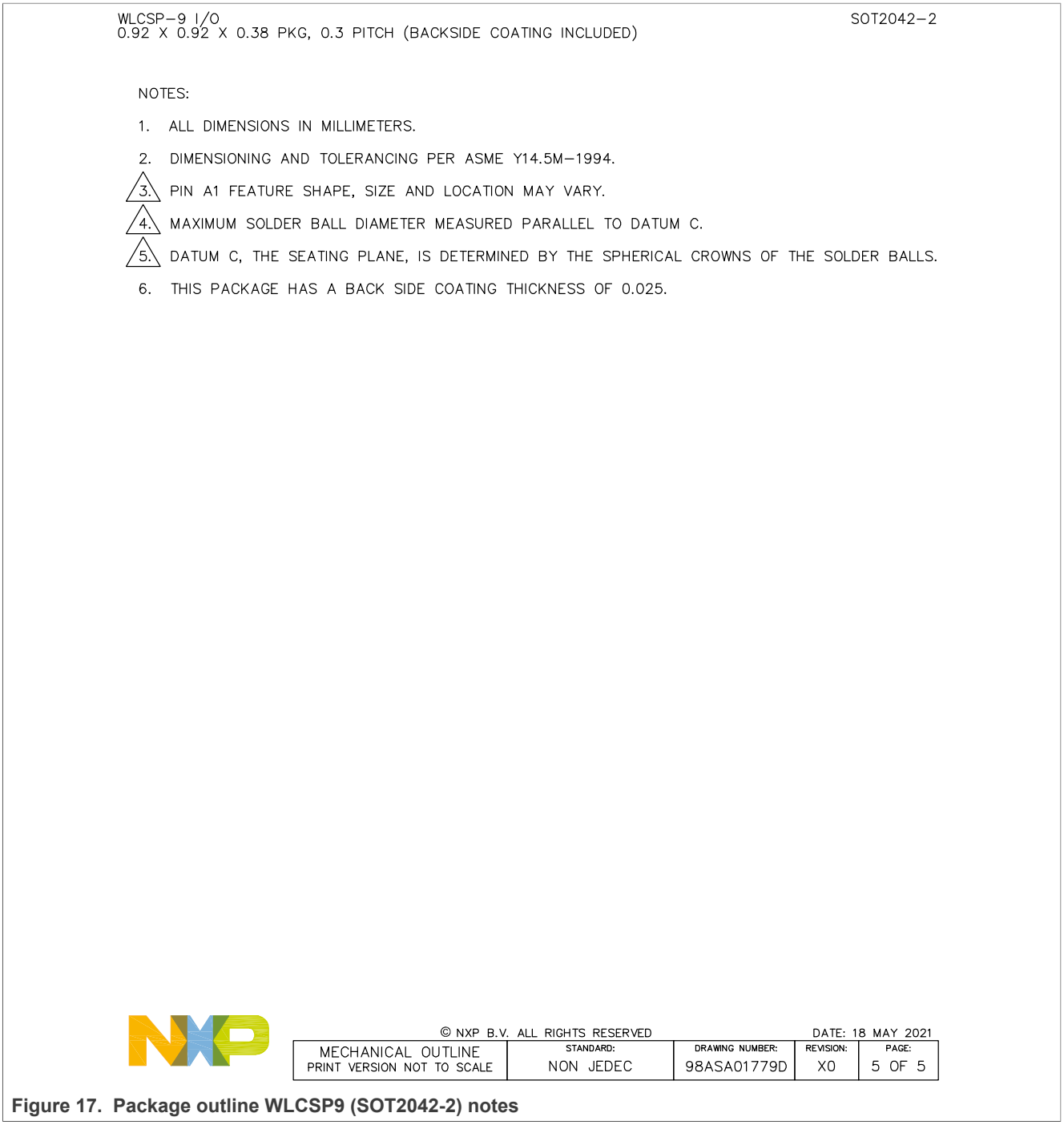
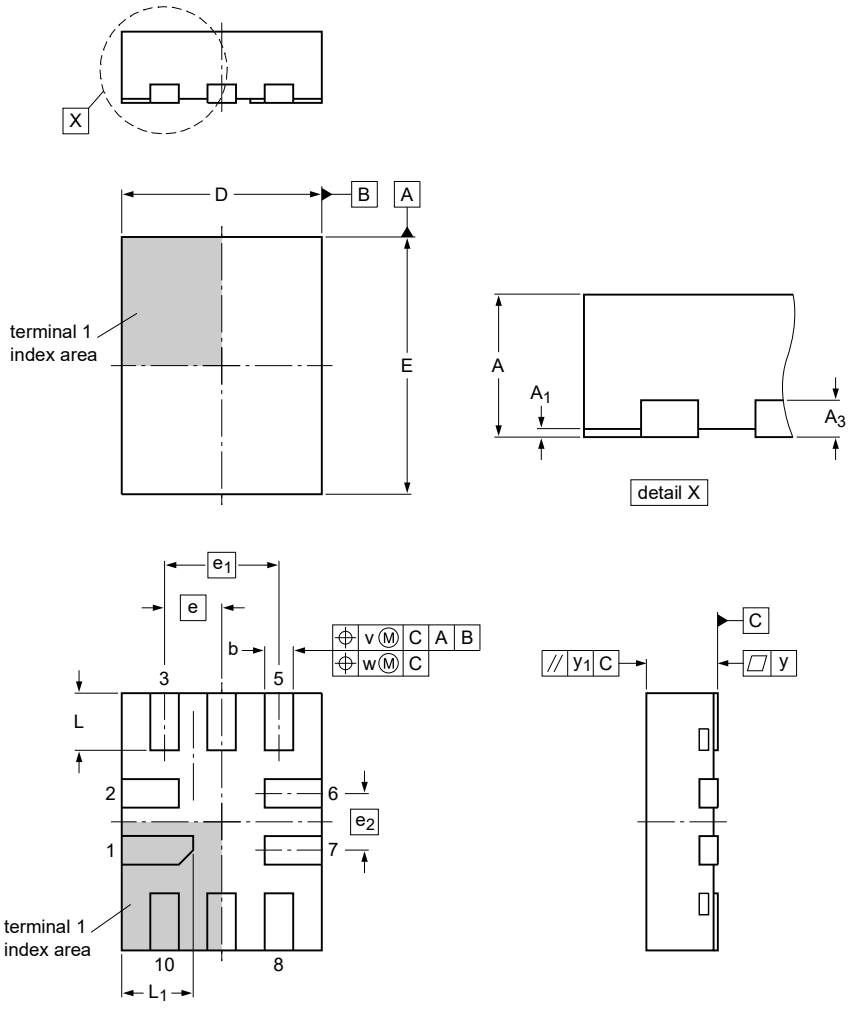


Figure 17. Package outline WLCSP9 (SOT2042-2) notes

XQFN10: plastic, extremely thin quad flat package; no leads; 10 terminals; body 1.40 x 1.80 x 0.50 mm **SOT1160-1**



Dimensions

Unit(1)		A	A_1	A_3	b	D	E	e	e_1	e_2	L	L_1	v	w	y	y_1
mm	max	0.50	0.05		0.25	1.5	1.9				0.45	0.55				
	nom	0.45		0.127	0.20	1.4	1.8	0.4	0.8	0.4	0.40	0.50	0.1	0.05	0.05	0.05
	min	0.40	0.00		0.15	1.3	1.7				0.35	0.45				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1160-1_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1160-1	- - -	- - -	- - -		~~09-12-29~~ 21-01-26

Figure 18. Package outline XQFN10 (SOT1160-1)

12 PCB layout

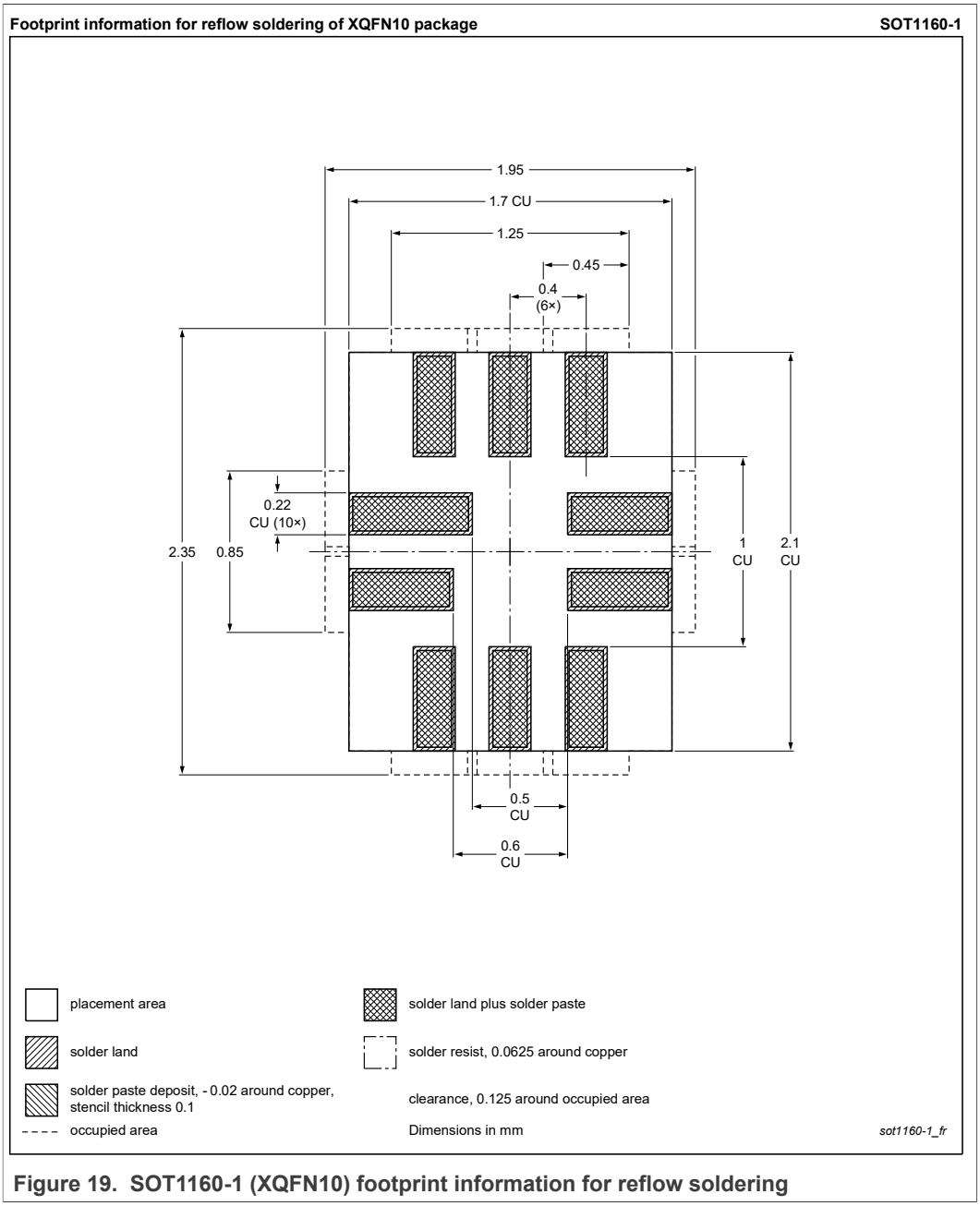


Figure 19. SOT1160-1 (XQFN10) footprint information for reflow soldering

13 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 20) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 10 and Table 11

Table 10. SnPb eutectic process (from J-STD-020D)

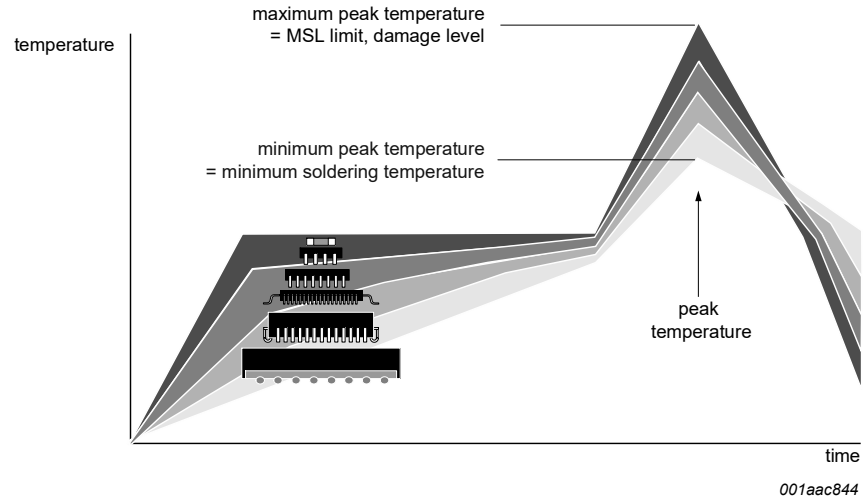
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 11. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 20.



MSL: Moisture Sensitivity Level

Figure 20. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14 Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged-Device Model
DP	Dry Pack
ESD	ElectroStatic Discharge
ESR	Equivalent Series Resistance
HBM	Human Body Model
I/O	Input/Output
LDO	Low DropOut regulator
PCB	Printed-Circuit Board
PMOS	Positive-channel Metal-Oxide Semiconductor
SIM	Subscriber Identification Module

15 Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NVT4557 v.2.1	20211112	Product data sheet	CIN 202111014I	NVT4557 v.2.0
Modifications	• Global changes: revised 1.95 V to 1.98 V and revised 1.65 V to 1.62 V throughout the data sheet. • Section 2, revised "Automatic enable and disable through V_{CCB} (Enable pin on NVT4557HK 10 pin package only)" adding parenthetical comment to the feature. • Section 4, Table 1 revised the topside marking for NVT4557UK from "557" to "7". • Section 4, Table 2 revised orderable part number from "NTV4557UKJ" to "NTV4557UKAZ", added "DP" to the packing method, and added "NDP" to the packing method for NVT4557HK. • Section 6.1, Table 3, added "(Only on 10 pin version - for 9 pin version EN is pulled to V_{CCA}.)" to the description for Symbol "EN". • Section 9, Table 7, revised as follows: – I_{CCA}: revised the conditions, adding "=V_{CCA}" after "IO_HOST" and added new footnote after "EN = GND". – I_{CCB}: revised the conditions, adding "V_{CCB} = 3.6 V", revised the Typ value from "20" to "300", revised the Max value from "30" to "350", added new footnote after "EN = GND" and revised the I_{CCB} Max value from "4.2" to "10". • Section 9, Figure 8, revised the figure and added new Figure 9. • Section 9, Table 8, revised as follows: – V_{CCB_EN}: revised Min, Typ, and Max values. – V_{CCB_DIS}: revised Min, Typ, and Max values. – ΔV_{CCBen}: removed row. – V_{IH}: revised the conditions. – V_{IL}: revised the condition. – V_{OH}: revised the three Min values from 0.75 to 0.8 and revised the IO_Host condition from -10 µA to -8 µA. – R_{pd}: removed "EN = 0" from the condition and added a footnote. • Section 10, Figure 11, revised the image.			
NVT4557 v.2.0	20210915	Product data sheet	—	NVT4557 v.1.0
Modifications:	• Added NVT4557UK • Table 6: Corrected V_I to be consistent with V_I in recommended values table; added note to air discharge ESD			
NVT4557 v.1.0	20210421	Product data sheet	—	—

16 Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".
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