

UM11582

NVT4858-4557-EVB evaluation board

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User manual

Document information

Information	Content
Keywords	NVT4858, NVT4557, Level Shifter, Level Translator, SD card, SIM card, NVT4858 user manual, NVT4757 user manual, NVT4858 evaluation board, NVT4858 evaluation board
Abstract	The NVT4858 is an SD 3.0 compliant dual voltage level translator with auto-direction control. The NVT4557 is a SIM SIO-7816 Smart Card compliant dual voltage level translator with auto-direction control. This document is intended to help the users to quickly setup, configure and operate the evaluation board in the users' hardware platform.



Revision history

Rev	Date	Description
v.1	20211129	Initial version

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1 Introduction

The NVT4858/NVT4557 are dual supply translating transceivers with auto direction sensing, enabling bidirectional voltage level translation. V_{CCA} on the host side can be supplied at any voltage between 1.08 V and 1.98 V and V_{CCB} on the card side can be supplied at any voltage between 1.62 V and 3.6 V.

The NVT4858 supports SD 3.0 SDR104, SDR50, DDR50, SDR25, SDR12 and SD 2.0 High-Speed (50 MHz) and Default-Speed (25 MHz) modes. The NVT4557 is compliant with all ETSI, IMT-2000 and ISO-7816 SIM/Smart card interface requirements

This document is intended to help the users to quickly setup, configure and operate the NVT4858-4557-EVB evaluation board in the users' hardware platform.

2 Finding kit resources and information on the NXP web site

NXP Semiconductors provides online resources for this evaluation board and its supported device(s) on <http://www.nxp.com>.

The information page for NVT4858-4557-EVB evaluation board is at <http://www.nxp.com/NVT4858-4557-EVB>. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a **Getting Started** tab. The **Getting Started** tab provides quick-reference information applicable to using the NVT4858-4557-EVB evaluation board, including the downloadable assets referenced in this document.

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3 Getting ready

Working with the NVT4858-4557-EVB evaluation board requires the kit contents.

3.1 Kit contents

- Assembled and tested evaluation board in an anti-static bag
- Quick Start Guide

4 Getting to know the hardware

As default, NVT4858-4557-EVB evaluation board is loaded with the NVT4858 (SD level shifter) as well as the NVT4557 (SIM level shifter) along with one SD card socket and one SIM card socket.

The demo board is designed to be a stand-alone board to allow the users to evaluate the performance of the NVT4858 or the NVT4557. There are four 100 mil headers, and the connections to all of the pins of the NVT4858 and the NVT4557 are available at these headers. In addition, there is one SIM card socket and one SD card socket available on the board. The SIM card, or the SD card that is inserted in the socket can be directly

accessed by the SD host controller or the SIM controller via the 100 mil headers on the host interface side of the level shifter.

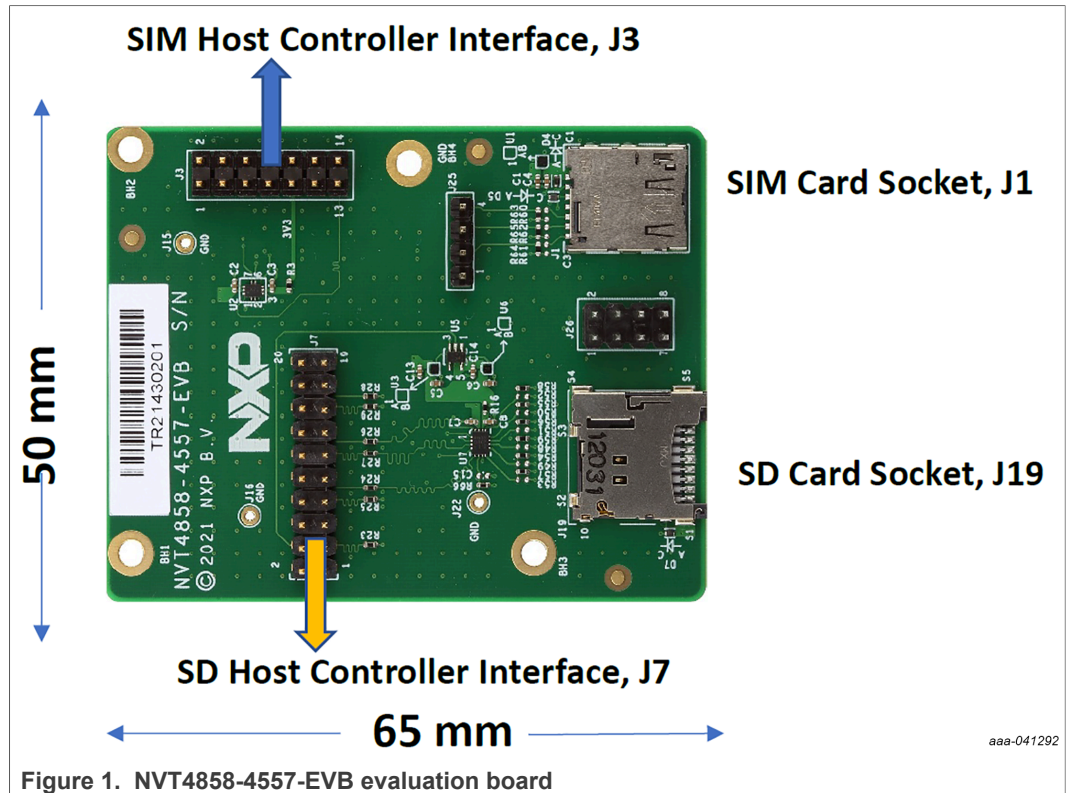
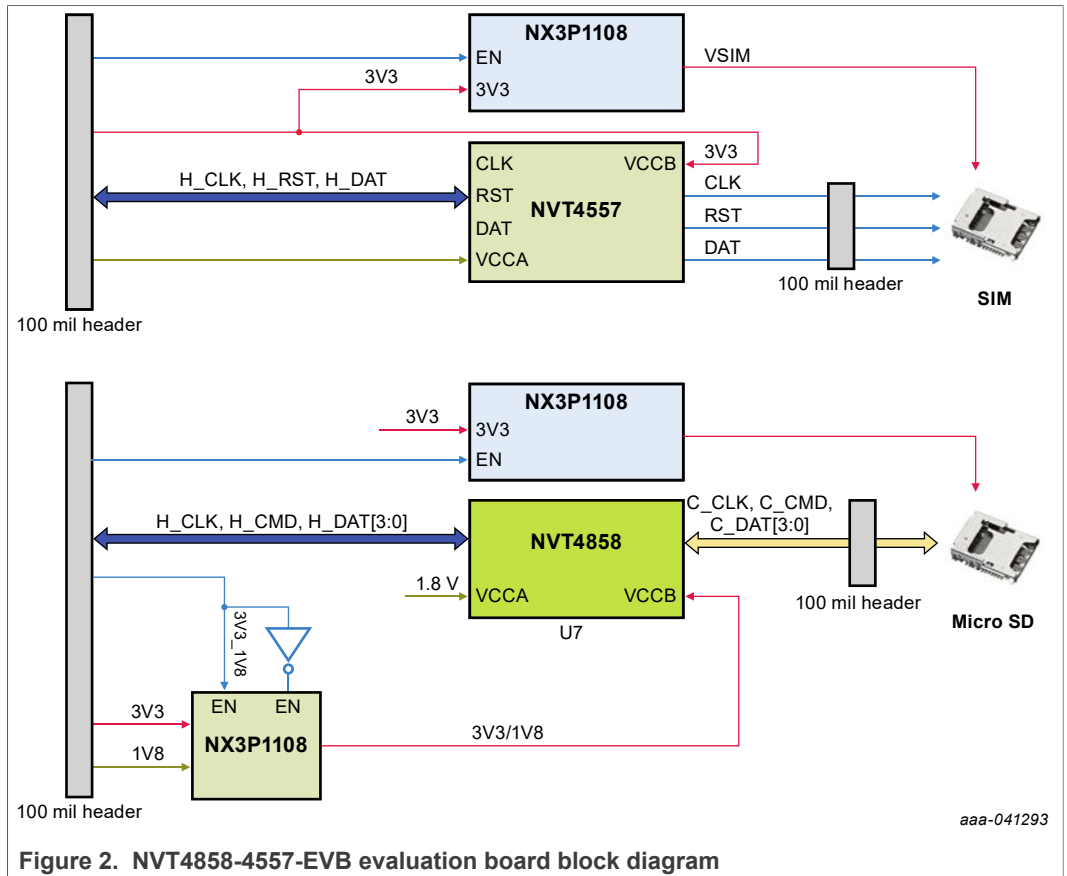
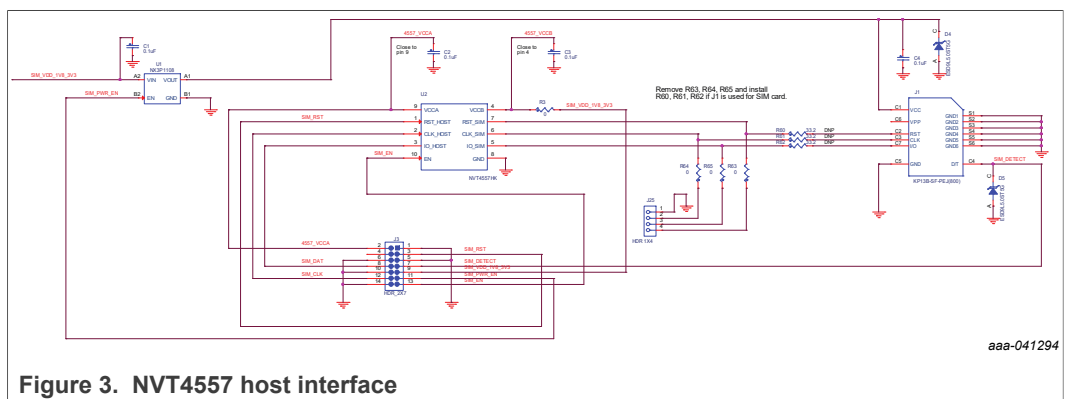


Figure 1. NVT4858-4557-EVB evaluation board



4.1 SIM level shifter and host controller interface

Please refer to [Figure 1](#) to find the location of connectors and jumpers on the evaluation board.



4.2 NVT4557 to SIM controller interface via J3

User can connect the NVT4858-4557-EVB evaluation board to the SIM controller via J3 with a 14-pin ribbon cable. The pin map for the SIM interface header is shown below.

Table 1. SIM controller interface header

J3 on NVT4858-4557-EVB	SIM controller	Comment
2 – 4557_VCCA	VCC	Level Shifter VCCA (1.08V – 2.0V)
3 – SIM_RST	SIM RST	SIM reset
4 – NO CONNECT	-	NO CONNECT
7 – SIM_DETECT	GPIO	SIM card insert detection, active low, pull-up on host side
8 – SIM_DAT	SIM I/O	SIM Input/output data
9 – SIM_VDD_1V8_3V3	POWER	SIM card power – 1V8 or 3V3
11 – SIM_PWR_EN	GPIO	SIM card power enable, active high, 1.1V min
12 – SIM_CLK	SIM CLK	SIM clock
13 – SIM_EN	GPIO	Level shifter enable, reference to VCCA
1, 5, 6, 10, 14 – GND	GND	ground

4.3 SIM interface resistor loading options

The SIM interface of NVT4557 (U2) can be routed to a 4-pin header, or to the SIM card socket. When the interface is routed to the header (J25), this option allows the user an easy way to scope out the SIM signals and this is the default configuration.

If the SIM interface of NVT4557 must be routed to the SIM socket (J1) to access the SIM card, then R63, R64, R65 must be removed and R60, R61, R62 must be stuffed.

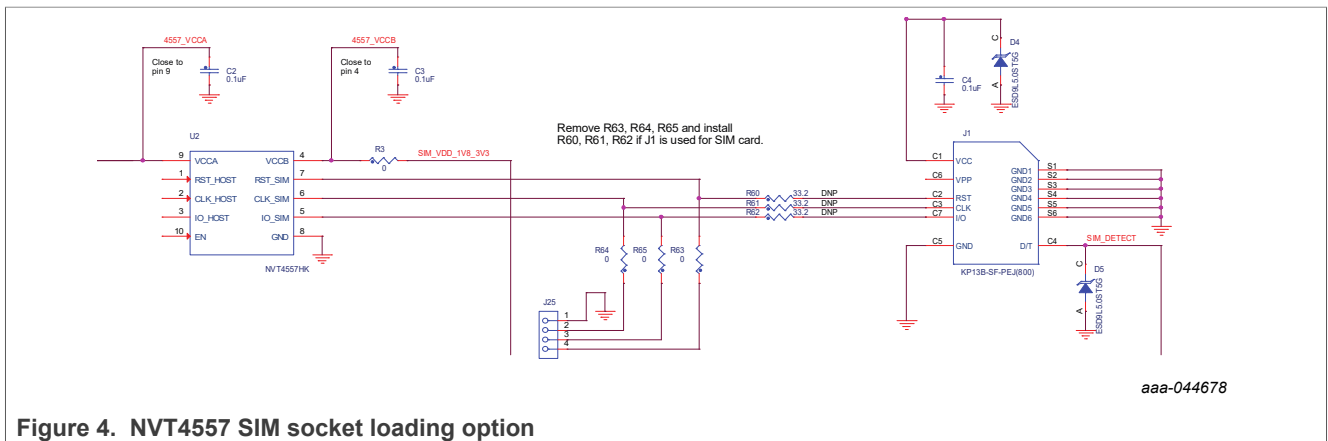


Figure 4. NVT4557 SIM socket loading option

4.4 SD level shifter host controller interface

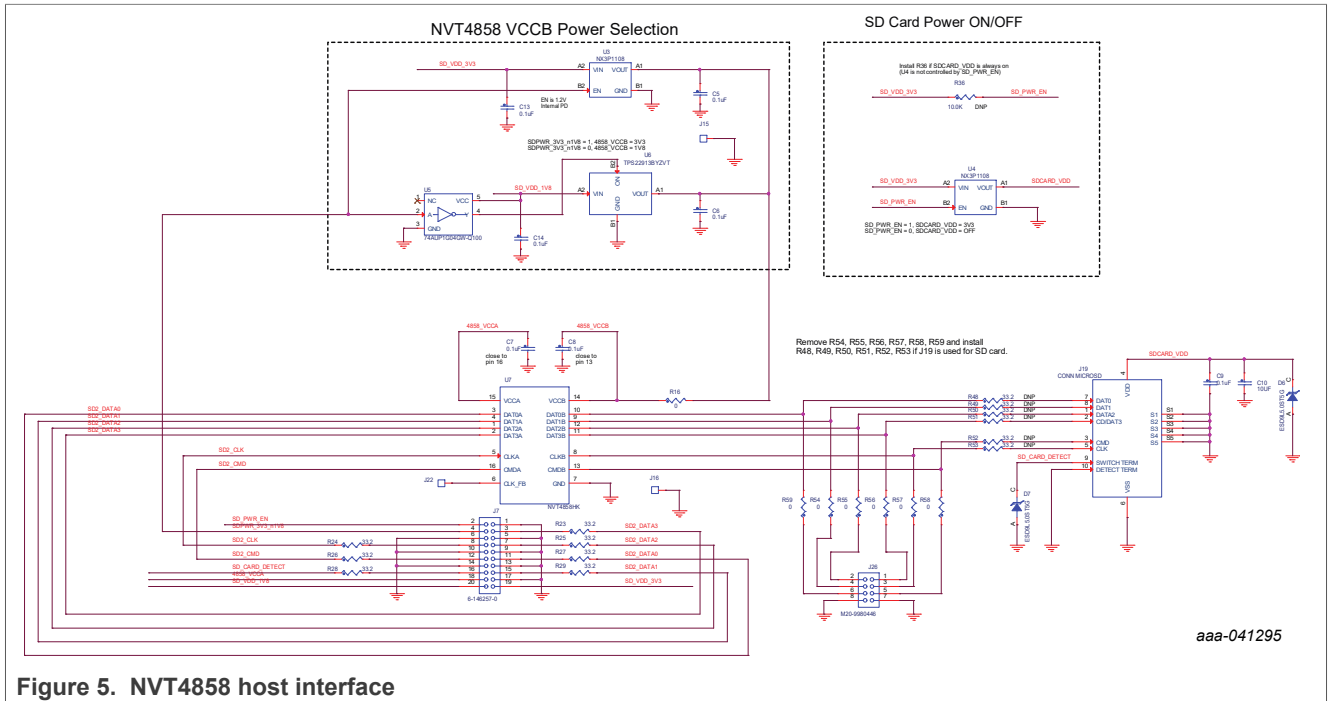


Figure 5. NVT4858 host interface

4.5 NVT4858 to SIM controller interface via J7

Table 2. SD controller interface header

J7 on NVT4858-4557-EVB	SD host controller	Comment
2 – SD_PWR_EN	GPIO	0 = turn off SD card power 1 = turn on SD card power
3 – SD2_DATA3	DAT3	SD data3
4 – SD_PWR_3V3_1V8	GPIO	SD card interface voltage (1V8 or 3V3 card) 0 = 1V8 1 = 3V3
7 – SD2_DATA2	DAT2	SD data2
8 – SD2_CLK	CLK	SD clock
11 – SD2_DATA0	DAT0	SD data0
12 – SD2_CMD	CMD	SD command
15 – SD2_DATA1	DAT1	SD data1
16 – SD_CARD_DETECT	GPIO	SD card detect, active low
18 – 4858_VCCA	Power	Level Shifter VCCA (1.08V – 2.0V)
19 – SD_VDD_3V3	Power	SD card interface voltage – 3V3 (3V3 card)
20 – SD_VDD_1V8	Power	SD card interface voltage – 1V8 (1V8 card)
1, 5, 6, 9, 10, 13, 14, 17 - GND	Ground	Ground

4.6 SD interface resistor loading options

The SD card interface of NVT4848 (U7) can be routed to an 8-pin header, or to the SD card socket. When the interface is routed to the header (J26), this option allows the user an easy way to scope out the SD signals; this is the default configuration.

If the SD interface of NVT4858 must be routed to the SD socket (J19) to access the SD card, then R54, R55, R56, R57, R58, R59 must be removed and R48, R49, R50, R51, R52, R53 must be stuffed.

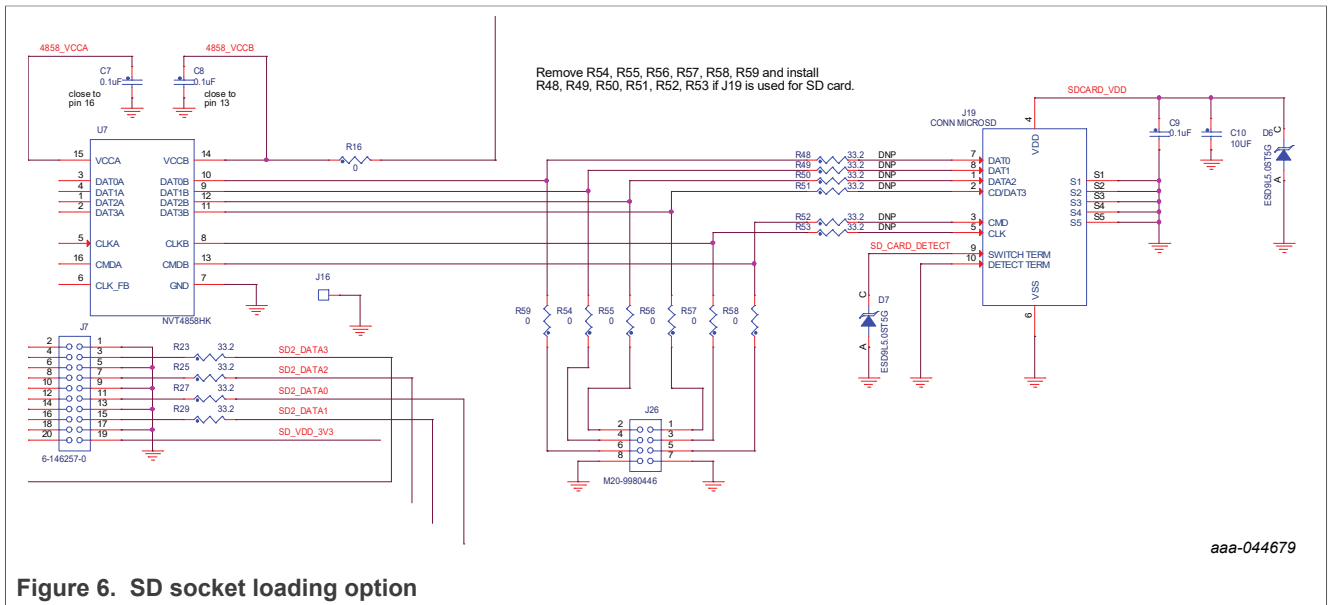


Figure 6. SD socket loading option

5 Errata list

Table 3. Errata list

Date	Errata Description	Demo Impact	Solution
-	None	None	None

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