NX3L4053

Triple low-ohmic single-pole double-throw analog switch

Rev. 5.1 — 30 March 2021 Product data sheet

1 General description

The NX3L4053 is a triple low-ohmic single-pole double-throw analog switch, suitable for use as an analog or digital multiplexer/demultiplexer. Each switch has a digital select input (nS), two independent inputs/outputs (nY0 and nY1) and a common input/output (nZ). All three switches share an enable input ($\overline{E}$). A digital enable pin $\overline{E}$ is common to all switches.When $\overline{E}$ is HIGH, the switches are turned off.

Schmitt trigger action at the digital inputs makes the circuit tolerant to slower input rise and fall times. Low threshold digital inputs allows this device to be driven by 1.8 V logic levels in 3.3 V applications without significant increase in supply current I_{CC}. This makes it possible for the NX3L4053 to switch 4.3 V signals with a 1.8 V digital controller, eliminating the need for logic level translation. The NX3L4053 allows signals with amplitude up to V_{CC} to be transmitted from nZ to nY0 or nY1; or from nY0 or nY1 to nZ. Its low ON resistance (0.5 Ω) and flatness (0.13 Ω) ensures minimal attenuation and distortion of transmitted signals.

2 Features and benefits

- Wide supply voltage range from 1.4 V to 4.3 V
- Very low ON resistance (peak):
  - 1.8 Ω (typical) at V_{CC} = 1.4 V
  - 1.0 Ω (typical) at V_{CC} = 1.65 V
  - 0.6 Ω (typical) at V_{CC} = 2.3 V
  - 0.6 Ω (typical) at V_{CC} = 2.7 V
  - 0.5 Ω (typical) at V_{CC} = 4.3 V
- Break-before-make switching
- High noise immunity
- ESD protection:
  - HBM JESD22-A114F Class 3A exceeds 4000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM AEC-Q100-011 revision B exceeds 1000 V
  - IEC61000-4-2 contact discharge exceeds 6000 V for switch ports
- CMOS low-power consumption
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level A
- 1.8 V control logic at V_{CC} = 3.6 V
- Control input accepts voltages above supply voltage
- Very low supply current, even when input is below V_{CC}
- High current handling capability (350 mA continuous current under 3.3 V supply)
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3 Applications

- Cell phone
- PDA
- Portable media player
- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

4 Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
NX3L4053PW	X3L4053	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
NX3L4053HR	M43	HXQFN16	plastic thermal enhanced extremely thin quad flat package; no leads; 16 terminals; body 3 × 3 × 0.5 mm	SOT1039-2

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
NX3L4053PW	NX3L4053PW,118	TSSOP16	Reel 13" Q1/T1 NDP	2500	T_{amb} = -40 °C to +125 °C
NX3L4053HR	NX3L4053HRZ	HXQFN16	Reel 7" Q1/T1 NDP SSB [1]	1500	T_{amb} = -40 °C to +125 °C
	NX3L4053HR,115 [2]	HXQFN16	Reel 7" Q1/T1 NDP	1500	T_{amb} = -40 °C to +125 °C

[1] This packing method uses a Static Shielding Bag (SSB) solution. Material is to be kept in the sealed bag between uses.
[2] Will go EOL - migrate to new leadframe NX3L2467HRZ orderable part number.

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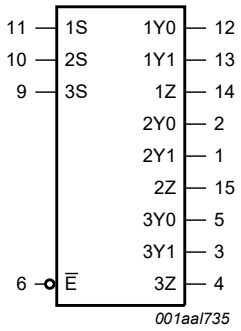
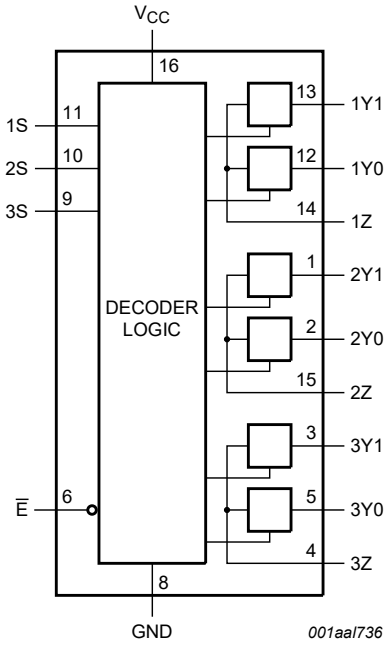
5 Functional diagram



Pin numbers are shown for TSSOP16 package only.

Figure 1. Logic symbol

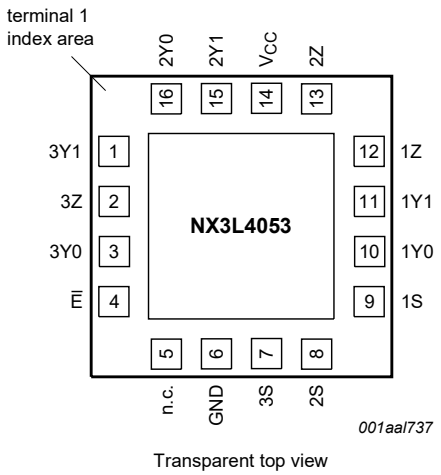


Pin numbers are shown for TSSOP16 package only.

Figure 2. Logic diagram

6 Pinning information

6.1 Pinning



Transparent top view

Figure 3. Pin configuration SOT1039-2 (HXQFN16)

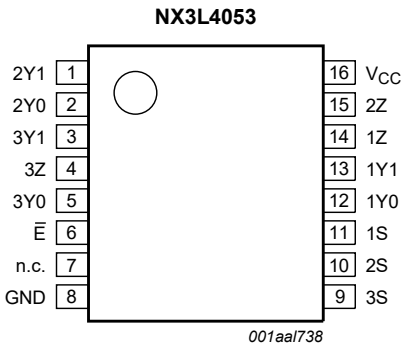


Figure 4. Pin configuration SOT403-1 (TSSOP16)

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6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT1039-2	SOT403-1	
$\overline{E}$	4	6	enable input (active LOW)
n.c.	5	7	not connected
GND	6	8	ground (0 V)
1S, 2S, 3S	9, 8, 7	11, 10 ,9	select input
1Y0, 2Y0, 3Y0	10, 16, 3	12, 2, 5	independent input or output
1Y1, 2Y1, 3Y1	11, 15, 1	13, 1, 3	independent input or output
1Z , 2Z, 3Z	12, 13, 2	14, 15, 4	independent output or input
V_{CC}	14	16	supply voltage

7 Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Inputs		Channel on
$\overline{E}$	nS	
L	L	nY0 to nZ
L	H	nY1 to nZ
H	X	switches off

8 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+4.6	V
V_I	input voltage	nS and $\overline{E}$	[1]	-0.5	+4.6	V
V_{SW}	switch voltage		[2]	-0.5	V_{CC} + 0.5	V
I_{IK}	input clamping current	V_I < -0.5 V		-50	-	mA
I_{SK}	switch clamping current	V_I < -0.5 V or V_I > V_{CC} + 0.5 V		-	±50	mA
I_{SW}	switch current	V_{SW} > -0.5 V or V_{SW} < V_{CC} + 0.5 V; source or sink current		-	±350	mA
		V_{SW} > -0.5 V or V_{SW} < V_{CC} + 0.5 V; pulsed at 1 ms duration, < 10 % duty cycle; peak current		-	±500	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C				
		HXQFN16	[3]	-	250	mW

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Table 5. Limiting values...*continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
		TSSOP16	[4]	-	500	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.
[2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed but may not exceed 4.6 V.
[3] For HXQFN16 package: above 135 °C the value of P_{tot} derates linearly with 16.9 mW/K.
[4] For TSSOP16 package: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

9 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			1.4	4.3	V
V_I	input voltage	nS and $\overline{E}$		0	4.3	V
V_{SW}	switch voltage		[1]	0	V_{CC}	V
T_{amb}	ambient temperature			-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	nS and $\overline{E}$; V_{CC} = 1.4 V to 4.3 V		-	200	ns/V

[1] To avoid sinking GND current from terminal nZ when switch current flows in terminal nYn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal nZ, no GND current will flow from terminal nYn. In this case, there is no limit for the voltage drop across the switch.

10 Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions		T_{amb} = 25 °C			T_{amb} = -40 °C to +125 °C			Unit
				Min	Typ	Max	Min	Max (85 °C)	Max (125 °C)	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.4 V to 1.6 V		0.9	-	-	0.9	-	-	V
		V_{CC} = 1.65 V to 1.95 V		0.9	-	-	0.9	-	-	V
		V_{CC} = 2.3 V to 2.7 V		1.1	-	-	1.1	-	-	V
		V_{CC} = 2.7 V to 3.6 V		1.3	-	-	1.3	-	-	V
		V_{CC} = 3.6 V to 4.3 V		1.4	-	-	1.4	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.4 V to 1.6 V		-	-	0.3	-	0.3	0.3	V
		V_{CC} = 1.65 V to 1.95 V		-	-	0.4	-	0.4	0.3	V
		V_{CC} = 2.3 V to 2.7 V		-	-	0.4	-	0.4	0.4	V
		V_{CC} = 2.7 V to 3.6 V		-	-	0.5	-	0.5	0.5	V
		V_{CC} = 3.6 V to 4.3 V		-	-	0.6	-	0.6	0.6	V
I_I	input leakage current	nS and $\overline{E}$; V_I = GND to 4.3 V; V_{CC} = 1.4 V to 4.3 V		-	-	-	-	±0.5	±1	µA

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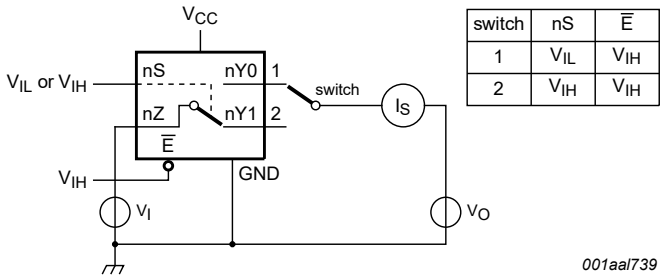
Table 7. Static characteristics...*continued*

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = -40 °C to +125 °C			Unit
			Min	Typ	Max	Min	Max (85 °C)	Max (125 °C)	
$I_{S(OFF)}$	OFF-state leakage current	nY0 and nY1 port; see Figure 5							
		V_{CC} = 1.4 V to 3.6 V	-	-	±5	-	±50	±500	nA
		V_{CC} = 3.6 V to 4.3 V	-	-	±10	-	±50	±500	nA
$I_{S(ON)}$	ON-state leakage current	nZ port; V_{CC} = 1.4 V to 3.6 V; see Figure 6							
		V_{CC} = 1.4 V to 3.6 V	-	-	±5	-	±50	±500	nA
		V_{CC} = 3.6 V to 4.3 V	-	-	±10	-	±50	±500	nA
I_{CC}	supply current	V_I = V_{CC} or GND; V_{SW} = GND or V_{CC}							
		V_{CC} = 3.6 V	-	-	100	-	500	5000	nA
		V_{CC} = 4.3 V	-	-	150	-	800	6000	nA
ΔI_{CC}	additional supply current	V_{SW} = GND or V_{CC}							
		V_I = 2.6 V; V_{CC} = 4.3 V	-	2.0	4.0	-	7	7	µA
		V_I = 2.6 V; V_{CC} = 3.6 V	-	0.35	0.7	-	1	1	µA
		V_I = 1.8 V; V_{CC} = 4.3 V	-	7.0	10.0	-	15	15	µA
		V_I = 1.8 V; V_{CC} = 3.6 V	-	2.5	4.0	-	5	5	µA
		V_I = 1.8 V; V_{CC} = 2.5 V	-	50	200	-	300	500	nA
C_I	input capacitance	nS and $\overline{E}$	-	1.0	-	-	-	-	pF
$C_{S(OFF)}$	OFF-state capacitance		-	35	-	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance		-	130	-	-	-	-	pF

10.1 Test circuits



switch	nS	$\overline{E}$
1	V_{IL}	V_{IH}
2	V_{IH}	V_{IH}

V_I = 0.3 V or V_{CC} - 0.3 V; V_O = V_{CC} - 0.3 V or 0.3 V.

Figure 5. Test circuit for measuring OFF-state leakage current

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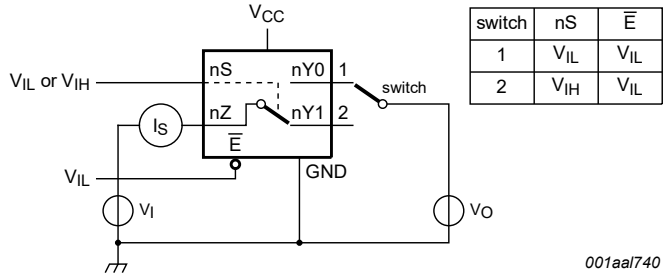

switch	nS	$\overline{E}$
1	V_{IL}	V_{IL}
2	V_{IH}	V_{IL}

V_I = 0.3 V or V_{CC} - 0.3 V; V_O = V_{CC} - 0.3 V or 0.3 V.

Figure 6. Test circuit for measuring ON-state leakage current

10.2 ON resistance

Table 8. ON resistance[1]

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for graphs see Figure 8 to Figure 14.

Symbol	Parameter	Conditions		T_{amb} = -40 °C to +85 °C			T_{amb} = -40 °C to +125 °C		Unit
				Min	Typ[2]	Max	Min	Max	
$R_{ON(peak)}$	ON resistance (peak)	V_I = GND to V_{CC}; I_{SW} = 100 mA; see Figure 7							
		V_{CC} = 1.4 V		-	1.8	3.8	-	4.2	Ω
		V_{CC} = 1.65 V		-	1.0	1.7	-	1.8	Ω
		V_{CC} = 2.3 V		-	0.6	0.9	-	1.0	Ω
		V_{CC} = 2.7 V		-	0.6	0.80	-	1.0	Ω
		V_{CC} = 4.3 V		-	0.5	0.80	-	1.0	Ω
ΔR_{ON}	ON resistance mismatch between channels	V_I = GND to V_{CC}; I_{SW} = 100 mA	[3]						
		V_{CC} = 1.4 V; V_{SW} = 0.4 V		-	0.23	0.38	-	0.38	Ω
		V_{CC} = 1.65 V; V_{SW} = 0.5 V		-	0.23	0.28	-	0.38	Ω
		V_{CC} = 2.3 V; V_{SW} = 0.7 V		-	0.12	0.15	-	0.18	Ω
		V_{CC} = 2.7 V; V_{SW} = 0.8 V		-	0.12	0.15	-	0.18	Ω
		V_{CC} = 4.3 V; V_{SW} = 0.8 V		-	0.12	0.15	-	0.18	Ω
$R_{ON(flat)}$	ON resistance (flatness)	V_I = GND to V_{CC}; I_{SW} = 100 mA	[4]						
		V_{CC} = 1.4 V		-	1.0	3.3	-	3.6	Ω
		V_{CC} = 1.65 V		-	0.5	1.2	-	1.3	Ω
		V_{CC} = 2.3 V		-	0.15	0.3	-	0.35	Ω
		V_{CC} = 2.7 V		-	0.13	0.3	-	0.35	Ω
		V_{CC} = 4.3 V		-	0.2	0.4	-	0.45	Ω

[1] For NX3L4053PW (TSSOP16 package), all ON resistance values are up to 0.05 Ω higher.
[2] Typical values are measured at T_{amb} = 25 °C.
[3] Measured at identical V_{CC}, temperature and input voltage.
[4] Flatness is defined as the difference between the maximum and minimum value of ON resistance measured at identical V_{CC} and temperature.

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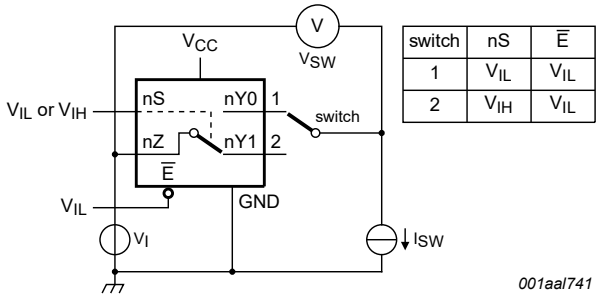
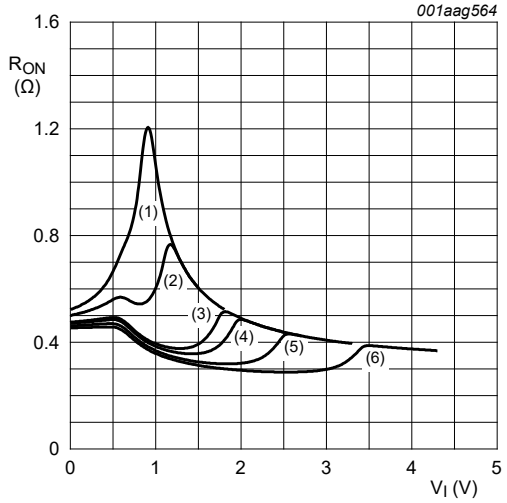
10.3 ON resistance test circuit and graphs



switch	nS	$\overline{E}$
1	V_{IL}	V_{IL}
2	V_{IH}	V_{IL}

$R_{ON} = V_{SW} / I_{SW}$.

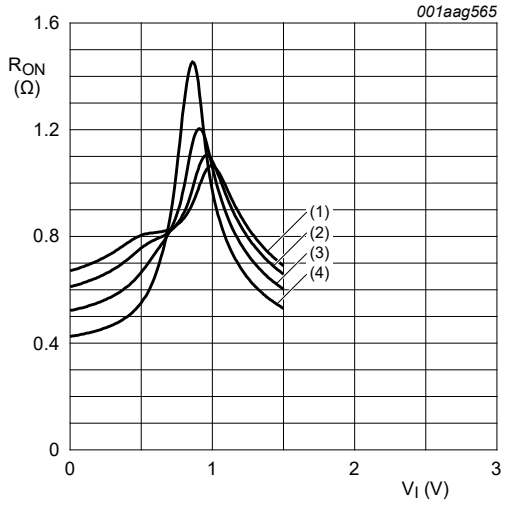
Figure 7. Test circuit for measuring ON resistance



1. V_{CC} = 1.5 V.
2. V_{CC} = 1.8 V.
3. V_{CC} = 2.5 V.
4. V_{CC} = 2.7 V.
5. V_{CC} = 3.3 V.
6. V_{CC} = 4.3 V.

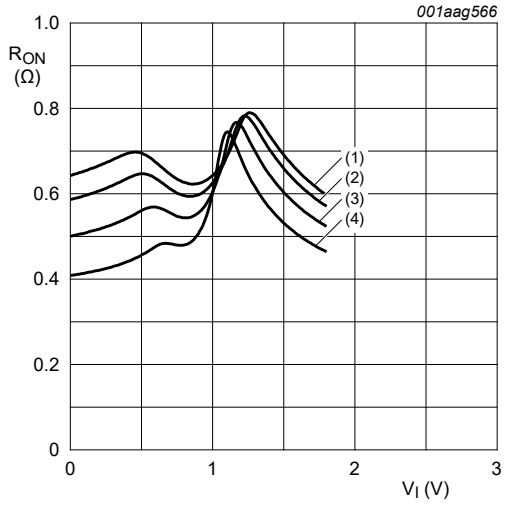
Measured at T_{amb} = 25 °C.

Figure 8. Typical ON resistance as a function of input voltage



1. T_{amb} = 125 °C.
2. T_{amb} = 85 °C.
3. T_{amb} = 25 °C.
4. T_{amb} = -40 °C.

Figure 9. ON resistance as a function of input voltage; V_{CC} = 1.5 V



1. T_{amb} = 125 °C.
2. T_{amb} = 85 °C.
3. T_{amb} = 25 °C.
4. T_{amb} = -40 °C.

Figure 10. ON resistance as a function of input voltage; V_{CC} = 1.8 V

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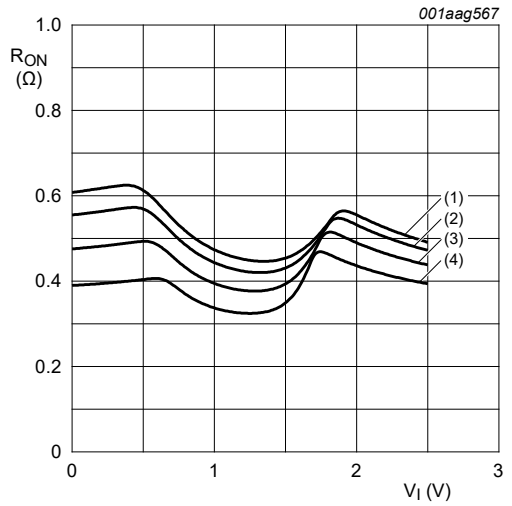
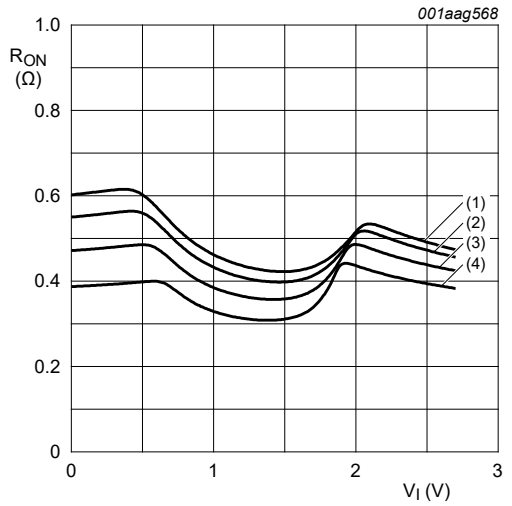


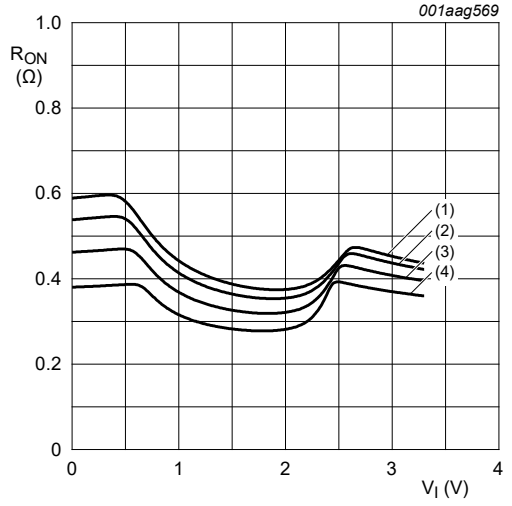
1. T_{amb} = 125 °C.
2. T_{amb} = 85 °C.
3. T_{amb} = 25 °C.
4. T_{amb} = -40 °C.

Figure 11. ON resistance as a function of input voltage; V_{CC} = 2.5 V



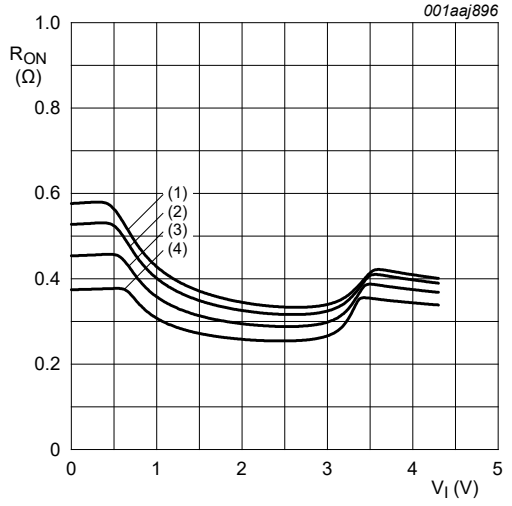
1. T_{amb} = 125 °C.
2. T_{amb} = 85 °C.
3. T_{amb} = 25 °C.
4. T_{amb} = -40 °C.

Figure 12. ON resistance as a function of input voltage; V_{CC} = 2.7 V



1. T_{amb} = 125 °C.
2. T_{amb} = 85 °C.
3. T_{amb} = 25 °C.
4. T_{amb} = -40 °C.

Figure 13. ON resistance as a function of input voltage; V_{CC} = 3.3 V



1. T_{amb} = 125 °C.
2. T_{amb} = 85 °C.
3. T_{amb} = 25 °C.
4. T_{amb} = -40 °C.

Figure 14. ON resistance as a function of input voltage; V_{CC} = 4.3 V

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11 Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for load circuit see Figure 17.

Symbol	Parameter	Conditions		T_{amb} = 25 °C			T_{amb} = -40 °C to +125 °C			Unit
				Min	Typ[1]	Max	Min	Max (85 °C)	Max (125 °C)	
t_{en}	enable time	$\overline{E}$, nS to nZ or nYn; see Figure 15								
		V_{CC} = 1.4 V to 1.6 V		-	49	90	-	120	120	ns
		V_{CC} = 1.65 V to 1.95 V		-	35	70	-	80	90	ns
		V_{CC} = 2.3 V to 2.7 V		-	23	45	-	50	55	ns
		V_{CC} = 2.7 V to 3.6 V		-	21	40	-	45	50	ns
		V_{CC} = 3.6 V to 4.3 V		-	21	40	-	45	50	ns
t_{dis}	disable time	$\overline{E}$, nS to nZ or nYn; see Figure 15								
		V_{CC} = 1.4 V to 1.6 V		-	32	70	-	80	90	ns
		V_{CC} = 1.65 V to 1.95 V		-	17	55	-	60	65	ns
		V_{CC} = 2.3 V to 2.7 V		-	11	25	-	30	35	ns
		V_{CC} = 2.7 V to 3.6 V		-	8	20	-	25	30	ns
		V_{CC} = 3.6 V to 4.3 V		-	8	20	-	25	30	ns
t_{b-m}	break-before-make time	see Figure 16	[2]							
		V_{CC} = 1.4 V to 1.6 V		-	19	-	9	-	-	ns
		V_{CC} = 1.65 V to 1.95 V		-	17	-	7	-	-	ns
		V_{CC} = 2.3 V to 2.7 V		-	13	-	4	-	-	ns
		V_{CC} = 2.7 V to 3.6 V		-	10	-	3	-	-	ns
		V_{CC} = 3.6 V to 4.3 V		-	9	-	2	-	-	ns

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.5 V, 1.8 V, 2.5 V, 3.3 V and 4.3 V respectively.
[2] Break-before-make guaranteed by design.

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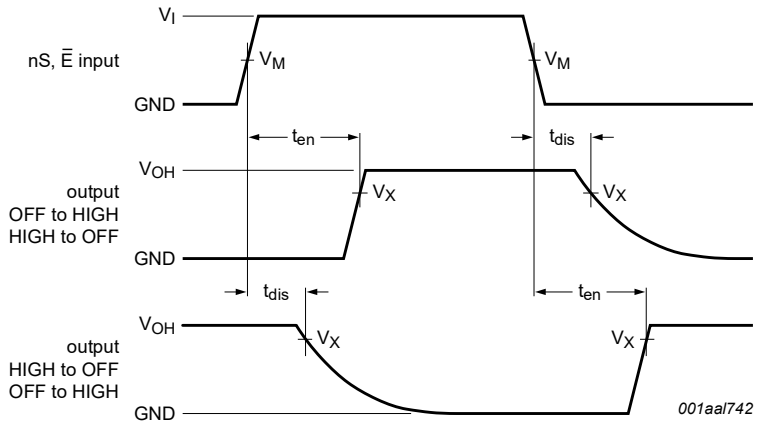
11.1 Waveform and test circuits



Measurement points are given in Table 10.

Logic level: V_{OH} is typical output voltage level that occurs with the output load.

Figure 15. Enable and disable times

Table 10. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_X
1.4 V to 4.3 V	$0.5V_{CC}$	$0.9V_{OH}$

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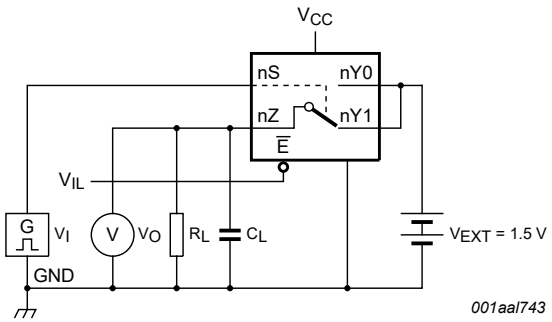
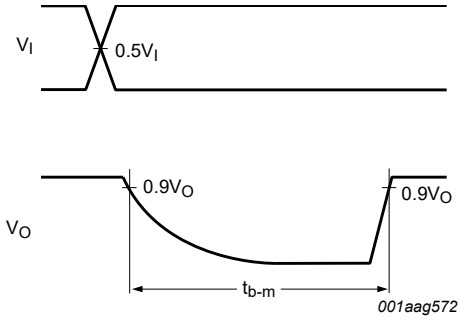
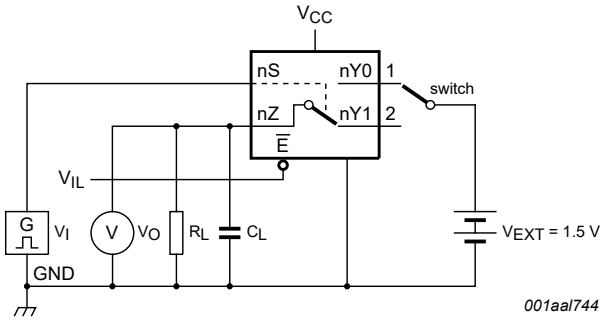


a. Test circuit



b. Input and output measurement points

Figure 16. Test circuit for measuring break-before-make timing



Test data is given in Table 11.

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

V_{EXT} = External voltage for measuring switching times.

V_I may be connected to nS or $\overline{E}$.

Figure 17. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Input		Load	
V_{CC}	V_I	t_r, t_f	C_L	R_L
1.4 V to 4.3 V	V_{CC}	≤ 2.5 ns	35 pF	50 Ω

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11.2 Additional dynamic characteristics

Table 12. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); V_I = GND or V_{CC} (unless otherwise specified); $t_r = t_f \leq 2.5$ ns; T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
THD	total harmonic distortion	f_i = 20 Hz to 20 kHz; R_L = 32 Ω; see Figure 18	[1]				
		V_{CC} = 1.4 V; V_I = 1 V (p-p)		-	0.15	-	%
		V_{CC} = 1.65 V; V_I = 1.2 V (p-p)		-	0.10	-	%
		V_{CC} = 2.3 V; V_I = 1.5 V (p-p)		-	0.02	-	%
		V_{CC} = 2.7 V; V_I = 2 V (p-p)		-	0.02	-	%
		V_{CC} = 4.3 V; V_I = 2 V (p-p)		-	0.02	-	%
$f_{(-3dB)}$	-3 dB frequency response	R_L = 50 Ω; see Figure 19	[1]				
		V_{CC} = 1.4 V to 4.3 V		-	60	-	MHz
α_{iso}	isolation (OFF-state)	f_i = 100 kHz; R_L = 50 Ω; see Figure 20	[1]				
		V_{CC} = 1.4 V to 4.3 V		-	-90	-	dB
V_{ct}	crosstalk voltage	between digital inputs and switch; f_i = 1 MHz; C_L = 50 pF; R_L = 50 Ω; see Figure 21					
		V_{CC} = 1.4 V to 3.6 V		-	0.2	-	V
		V_{CC} = 3.6 V to 4.3 V		-	0.3	-	V
Xtalk	crosstalk	between switches; f_i = 100 kHz; R_L = 50 Ω; see Figure 22	[1]				
		V_{CC} = 1.4 V to 4.3 V		-	-90	-	dB
Q_{inj}	charge injection	f_i = 1 MHz; C_L = 0.1 nF; R_L = 1 MΩ; V_{gen} = 0 V; R_{gen} = 0 Ω; see Figure 23					
		V_{CC} = 1.5 V		-	3	-	pC
		V_{CC} = 1.8 V		-	4	-	pC
		V_{CC} = 2.5 V		-	6	-	pC
		V_{CC} = 3.3 V		-	9	-	pC
		V_{CC} = 4.3 V		-	15	-	pC

[1] f_i is biased at $0.5V_{CC}$.

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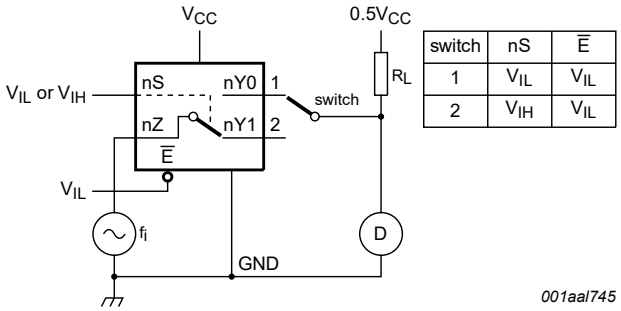
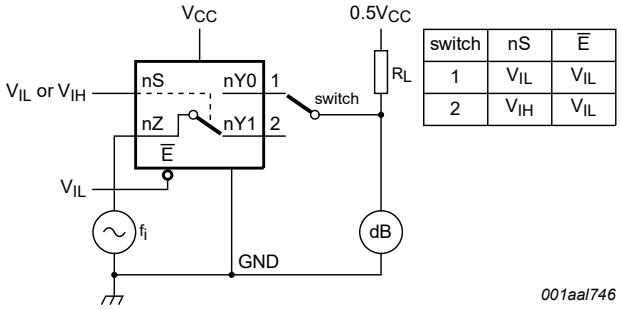
11.3 Test circuits



switch	nS	$\overline{E}$
1	V_{IL}	V_{IL}
2	V_{IH}	V_{IL}

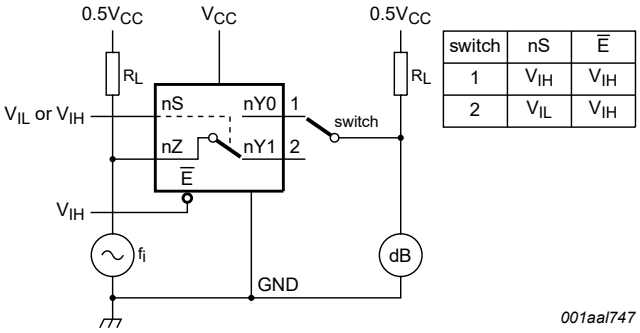
Figure 18. Test circuit for measuring total harmonic distortion



switch	nS	$\overline{E}$
1	V_{IL}	V_{IL}
2	V_{IH}	V_{IL}

Adjust f_i voltage to obtain 0 dBm level at output. Increase f_i frequency until dB meter reads -3 dB.

Figure 19. Test circuit for measuring the frequency response when channel is in ON-state



switch	nS	$\overline{E}$
1	V_{IH}	V_{IH}
2	V_{IL}	V_{IH}

Adjust f_i voltage to obtain 0 dBm level at input.

Figure 20. Test circuit for measuring isolation (OFF-state)

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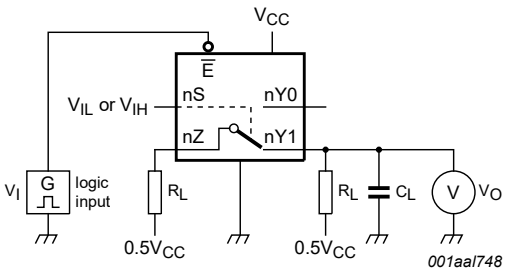
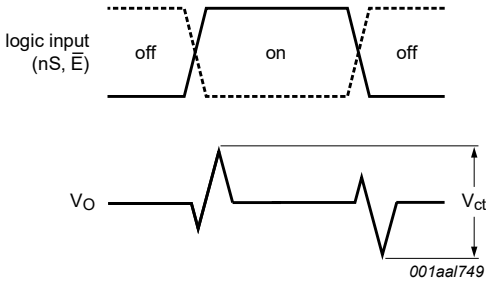


a. Test circuit



b. Input and output pulse definitions

Figure 21. Test circuit for measuring crosstalk voltage between digital inputs and switch

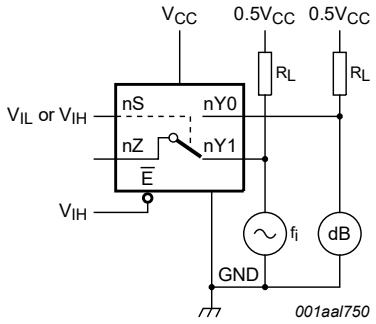


Figure 22. Test circuit for measuring crosstalk between switches

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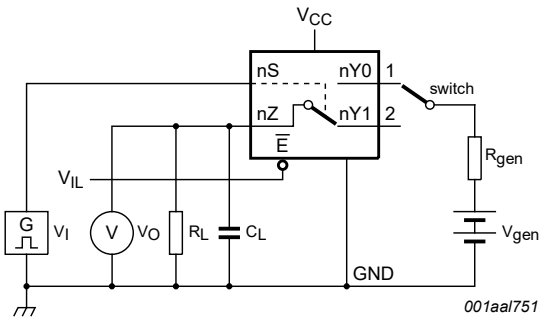
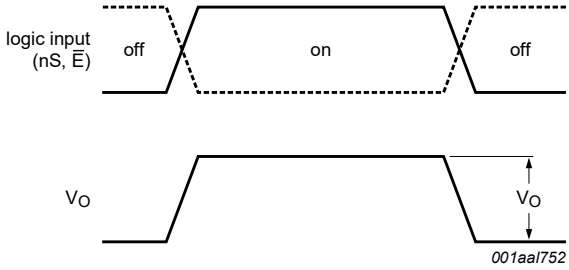


a. Test circuit



b. Input and output pulse definitions

Definition: $Q_{inj} = \Delta V_O \times C_L$.

ΔV_O = output voltage variation.

R_{gen} = generator resistance.

V_{gen} = generator voltage.

V_I may be connected to nS or $\overline{E}$.

Figure 23. Test circuit for measuring charge injection

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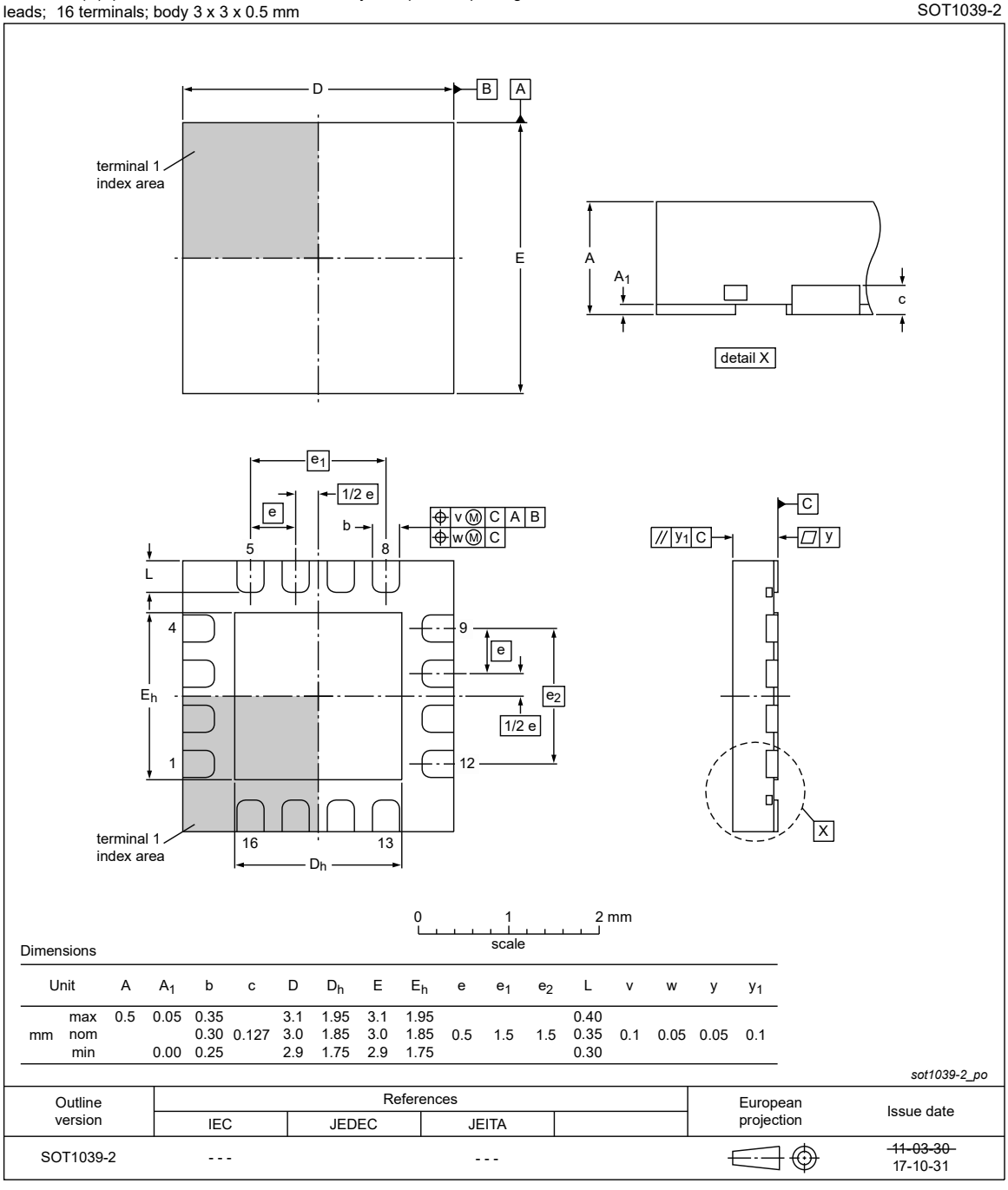
12 Package outline

HXQFN16 (U): plastic thermal enhanced extremely thin quad flat package; no leads; 16 terminals; body 3 x 3 x 0.5 mm

SOT1039-2



Dimensions

Unit		A	A_1	b	c	D	D_h	E	E_h	e	e_1	e_2	L	v	w	y	y_1
	max	0.5	0.05	0.35		3.1	1.95	3.1	1.95				0.40				
mm	nom			0.30	0.127	3.0	1.85	3.0	1.85	0.5	1.5	1.5	0.35	0.1	0.05	0.05	0.1
	min		0.00	0.25		2.9	1.75	2.9	1.75				0.30				

sot1039-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1039-2	- - -		- - -			~~11-03-30~~ 17-10-31

Figure 24. Package outline SOT1039-2 (HXQFN16)

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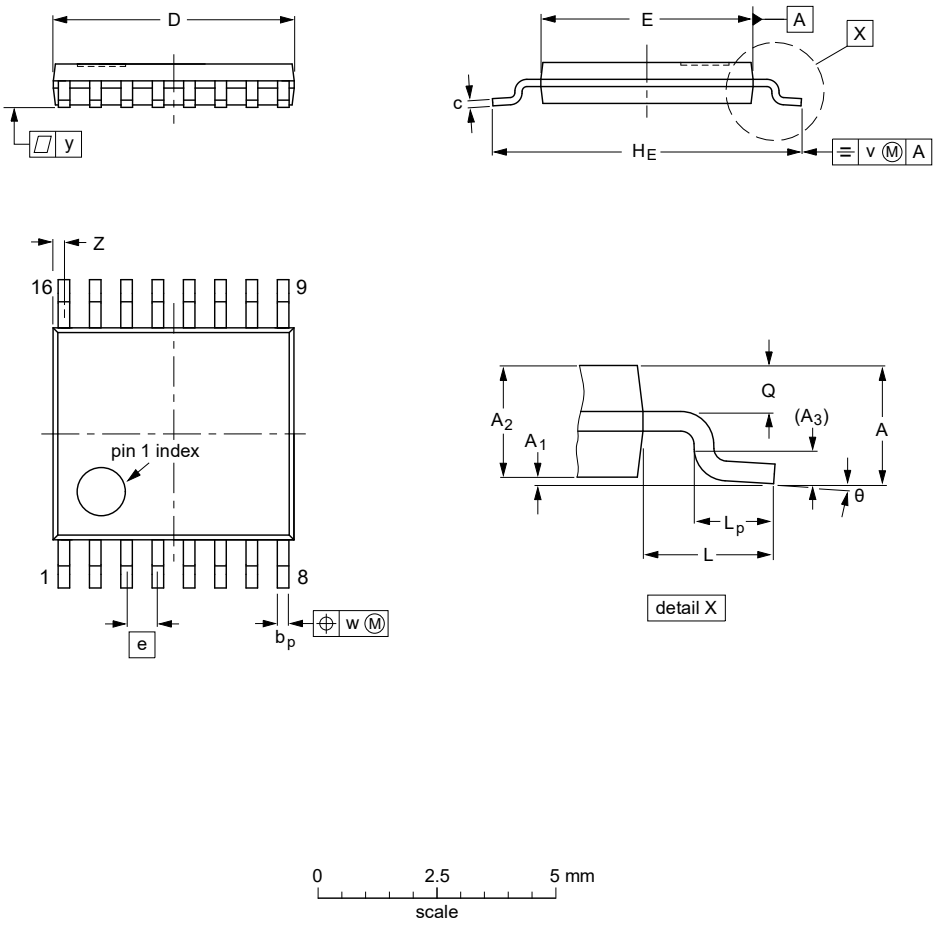
TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Figure 25. Package outline SOT403-1 (TSSOP16)

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13 Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
PDA	Personal Digital Assistant

14 Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX3L4053 v.5.1	20210330	Product data sheet	-	NX3L4053 v.5
Modifications:	• Updated Section 4 "Ordering information".			
NX3L4053 v.5	20120625	Product data sheet	-	NX3L4053 v.4
NX3L4053 v.4	20111107	Product data sheet	-	NX3L4053 v.3
Modifications:	• Legal pages updated.			
NX3L4053 v.3	20101223	Product data sheet	-	NX3L4053 v.2
NX3L4053 v.2	20100811	Product data sheet	-	NX3L4053 v.1
NX3L4053 v.1	20100416	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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