

# F1-2 PACK SiC MOSFET Module

## Product Preview

### NXH040P120MNF1PTG, NXH040P120MNF1PG

The NXH040P120MNF1 is a power module containing an 40 mΩ/1200 V SiC MOSFET half bridge and a thermistor in an F1 package.

#### Features

- 40 mΩ/1200 V SiC MOSFET Half Bridge
- Thermistor
- Options with Pre-applied Thermal Interface Material (TIM) and without Pre-applied TIM
- Press-fit Pins

#### Typical Applications

- Solar Inverter
- Uninterruptible Power Supplies
- Electric Vehicle Charging Stations
- Industrial Power

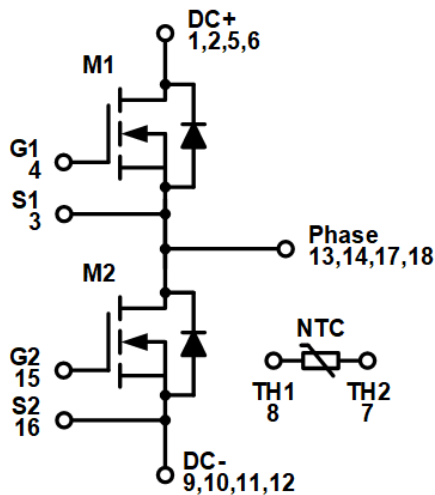
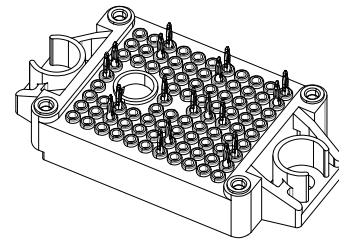


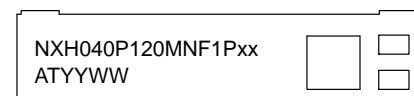
Figure 1. NXH040P120MNF1 Schematic Diagram

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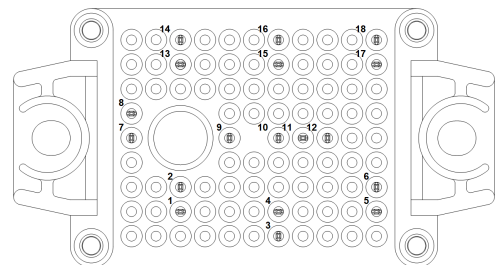
PIM18 33.8x42.5 (PRESS FIT)  
CASE 180BW

#### MARKING DIAGRAM



NXH040P120MNF1PTG= Specific Device Code  
NXH040P120MNF1PG = Specific Device Code  
AT = Assembly & Test Site Code  
YYWW = Year and Work Week Code

#### PIN CONNECTIONS



See Pin Function Description for pin names

#### ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

# NXH040P120MNF1PTG, NXH040P120MNF1PG

## PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	DC+	DC Positive Bus connection
2	DC+	DC Positive Bus connection
3	S1	Q1 Kelvin Emitter (High side switch)
4	G1	Q1 Gate (High side switch)
5	DC+	DC Positive Bus connection
6	DC+	DC Positive Bus connection
7	TH2	Thermistor Connection 2
8	TH1	Thermistor Connection 1
9	DC-	DC Negative Bus connection
10	DC-	DC Negative Bus connection
11	DC-	DC Negative Bus connection
12	DC-	DC Negative Bus connection
13	PHASE	Center point of half bridge
14	PHASE	Center point of half bridge
15	G2	Q2 Gate (Low side switch)
16	S2	Q2 Kelvin Emitter (High side switch)
17	PHASE	Center point of half bridge
18	PHASE	Center point of half bridge

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
<b>SiC MOSFET</b>			
Drain-Source Voltage	$V_{DSS}$	1200	V
Gate-Source Voltage	$V_{GS}$	+25/-15	V
Continuous Drain Current @ $T_C = 80^\circ\text{C}$ ( $T_J = 175^\circ\text{C}$ )	$I_D$	30	A
Pulsed Drain Current ( $T_J = 175^\circ\text{C}$ )	$I_{Dpulse}$	90	A
Maximum Power Dissipation ( $T_J = 175^\circ\text{C}$ )	$P_{tot}$	74	W
Short Circuit Withstand Time @ $V_{GE} = -5V/20\text{ V}$ , $V_{CE} = 600\text{ V}$ , $T_J \leq 150^\circ\text{C}$	$T_{sc}$	TBD	$\mu\text{s}$
Minimum Operating Junction Temperature	$T_{JMIN}$	-40	$^\circ\text{C}$
Maximum Operating Junction Temperature	$T_{JMAX}$	175	$^\circ\text{C}$

### THERMAL PROPERTIES

Storage Temperature range	$T_{stg}$	-40 to 150	$^\circ\text{C}$
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### INSULATION PROPERTIES

Isolation test voltage, $t = 1\text{ s}$ , 60 Hz	$V_{is}$	4800	$V_{RMS}$
Creepage distance		12.7	mm

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.

## RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Module Operating Junction Temperature	$T_J$	-40	150	$^\circ\text{C}$

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# NXH040P120MNF1PTG, NXH040P120MNF1PG

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit	
<b>SIC MOSFET CHARACTERISTICS</b>							
Drain–Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 200 μA	V <sub>(BR)DSS</sub>	1200	–	–	V	
Zero Gate Voltage Drain Current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 1200 V	I <sub>DSS</sub>	–	–	100	μA	
Drain–Source On Resistance	V <sub>GS</sub> = 20 V, I <sub>D</sub> = 25 A, T <sub>J</sub> = 25°C	R <sub>DS(ON)</sub>	–	42	56	mΩ	
	V <sub>GS</sub> = 20 V, I <sub>D</sub> = 25 A, T <sub>J</sub> = 125°C		–	55	–		
	V <sub>GS</sub> = 20 V, I <sub>D</sub> = 25 A, T <sub>J</sub> = 150°C		–	61	–		
Gate–Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 10 mA	V <sub>GS(TH)</sub>	1.8	2.81	4.3	V	
Gate Leakage Current	V <sub>GS</sub> = –10/20 V, V <sub>DS</sub> = 0 V	I <sub>GSS</sub>	–250	–	250	nA	
Internal Gate Resistance		R <sub>G</sub>		2.2		Ω	
Input Capacitance	V <sub>DS</sub> = 800 V, V <sub>GS</sub> = 0 V, f = 1 MHz	C <sub>ISS</sub>	–	1505	–	pF	
Reverse Transfer Capacitance		C <sub>RSS</sub>	–	12	–		
Output Capacitance		C <sub>OSS</sub>	–	159	–		
C <sub>OSS</sub> Stored Energy	V <sub>DS</sub> = 0 V to 800 V, V <sub>GS</sub> = 0 V	E <sub>OSS</sub>	–	66	–	μJ	
Total Gate Charge	V <sub>DS</sub> = 800 V, V <sub>GS</sub> = 20 V, I <sub>D</sub> = 25 A	Q <sub>G(TOTAL)</sub>	–	122.1	–	nC	
Gate–Source Charge		Q <sub>GS</sub>	–	32.2	–	nC	
Gate–Drain Charge		Q <sub>GD</sub>	–	34.7	–	nC	
Turn–on Delay Time	T <sub>J</sub> = 25°C V <sub>DS</sub> = 600 V, I <sub>D</sub> = 25 A V <sub>GS</sub> = –5 V/18 V, R <sub>G</sub> = TBD Ω	t <sub>d(on)</sub>	–	TBD	–	ns	
Rise Time		t <sub>r</sub>	–	TBD	–		
Turn–off Delay Time		t <sub>d(off)</sub>	–	TBD	–		
Fall Time		t <sub>f</sub>	–	TBD	–		
Turn–on Switching Loss per Pulse		E <sub>ON</sub>	–	TBD	–		mJ
Turn off Switching Loss per Pulse		E <sub>OFF</sub>	–	TBD	–		
Turn–on Delay Time	T <sub>J</sub> = 150°C V <sub>DS</sub> = 6 V, I <sub>D</sub> = 25 A V <sub>GS</sub> = –5 V/18 V, R <sub>G</sub> = TBD Ω	t <sub>d(on)</sub>	–	TBD	–	ns	
Rise Time		t <sub>r</sub>	–	TBD	–		
Turn–off Delay Time		t <sub>d(off)</sub>	–	TBD	–		
Fall Time		t <sub>f</sub>	–	TBD	–		
Turn–on Switching Loss per Pulse		E <sub>ON</sub>	–	TBD	–		mJ
Turn off Switching Loss per Pulse		E <sub>OFF</sub>	–	TBD	–		
Diode Forward Voltage	I <sub>D</sub> = 25 A, T <sub>J</sub> = 25°C	V <sub>SD</sub>	–	3.97	6	V	
	I <sub>D</sub> = 25 A, T <sub>J</sub> = 150°C		–	3.44	–		
Reverse Recovery Time	T <sub>J</sub> = 25°C V <sub>DS</sub> = 600 V, I <sub>D</sub> = 25 A V <sub>GS</sub> = –5 V/18 V, R <sub>G</sub> = TBD Ω	t <sub>rr</sub>	–	TBD	–	ns	
Reverse Recovery Charge		Q <sub>rr</sub>	–	TBD	–	nC	
Peak Reverse Recovery Current		I <sub>RRM</sub>	–	TBD	–	A	
Peak Rate of Fall of Recovery Current		di/dt	–	TBD	–	A/μs	
Reverse Recovery Energy		E <sub>rr</sub>	–	TBD	–	μJ	
Reverse Recovery Time		T <sub>J</sub> = 150°C V <sub>DS</sub> = 600 V, I <sub>D</sub> = 25 A V <sub>GS</sub> = –5 V/18 V, R <sub>G</sub> = TBD Ω	t <sub>rr</sub>	–	TBD	–	ns
Reverse Recovery Charge	Q <sub>rr</sub>		–	TBD	–	μC	
Peak Reverse Recovery Current	I <sub>RRM</sub>		–	TBD	–	A	
Peak Rate of Fall of Recovery Current	di/dt		–	TBD	–	A/μs	
Reverse Recovery Energy	E <sub>rr</sub>		–	TBD	–	μJ	
Thermal Resistance – chip–to–case	M1, M2		R <sub>thJC</sub>	–	0.8356	–	°C/W
Thermal Resistance – chip–to–heatsink	Thermal grease, Thickness = 2 Mil ±2%, A = 2.8 W/mK	R <sub>thJH</sub>	–	1.291	–	°C/W	

## NXH040P120MNF1PTG, NXH040P120MNF1PG

### ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
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#### THERMISTOR CHARACTERISTICS

Nominal resistance	T = 25°C	R <sub>25</sub>	–	5	–	kΩ
Nominal resistance	T = 100°C	R <sub>100</sub>	–	457	–	Ω
Deviation of R25		ΔR/R	–3	–	3	%
Power dissipation		P <sub>D</sub>	–	50	–	mW
Power dissipation constant			–	5	–	mW/K
B-value	B(25/50), tolerance ±3%		–	3375	–	K
B-value	B(25/100), tolerance ±3%		–	3455	–	K

#### ORDERING INFORMATION

Orderable Part Number	Marking	Package	Shipping
NXH040P120MNF1PG	NXH040P120MNF1PG	F1-2PACK: Case 180BW Press-fit Pins (Pb – Free and Halide – Free)	28 Units / Blister Tray
NXH040P120MNF1PTG	NXH040P120MNF1PTG	F1-2PACK: Case 180BW Press-fit Pins with pre – applied thermal interface material (TIM) (Pb – Free and Halide – Free)	28 Units / Blister Tray

# NXH040P120MNF1PTG, NXH040P120MNF1PG

## TYPICAL CHARACTERISTICS

SiC MOSFET (M1, M2)

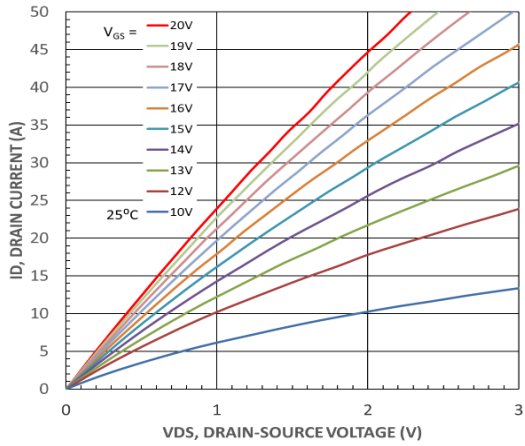


Figure 2. MOSFET Typical Output Characteristics

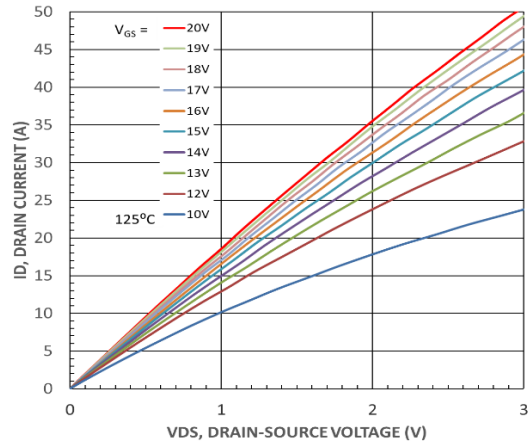


Figure 3. MOSFET Typical Output Characteristics

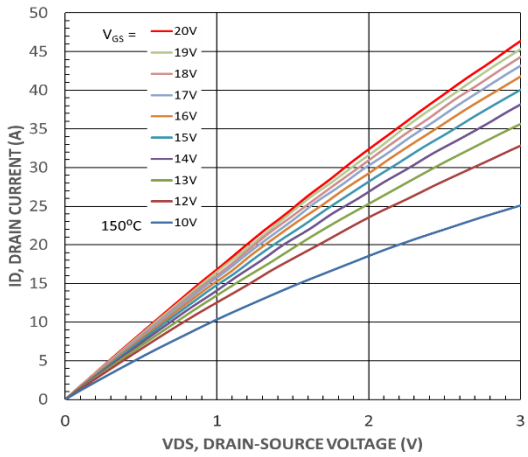


Figure 4. MOSFET Typical Output Characteristics

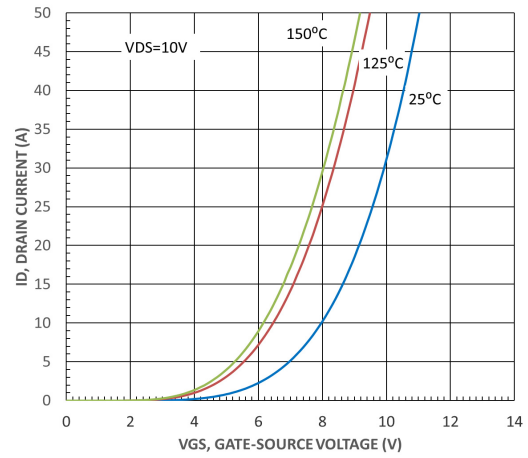


Figure 5. MOSFET Typical Transfer Characteristics

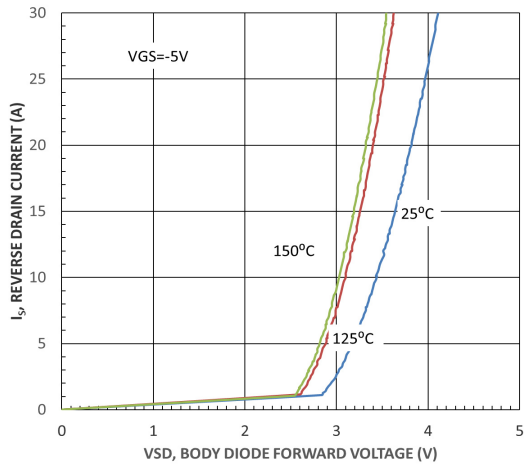


Figure 6. Body Diode Forward Characteristics

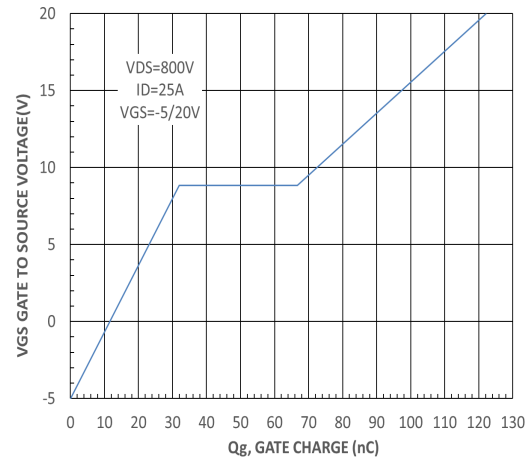
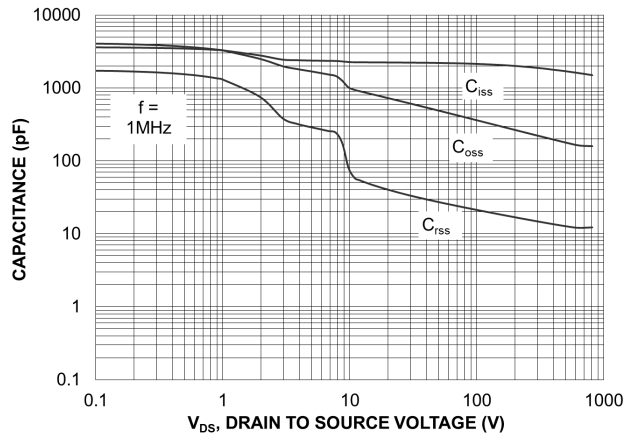


Figure 7. Gate-to-Source Voltage vs. Total Charge

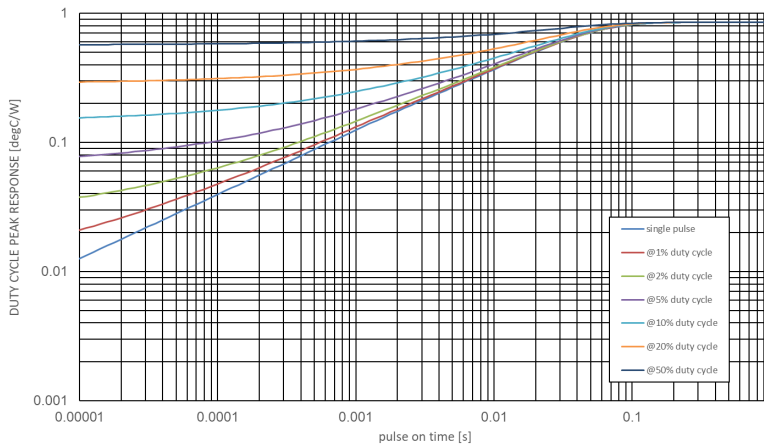
# NXH040P120MNF1PTG, NXH040P120MNF1PG

## TYPICAL CHARACTERISTICS

SiC MOSFET (M1, M2)



**Figure 8. Capacitance vs. Drain-to-Source Voltage**



**Figure 9. SiC MOSFET Junction-to-Case Transient Thermal Impedance**

**Table 1. FOSTER NETWORKS – M1, M2**

Foster Element #	M1		M2	
	Rth (K/W)	Cth (Ws/K)	Rth (K/W)	Cth (Ws/K)
1	0.051996	0.002404	0.054881	0.002284
2	0.046504	0.020373	0.010554	0.082427
3	0.008903	0.221087	0.064895	0.028973
4	0.165341	0.039489	0.094862	0.058574
5	0.600991	0.065660	0.610507	0.052914

**Table 2. CAUER NETWORKS – M1, M2**

Cauer Element #	M1		M2	
	Rth (K/W)	Cth (Ws/K)	Rth (K/W)	Cth (Ws/K)
1	0.076857	0.001961	0.076754	0.001921
2	0.141063	0.010485	0.182594	0.011596
3	0.274014	0.018050	0.136313	0.018196
4	0.113973	0.038620	0.215815	0.019717
5	0.267827	0.046224	0.224225	0.049799

# MECHANICAL CASE OUTLINE

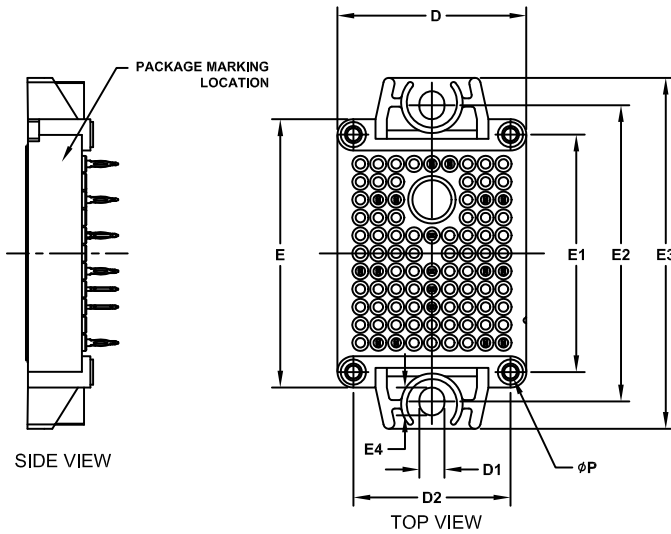
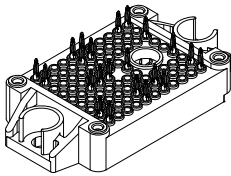
## PACKAGE DIMENSIONS

ON Semiconductor®



### PIM18 33.8x42.5 (PRESS FIT) CASE 180BW ISSUE B

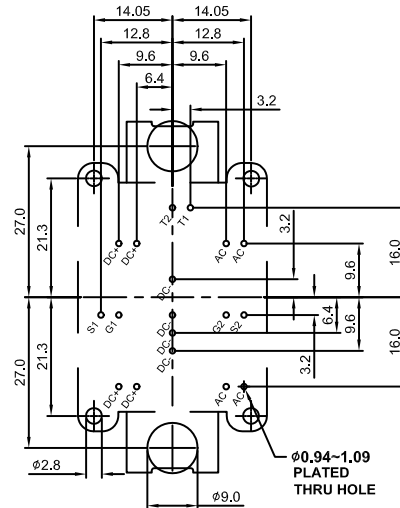
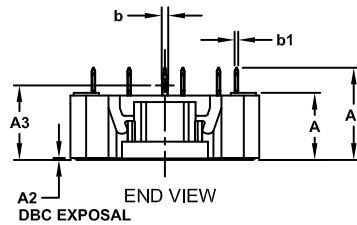
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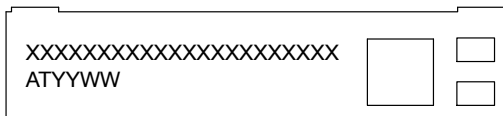
**NOTES:**

1. CONTROLLING DIMENSION: MILLIMETERS
2. PIN POSITION TOLERANCE IS  $\pm 0.4\text{mm}$

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	11.65	12.00	12.35
A1	16.00	16.50	17.00
A2	0.00	0.35	0.60
A3	12.85	13.35	13.85
b	1.15	1.20	1.25
b1	0.59	0.64	0.69
D	33.50	33.80	34.10
D1	4.40	4.50	4.60
D2	27.95	28.10	28.25
E	47.70	48.00	48.30
E1	42.35	42.50	42.65
E2	52.90	53.00	53.10
E3	62.30	62.80	63.30
E4	4.90	5.00	5.10
P	2.20	2.30	2.40



### GENERIC MARKING DIAGRAM\*



XXXXX = Specific Device Code  
AT = Assembly & Test Site Code  
YYWW = Year and Work Week Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "\*", may or may not be present. Some products may not follow the Generic Marking.

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<b>DESCRIPTION:</b>	<b>PIM18 33.8x42.5 (PRESS FIT)</b>	<b>PAGE 1 OF 1</b>

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